1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	
				2009-05-19

SCHEM,ANGEL_ISLAND,MLB,K17

Rev.A 02/23/10

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16	17	CPU Non-GFX Decoupling (2 of 2)	K17_REF	06/24/2009
17	18	PCH SATA/PCIE/CLK/LPC/SPI	K17_REF	08/24/2009
18	19	PCH DMI/FDI/Graphics	K17_WFERRY	06/09/2009
19	20	PCH PCI/FlashCache/USB	K18_MLB	10/07/2009
20	21	PCH MISC	K18_MLB	11/13/2009
21	22	PCH Power	K18_MLB	10/02/2009
22	23	PCH Grounds	T22_MLB	03/26/2009
23	24	PCH Non-GFX Decoupling	K17_WFERRY	06/09/2009
24	25	CPU/PCH GFX Decoupling	K17_WFERRY	06/09/2009
25	26	eXtended Debug Port (XDP)	K18_MLB	06/22/2009
26	27	Clock (CK505)	K17_REF	05/19/2009
27	28	Chipset Support	K17_REF	06/17/2009
28	29	DDR3 SO-DIMM Connector A	K17_REF	05/13/2009
29	30	DDR3 Byte/Bit Swaps	K18_MLB	06/19/2009
30	31	DDR3 SO-DIMM Connector B	K17_WFERRY	06/09/2009
31	32	CPU Memory S3 Support	K18_MLB	10/14/2009
32	33	FSB/DDR3/FRAMEBUF Vref Margining	K17_WFERRY	06/09/2009
33	34	X16/ALS/CAMERA CONNECTOR	K18_MLB	06/19/2009
34	35	ExpressCard Connector	K17_WFERRY	06/09/2009
35	36	USB HUB 1	K18_MLB	10/07/2009
36	37	USB HUB 2	K18_MLB	10/09/2009
37	39	Ethernet PHY (Caesar II/IV)	K18_MLB	10/28/2009
38	40	Ethernet Connector	K17_WFERRY	06/09/2009
39	41	FireWire LLC/PHY (FW643)	K20A_MLB	03/26/2009
40	42	FireWire Port Power	K20A_MLB	03/26/2009
41	43	FireWire Ports	K18_MLB	07/08/2009
42	45	SATA Connectors	K20A_MLB	03/26/2009
43	46	External USB Connectors	K17_WFERRY	06/09/2009
44	47	PROJECT SPECIFIC CONNS	K20A_MLB	03/26/2009
45	48	Front Flex Support	K20A_MLB	03/26/2009
46	49	SMC	K17_WFERRY	06/09/2009
47	50	SMC Support	K17_REF	06/17/2009
48	51	LPC+SPI Debug Connector	T22_MLB	03/30/2009
49	52	K17 SMBus Connections	K17_WFERRY	05/20/2009
50	53	Current & Voltage Sensing	K17_REF	06/17/2009
51	54	Current Sensing	K17_CHENGD	06/04/2009
52	55	Thermal Sensors	K17_CHENGD	07/08/2009
53	56	Fan Connectors	K20A_MLB	03/26/2009
54	57	WELLSPRING 1	K17_WFERRY	06/09/2009
55	58	WELLSPRING 2	K17_WFERRY	06/09/2009
56	59	Sudden Motion Sensor (SMS)	K20A_MLB	03/26/2009
57	60	DEBUG SENSORS AND ADC	K17_CHENGD	07/08/2009
58	61	SPI ROM	K17_WFERRY	06/09/2009
59	62	AUDIO:CODEC	K17_REF	05/30/2009
60	63	AUDIO: LINE IN	K17_REF	05/30/2009
61	65	AUDIO: HEADPHONE OUT	K17_REF	05/30/2009
62	66	AUDIO:SPEAKER AMP	K17_REF	05/30/2009
63	67	AUDIO: JACKS	K17_LENGO	11/24/2009
64	68	AUDIO: JACK TRANSLATORS	K17_REF	05/30/2009
65	69	DC-In & Battery Connectors	K17_REF	04/29/2009
66	70	PBus Supply & Battery Charger	K17_REF	04/29/2009
67	72	5V / 3.3V Power Supply	K20A_MLB	03/26/2009
68	73	1.5V DDR3 Supply	K17_REF	06/24/2009
69	74	CPU IMVP VCore Regulator	K18_POWER	06/29/2009
70	75	GFX IMVP VCore Regulator	T22_MLB	03/26/2009
71	76	CPUVTT (1.05V) Power Supply	T22_MLB	03/26/2009
72	77	Misc Power Supplies	K17_WFERRY	06/09/2009
73	78	Power FETs	K17_WFERRY	06/09/2009
74	79	Power Control	K17_WFERRY	06/09/2009
75	80	NV GT216 PCI-E	K18_MLB	06/29/2009
76	81	NV GT216 CORE/FB POWER	GT216	03/26/2009
77	82	NV GT216 FRAME BUFFER I/F	K18_MLB	06/29/2009
78	84	GDDR3 Frame Buffer A (Top)	GT216	03/26/2009
79	85	GDDR3 Frame Buffer B (Top)	GT216	03/26/2009
80	86	NV GT216 GPIO/MIO/MISC	K18_MLB	06/29/2009
81	87	GT216 GPIOS & STRAPS	K18_MLB	07/01/2009
82	88	NV GT216 VIDEO INTERFACES	K18_MLB	06/29/2009
83	89	GPU (GT216) CORE SUPPLY	K17_WFERRY	06/09/2009
84	90	LVDS Display Connector	K20A_MLB	03/26/2009
85	93	Muxed Graphics Support	K17_REF	06/17/2009
86	94	DisplayPort Connector	K20A_MLB	03/26/2009
87	95	1.05V GPU / 1V8 FB Power Supply	K17_REF	06/17/2009
88	96	Graphics MUX (GMUX)	K17_REF	06/24/2009
89	97	LCD Backlight Driver (MC34845)	K17_VEMURI	12/16/2009
90	98	LCD Backlight Support	K20A_MLB	03/26/2009
91	100	CPU Constraints	K17_WFERRY	06/09/2009
92	101	Memory Constraints	K17_WFERRY	06/09/2009
93	102	PCH Constraints 1	K17_WFERRY	06/09/2009
94	103	PCH Constraints 2	K17_REF	06/17/2009
95	104	Ethernet Constraints	K17_WFERRY	06/09/2009
96	105	FireWire Constraints	K17_WFERRY	06/09/2009
97	106	SMC Constraints	K17_WFERRY	06/09/2009
98	107	GPU (GT216) CONSTRAINTS	K17_WFERRY	06/09/2009
99	108	Project Specific Constraints	K17_REF	06/17/2009
100	109	PCB Rule Definitions	K17_WFERRY	06/09/2009
101	121	Ibex Peak-M Power Aliases	K17_REF	06/17/2009
102	122	Current Sensing	K17_REF	06/17/2009
103	132	T57 Card Connector	K17_WFERRY	05/20/2009

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8503	1	SCHEM,ANGEL_ISLAND,MLB,K17	SCH	CRITICAL	
820-2849	1	PCBF,ANGEL_ISLAND,MLB,K17	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Feb 23 21:52:40 2010

DRAWING TITLE: SCHEM,TREASURE_ISLAND,MLB,K17

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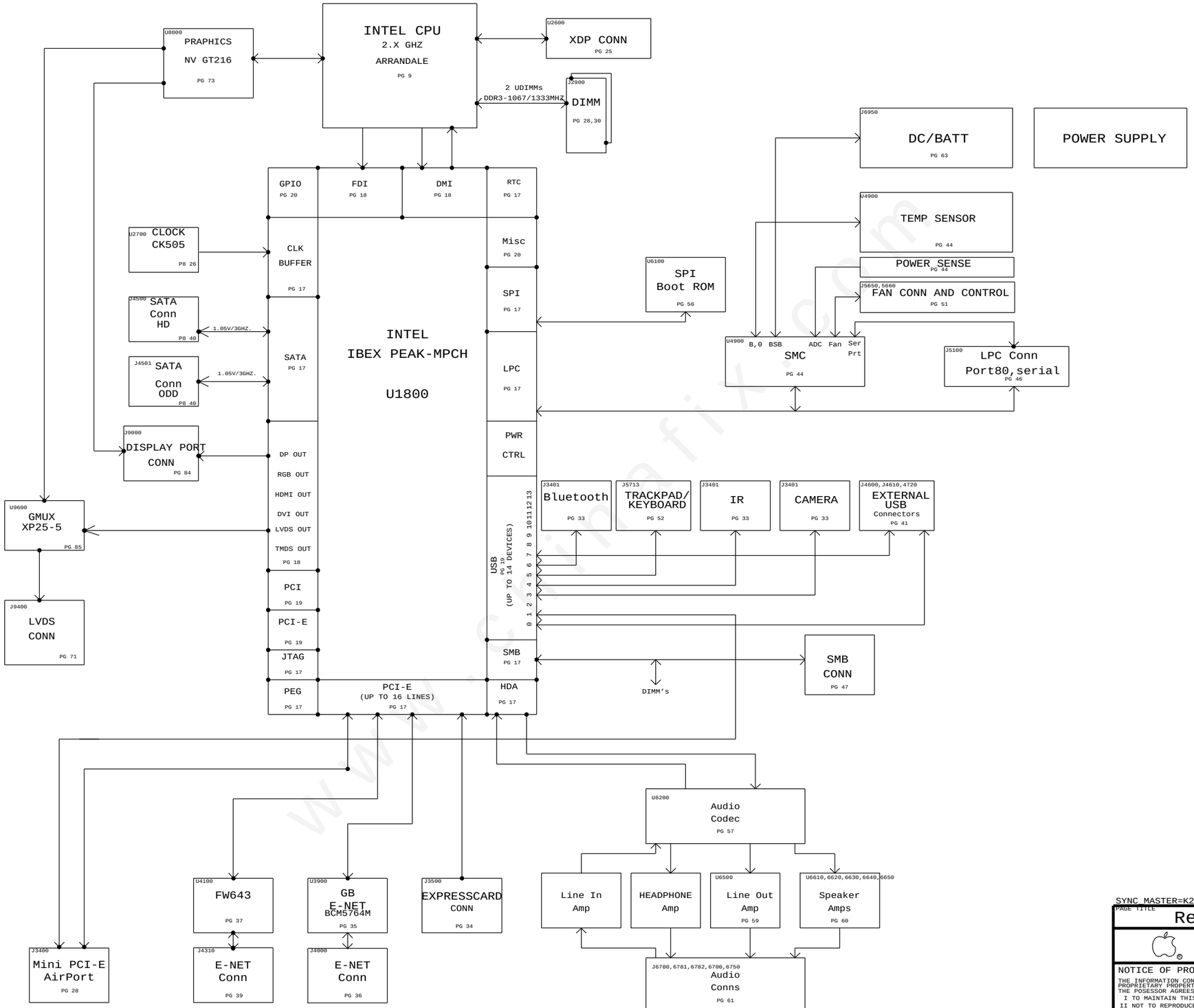

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K17 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(16.5V)
F6905 6A FUSE
SMC_DCIN_ISENSE
R7020
PPDCIN_G3H_OR_PBUS_R
R6905
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64)
VIN
VOUT
PPVBAT_G3H_CHGR_REG
F7040
F7041 8A FUSE
R7050
SMC_BATT_ISENSE
PPBUS_G3H
SMC_PBUS_VSENSE
Q5315
ENABLE 3.425V G3HOT LT3470A U6990 (PAGE 63)
PP3V42_G3H
SMC PWRGD NCP303LSN U5000 (PAGE 45)
SMC_RESET_L
SMC AVREF SUPPLY VR5020 (PAGE 45)
PP3V3_S5_AVREF_SMC
SMC_TPAD_RST_L
SMC_ONOFF_L
U5001

J6950
2S4P (6 TO 8.4V)
PPVBATT_G3H_CONN
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R

PP5V_S3_GPUVCORE
GPU VCORE ISL6263C U8900 (PAGE 81)
VR_ON
PGOOD
GPUVCORE_EN
U5410
SMC_GPU_ISENSE
SMC_GPU_VSENSE
PPVCORE_GPU
GPUVCORE_PGOOD
PP5V_S0_CPUVTTS0
1.05V TPS51513 U7600 (PAGE 69)
CPUVTTS0_EN
CPUVTTS0_PGOOD
R7640
PPCPUVTT_S0
SMC_CPU_FSB_ISENSE

SMC_CPU_HI_ISENSE
R5388
CPU VCORE ISL9522 U7400
CPUIMVP_VR_ON
CPUIMVP_GOOD
SMC_CPU_ISENSE
SMC_CPU_VSENSE
PPVCORE_S0_CPU

GMUX U9600 XP25-5 (PAGE 86)
PB16B EG_RAIL1_EN — P1V1GPU_EN
PB17A EG_RAIL2_EN — P3V3GPU_EN
PB17B EG_RAIL3_EN — GPUVCORE_EN
PB18A EG_RAIL4_EN — P1V8_S0GPU_EN
PL32A PM_ALL_GPU_PGOOD

SMC U4900 (PAGE 44)
P60 SMC_PM_G2_EN
RC DELAY
P3V3S5_EN

IBEX_PEAK_M U1800 (PAGE 17~22)
SLP_S5#(E4)
SLP_S4#(H7)
SLP_S3#(P12)
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
P5VS3_EN
DDRREG_EN
P3V3S3_EN
R7978
PM_SLP_S3_L_R
P1V8S0_EN
P1V2GMUX_EN
CPUVTTS0_EN
P1V5DDR_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN

P1V1GPU_EN
P1V8FB_EN
1.103V(L/H) 1.8V(R/H)
ISL6236 U9500 (PAGE 85)
PP1V1_S0GPU
R5413
PP1V8_S0GPU
SMC_GPU_1V8_ISENSE
P1V1GPU_PGOOD
P1V8FB_PGOOD

PP5V_S3_DDRREG
DDRREG_EN
DDRVTT_EN
1.5V S5 / 0.75V S3 TPS51116 U7300 (PAGE 66)
PPDDR_S3_REG
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
R7350
SMC_DDR_ISENSE
U5440
SMC_CPU_DDR_VSENSE
PP1V5_S3

Q7860
PP5V_S0_FET
P5VS0_EN
P1V5DDR_EN
SLG8AP026 U7801
PP1V5_S0
Q7850
PP1V2_GMUX_FET
P1V2GMUX_EN

P5VS3_EN
P3V3S5_EN
5V (L/H) 3.3V (R/H) TPS51980 U7201 (PAGE 65)
PP5V_S3
PP3V3_S5
P3V3S5_PGOOD
P5VS3_PGOOD
Q9806
BKLT_PLT_RST_L && LCD_BKLT_EN
BKLT_EN
APP001 U9700 (PAGE 87)
PPVOUT_S0_LCDBKLT

Q7870
PP3V3_S0_GPU
P3V3GPU_EN
Q7810
PP3V3_S3
P3V3S3_EN
Q7830
PP3V3_S0_FET
P3V3S0_EN
Q3810

P1V2ENET_EN
ISL8009B U7760 (PAGE 70)
PP1V2_ENET
P1V5_EXP_S0_EN
ISL8009B U7710 (PAGE 70)
PP1V5_EXP_S0
Q7922
PP3V3_ENET
PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN
PP3V3_S0_PWRCTL
P1V8S0_PGOOD
P5VS3_PGOOD
S0PGOOD_PWROK

P1V8_S0_EN
ISL8014 U7720 (PAGE 70)
PP1V8_S0
P1V8S0_PGOOD
Q4291
PP3V3_FW_EN
FW_PWR_EN
PP3V3_S0
U7971 ISL88042IRTEZ (PAGE 72)
PP1V5_S0
PP1V05_S0
TRST = 200mS

Q4260
SMC_ADAPTER_EN&&PM_SLP_S3_L
LTC1872 U7790 (PAGE 70)
PFWBOOST

SMC_GFX_VSENSE
R7540
GFXIMVP_ISENSE
1.05V AUX TPS51981 U7500 (PAGE 68)
GFX_VR_EN
GFX_DPRSLPVR
PPVCORE_S0_GFX
GFXIMVP_PGOOD

U2850
PM_PCH_PWRGD
IBEX PEAK M U1800 (PAGE 17~22)
PM_PWRBTN_L
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
CPU U1000 (PAGE 9~14)
SM_DRAMPWROK
VCCCPUPWRGD
RESET#

U7980
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SMC U4900 (PAGE 44)
SMC_ADAPTER_EN
PM_RSMRST_L
IMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L

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(For changes prior to Rev. A, refer to earlier schematics)

Rev. A:

02/23/10
MLB_TI_IMVP65
csa. 5 Added K17_PVT BOM group
csa. 74 Updated Symbol for U7400; new VPN is TPS51983
csa. 121 Changed ARB_ONLY sense Rs to XWs

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0973	PCBA,2.53GHZ,512SAM_VRAM,K17	K17_COMMON,CPU_2_53GHZ,FB_512_SAMSUNG,EEEE_DCMV,K17_PVT
639-0971	PCBA,2.53GHZ,512HYN_VRAM,K17	K17_COMMON,CPU_2_53GHZ,FB_512_HYNIX,EEEE_DCMR,K17_PVT
639-0972	PCBA,2.66GHZ,512SAM_VRAM,K17	K17_COMMON,CPU_2_66GHZ,FB_512_SAMSUNG,EEEE_DCMT,K17_PVT
639-0970	PCBA,2.66GHZ,512HYN_VRAM,K17	K17_COMMON,CPU_2_66GHZ,FB_512_HYNIX,EEEE_DCMQ,K17_PVT
085-1425	K17 MLB DEVELOPMENT	K17_DEVEL_ENG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
516S0806	516S0805		ALL	FOXCONN ALT TO MOLEX
138S0612	138S0602		ALL	Taiyo Yuden alt to Samsung
353S2805	353S2603		ALL	Fairchild 8 in alt to 6 in wafer
127S0111	127S0060		ALL	Rohm alt to Kemet
128S0299	128S0218		ALL	NEC/TOKIN alt to Sanyo
337S3808	337S3839		ALL	GT216 A02 alt to A03 part
376S0887	376S0749		ALL	Fairchild alt to Vishay

K17 BOM GROUPS

BOM GROUP	BOM OPTIONS
K17_COMMON	ALTERNATE,COMMON,K17_COMMON1,K17_COMMON2,K17_PROGPARTS
K17_COMMON1	BCM5764M,DCI,GMUX_VSYNC,CPUPOC_IMAX_40_50,PCH_NAND_3V3,CPUMEM_S0,EXT_HP_AMP,VFRQ_SLPS3,SMC_DEBUG_YES,DPMUX_EN_PLD,FB1V35,USBHUB_2061
K17_COMMON2	GPUVID_0P90V,BKLT_PWR_PBUS,DP_ESD,DP_CA_DET_EG_PLD,SMC_EXCARD_NOT,GPU_SS_INT,RDRV_8515_A2,GMUXPLL_3V3,HUB1_2NONREM,HUB2_2NONREM,RAIL_MON
K17_DEVEL_ENG	ARB_ONLY,CALPELLA_XDP,DEBUG_ADC,LPCPLUS,VREFMRGN,GMUX_JTAG_CONN,EFI_DEBUG,BMON_ENG,SMC_OSC_YES
K17_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG
K17_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM

BOM GROUP	BOM OPTIONS
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX
CALPELLA_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_NORMAL,XDP_PCH

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMQ]	CRITICAL	EEEE_DCMQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMR]	CRITICAL	EEEE_DCMR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMT]	CRITICAL	EEEE_DCMT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMV]	CRITICAL	EEEE_DCMV

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3847	1	ARD,SLBPF,PRQ,2.53,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3848	1	ARD,SLBPE,PRQ,2.66,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3846	1	ARD,SLBNA,PRQ,2.40,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IBEX (HM55),SLGZS,PRQ,B3	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP++,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8X8,64 QFN	U3900	CRITICAL	BCM5764M
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0229	1	IC,SMC,K17	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341T0244	1	IC,EFI ROM,K17	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,TP PSOC,K17,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2568	1	IC,CPLD,LATTICE,132CSBGA,K17MLB	U9600	CRITICAL	GMUX_PROG
333S0533	4	IC,SGRAM,GDDR3,32MX32,1GHZ,D-DIE,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,900MHZ,TIVA,HF	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX
341S2731	1	IC,1MBIT,SPI FLASH K17/K18	U3990	CRITICAL	
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,NON/SC	J3100	CRITICAL	
197S0350	1	OSC,XTAL,32.768KHZ,9-3.6V,12P SOIC,HF	U5010	CRITICAL	SMC_OSC_YES

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE PP5V_S0 — 70 71 73 87 / 45 53 55 69 / 102 — 3 TPs per Fan
TRUE FAN_LT_PWM — 53
TRUE FAN_LT_TACH — 53

J5660 (RIGHT FAN CONN)

TRUE FAN_RT_PWM — 53
TRUE FAN_RT_TACH — 53
TRUE GND — 4 TPs per Fan

J6780 (MIC CONN)

L55 TRUE INT_MIC_N — 63 99
L55 TRUE INT_MIC_SHIELD — 63
L55 TRUE INT_MIC_P — 63 99

J6781 (LEFT SPEAKER)

L95 TRUE SPKRAMP_FL_OUT_P — 62 63 99
L95 TRUE SPKRAMP_FL_OUT_N — 62 63 99
L95 TRUE SPKRAMP_BL_OUT_P — 62 63 99
L95 TRUE SPKRAMP_BL_OUT_N — 62 63 99

J6782 (RIGHT & SUB SPEAKER)

L95 TRUE SPKRAMP_LFE_OUT_P — 62 63 99
L95 TRUE SPKRAMP_LFE_OUT_N — 62 63 99
L95 TRUE SPKRAMP_FR_OUT_P — 62 63 99
L95 TRUE SPKRAMP_FR_OUT_N — 62 63 99
L95 TRUE SPKRAMP_BR_OUT_P — 62 63 99
L95 TRUE SPKRAMP_BR_OUT_N — 62 63 99

J9000 (LVDS CONN)

L195 TRUE LVDS_CONN_BKL_SYNC — 8 84
L195 TRUE PP3V3_SW_LCD — 84
L195 TRUE PP3V3_S0 — 73 74 81 84 85 86 88 99 101 / 6 7 8 23 42 48 53 55 69 70 71 73 87 102 — 2 TP needed
L195 TRUE PPVOUT_S0_LCDBKLT — 57 84 89
L195 TRUE LVDS_DDC_CLK — 84 85
L195 TRUE LVDS_DDC_DATA — 84 85
L195 TRUE LVDS_CONN_A_DATA_P<0> — 84 85 98
L195 TRUE LVDS_CONN_A_DATA_N<0> — 84 85 98
L195 TRUE LVDS_CONN_A_DATA_P<1> — 84 85 98
L195 TRUE LVDS_CONN_A_DATA_N<1> — 84 85 98
L195 TRUE LVDS_CONN_A_DATA_P<2> — 84 85 98
L195 TRUE LVDS_CONN_A_DATA_N<2> — 84 85 98
L195 TRUE LVDS_CONN_A_CLK_F_P — 84 98
L195 TRUE LVDS_CONN_A_CLK_F_N — 84 98
L195 TRUE LVDS_CONN_B_DATA_P<0> — 84 85 98
L195 TRUE LVDS_CONN_B_DATA_N<0> — 84 85 98
L195 TRUE LVDS_CONN_B_DATA_P<1> — 84 85 98
L195 TRUE LVDS_CONN_B_DATA_N<1> — 84 85 98
L195 TRUE LVDS_CONN_B_DATA_P<2> — 84 85 98
L195 TRUE LVDS_CONN_B_DATA_N<2> — 84 85 98
L195 TRUE LVDS_CONN_B_CLK_F_P — 84 98
L195 TRUE LVDS_CONN_B_CLK_F_N — 84 98
L195 TRUE LED_RETURN_1 — 84 89
L195 TRUE LED_RETURN_2 — 84 89
L195 TRUE LED_RETURN_3 — 84 89
L195 TRUE LED_RETURN_4 — 84 89
L195 TRUE LED_RETURN_5 — 84 89
L195 TRUE LED_RETURN_6 — 84 89
TRUE GND — 5 TPs

J4500 (SATA ODD CONN)

L195 TRUE PP5V_SW_ODD — 42 57
L195 TRUE SMC_ODD_DETECT — 42 46
L195 TRUE SATA_ODD_D2R_UF_P — 42 99
L195 TRUE SATA_ODD_D2R_UF_N — 42 99
L195 TRUE SATA_ODD_R2D_P — 42 93
L195 TRUE SATA_ODD_R2D_N — 42 93
TRUE GND — 3 TPs

J4501 (SATA HDD CONN)

L195 TRUE PP5V_S0_HDD_FLT — 42
L195 TRUE SATA_HDD_R2D_P — 42 93
L195 TRUE SATA_HDD_R2D_N — 42 93
L195 TRUE SATA_HDD_D2R_UF_N — 42 99
L195 TRUE SATA_HDD_D2R_UF_P — 42 99
TRUE GND — 4 TPs

J5815 (KBD BACKLIGHT CONN)

L195 TRUE KBDLED_ANODE — 55
L195 TRUE SMC_KDBLED_PRESENT_L — 55
TRUE GND — 2 TPs

FUNC_TEST
TRUE GND
TRUE GND — 6 TPs

USB PORTS

L195 TRUE PP5V_S3_RTUSB_A_F — 43
L195 TRUE USB2_LT1_N — 43 99
L195 TRUE USB2_LT1_P — 43 99
TRUE GND — 3 TPs per Fan

L195 TRUE PP5V_S3_RTUSB_B_F — 43
L195 TRUE USB_LT2_N — 43 99
L195 TRUE USB_LT2_P — 43 99
TRUE GND — 3 TPs per Fan

L195 TRUE PP5V_S3_RTUSB_C_F — 44
L195 TRUE USB_LT3_N — 44 99
L195 TRUE USB_LT3_P — 44 99
TRUE GND — 4 TPs per Fan

J3401, J3402 (AIRPORT/BT/CAMERA CONN)

L195 TRUE PCIE_AP_R2D_P — 33 94
L195 TRUE PCIE_AP_R2D_N — 33 94
L195 TRUE PCIE_AP_D2R_P — 17 33 94
L195 TRUE PCIE_AP_D2R_N — 17 33 94
L195 TRUE PCIE_CLK100M_AP_CONN_P — 33 94
L195 TRUE PCIE_CLK100M_AP_CONN_N — 33 94
L195 TRUE AP_CLKREQ_Q_L — 33
L195 TRUE PCIE_WAKE_L — 6 18 27 33 34
L195 TRUE AP_RESET_CONN_L — 33
L195 TRUE PP3V3_WLAN — 33
L195 TRUE PP3V3_S3_BT_F — 33
L195 TRUE SMBUS_SMC_A_S3_SDA — 6 33 46 49 55 97
L195 TRUE SMBUS_SMC_A_S3_SCL — 6 33 46 49 55 97
L195 TRUE USB_CAMERA_CONN_P — 33 99
L195 TRUE USB_CAMERA_CONN_N — 33 99
L195 TRUE CONN_USB2_BT_P — 33 99
L195 TRUE CONN_USB2_BT_N — 33 99
J4400 TRUE PP5V_S3_ALSCAMERA_F — 33

J3500 (EXPRESS CARD CONN)

L195 TRUE PP1V5_S0_EXCARD_SWITCH — 34
L195 TRUE PCIE_WAKE_L — 6 18 27 33 34
L195 TRUE SMBUS_PCH_CLK — 17 25 26 28 30 32 34 42 48 49
L195 TRUE SMBUS_PCH_DATA — 17 25 26 28 30 32 34 42 48 49
L195 TRUE PP3V3_S0_EXCARD_SWITCH — 34
L195 TRUE PP3V3_S3_EXCARD_SWITCH — 34
L195 TRUE USB2_EXCARD_CONN_N — 34 99
L195 TRUE USB2_EXCARD_CONN_P — 34 99
L195 TRUE EXCARD_CPUSB_L — 34
L195 TRUE EXCARD_CLKREQ_CONN_L — 34
L195 TRUE EXCARD_CPPE_L — 34
L195 TRUE PLT_RESET_SWITCH_L — 34
L195 TRUE PCIE_EXCARD_D2R_P — 17 34 94
L195 TRUE PCIE_EXCARD_D2R_N — 17 34 94
L195 TRUE PCIE_EXCARD_R2D_P — 34 94
L195 TRUE PCIE_EXCARD_R2D_N — 34 94
L195 TRUE PCIE_CLK100M_EXCARD_CONN_P — 34 99
L195 TRUE PCIE_CLK100M_EXCARD_CONN_N — 34 99

J5800 (IPD FLEX CONN)

L195 TRUE PP3V3_S3 — 6 7 17 20 31 32 33 34 35 36 49 50 51 54 / 55 56 72 74 88 102 103
L195 TRUE PP18V5_S3 — 6 55
L195 TRUE TPAD_GND_F — 55
L195 TRUE Z2_CS_L — 54 55
L195 TRUE Z2_DEBUG3 — 54 55
L195 TRUE Z2_MISO — 54 55
L195 TRUE Z2_BOOST_EN — 55
L195 TRUE Z2_BOOT_CFG1 — 54 55
L195 TRUE Z2_CLKIN — 54 55
L195 TRUE Z2_KEY_ACT_L — 54 55
L195 TRUE Z2_RESET — 54 55
L195 TRUE PSOC_F_CS_L — 54 55
L195 TRUE PICKB_L — 54 55
L195 TRUE PSOC_MISO — 54 55
L195 TRUE PSOC_MOSI — 54 55
L195 TRUE PSOC_SCLK — 54 55
L195 TRUE SMBUS_SMC_A_S3_SCL — 6 33 46 49 55 97
L195 TRUE SMBUS_SMC_A_S3_SDA — 6 33 46 49 55 97

J6900 (DC POWER CONN)

L195 TRUE ADAPTER_SENSE — 65
L195 TRUE PP18V5_DCIN_FUSE — 65 — 2 TPs
TRUE GND — 4 TPs

J6950 (MAIN BATT CONN)

L195 TRUE PPVBAT_G3H_CONN — 65 66 — 5 TPs
L195 TRUE SMBUS_SMC_BSA_SCL — 6 46 49 65 66 97
L195 TRUE SMBUS_SMC_BSA_SDA — 6 46 49 65 66 97
L195 TRUE SMC_BS_ALRT_L
TRUE GND — 5 TPs

J6995 (BAT LED CONN)

L195 TRUE PP3V42_G3H — 65 66 74 / 6 7 17 20 31 49 — 6 45 46 47 48 49 50 51 54
L195 TRUE SMBUS_SMC_BSA_SDA — 6 46 49 65 66 97
L195 TRUE SMBUS_SMC_BSA_SCL — 6 46 49 65 66 97
L195 TRUE SMC_BIL_BUTTON_L — 46 47 65
TRUE GND

J5713 (KEY BOARD CONN)

L195 TRUE PP3V3_S3 — 34 74 88 102 103 / 6 7 8 23 42 48 53 55 69 70 71 73 87 102
L195 TRUE PP3V42_G3H — 6 7 17 20 31 49 / 7 17 21 23 / 48 49 50 51 / 54 65 66 74
L195 TRUE WS_KBD1 — 54
L195 TRUE WS_KBD2 — 54
L195 TRUE WS_KBD3 — 54
L195 TRUE WS_KBD4 — 54
L195 TRUE WS_KBD5 — 54
L195 TRUE WS_KBD6 — 54
L195 TRUE WS_KBD7 — 54
L195 TRUE WS_KBD8 — 54
L195 TRUE WS_KBD9 — 54
L195 TRUE WS_KBD10 — 54
L195 TRUE WS_KBD11 — 54
L195 TRUE WS_KBD12 — 54
L195 TRUE WS_KBD13 — 54
L195 TRUE WS_KBD14 — 54
L195 TRUE WS_KBD15_CAP — 54
L195 TRUE WS_KBD16_NUM — 54
L195 TRUE WS_KBD17 — 54
L195 TRUE WS_KBD18 — 54
L195 TRUE WS_KBD19 — 54
L195 TRUE WS_KBD20 — 54
L195 TRUE WS_KBD21 — 54
L195 TRUE WS_KBD22 — 54
L195 TRUE WS_KBD23 — 54
L195 TRUE WS_KBD_ONOFF_L — 54
L195 TRUE WS_LEFT_SHIFT_KBD — 54
L195 TRUE WS_LEFT_OPTION_KBD — 54
L195 TRUE WS_CONTROL_KBD — 54

J4800 (FRONT CABLE CONN)

L195 TRUE PP3V42_G3H_LIDSWITCH_R — 45
L195 TRUE PP5V_S3_IR_R — 45
L195 TRUE SMC_LID_R — 45
L195 TRUE IR_RX_OUT — 45
L195 TRUE SYS_LED_ANODE — 45 47
TRUE GND

FUNC_TEST

L195 TRUE SYS_LED_ANODE_R — 45
L195 TRUE LPC_CLK33M_LPCPLUS — 27 48 94
L195 TRUE LPC_AD<0..3> — 17 46 48 88 94
L195 TRUE SPI_ALT_MOSI — 48
L195 TRUE SPI_ALT_MISO — 48
L195 TRUE LPC_FRAME_L — 17 46 48 88 94
L195 TRUE PM_CLKRUN_L — 18 46 48
L195 TRUE SMC_TMS — 46 47 48
L195 TRUE LPCPLUS_RESET_L — 27 48 88 94
L195 TRUE SMC_TDO — 46 47 48
L195 TRUE SMC_TRST_L — 46 48
L195 TRUE SMC_MD1 — 46 48
L195 TRUE SMC_TX_L — 43 46 47 48
L195 TRUE SPIROM_USE_MLB — 20 48 58
L195 TRUE SPI_ALT_CLK — 48
L195 TRUE SPI_ALT_CS_L — 48
L195 TRUE LPC_SERIRO — 17 46 48
L195 TRUE LPC_PWRDWN_L — 18 46 48
L195 TRUE SMC_TDI — 46 47 48
L195 TRUE SMC_TCK — 46 47 48
L195 TRUE SMC_RESET_L — 46 47 48 66
L195 TRUE SMC_NMI — 46 48
L195 TRUE SMC_RX_L — 43 46 47 48
L195 TRUE LPCPLUS_GPIO — 20 48
L195 TRUE ISSP_SCLK_P1_1 — 54
L195 TRUE ISSP_SDATA_P1_0 — 54
L195 TRUE SMC_ONOFF_L — 46 47 54
L195 TRUE PM_SYSRST_L — 18 27 46
L195 TRUE LCD_BKLT_PWM — 88 89

POWER RAILS

FUNC_TEST

L195 TRUE PM_SLP_S3_L — 18 31 46 74 86
L195 TRUE PPBUS_G3H — 7 8 40 50 66 67 68 70 71 83 87
L195 TRUE PPBUS_CPU_IMVP_ISNS — 7 50 69
L195 TRUE PP3V42_G3H — 6 7 17 21 23 43 45 46 47 48 49 / 50 51 54 65 66 74
L195 TRUE PP5V_S3 — 7 31 33 43 44 45 47 51 55 68 73 83 103
L195 TRUE PP5V_S0 — 6 7 8 23 42 48 53 55 69 70 71 73 87 102
L195 TRUE PPVCORE_S0_CPU — 7 12 15 50 69
L195 TRUE PP3V3_S5 — 101 / 99 99 / 68 72 73 — 2 TPs
L195 TRUE PP3V3_S3 — 6 7 17 20 31 32 33 34 35 36 49 50 51 54 / 7 31 35 / 49 50 51
L195 TRUE PP3V3_S0 — 34 85 86 88 99 101 55 56 72 74 88 102 103 / 6 7 8 23 42 48 49 53 55 69 70 71 73 87 / 52 53 55 59 63 64 69 70 71 72 73 87 102
L195 TRUE PP1V2_S0 — 7 73 88
L195 TRUE PP1V8_S0 — 7 12 16 72 73 88 101
L195 TRUE PPCPUVTT_S0 — 7 10 12 13 15 25 26 40 71 74 101
L195 TRUE PPVP_FW — 7 40 41
L195 TRUE PP1V0_FW — 7 40 72
L195 TRUE PP3V3_S0GPU — 7 73 75 80 81 82 83 85
L195 TRUE PP1V05_S0GPU — 7 51 75 77 80 82
L195 TRUE PP1V8_S0GPU_ISNS — 7 8 51 76 77 78 79
L195 TRUE PPVCORE_GPU — 7 50 76 83
L195 TRUE PP1V8_S0GPU_ISNS_R — 7 51 87
L195 TRUE PP3V3_S5_AVREF_SMC — 46 47
L195 TRUE PP18V5_S3 — 6 55
L195 TRUE PPDCIN_G3H — 7 65 66
L195 TRUE PPVTTDDR_S3 — 7 32 68
L195 TRUE PP1V8_GPUIFPX — 7 73 82

NC NO_TESTS

NO_TEST

L195 TRUE PCIE_PE5_D2RN — MAKE_BASE=TRUE — PCIE_PE5_D2RN
L195 TRUE PCIE_PE5_D2RP — MAKE_BASE=TRUE — PCIE_PE5_D2RP
L195 TRUE PCIE_PE5_R2D_CN — MAKE_BASE=TRUE — PCIE_PE5_R2D_CN
L195 TRUE PCIE_PE5_R2D_CP — MAKE_BASE=TRUE — PCIE_PE5_R2D_CP
L195 TRUE PCIE_PE6_D2RN — MAKE_BASE=TRUE — PCIE_PE6_D2RN
L195 TRUE PCIE_PE6_D2RP — MAKE_BASE=TRUE — PCIE_PE6_D2RP
L195 TRUE PCIE_PE6_R2D_CN — MAKE_BASE=TRUE — PCIE_PE6_R2D_CN
L195 TRUE PCIE_PE6_R2D_CP — MAKE_BASE=TRUE — PCIE_PE6_R2D_CP
L195 TRUE PCIE_PE7_D2RN — MAKE_BASE=TRUE — PCIE_PE7_D2RN
L195 TRUE PCIE_PE7_D2RP — MAKE_BASE=TRUE — PCIE_PE7_D2RP
L195 TRUE PCIE_PE7_R2D_CN — MAKE_BASE=TRUE — PCIE_PE7_R2D_CN
L195 TRUE PCIE_PE7_R2D_CP — MAKE_BASE=TRUE — PCIE_PE7_R2D_CP
L195 TRUE PCIE_PE8_D2RN — MAKE_BASE=TRUE — PCIE_PE8_D2RN
L195 TRUE PCIE_PE8_D2RP — MAKE_BASE=TRUE — PCIE_PE8_D2RP
L195 TRUE PCIE_PE8_R2D_CN — MAKE_BASE=TRUE — PCIE_PE8_R2D_CN
L195 TRUE PCIE_PE8_R2D_CP — MAKE_BASE=TRUE — PCIE_PE8_R2D_CP

ICT Test Points

CPU NO_TESTS

NO_TEST

TP_CPU_RSVD<65..62> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<65..62>
TP_CPU_RSVD<58..45> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<58..45>
TP_CPU_RSVD<43..32> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<43..32>
TP_CPU_RSVD<27..26> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<27..26>
TP_CPU_RSVD<24..15> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<24..15>
TP_CPU_RSVD<2..1> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<2..1>
TP_CPU_RSVD_NCTF<8..5> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD_NCTF<8..5>

NC NO_TESTS

NO_TEST

NC_CRT_IG_BLUE — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_BLUE
NC_CRT_IG_GREEN — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_GREEN
NC_CRT_IG_RED — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_RED
NC_CRT_IG_DDC_CLK — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_HSYNC
NC_CRT_IG_VSYNC — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_VSYNC
NC_LVDS_IG_CTRL_CLK — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_CTRL_CLK
NC_LVDS_IG_CTRL_DATA — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_CTRL_DATA
NC_PCH_LVDS_VBG — TRUE — MAKE_BASE=TRUE — NC_PCH_LVDS_VBG
NC_HDA_SDIN1 — TRUE — MAKE_BASE=TRUE — NC_HDA_SDIN1
NC_HDA_SDIN2 — TRUE — MAKE_BASE=TRUE — NC_HDA_SDIN2
NC_HDA_SDIN3 — TRUE — MAKE_BASE=TRUE — NC_HDA_SDIN3

NC_NO_TESTS

NO_TEST

TP_PCI_AD<31..0> — TRUE — MAKE_BASE=TRUE — NC_PCI_AD<31..0>
TP_PCI_C_BE_L<3..0> — TRUE — MAKE_BASE=TRUE — NC_PCI_C_BE_L<3..0>
NC_PCI_GNT3_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT3_L
NC_PCI_GNT2_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT2_L
NC_PCI_GNT1_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT1_L
NC_PCI_GNT0_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT0_L
NC_PCI_PAR — TRUE — MAKE_BASE=TRUE — NC_PCI_PAR
NC_PCI_RESET_L — TRUE — MAKE_BASE=TRUE — NC_PCI_RESET_L
NC_PCI_PME_L — TRUE — MAKE_BASE=TRUE — NC_PCI_PME_L
NC_PCI_CLK33M_OUT3 — TRUE — MAKE_BASE=TRUE — NC_PCI_CLK33M_OUT3
TP_NV_DQ<15..0> — TRUE — MAKE_BASE=TRUE — NC_NV_DQ<15..0>
TP_NV_DQS<1..0> — TRUE — MAKE_BASE=TRUE — NC_NV_DQS<1..0>
TP_NV_CE_L<3..0> — TRUE — MAKE_BASE=TRUE — NC_NV_CE_L<3..0>
NC_NV_ALE — TRUE — MAKE_BASE=TRUE — NC_NV_ALE
NC_NV_CLE — TRUE — MAKE_BASE=TRUE — NC_NV_CLE
NC_NV_RB_L — TRUE — MAKE_BASE=TRUE — NC_NV_RB_L
TP_NV_WR_RE_L<1..0> — TRUE — MAKE_BASE=TRUE — NC_NV_WR_RE_L<1..0>
TP_NV_WE_CK_L<1..0> — TRUE — MAKE_BASE=TRUE — NC_NV_WE_CK_L<1..0>
NC_PCIE_CLK100M_PE4N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE4N
NC_PCIE_CLK100M_PE4P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE4P
NC_PCIE_CLK100M_PE5N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_PE6N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE6N
NC_PCIE_CLK100M_PE6P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE6P
NC_PCIE_CLK100M_PE7N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE7N
NC_PCIE_CLK100M_PE7P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE7P
NC_PSOC_P1_3 — TRUE — MAKE_BASE=TRUE — NC_PSOC_P1_3
NC_SATA_C_D2RN — TRUE — MAKE_BASE=TRUE — NC_SATA_C_D2RN
NC_SATA_C_D2RP — TRUE — MAKE_BASE=TRUE — NC_SATA_C_D2RP
NC_SATA_C_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_SATA_C_R2D_CN
NC_SATA_C_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_SATA_C_R2D_CP
NC_SATA_D_D2RN — TRUE — MAKE_BASE=TRUE — NC_SATA_D_D2RN
NC_SATA_D_D2RP — TRUE — MAKE_BASE=TRUE — NC_SATA_D_D2RP
NC_SATA_D_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_SATA_D_R2D_CP
NC_SATA_SSD2_D2RN — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_D2RN
NC_SATA_SSD2_D2RP — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_D2RP
NC_SATA_SSD2_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_R2D_CN
NC_SATA_SSD2_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_R2D_CP
TP_SMC_P92 — TRUE — MAKE_BASE=TRUE — NC_SMC_P92
NC_USB_WMN — TRUE — MAKE_BASE=TRUE — NC_USB_WMN
NC_USB_WMP — TRUE — MAKE_BASE=TRUE — NC_USB_WMP
NC_USB_EXTDN — TRUE — MAKE_BASE=TRUE — NC_USB_EXTDN
NC_USB_EXTDP — TRUE — MAKE_BASE=TRUE — NC_USB_EXTDP
NC_USB_MININ — TRUE — MAKE_BASE=TRUE — NC_USB_MININ
NC_USB_MINIP — TRUE — MAKE_BASE=TRUE — NC_USB_MINIP
NC_USB_6N — TRUE — MAKE_BASE=TRUE — NC_USB_6N
NC_USB_6P — TRUE — MAKE_BASE=TRUE — NC_USB_6P
NC_USB_7N — TRUE — MAKE_BASE=TRUE — NC_USB_7N
NC_USB_7P — TRUE — MAKE_BASE=TRUE — NC_USB_7P

NC NO_TESTs

NO_TEST

NC_SMC_FAN_3_TACH — TRUE — NC_SMC_FAN_3_TACH
NC_SMC_FAN_3_CTL — TRUE — NC_SMC_FAN_3_CTL
NC_SMC_FAN_2_TACH — TRUE — NC_SMC_FAN_2_TACH
NC_SMC_FAN_2_CTL — TRUE — NC_SMC_FAN_2_CTL
NC_FW2_TPBP — TRUE — NC_FW2_TPBP
NC_FW2_TPBN — TRUE — NC_FW2_TPBN
NC_FW2_TPBIAS — TRUE — NC_FW2_TPBIAS
NC_FW2_TPAP — TRUE — NC_FW2_TPAP
NC_FW2_TPAN — TRUE — NC_FW2_TPAN
NC_FW0_TPBP — TRUE — NC_FW0_TPBP
NC_FW0_TPBN — TRUE — NC_FW0_TPBN
NC_FW0_TPAP — TRUE — NC_FW0_TPAP
NC_ESTARLDO_EN — TRUE — NC_ESTARLDO_EN
NC_ALS_GAIN — TRUE — NC_ALS_GAIN
NC_FW643_AVREG — TRUE — MAKE_BASE=TRUE — NC_FW643_AVREG
NC_FW643_TDI — TRUE — MAKE_BASE=TRUE — NC_FW643_TDI
NC_DP_IG_C_HPD — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_HPD
NC_DP_IG_C_CTRL_CLK — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_CTRL_CLK
NC_DP_IG_C_CTRL_DATA — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_CTRL_DATA
TP_DP_IG_C_MLP<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_MLP<3..0>
TP_DP_IG_C_MLN<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_MLN<3..0>
NC_DP_IG_C_AUXP — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_AUXP
NC_DP_IG_C_AUXN — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_AUXN
NC_DP_IG_D_HPD — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_HPD
NC_DP_IG_D_CTRL_CLK — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_CTRL_CLK
NC_DP_IG_D_CTRL_DATA — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_CTRL_DATA
TP_DP_IG_D_MLP<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_MLP<3..0>
TP_DP_IG_D_MLN<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_MLN<3..0>
NC_DP_IG_D_AUXP — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_AUXP
NC_DP_IG_D_AUXN — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_AUXN
NC_SDVO_TVCLKINN — TRUE — MAKE_BASE=TRUE — NC_SDVO_TVCLKINN
NC_SDVO_TVCLKINP — TRUE — MAKE_BASE=TRUE — NC_SDVO_TVCLKINP
NC_SDVO_STALLN — TRUE — MAKE_BASE=TRUE — NC_SDVO_STALLN
NC_SDVO_STALLP — TRUE — MAKE_BASE=TRUE — NC_SDVO_STALLP
NC_SDVO_INTN — TRUE — MAKE_BASE=TRUE — NC_SDVO_INTN
NC_SDVO_INTP — TRUE — MAKE_BASE=TRUE — NC_SDVO_INTP
NC_GPU_BUFRST_L — TRUE — MAKE_BASE=TRUE — NC_GPU_BUFRST_L
TP_GPU_GSTATE<0> — TRUE — MAKE_BASE=TRUE — NC_GPU_GSTATE<0>
TP_GPU_GSTATE<1> — TRUE — MAKE_BASE=TRUE — NC_GPU_GSTATE<1>
TP_GPU_MIOA_D<9..0> — TRUE — MAKE_BASE=TRUE — NC_GPU_MIOA_D<9..0>
TP_GPU_MIOA_DE — TRUE — MAKE_BASE=TRUE — NC_GPU_MIOA_DE
TP_LVDS_EG_B_CLK_N — TRUE — MAKE_BASE=TRUE — NC_LVDS_EG_B_CLKN
TP_LVDS_EG_B_CLK_P — TRUE — MAKE_BASE=TRUE — NC_LVDS_EG_B_CLKP
NC_LVDS_EG_BKL_PWM — TRUE — MAKE_BASE=TRUE — NC_LVDS_EG_BKL_PWM
TP_LVDS_IG_B_CLKN — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_B_CLKN
TP_LVDS_IG_B_CLKP — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_B_CLKP
TP_LVDS_IG_BKL_PWM — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_BKL_PWM
NC_PCH_SST — TRUE — MAKE_BASE=TRUE — NC_PCH_SST
NC_PCH_NC1 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC1
NC_PCH_NC2 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC2
NC_PCH_NC3 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC3
NC_PCH_NC4 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC4
NC_PCH_NC5 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC5
NC_PCH_TP19 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP19
NC_PCH_TP18 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP18
NC_PCH_TP17 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP17
NC_PCH_TP16 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP16
NC_PCH_TP15 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP15
NC_PCH_TP14 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP14
NC_PCH_TP13 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP13
NC_PCH_TP12 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP12
NC_PCH_TP11 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP11
NC_PCH_TP10 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP10
NC_PCH_TP9 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP9
NC_PCH_TP8 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP8
NC_PCH_TP7 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP7
NC_PCH_TP6 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP6
NC_PCH_TP5 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP5
NC_PCH_TP4 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP4
NC_PCH_TP3 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP3
NC_PCH_TP2 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP2
NC_PCH_TP1 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP1
PCH_VSS_NCTF<1> — TRUE — PCH_VSS_NCTF<15>
PCH_VSS_NCTF<2> — TRUE — PCH_VSS_NCTF<17>
PCH_VSS_NCTF<5> — TRUE — PCH_VSS_NCTF<19>
PCH_VSS_NCTF<7> — TRUE — PCH_VSS_NCTF<21>
PCH_VSS_NCTF<9> — TRUE — PCH_VSS_NCTF<25>
PCH_VSS_NCTF<11> — TRUE — PCH_VSS_NCTF<27>
PCH_VSS_NCTF<12> — TRUE — PCH_VSS_NCTF<29>

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8V
MAKE_BASE=TRUE
PPBUS_G3H ×10
PPBUS_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8V
MAKE_BASE=TRUE
PPBUS_CPU_IMVP_ISNS
PPDCIN_G3H
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=15.6V
MAKE_BASE=TRUE
PPDCIN_G3H
PP3V42_G3H
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
PP3V42_G3H ×16

5V Rails

PP5V_S5
PP5V_S5
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S5 ×10
PP5V_S3
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S3 ×16
PP5V_S3_ISNS_R
PP5V_S3_ISNS_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S3_ISNS_R
PP5V_S0
PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0 ×20
PP5V_S0_ISNS_R
PP5V_S0_ISNS_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0_ISNS_R

PP3V3_S5
PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5 ×30
PP3V3_S5_ISNS_R
PP3V3_S5_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5_ISNS_R
PP3V3_S3
PP3V3_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S3 ×30
PP3V3_S3_ISNS_R
PP3V3_S3_ISNS_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S3_ISNS_R
PP3V3_S0
PP3V3_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0 ×30
PP1V8_S0
PP1V8_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0 ×4

3.3V/1.8V Rails

PP1V5_S3
PP1V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3 ×30
PP1V5_S3RS0
PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3RS0
PPCPUDDR_ISNS
PPCPUDDR_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPCPUDDR_ISNS
PPVTTDDR_S3
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PPVTTDDR_S3
PP0V75_S0_DDRVTT
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PP0V75_S0_DDRVTT ×3
PP1V5_S0
PP1V5_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S0 ×30
PP1V2_S0
PP1V2_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S0 ×4
PP1V05_S5
PP1V05_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S5 ×4
PPCPUVTT_S0
PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPCPUVTT_S0 ×30
? mA

DDR Rails

PP1V5_S3
PP1V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3 ×30
PP1V5_S3RS0
PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3RS0
PPCPUDDR_ISNS
PPCPUDDR_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPCPUDDR_ISNS
PPVTTDDR_S3
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PPVTTDDR_S3
PP0V75_S0_DDRVTT
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PP0V75_S0_DDRVTT ×3

1.5V/1.05V Rails

PP1V5_S0
PP1V5_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S0 ×30
PP1V2_S0
PP1V2_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S0 ×4
PP1V05_S5
PP1V05_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S5 ×4
PPCPUVTT_S0
PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPCPUVTT_S0 ×30

Chipset "VCore" Rails

PPVCORE_S0_CPU
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PPVCORE_S0_CPU
PPVCORE_S0_GFX
PPVCORE_S0_GFX
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPVCORE_S0_GFX
PPVCORE_S0_CPU_VCAP0
PPVCORE_S0_CPU_VCAP0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PPVCORE_S0_CPU_VCAP1
PPVCORE_S0_CPU_VCAP1
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PPVCORE_S0_CPU_VCAP2
PPVCORE_S0_CPU_VCAP2
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

ENET Rails

PP3V3_ENET
PP3V3_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_ENET
PP1V2_ENET
PP1V2_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_ENET ×2

"FW" (FireWire) Rails

PPBUS_FW_FWBOOST
PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8V
MAKE_BASE=TRUE
PPBUS_FW_FWBOOST
PP10V_FW
PP10V_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=10V
MAKE_BASE=TRUE
PP10V_FW ×3
PPVP_FW
PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=10V
MAKE_BASE=TRUE
PPVP_FW ×2
PP3V3_FW_FWPHY
PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_FW_FWPHY ×2
PP1V0_FW
PP1V0_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V0_FW
PPVIN_FW_FWPHY
PPVIN_FW_FWPHY
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.0V
MAKE_BASE=TRUE
PPVIN_FW_FWPHY

"GPU" Rails

PP3V3_S0GPU
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0GPU ×4
PP1V8_GPUIFPX
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_GPUIFPX
PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0GPU_ISNS ×4
PP1V8_S0GPU_ISNS_R
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PP1V8_S0GPU_ISNS_R
PP1V05_S0GPU_ISNS_R
PP1V05_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0GPU_ISNS_R
PP1V05_S0GPU
PP1V05_S0GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0GPU ×10
PPVCORE_GPU
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PPVCORE_GPU

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Thermal Module Holes

ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH

Left CPU TM Hole
Right CPU TM Hole
Top GPU Right TM Hole
Bottom Left GPU TM Hole

Frame Holes

ZT0915 3R2P5 GND
ZT0932 3R2P5
ZT0960 3R2P5
ZT0971 3R2P5
ZT0940 3R2P5
ZT0970 3R2P5

ZT0934 STDOFF-4.0OD3.0H-SM
ZT0931 STDOFF-4.0OD3.0H-SM
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98

Bosses for Flex Protector Bracket

ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35

GMUX ALIASES

PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG
EG_RESET_L
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
LCD_BKLT_EN
PEX_CLKREQ_L
PEG_CLKREQ_L
PP3V3_S0
PM_ENET_EN
GND
FW_PLUG_DET_L
FW643_WAKE_L

CPU signals

CPU_VID<0..6> = CPUIMVP_VID<0..6>
GFX_VID<0..6> = GFXIMVP_VID<0..6>
MEMVTT_EN = MEMVTT_EN
TP_CPU_VTT_SELECT = TP_CPU_VTT_SELECT

GPU signals

PEG_D2R_P<15..0> = =PEG_D2R_P<0..15>
PEG_D2R_N<15..0> = =PEG_D2R_N<0..15>
PEG_R2D_C_P<15..0> = =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<15..0> = =PEG_R2D_C_N<0..15>

** PEG LANES REVERSED. ARD STRAP REQ'D. **

R0902 3.0K 5% 1/10W MF-LF 402
CPU_CFG<3>

DP_IG_ML_P<3..0> = DP_IG_B_ML_P<3..0>
DP_IG_ML_N<3..0> = DP_IG_B_ML_N<3..0>
DP_IG_AUX_CH_P
DP_IG_AUX_CH_N
DP_IG_DDC_CLK
DP_IG_DDC_DATA
DP_IG_HPD
TP_SATA_EXTA_D2R_N
TP_SATA_EXTA_D2R_P
TP_SATA_EXTA_R2D_C_N
TP_SATA_EXTA_R2D_C_P

NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3>
TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM

USB Hub Aliases

EXCARD_OC_L
USB_EXTC_OC_L
USB_EXCARD_N
USB_EXCARD_P

Rev. A NCs

NC_ISNS_P1V05S0PCH_N
NC_ISNS_P1V05S0PCH_P
NC_ISNS_P3V3S0MPCH_N
NC_ISNS_P3V3S0MPCH_P
NC_ISNS_PVTTS0PCH_N
NC_ISNS_PVTTS0PCH_P

Per WF: R0914 can't be stuffed, it will break CPU IMON Calculation.
It will be removed from the design after protol.

R0900 10 1% 1/10W MF-LF 402
PP1V8_S0GPU_ISNS
GPU_FB_A_VREF_DIV
R0901 10 1% 1/10W MF-LF 402
GPU_FB_B_VREF_DIV

AUDIO ALIASES

PP5V_S0
XW0900 PP5V_S0_AUDIO MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
XW0901 PP5V_S0_AUDIO_AMP_R MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
XW0902 PP5V_S0_AUDIO_AMP_L MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

BKLT_PWR_PBUS
R0904 0 5% 1/10W MF-LF 603
PPBUS_G3H
PPVIN_S0_LCDBKLT MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
R0903 0 5% 1/10W MF-LF 603
PP10V_FW
BKLT_PWR_FW10V

GMUX_VSYNC
BKL_SYNC
R0906 0 5% 1/16W MF-LF 402
R0907 0 5% 1/16W MF-LF 402
LVDS_CONN_BKL_SYNC
PANEL_VSYNC

Digital Ground

GND MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

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DMI

DMI_S2N_N<0>	F7	DMI_RX0*
DMI_S2N_N<1>	J8	DMI_RX1*
DMI_S2N_N<2>	K8	DMI_RX2*
DMI_S2N_N<3>	J4	DMI_RX3*
DMI_S2N_P<0>	F9	DMI_RX0
DMI_S2N_P<1>	J6	DMI_RX1
DMI_S2N_P<2>	K9	DMI_RX2
DMI_S2N_P<3>	J2	DMI_RX3
DMI_N2S_N<0>	H17	DMI_TX0*
DMI_N2S_N<1>	K15	DMI_TX1*
DMI_N2S_N<2>	J13	DMI_TX2*
DMI_N2S_N<3>	F16	DMI_TX3*
DMI_N2S_P<0>	G17	DMI_TX0
DMI_N2S_P<1>	M15	DMI_TX1
DMI_N2S_P<2>	G13	DMI_TX2
DMI_N2S_P<3>	J11	DMI_TX3

FLEXIBLE DISPLAY INTERFACE

FDI_DATA_N<0>	L2	FDI_TX0*
FDI_DATA_N<1>	N7	FDI_TX1*
FDI_DATA_N<2>	M4	FDI_TX2*
FDI_DATA_N<3>	P1	FDI_TX3*
FDI_DATA_N<4>	N10	FDI_TX4*
FDI_DATA_N<5>	R7	FDI_TX5*
FDI_DATA_N<6>	U7	FDI_TX6*
FDI_DATA_N<7>	W8	FDI_TX7*
FDI_DATA_P<0>	K1	FDI_TX0
FDI_DATA_P<1>	N5	FDI_TX1
FDI_DATA_P<2>	N2	FDI_TX2
FDI_DATA_P<3>	R2	FDI_TX3
FDI_DATA_P<4>	N9	FDI_TX4
FDI_DATA_P<5>	R8	FDI_TX5
FDI_DATA_P<6>	U6	FDI_TX6
FDI_DATA_P<7>	W10	FDI_TX7
FDI_FSYNC<0>	AC7	FDI_FSYNC0
FDI_FSYNC<1>	AC9	FDI_FSYNC1
FDI_INT	AB5	FDI_INT
FDI_LSYNC<0>	AA1	FDI_LSYNC0
FDI_LSYNC<1>	AB2	FDI_LSYNC1

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI	B12	CPU_PEG_COMP
PEG_ICOMPO	A13	
PEG_RCOMPO	D12	
PEG_RBIAS	B11	CPU_PEG_RBIAS
PEG_RX0*	G40	PEG_D2R_N<15>
PEG_RX1*	G38	PEG_D2R_N<14>
PEG_RX2*	H34	PEG_D2R_N<13>
PEG_RX3*	P34	PEG_D2R_N<12>
PEG_RX4*	G28	PEG_D2R_N<11>
PEG_RX5*	H25	PEG_D2R_N<10>
PEG_RX6*	H24	PEG_D2R_N<9>
PEG_RX7*	D29	PEG_D2R_N<8>
PEG_RX8*	B26	PEG_D2R_N<7>
PEG_RX9*	D26	PEG_D2R_N<6>
PEG_RX10*	B23	PEG_D2R_N<5>
PEG_RX11*	D22	PEG_D2R_N<4>
PEG_RX12*	A20	PEG_D2R_N<3>
PEG_RX13*	D19	PEG_D2R_N<2>
PEG_RX14*	A17	PEG_D2R_N<1>
PEG_RX15*	B14	PEG_D2R_N<0>
PEG_RX0	F40	PEG_D2R_P<15>
PEG_RX1	J38	PEG_D2R_P<14>
PEG_RX2	G34	PEG_D2R_P<13>
PEG_RX3	M34	PEG_D2R_P<12>
PEG_RX4	J28	PEG_D2R_P<11>
PEG_RX5	G25	PEG_D2R_P<10>
PEG_RX6	K24	PEG_D2R_P<9>
PEG_RX7	B28	PEG_D2R_P<8>
PEG_RX8	A27	PEG_D2R_P<7>
PEG_RX9	B25	PEG_D2R_P<6>
PEG_RX10	A24	PEG_D2R_P<5>
PEG_RX11	B21	PEG_D2R_P<4>
PEG_RX12	B19	PEG_D2R_P<3>
PEG_RX13	B18	PEG_D2R_P<2>
PEG_RX14	B16	PEG_D2R_P<1>
PEG_RX15	D15	PEG_D2R_P<0>
PEG_TX0*	N40	=PEG_R2D_C_N<0>
PEG_TX1*	L38	=PEG_R2D_C_N<1>
PEG_TX2*	M32	=PEG_R2D_C_N<2>
PEG_TX3*	D40	=PEG_R2D_C_N<3>
PEG_TX4*	A38	=PEG_R2D_C_N<4>
PEG_TX5*	G32	=PEG_R2D_C_N<5>
PEG_TX6*	B33	=PEG_R2D_C_N<6>
PEG_TX7*	B35	=PEG_R2D_C_N<7>
PEG_TX8*	L30	=PEG_R2D_C_N<8>
PEG_TX9*	A31	=PEG_R2D_C_N<9>
PEG_TX10*	B32	=PEG_R2D_C_N<10>
PEG_TX11*	L28	=PEG_R2D_C_N<11>
PEG_TX12*	N26	=PEG_R2D_C_N<12>
PEG_TX13*	M24	=PEG_R2D_C_N<13>
PEG_TX14*	G21	=PEG_R2D_C_N<14>
PEG_TX15*	J20	=PEG_R2D_C_N<15>
PEG_TX0	L40	=PEG_R2D_C_P<0>
PEG_TX1	N38	=PEG_R2D_C_P<1>
PEG_TX2	N32	=PEG_R2D_C_P<2>
PEG_TX3	B39	=PEG_R2D_C_P<3>
PEG_TX4	B37	=PEG_R2D_C_P<4>
PEG_TX5	H32	=PEG_R2D_C_P<5>
PEG_TX6	A34	=PEG_R2D_C_P<6>
PEG_TX7	D36	=PEG_R2D_C_P<7>
PEG_TX8	J30	=PEG_R2D_C_P<8>
PEG_TX9	B30	=PEG_R2D_C_P<9>
PEG_TX10	D33	=PEG_R2D_C_P<10>
PEG_TX11	N28	=PEG_R2D_C_P<11>
PEG_TX12	M25	=PEG_R2D_C_P<12>
PEG_TX13	N24	=PEG_R2D_C_P<13>
PEG_TX14	F21	=PEG_R2D_C_P<14>
PEG_TX15	L20	=PEG_R2D_C_P<15>

R1012 750 1% 1/16W MF-LF 402
R1010 49.9 1% 1/16W MF-LF 402

Embedded DisplayPort (eDP) pins (Auburndale only):

eDP_AUX#

NOTE: HPD must be inverted and level-shifted for Auburndale (1.05V).

eDP_HPD#
eDP_AUX

eDP_TX#<3>
eDP_TX#<2>
eDP_TX#<1>
eDP_TX#<0>

eDP_TX<3>
eDP_TX<2>
eDP_TX<1>
eDP_TX<0>

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CPU_CFG<0>	AL4	CFG0 (IPU)
CPU_CFG<1>	AM2	CFG1 (IPU)
CPU_CFG<2>	AK1	CFG2 (IPU)
CPU_CFG<3>	AK2	CFG3 (IPU)
CPU_CFG<4>	AK4	CFG4 (IPU)
CPU_CFG<5>	AJ2	CFG5 (IPU)
CPU_CFG<6>	AT2	CFG6 (IPU)
CPU_CFG<7>	AG7	CFG7 (IPU)
CPU_CFG<8>	AF4	CFG8 (IPU)
CPU_CFG<9>	AG2	CFG9 (IPU)
CPU_CFG<10>	AH1	CFG10 (IPU)
CPU_CFG<11>	AC2	CFG11 (IPU)
CPU_CFG<12>	AC4	CFG12 (IPU)
CPU_CFG<13>	AE2	CFG13 (IPU)
CPU_CFG<14>	AD1	CFG14 (IPU)
CPU_CFG<15>	AF8	CFG15 (IPU)
CPU_CFG<16>	AF6	CFG16 (IPU)
CPU_CFG<17>	AB7	CFG17 (IPU)

RESERVED

TP_CPU_RSVD_TP0	AU1	RSVD_TP0
TP_CPU_RSVD<15>	T4	RSVD15
TP_CPU_RSVD<16>	T2	RSVD16
TP_CPU_RSVD<17>	U1	RSVD17
TP_CPU_RSVD<18>	V2	RSVD18
TP_CPU_RSVD<19>	AV71	RSVD19
TP_CPU_RSVD<20>	AW70	RSVD20
TP_CPU_RSVD<21>	AY69	RSVD21
TP_CPU_RSVD<22>	BB69	RSVD22
TP_CPU_RSVD<23>	D8	RSVD23
TP_CPU_RSVD<24>	B7	RSVD24
TP_CPU_RSVD<26>	A10	RSVD26
TP_CPU_RSVD<27>	B9	RSVD27
NC_TP_CPU_RSVD_NCTF<7>	C5	RSVD_NCTF7
NC_TP_CPU_RSVD_NCTF<8>	A6	RSVD_NCTF8
NC_TP_CPU_RSVD_NCTF<6>	E3	RSVD_NCTF6
NC_TP_CPU_RSVD_NCTF<5>	F1	RSVD_NCTF5

RSVD32	W66	NC_TP_CPU_RSVD<32>
RSVD33	W64	NC_TP_CPU_RSVD<33>
RSVD34	AC69	NC_TP_CPU_RSVD<34>
RSVD35	AC71	NC_TP_CPU_RSVD<35>
RSVD36	AA71	NC_TP_CPU_RSVD<36>
RSVD37	AA69	NC_TP_CPU_RSVD<37>
RSVD38	R66	NC_TP_CPU_RSVD<38>
RSVD39	R64	NC_TP_CPU_RSVD<39>
RSVD_NCTF3	BT5	NC_TP_CPU_RSVD<40>
RSVD_NCTF4	BR5	NC_TP_CPU_RSVD<41>
RSVD_NCTF2	BV6	NC_TP_CPU_RSVD<42>
RSVD_NCTF1	BV8	NC_TP_CPU_RSVD<43>
RSVD45	AV69	TP_CPU_RSVD<45>
RSVD46	AK71	TP_CPU_RSVD<46>
RSVD47	AN69	TP_CPU_RSVD<47>
RSVD48	AP66	TP_CPU_RSVD<48>
RSVD49	AH66	TP_CPU_RSVD<49>
RSVD50	AK66	TP_CPU_RSVD<50>
RSVD51	AR71	TP_CPU_RSVD<51>
RSVD52	AM66	TP_CPU_RSVD<52>
RSVD53	AK69	TP_CPU_RSVD<53>
RSVD54	AU71	TP_CPU_RSVD<54>
RSVD55	AT70	TP_CPU_RSVD<55>
RSVD56	AR69	TP_CPU_RSVD<56>
RSVD57	AU69	TP_CPU_RSVD<57>
RSVD58	AT67	TP_CPU_RSVD<58>
RSVD_TP2	AP2	TP_CPU_RSVD<2>
RSVD_TP1	AN7	TP_CPU_RSVD<1>
RSVD62	AV4	CPU_THERMD_P
RSVD63	AU2	CPU_THERMD_N
RSVD64	BE69	TP_CPU_RSVD<64>
RSVD65	BE71	TP_CPU_RSVD<65>

DC_TEST_BV71	BV71	CPU_TEST_BV71_BV69
DC_TEST_BV69	BV69	
DC_TEST_BV68	BV68	TP_CPU_TEST_BV68
DC_TEST_BV5	BV5	TP_CPU_TEST_BV5
DC_TEST_BV3	BV3	CPU_TEST_BV3_BT3
DC_TEST_BV1	BV1	CPU_TEST_BV1_BT1
DC_TEST_BT71	BT71	CPU_TEST_BT71_BT69
DC_TEST_BT69	BT69	
DC_TEST_BT3	BT3	
DC_TEST_BT1	BT1	
DC_TEST_BR71	BR71	TP_CPU_TEST_BR71
DC_TEST_BR1	BR1	TP_CPU_TEST_BR1
DC_TEST_E71	E71	TP_CPU_TEST_E71
DC_TEST_E1	E1	TP_CPU_TEST_E1
DC_TEST_C71	C71	CPU_TEST_C71_A71
DC_TEST_C69	C69	CPU_TEST_C69_A69
DC_TEST_C3	C3	TP_CPU_TEST_C3
DC_TEST_A71	A71	
DC_TEST_A69	A69	
DC_TEST_A68	A68	TP_CPU_TEST_A68
DC_TEST_A5	A5	TP_CPU_TEST_A5

CFG0: PCIe Configuration Select 1 = Single PEG 0 = Bifurcation Enabled
CFG3: PCIe Lane Reversal 1 = Normal Operation 0 = Lanes Reversed
CFG4: Display Port Presence 1 = eDP Disabled 0 = Embedded Display Port Enabled

WF: RSVD nets with arrows have offpage marks on CRB schematic.
WF: RSVD nets with red wires have 0-ohm resistors to GND in CRB schematic.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

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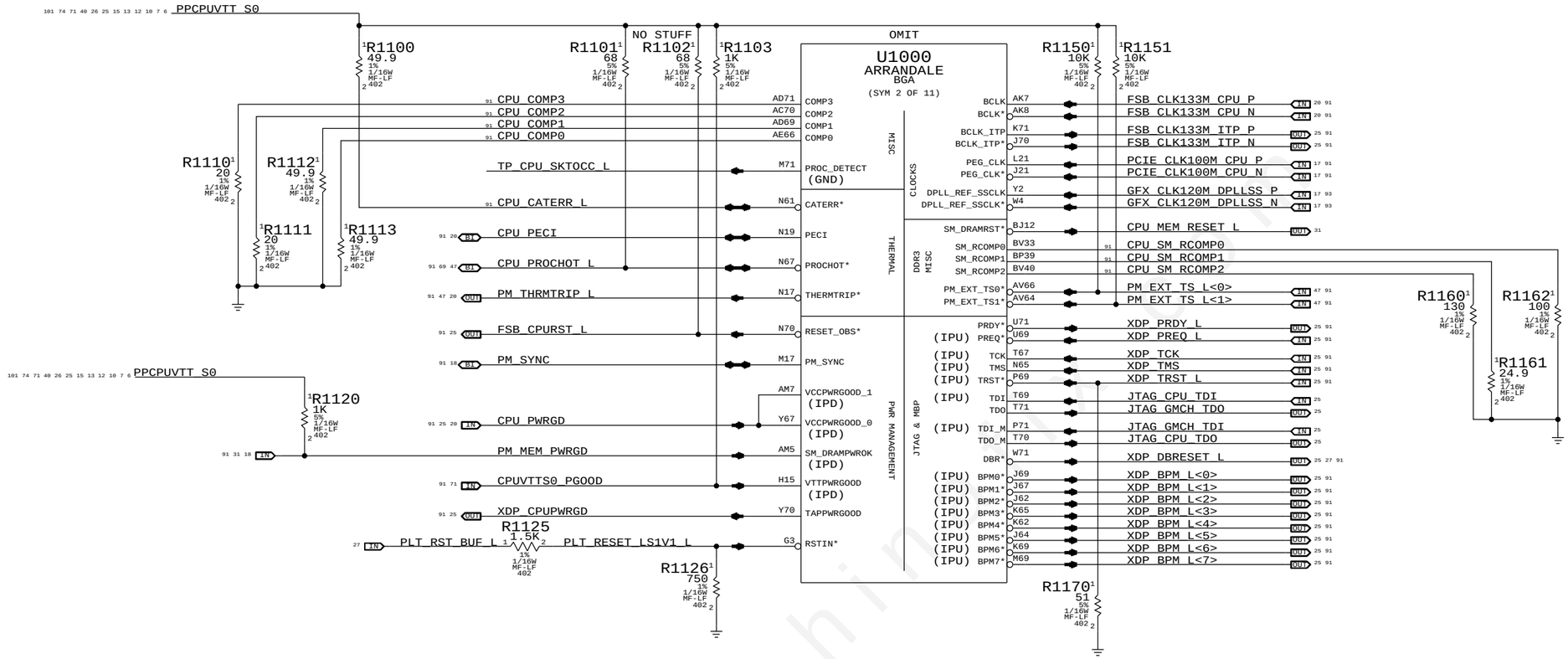

SYNC_MASTER=K18_MLB SYNC_DATE=10/14/2009

PAGE TITLE

CPU Clock/Misc/JTAG

Apple Inc.

DRAWING NUMBER — SIZE D

REVISION

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DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AT8	SA_DQ0	
MEM_A_DQ<1>	AT6	SA_DQ1	
MEM_A_DQ<2>	BB5	SA_DQ2	
MEM_A_DQ<3>	BB9	SA_DQ3	
MEM_A_DQ<4>	AV7	SA_DQ4	
MEM_A_DQ<5>	AV6	SA_DQ5	
MEM_A_DQ<6>	BE6	SA_DQ6	
MEM_A_DQ<7>	BE8	SA_DQ7	
MEM_A_DQ<8>	BF11	SA_DQ8	
MEM_A_DQ<9>	BE11	SA_DQ9	
MEM_A_DQ<10>	BK5	SA_DQ10	
MEM_A_DQ<11>	BH13	SA_DQ11	
MEM_A_DQ<12>	BF9	SA_DQ12	
MEM_A_DQ<13>	BF6	SA_DQ13	
MEM_A_DQ<14>	BK7	SA_DQ14	
MEM_A_DQ<15>	BN8	SA_DQ15	
MEM_A_DQ<16>	BN11	SA_DQ16	
MEM_A_DQ<17>	BN9	SA_DQ17	
MEM_A_DQ<18>	BG17	SA_DQ18	
MEM_A_DQ<19>	BK15	SA_DQ19	
MEM_A_DQ<20>	BK9	SA_DQ20	
MEM_A_DQ<21>	BG15	SA_DQ21	
MEM_A_DQ<22>	BH17	SA_DQ22	
MEM_A_DQ<23>	BK17	SA_DQ23	
MEM_A_DQ<24>	BN20	SA_DQ24	
MEM_A_DQ<25>	BN17	SA_DQ25	
MEM_A_DQ<26>	BK25	SA_DQ26	
MEM_A_DQ<27>	BH25	SA_DQ27	
MEM_A_DQ<28>	BJ20	SA_DQ28	
MEM_A_DQ<29>	BH21	SA_DQ29	
MEM_A_DQ<30>	BG24	SA_DQ30	
MEM_A_DQ<31>	BG25	SA_DQ31	
MEM_A_DQ<32>	BJ40	SA_DQ32	
MEM_A_DQ<33>	BM43	SA_DQ33	
MEM_A_DQ<34>	BF47	SA_DQ34	
MEM_A_DQ<35>	BF48	SA_DQ35	
MEM_A_DQ<36>	BN40	SA_DQ36	
MEM_A_DQ<37>	BH43	SA_DQ37	
MEM_A_DQ<38>	BN44	SA_DQ38	
MEM_A_DQ<39>	BN47	SA_DQ39	
MEM_A_DQ<40>	BN48	SA_DQ40	
MEM_A_DQ<41>	BN51	SA_DQ41	
MEM_A_DQ<42>	BH53	SA_DQ42	
MEM_A_DQ<43>	BJ55	SA_DQ43	
MEM_A_DQ<44>	BH48	SA_DQ44	
MEM_A_DQ<45>	BJ48	SA_DQ45	
MEM_A_DQ<46>	BM53	SA_DQ46	
MEM_A_DQ<47>	BN55	SA_DQ47	
MEM_A_DQ<48>	BF55	SA_DQ48	
MEM_A_DQ<49>	BN57	SA_DQ49	
MEM_A_DQ<50>	BN65	SA_DQ50	
MEM_A_DQ<51>	BJ61	SA_DQ51	
MEM_A_DQ<52>	BF57	SA_DQ52	
MEM_A_DQ<53>	BJ57	SA_DQ53	
MEM_A_DQ<54>	BK64	SA_DQ54	
MEM_A_DQ<55>	BK61	SA_DQ55	
MEM_A_DQ<56>	BJ63	SA_DQ56	
MEM_A_DQ<57>	BF64	SA_DQ57	
MEM_A_DQ<58>	BB64	SA_DQ58	
MEM_A_DQ<59>	BB66	SA_DQ59	
MEM_A_DQ<60>	BJ66	SA_DQ60	
MEM_A_DQ<61>	BF65	SA_DQ61	
MEM_A_DQ<62>	AY64	SA_DQ62	
MEM_A_DQ<63>	BC70	SA_DQ63	
MEM_A_BA<0>	BT38	SA_BS0	
MEM_A_BA<1>	BH38	SA_BS1	
MEM_A_BA<2>	BF21	SA_BS2	
MEM_A_CAS_L	BK43	SA_CAS*	
MEM_A_RAS_L	BL38	SA_RAS*	
MEM_A_WE_L	BF38	SA_WE*	

SA_CK0	BM34	MEM_A_CLK_P<0>	
SA_CK0*	BP35	MEM_A_CLK_N<0>	
SA_CKE0	BF20	MEM_A_CKE<0>	
SA_CK1	BK36	MEM_A_CLK_P<1>	
SA_CK1*	BH36	MEM_A_CLK_N<1>	
SA_CKE1	BK24	MEM_A_CKE<1>	
SA_CS0*	BH40	MEM_A_CS_L<0>	
SA_CS1*	BJ47	MEM_A_CS_L<1>	
SA_ODT0	BF43	MEM_A_ODT<0>	
SA_ODT1	BL47	MEM_A_ODT<1>	
SA_DM0	BB10	MEM_A_DM<0>	
SA_DM1	BJ10	MEM_A_DM<1>	
SA_DM2	BM15	MEM_A_DM<2>	
SA_DM3	BN24	MEM_A_DM<3>	
SA_DM4	BG44	MEM_A_DM<4>	
SA_DM5	BG53	MEM_A_DM<5>	
SA_DM6	BN62	MEM_A_DM<6>	
SA_DM7	BH59	MEM_A_DM<7>	
SA_DQS0*	AY5	MEM_A_DQS_N<0>	
SA_DQS1*	BJ7	MEM_A_DQS_N<1>	
SA_DQS2*	BN13	MEM_A_DQS_N<2>	
SA_DQS3*	BL21	MEM_A_DQS_N<3>	
SA_DQS4*	BH44	MEM_A_DQS_N<4>	
SA_DQS5*	BK51	MEM_A_DQS_N<5>	
SA_DQS6*	BP58	MEM_A_DQS_N<6>	
SA_DQS7*	BE62	MEM_A_DQS_N<7>	
SA_DQS0	AY7	MEM_A_DQS_P<0>	
SA_DQS1	BJ5	MEM_A_DQS_P<1>	
SA_DQS2	BL13	MEM_A_DQS_P<2>	
SA_DQS3	BN21	MEM_A_DQS_P<3>	
SA_DQS4	BK44	MEM_A_DQS_P<4>	
SA_DQS5	BH51	MEM_A_DQS_P<5>	
SA_DQS6	BM60	MEM_A_DQS_P<6>	
SA_DQS7	BE64	MEM_A_DQS_P<7>	
SA_MA0	BT36	MEM_A_A<0>	
SA_MA1	BP33	MEM_A_A<1>	
SA_MA2	BV36	MEM_A_A<2>	
SA_MA3	BG34	MEM_A_A<3>	
SA_MA4	BG32	MEM_A_A<4>	
SA_MA5	BN32	MEM_A_A<5>	
SA_MA6	BK32	MEM_A_A<6>	
SA_MA7	BJ30	MEM_A_A<7>	
SA_MA8	BN30	MEM_A_A<8>	
SA_MA9	BF28	MEM_A_A<9>	
SA_MA10	BH34	MEM_A_A<10>	
SA_MA11	BH30	MEM_A_A<11>	
SA_MA12	BJ28	MEM_A_A<12>	
SA_MA13	BF40	MEM_A_A<13>	
SA_MA14	BN28	MEM_A_A<14>	
SA_MA15	BN25	MEM_A_A<15>	

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DDR SYSTEM MEMORY B

MEM_B_DQ<0>	BA2	SB_DQ0	
MEM_B_DQ<1>	AW2	SB_DQ1	
MEM_B_DQ<2>	BD1	SB_DQ2	
MEM_B_DQ<3>	BE4	SB_DQ3	
MEM_B_DQ<4>	AY1	SB_DQ4	
MEM_B_DQ<5>	BC2	SB_DQ5	
MEM_B_DQ<6>	BF2	SB_DQ6	
MEM_B_DQ<7>	BH2	SB_DQ7	
MEM_B_DQ<8>	BG4	SB_DQ8	
MEM_B_DQ<9>	BG1	SB_DQ9	
MEM_B_DQ<10>	BR6	SB_DQ10	
MEM_B_DQ<11>	BR8	SB_DQ11	
MEM_B_DQ<12>	BJ4	SB_DQ12	
MEM_B_DQ<13>	BK2	SB_DQ13	
MEM_B_DQ<14>	BU9	SB_DQ14	
MEM_B_DQ<15>	BV10	SB_DQ15	
MEM_B_DQ<16>	BR10	SB_DQ16	
MEM_B_DQ<17>	BT12	SB_DQ17	
MEM_B_DQ<18>	BT15	SB_DQ18	
MEM_B_DQ<19>	BV15	SB_DQ19	
MEM_B_DQ<20>	BV12	SB_DQ20	
MEM_B_DQ<21>	BP12	SB_DQ21	
MEM_B_DQ<22>	BV17	SB_DQ22	
MEM_B_DQ<23>	BU16	SB_DQ23	
MEM_B_DQ<24>	BP15	SB_DQ24	
MEM_B_DQ<25>	BU19	SB_DQ25	
MEM_B_DQ<26>	BV22	SB_DQ26	
MEM_B_DQ<27>	BT22	SB_DQ27	
MEM_B_DQ<28>	BP19	SB_DQ28	
MEM_B_DQ<29>	BV19	SB_DQ29	
MEM_B_DQ<30>	BV20	SB_DQ30	
MEM_B_DQ<31>	BT20	SB_DQ31	
MEM_B_DQ<32>	BT48	SB_DQ32	
MEM_B_DQ<33>	BV48	SB_DQ33	
MEM_B_DQ<34>	BV50	SB_DQ34	
MEM_B_DQ<35>	BP49	SB_DQ35	
MEM_B_DQ<36>	BT47	SB_DQ36	
MEM_B_DQ<37>	BV52	SB_DQ37	
MEM_B_DQ<38>	BV54	SB_DQ38	
MEM_B_DQ<39>	BT54	SB_DQ39	
MEM_B_DQ<40>	BP53	SB_DQ40	
MEM_B_DQ<41>	BU53	SB_DQ41	
MEM_B_DQ<42>	BT59	SB_DQ42	
MEM_B_DQ<43>	BT57	SB_DQ43	
MEM_B_DQ<44>	BP56	SB_DQ44	
MEM_B_DQ<45>	BT55	SB_DQ45	
MEM_B_DQ<46>	BU60	SB_DQ46	
MEM_B_DQ<47>	BV59	SB_DQ47	
MEM_B_DQ<48>	BV61	SB_DQ48	
MEM_B_DQ<49>	BP60	SB_DQ49	
MEM_B_DQ<50>	BR66	SB_DQ50	
MEM_B_DQ<51>	BR64	SB_DQ51	
MEM_B_DQ<52>	BR62	SB_DQ52	
MEM_B_DQ<53>	BT61	SB_DQ53	
MEM_B_DQ<54>	BN68	SB_DQ54	
MEM_B_DQ<55>	BL69	SB_DQ55	
MEM_B_DQ<56>	BJ71	SB_DQ56	
MEM_B_DQ<57>	BF70	SB_DQ57	
MEM_B_DQ<58>	BG71	SB_DQ58	
MEM_B_DQ<59>	BC67	SB_DQ59	
MEM_B_DQ<60>	BK70	SB_DQ60	
MEM_B_DQ<61>	BK67	SB_DQ61	
MEM_B_DQ<62>	BD71	SB_DQ62	
MEM_B_DQ<63>	BD69	SB_DQ63	
MEM_B_BA<0>	BV43	SB_BS0	
MEM_B_BA<1>	BV41	SB_BS1	
MEM_B_BA<2>	BV24	SB_BS2	
MEM_B_CAS_L	BU46	SB_CAS*	
MEM_B_RAS_L	BT40	SB_RAS*	
MEM_B_WE_L	BT41	SB_WE*	

SB_CK0	BU33	MEM_B_CLK_P<0>	
SB_CK0*	BV34	MEM_B_CLK_N<0>	
SB_CKE0	BT26	MEM_B_CKE<0>	
SB_CK1	BV38	MEM_B_CLK_P<1>	
SB_CK1*	BU39	MEM_B_CLK_N<1>	
SB_CKE1	BT24	MEM_B_CKE<1>	
SB_CS0*	BP46	MEM_B_CS_L<0>	
SB_CS1*	BT43	MEM_B_CS_L<1>	
SB_ODT0	BV45	MEM_B_ODT<0>	
SB_ODT1	BU49	MEM_B_ODT<1>	
SB_DM0	BB4	MEM_B_DM<0>	
SB_DM1	BL4	MEM_B_DM<1>	
SB_DM2	BT13	MEM_B_DM<2>	
SB_DM3	BP22	MEM_B_DM<3>	
SB_DM4	BV47	MEM_B_DM<4>	
SB_DM5	BV57	MEM_B_DM<5>	
SB_DM6	BU65	MEM_B_DM<6>	
SB_DM7	BF67	MEM_B_DM<7>	
SB_DQS0*	BE2	MEM_B_DQS_N<0>	
SB_DQS1*	BM3	MEM_B_DQS_N<1>	
SB_DQS2*	BU12	MEM_B_DQS_N<2>	
SB_DQS3*	BT19	MEM_B_DQS_N<3>	
SB_DQS4*	BT52	MEM_B_DQS_N<4>	
SB_DQS5*	BV55	MEM_B_DQS_N<5>	
SB_DQS6*	BU63	MEM_B_DQS_N<6>	
SB_DQS7*	BG69	MEM_B_DQS_N<7>	
SB_DQS0	BD4	MEM_B_DQS_P<0>	
SB_DQS1	BN4	MEM_B_DQS_P<1>	
SB_DQS2	BV13	MEM_B_DQS_P<2>	
SB_DQS3	BT17	MEM_B_DQS_P<3>	
SB_DQS4	BT50	MEM_B_DQS_P<4>	
SB_DQS5	BU56	MEM_B_DQS_P<5>	
SB_DQS6	BV62	MEM_B_DQS_P<6>	
SB_DQS7	BJ69	MEM_B_DQS_P<7>	
SB_MA0	BT34	MEM_B_A<0>	
SB_MA1	BP30	MEM_B_A<1>	
SB_MA2	BV29	MEM_B_A<2>	
SB_MA3	BU30	MEM_B_A<3>	
SB_MA4	BV31	MEM_B_A<4>	
SB_MA5	BT33	MEM_B_A<5>	
SB_MA6	BT31	MEM_B_A<6>	
SB_MA7	BP26	MEM_B_A<7>	
SB_MA8	BV27	MEM_B_A<8>	
SB_MA9	BT27	MEM_B_A<9>	
SB_MA10	BU42	MEM_B_A<10>	
SB_MA11	BU26	MEM_B_A<11>	
SB_MA12	BT29	MEM_B_A<12>	
SB_MA13	BT45	MEM_B_A<13>	
SB_MA14	BV26	MEM_B_A<14>	
SB_MA15	BU23	MEM_B_A<15>	

SYNC_MASTER=K17_REF SYNC_DATE=04/29/2009

PAGE TITLE
CPU DDR3 Interfaces

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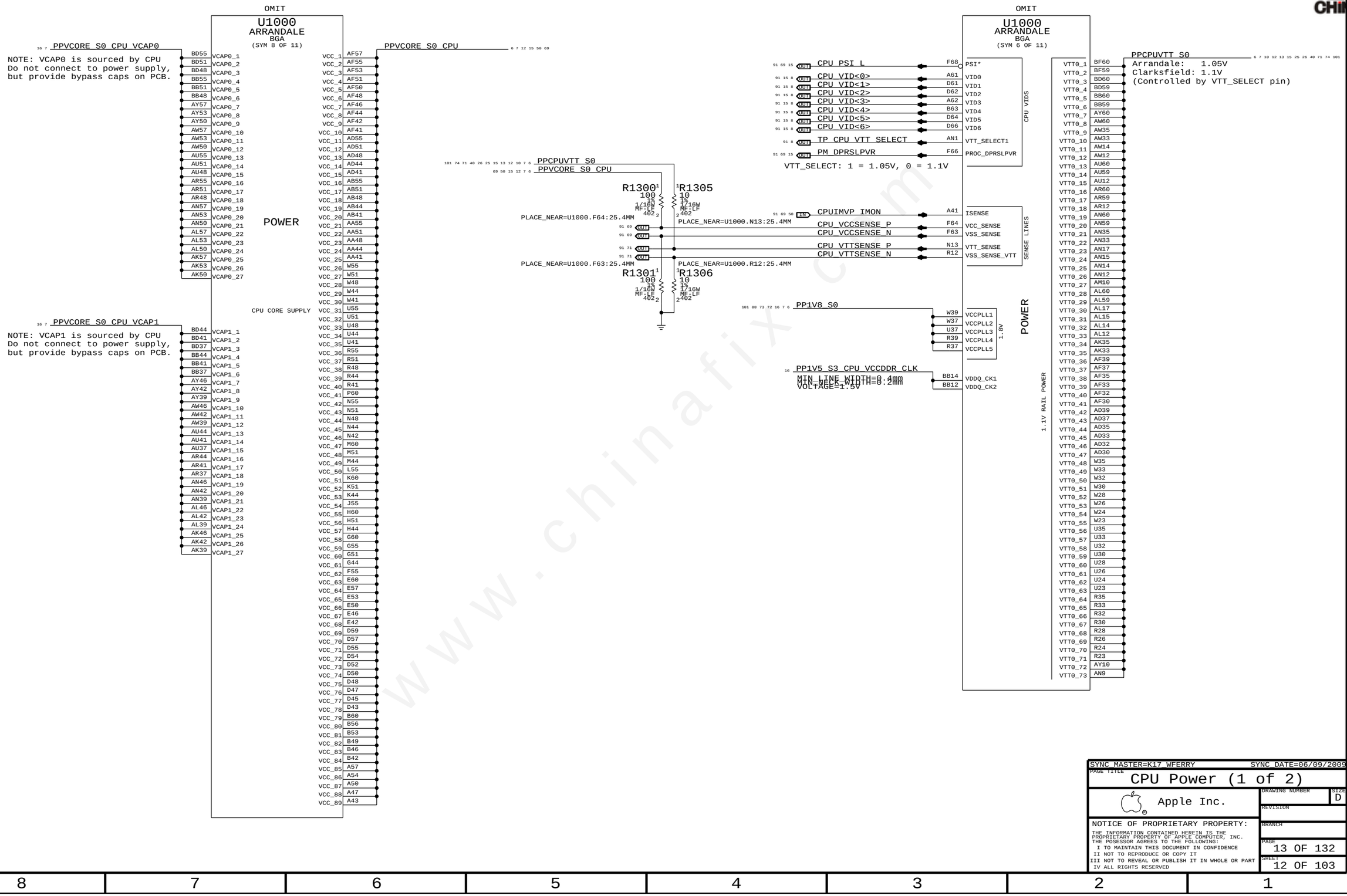
OMIT
U1000
ARRANDALE
BGA
(SYM 8 OF 11)
POWER
CPU CORE SUPPLY
PPVCORE_S0_CPU_VCAP0
NOTE: VCAP0 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.
PPVCORE_S0_CPU_VCAP1
NOTE: VCAP1 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.
PPVCORE_S0_CPU
PPCPUVTT_S0
PPVCORE_S0_CPU
R1300 100 1% 1/16W MF-LF 402
R1305 10 1% 1/16W MF-LF 402
R1301 100 1% 1/16W MF-LF 402
R1306 10 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.F64:25.4MM
PLACE_NEAR=U1000.N13:25.4MM
PLACE_NEAR=U1000.F63:25.4MM
PLACE_NEAR=U1000.R12:25.4MM
CPU_PSI_L
CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
TP_CPU_VTT_SELECT
PM_DPRSLPVR
VTT_SELECT: 1 = 1.05V, 0 = 1.1V
CPUIMVP_IMON
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VTTSENSE_P
CPU_VTTSENSE_N
PP1V8_S0
PP1V5_S3_CPU_VCCDDR_CLK
MIN_LINE_WIDTH=0.4mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V
OMIT
U1000
ARRANDALE
BGA
(SYM 6 OF 11)
CPU VIDS
SENSE LINES
POWER
1.1V RAIL POWER
PPCPUVTT_S0
Arrandale: 1.05V
Clarksfield: 1.1V
(Controlled by VTT_SELECT pin)
SYNC_MASTER=K17 WFERRY
SYNC_DATE=06/09/2009
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OMIT

U1000
ARRANDALE
BGA
(SYM 7 OF 11)

70 50 24 13 7 PPVCORE_S0_GFX

AN32	VAXG1	
AN30	VAXG2	
AN28	VAXG3	
AN26	VAXG4	
AN24	VAXG5	
AN23	VAXG6	
AN21	VAXG7	
AN19	VAXG8	
AL32	VAXG9	
AL30	VAXG10	
AL28	VAXG11	
AL26	VAXG12	
AL24	VAXG13	
AL23	VAXG14	
AL21	VAXG15	
AL19	VAXG16	
AK14	VAXG17	
AK12	VAXG18	
AJ10	VAXG19	
AH14	VAXG20	
AH12	VAXG21	
AF28	VAXG22	
AF26	VAXG23	
AF24	VAXG24	
AF23	VAXG25	
AF21	VAXG26	
AF19	VAXG27	
AF17	VAXG28	
AF15	VAXG29	
AF14	VAXG30	
AD28	VAXG31	
AD26	VAXG32	
AD24	VAXG33	
AD23	VAXG34	
AD21	VAXG35	
AD19	VAXG36	
AD17	VAXG37	

GRAPHICS

101 74 71 40 26 25 15 13 12 10 7 6 PPCPUVTT_S0

W21	VTT1_1
W19	VTT1_2
U21	VTT1_3
U19	VTT1_4
U17	VTT1_5
U15	VTT1_6
U14	VTT1_7
U12	VTT1_8
R21	VTT1_9
R19	VTT1_10
R17	VTT1_11

PEG & DMI

24 7 PPVCORE_S0_CPU_VCAP2

AK62	VCAP2_1
AK60	VCAP2_2
AK59	VCAP2_3
AH60	VCAP2_4
AH59	VCAP2_5
AF60	VCAP2_6
AF59	VCAP2_7
AD60	VCAP2_8
AD59	VCAP2_9
AB60	VCAP2_10
AB59	VCAP2_11
AA60	VCAP2_12
AA59	VCAP2_13
W60	VCAP2_14
W59	VCAP2_15
U60	VCAP2_16
U59	VCAP2_17
R60	VCAP2_18
R59	VCAP2_19

NOTE: VCAP2 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.

SENSE LINES

VAXG_SENSE	AF12	GFX_VSENSE_P
VSSAXG_SENSE	AF10	GFX_VSENSE_N

GRAPHICS VIDS

GFX_VID0	AF71	GFX_VID<0> OUT 8 91
GFX_VID1	AG67	GFX_VID<1> OUT 8 91
GFX_VID2	AG70	GFX_VID<2> OUT 8 91
GFX_VID3	AH71	GFX_VID<3> OUT 8 91
GFX_VID4	AN71	GFX_VID<4> OUT 8 91
GFX_VID5	AM67	GFX_VID<5> OUT 8 91
GFX_VID6	AM70	GFX_VID<6> OUT 8 91
GFX_VR_EN	AH69	GFX_VR_EN OUT 70 91
GFX_DPRSLPVR	AL71	GFX_DPRSLPVR OUT 70 91
GFX_IMON	AL69	GFXIMVP_IMON IN 70 91

70 50 24 13 7 PPVCORE_S0_GFX

R1400 1
100
1%
1/10W
MF-LF
402 2

PLACE_NEAR=U1000.AF12:25.4MM
OUT 70 91

PLACE_NEAR=U1000.AF10:25.4MM
OUT 70 91

R1401 1
100
1%
1/10W
MF-LF
402 2

OUT 70 91

R1405 1
4.7K
5%
1/10W
MF-LF
402 2

PPCPUDDR_ISNS 7 16 31 57

DDR3 ~1.5 V RAILS

VDDQ1	BU40
VDDQ2	BU35
VDDQ3	BU28
VDDQ4	BN38
VDDQ5	BM25
VDDQ6	BL30
VDDQ7	BJ38
VDDQ8	BH32
VDDQ9	BH28
VDDQ10	BG43
VDDQ11	BF16
VDDQ12	BF15
VDDQ13	BD35
VDDQ14	BD33
VDDQ15	BD32
VDDQ16	BD30
VDDQ17	BD28
VDDQ18	BD26
VDDQ19	BD24
VDDQ20	BD23
VDDQ21	BD21
VDDQ22	BD19
VDDQ23	BD17
VDDQ24	BD15
VDDQ25	BB35
VDDQ26	BB33
VDDQ27	BB32
VDDQ28	BB30
VDDQ29	BB28
VDDQ30	BB26
VDDQ31	BB24
VDDQ32	BB23
VDDQ33	BB21
VDDQ34	BB19
VDDQ35	BB17
VDDQ36	BB15

POWER

PP1V1R1V05_S0_CPU_VTT0_DDR 15

VTT0_DDR	AW32
VTT0_DDR1	AW30
VTT0_DDR2	AW28
VTT0_DDR3	AW26
VTT0_DDR4	AW24
VTT0_DDR5	AW23
VTT0_DDR6	AW21
VTT0_DDR7	AW19
VTT0_DDR8	AW17
VTT0_DDR9	AW15

PPCPUVTT_S0 6 7 10 12 13 15 25 26 40 71 74 101

VTT1_12	AD15
VTT1_13	AD14
VTT1_14	AD12
VTT1_15	AB12
VTT1_16	AA12
VTT1_17	W17
VTT1_18	W15
VTT1_19	W14
VTT1_20	W12
VTT1_21	R15

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BU62	VSS1	VSS76	AY62
BU58	VSS2	VSS77	AY59
BU55	VSS3	VSS78	AY55
BU51	VSS4	VSS79	AY51
BU48	VSS5	VSS80	AY48
BU44	VSS6	VSS81	AY44
BU37	VSS7	VSS82	AY41
BU32	VSS8	VSS83	AY37
BU25	VSS9	VSS84	AY35
BU21	VSS10	VSS85	AY33
BU18	VSS11	VSS86	AY32
BU14	VSS12	VSS87	AY30
BU11	VSS13	VSS88	AY28
BU7	VSS14	VSS89	AY26
BP42	VSS15	VSS90	AY24
BN64	VSS16	VSS91	AY23
BN6	VSS17	VSS92	AY21
BM70	VSS18	VSS93	AY19
BM51	VSS19	VSS94	AY17
BM44	VSS20	VSS95	AY15
BM32	VSS21	VSS96	AY14
BM24	VSS22	VSS97	AY12
BM17	VSS23	VSS98	AY8
BL57	VSS24	VSS99	AY4
BL55	VSS25	VSS100	AW67
BL48	VSS26	VSS101	AW62
BL40	VSS27	VSS102	AW59
BL28	VSS28	VSS103	AW55
BL20	VSS29	VSS104	AW51
BK63	VSS30	VSS105	AW48
BK60	VSS31	VSS106	AW44
BK53	VSS32	VSS107	AW41
BK34	VSS33	VSS108	AW37
BK10	VSS34	VSS109	AV9
BJ64	VSS35	VSS110	AV1
BJ21	VSS36	VSS111	AU70
BJ9	VSS37	VSS112	AU62
BJ1	VSS38	VSS113	AU57
BH70	VSS39	VSS114	AU53
BH57	VSS40	VSS115	AU50
BH55	VSS41	VSS116	AU46
BH47	VSS42	VSS117	AU42
BH24	VSS43	VSS118	AU39
BH20	VSS44	VSS119	AU35
BH15	VSS45	VSS120	AU33
BG51	VSS46	VSS121	AU32
BG36	VSS47	VSS122	AU30
BF62	VSS48	VSS123	AU28
BF30	VSS49	VSS124	AU26
BF13	VSS50	VSS125	AU24
BF8	VSS51	VSS126	AU23
BE70	VSS52	VSS127	AU21
BE65	VSS53	VSS128	AU19
BE9	VSS54	VSS129	AU17
BE1	VSS55	VSS130	AU15
BD57	VSS56	VSS131	AU14
BD53	VSS57	VSS132	AU4
BD50	VSS58	VSS133	AT64
BD46	VSS59	VSS134	AT10
BD42	VSS60	VSS135	AR62
BD39	VSS61	VSS136	AR57
BD14	VSS62	VSS137	AR53
BB71	VSS63	VSS138	AR50
BB62	VSS64	VSS139	AR46
BB57	VSS65	VSS140	AR42
BB53	VSS66	VSS141	AR39
BB50	VSS67	VSS142	AR35
BB46	VSS68	VSS143	AR33
BB42	VSS69	VSS144	AR32
BB39	VSS70	VSS145	AR30
BB7	VSS71	VSS146	AR28
BB1	VSS72	VSS147	AR26
BA70	VSS73	VSS148	AR24
AY71	VSS74	VSS149	AR23
AY66	VSS75	VSS150	AR21

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AR19	VSS151	VSS226	BN71
AR17	VSS152	VSS227	E68
AR15	VSS153	VSS228	AH28
AR14	VSS154	VSS229	AH41
AR4	VSS155	VSS230	A66
AR1	VSS156	VSS231	AH26
AP70	VSS157	VSS232	BN1
AP64	VSS158	VSS233	A64
AN62	VSS159	VSS234	AH24
AN55	VSS160	VSS235	AH39
AN51	VSS161	VSS236	E5
AN48	VSS162	VSS237	AH23
AN44	VSS163	VSS238	C68
AN41	VSS164	VSS239	AH21
AN37	VSS165	VSS240	AH19
AN5	VSS166	VSS241	AH17
AN4	VSS167	VSS242	AH15
AM64	VSS168	VSS243	AH4
AM8	VSS169	VSS244	AG64
AL62	VSS170	VSS245	AG9
AL55	VSS171	VSS246	AG6
AL51	VSS172	VSS247	AF69
AL48	VSS173	VSS248	AF62
AL44	VSS174	VSS249	AF1
AL41	VSS175	VSS250	AE70
AL37	VSS176	VSS251	AE64
AL35	VSS177	VSS252	AD62
AL33	VSS178	VSS253	AD57
AL1	VSS179	VSS254	AD53
AK70	VSS180	VSS255	AD50
AK64	VSS181	VSS256	AD46
AK55	VSS182	VSS257	AD42
AK51	VSS183	VSS258	AD4
AK48	VSS184	VSS259	AC67
AK44	VSS185	VSS260	AC64
AK41	VSS186	VSS261	AC10
AK37	VSS187	VSS262	AC5
AK32	VSS188	VSS263	AC1
AK30	VSS189	VSS264	AB70
AK28	VSS190	VSS265	AB62
AK26	VSS191	VSS266	AB57
AK24	VSS192	VSS267	AB53
AK23	VSS193	VSS268	AB50
AK21	VSS194	VSS269	AB46
AK19	VSS195	VSS270	AB42
AK17	VSS196	VSS271	AB39
AK15	VSS197	VSS272	AB37
AJ70	VSS198	VSS273	AB35
AH62	VSS199	VSS274	AB33
AH57	VSS200	VSS275	AB32
AH55	VSS201	VSS276	AB30
AH53	VSS202	VSS277	AB28
BV66	VSS203	VSS278	AB26
AH51	VSS204	VSS279	AB24
BV64	VSS205	VSS280	AB23
AH50	VSS206	VSS281	AB21
BT68	VSS207	VSS282	AB19
AH48	VSS208	VSS283	AB17
BR69	VSS209	VSS284	AB15
BL71	VSS210	VSS285	AB14
AH46	VSS211	VSS286	AB9
BL1	VSS212	VSS287	AA66
AH37	VSS213	VSS288	AA64
BR68	VSS214	VSS289	AA62
R14	VSS215	VSS290	AA57
AH35	VSS216	VSS291	AA53
AH44	VSS217	VSS292	AA50
H71	VSS218	VSS293	AA46
AH33	VSS219	VSS294	AA42
BR3	VSS220	VSS295	AA39
F71	VSS221	VSS296	AA37
AH32	VSS222	VSS297	AA35
AH42	VSS223	VSS298	AA33
E69	VSS224	VSS299	AA32
AH30	VSS225	VSS300	AA30

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AA28	VSS301	VSS367	K6
AA26	VSS302	VSS368	K4
AA24	VSS303	VSS369	J65
AA23	VSS304	VSS370	J57
AA21	VSS305	VSS371	J48
AA19	VSS306	VSS372	J47
AA17	VSS307	VSS373	J40
AA15	VSS308	VSS374	J9
AA14	VSS309	VSS375	H53
AA4	VSS310	VSS376	H43
W69	VSS311	VSS377	H36
W62	VSS312	VSS378	H1
W57	VSS313	VSS379	G70
W53	VSS314	VSS380	G57
W50	VSS315	VSS381	G53
W46	VSS316	VSS382	G48
W42	VSS317	VSS383	G47
W6	VSS318	VSS384	G43
W1	VSS319	VSS385	G30
V70	VSS320	VSS386	G24
U64	VSS321	VSS387	G20
U62	VSS322	VSS388	G15
U57	VSS323	VSS389	F61
U53	VSS324	VSS390	F48
U50	VSS325	VSS391	F47
U46	VSS326	VSS392	F28
U42	VSS327	VSS393	F20
U39	VSS328	VSS394	F4
U9	VSS329	VSS395	E37
U4	VSS330	VSS396	E33
T1	VSS331	VSS397	E30
R70	VSS332	VSS398	E16
R62	VSS333	VSS399	E12
R57	VSS334	VSS400	D41
R53	VSS335	VSS401	D38
R50	VSS336	VSS402	D34
R46	VSS337	VSS403	D31
R42	VSS338	VSS404	D27
R5	VSS339	VSS405	D24
P4	VSS340	VSS406	D20
N63	VSS341	VSS407	D17
N57	VSS342	VSS408	D13
N53	VSS343	VSS409	D10
N50	VSS344	VSS410	D6
N46	VSS345	VSS411	B65
N30	VSS346	VSS412	B62
N21	VSS347	VSS413	B58
N15	VSS348	VSS414	B55
M53	VSS349	VSS415	B51
M42	VSS350	VSS416	B48
M36	VSS351	VSS417	B44
M1	VSS352	VSS418	A59
L70	VSS353	VSS419	A55
L57	VSS354	VSS420	A52
L48	VSS355	VSS421	A48
L47	VSS356	VSS422	A45
L13	VSS357	VSS423	A40
K64	VSS358	VSS424	A36
K53	VSS359	VSS425	A33
K43	VSS360	VSS426	A29
K36	VSS361	VSS427	A26
K34	VSS362	VSS428	A22
K32	VSS363	VSS429	A19
K25	VSS364	VSS430	A15
K17	VSS365	VSS431	A12
K11	VSS366	VSS432	A8
		VSS433	B40

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CPU Grounds

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CPU VCore HF and Bulk Decoupling

3x 470uF 4.5mOhm, 1x 330uF, 15x 22uF 0603, 25x 1uF 0402

PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..

69 50 12 7 6 PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612
1UF 10% 16V X5R 402

C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
1UF 10% 16V X5R 402

PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.

NO STUFF C1626 C1627 NO STUFF C1628 C1629 NO STUFF C1630 NO STUFF C1631 NO STUFF C1632 C1633 C1634 C1691 C1694 C1698
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

NO STUFF C1635 C1637 C1638 NO STUFF C1639 C1640 NO STUFF C1641 C1643 C1644 C1645 NO STUFF C1646 C1647 NO STUFF C1648 C1699
22UF 20% 6.3V X5R-CERM 603

C1649 330UF 20% 2.0V POLY-TANT D2T-SM2

C1650 C1651 C1652 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NO STUFF C16A0 C16A1 C16A2 C16A3 C16A4 62UF 20% 11V ELEC CASE-B2

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

101 74 71 40 26 25 15 13 12 10 7 6 PPCPUVTT_S0

R1600 R1602 CPUPOC4U R1604 NO STUFF R1606 NO STUFF R1608
R1601 CPUPOC3U R1603 CPUPOC5U R1605 R1607
1K 5% 1/16W MF-LF 402

91 12 8 OUT CPU_VID<0>
91 12 8 OUT CPU_VID<1>
91 12 8 OUT CPU_VID<2>
91 12 8 OUT CPU_VID<3>
91 12 8 OUT CPU_VID<4>
91 12 8 OUT CPU_VID<5>
91 12 8 OUT CPU_VID<6>
91 69 12 OUT PM_DPRSLPVR
91 69 12 OUT CPU_PSI_L

R1610 NO STUFF R1612 CPUPOC4D R1614 R1616 R1618
NO STUFF R1611 CPUPOC3D R1613 CPUPOC5D R1615 NO STUFF R1617
1K 5% 1/16W MF-LF 402

VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_20	20A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_20_30	30A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_30_40	40A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_40_50	50A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_50_60	60A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_60_70	70A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_70_90	90A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly. Instead call out appropriate BOM GROUP defined in tables above.

VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000.

15 13 12 10 7 6 PPCPUVTT_S0

C1653 C1654 C1655 C1656
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..

C1657 C1658 C1659 C1660 C1661 C1662 C1663
10UF 20% 6.3V X5R 603

PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.

C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675
1UF 10% 10V X5R 402

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686 C1687
1UF 10% 10V X5R 402

C1688 C1689 C1690
330UF 20% 2.0V POLY-TANT D2T-SM2

VTT0_DDR DECOUPLING

3x 1uF 0402

PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.

L1695 30-OHM-5A 0603

PP1V1R1V05_S0_CPU_VTT0_DDR 13
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

C1695 C1696 C1697
1UF 10% 10V X5R 402

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: CPU Non-GFX Decoupling (1 of 2)

Apple Inc.

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Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

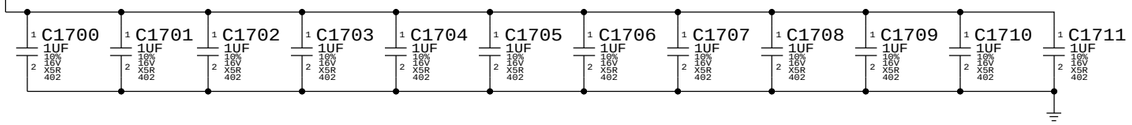
VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP0



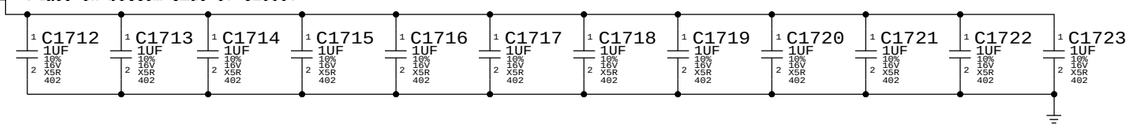
VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

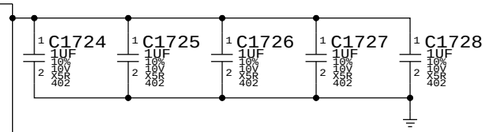
12 7 PPVCORE_S0_CPU_VCAP1



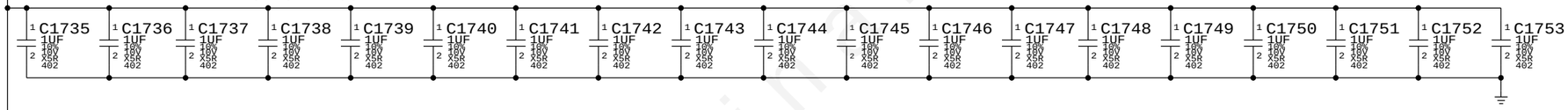
Memory (CPU VCCDDR) DECOUPLING

5x 1uF 0402

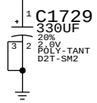
57 31 16 13 7 PPCPUDDR_ISNS



NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.



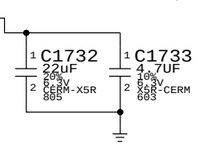
NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. 2x330uF on CSA73. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

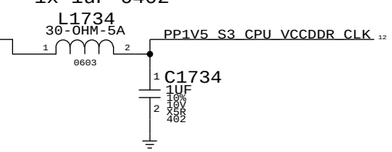
88 73 72 12 7 6 101 PP1V8_S0



DDR Clock (CPU VDDQ_CK) DECOUPLING

1x 1uF 0402

57 31 16 13 7 PPCPUDDR_ISNS



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F
actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC_MASTER=K17_REF SYNC_DATE=06/24/2009

PAGE TITLE: CPU Non-GFX Decoupling (2 of 2)

Apple Inc.

DRAWING NUMBER: | SIZE: D

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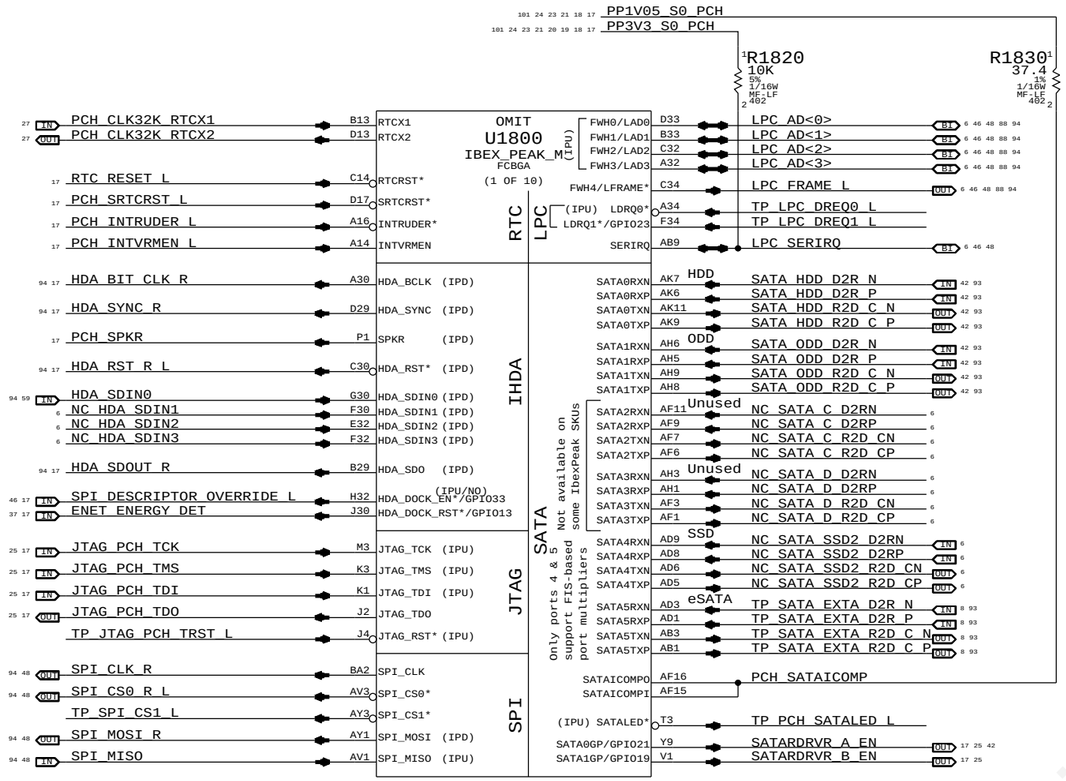

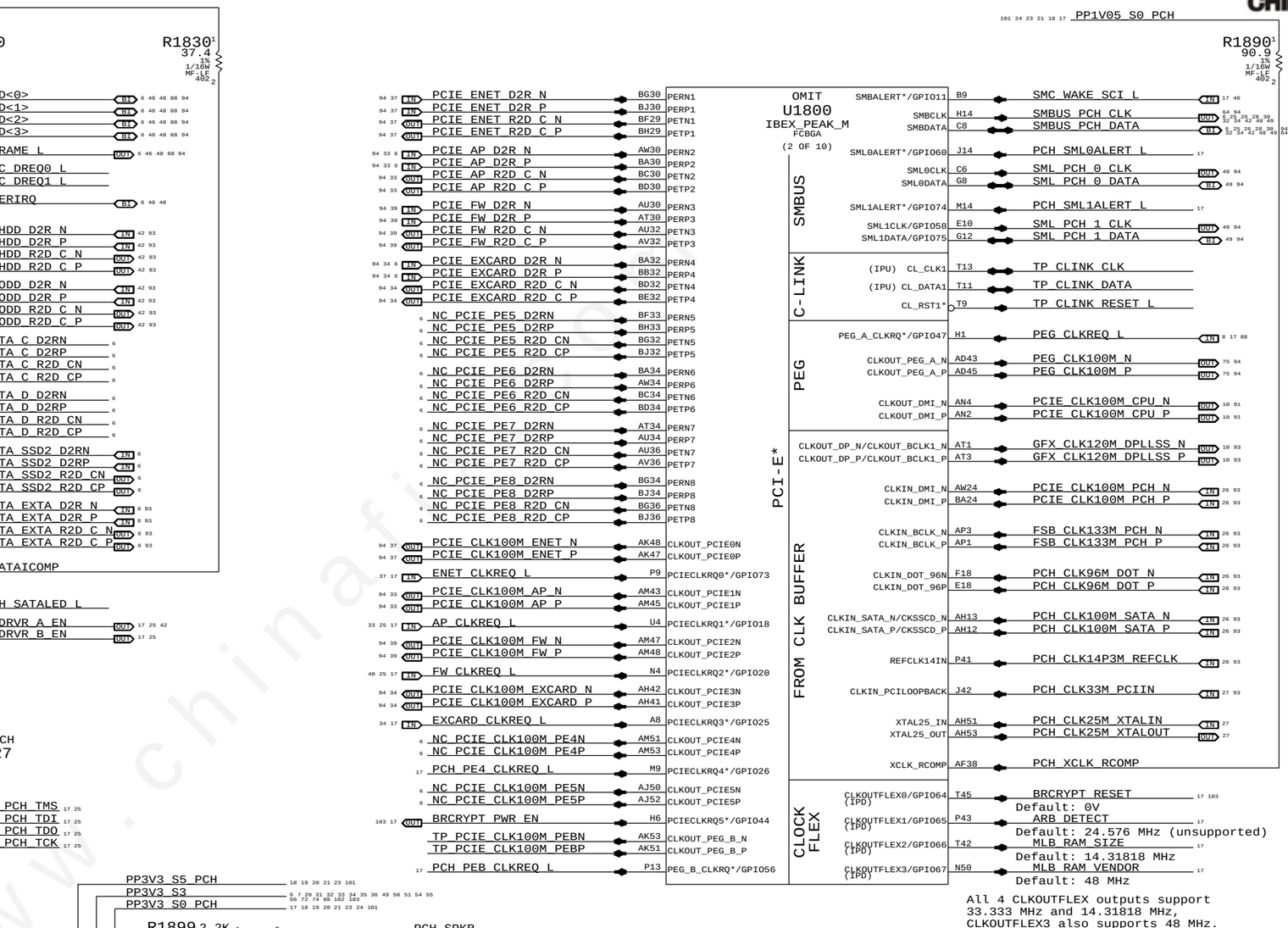

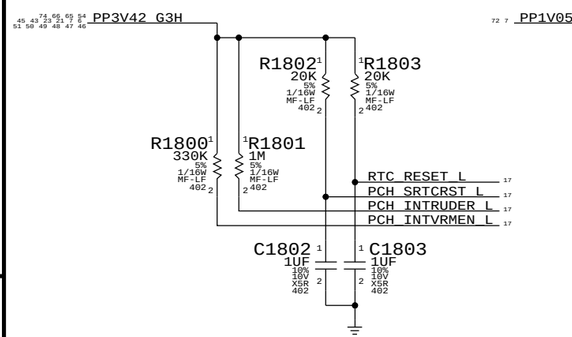

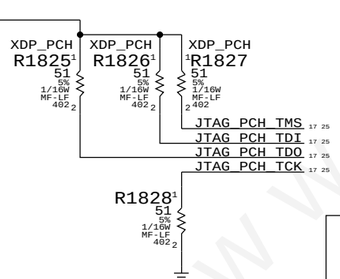

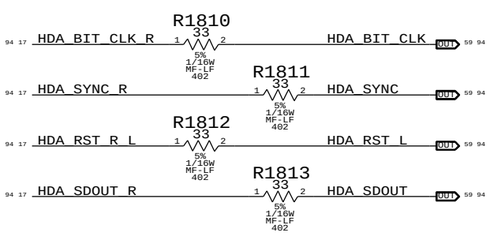

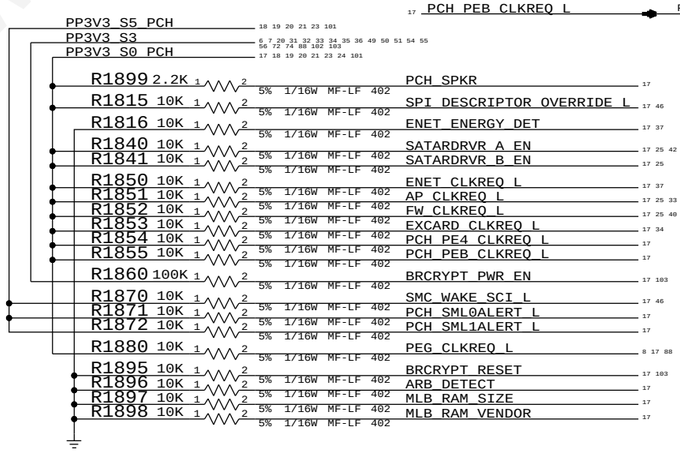

SYNC_MASTER=K17_REF SYNC_DATE=08/24/2009

PAGE TITLE

PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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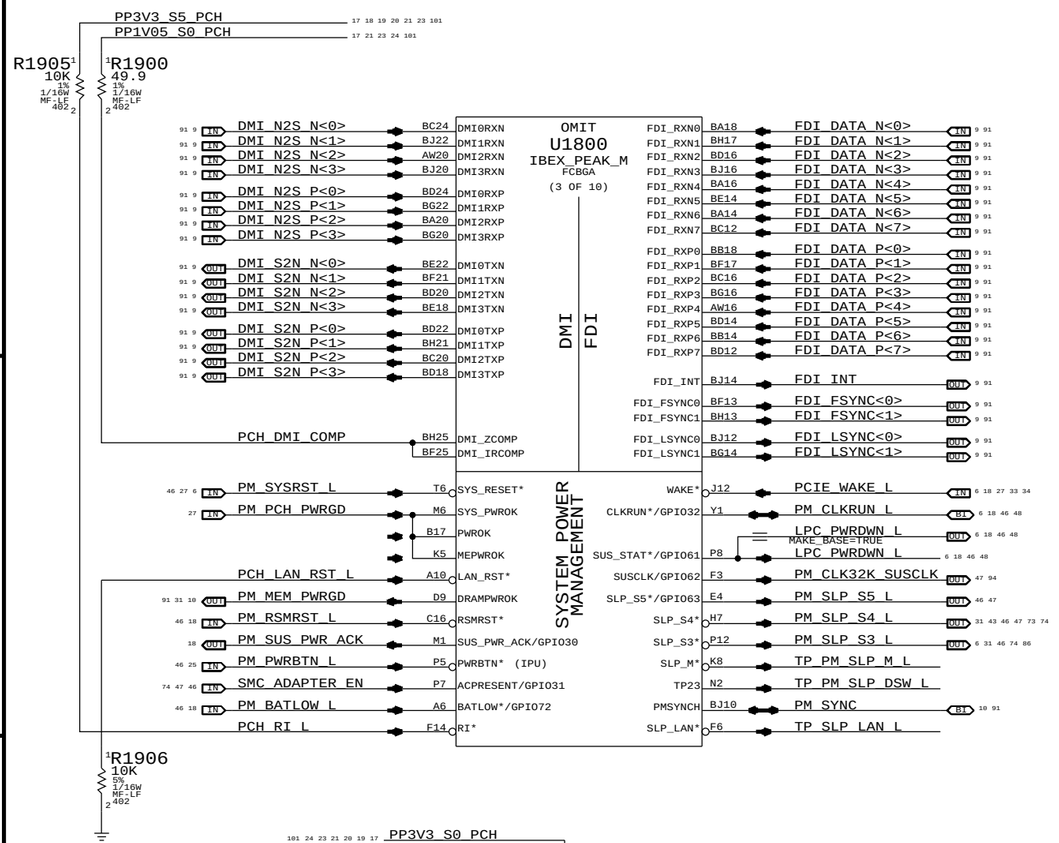

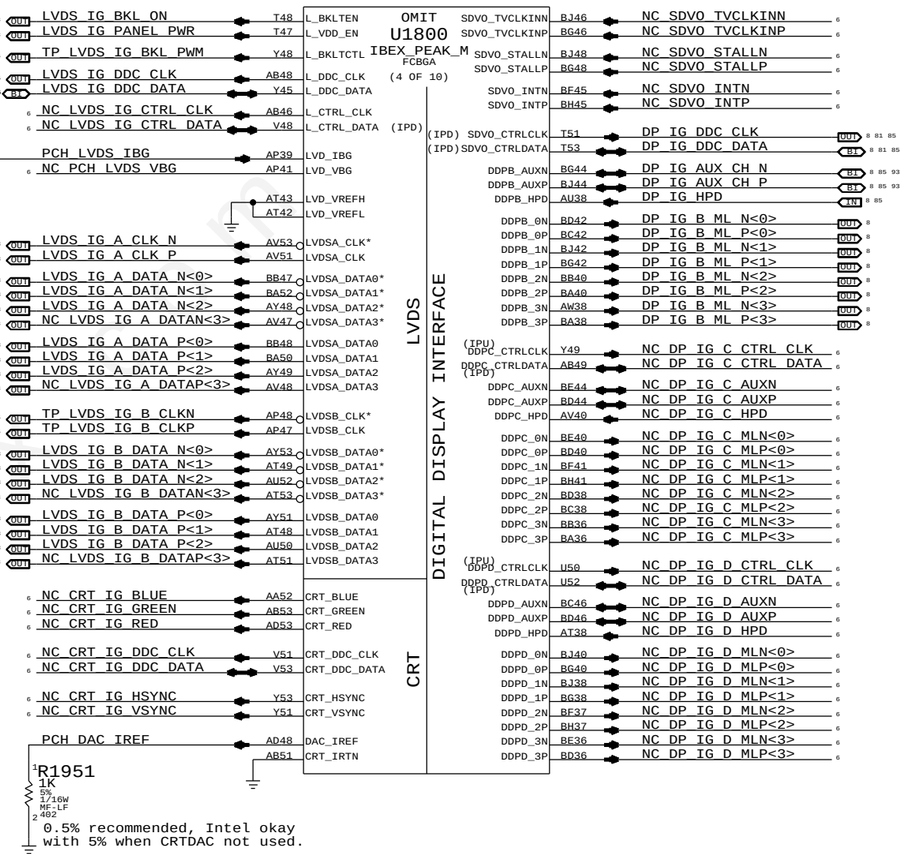

SYNC_MASTER=K17 WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: PCH DMI/FDI/Graphics

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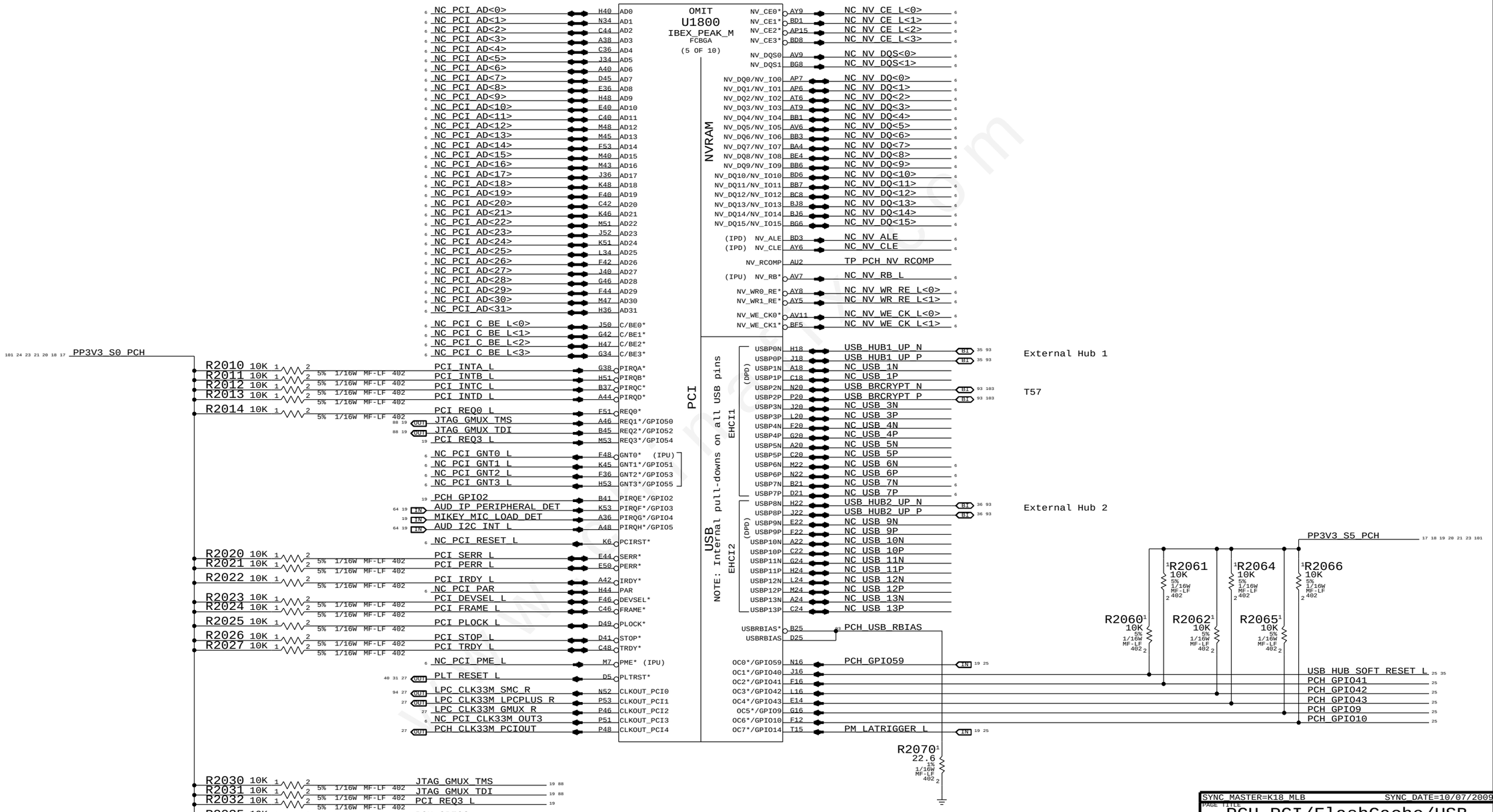
OMIT
U1800
IBEX_PEAK_M
FCBGA
(5 OF 10)
PCI
NVRAM
USB
NOTE: Internal pull-downs on all USB pins
EHCI1
EHCI2
(DPD)
External Hub 1
External Hub 2
T57
PP3V3_S0_PCH
PP3V3_S5_PCH
PCH PCI/FlashCache/USB
Apple Inc.
SYNC_MASTER=K18_MLB
SYNC_DATE=10/07/2009
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IPU* = Only on TACH function.

47 46 25 20	IN	SMC_IG_THROTTLE_L	Y3	BMBUSY*/GPIO0		
40 20 8	IN	FW_PLUG_DET_L	C38	TACH1/GPIO1 (IPU*)		
88 20	IN	GMUX_INT	D37	TACH2/GPIO6 (IPU*)		
46 20	IN	SMC_RUNTIME_SCI_L	J32	TACH3/GPIO7 (IPU*)		
20		PCH_FCIM_EN_L	F10	GPIO8 (IPU)		
37 20	OUT	ENET_LOW_PWR	K9	LAN_PHY_PWR_CTRL/GPIO12		
20		PCH_GPIO15	T7	GPIO15 (IPD)		
64 25 20	OUT	AUD_IPHS_SWITCH_EN	AA2	SATA4GP/GPIO16		
48 20 6	BI	LPCPLUS_GPIO	F38	TACH0/GPIO17 (IPU*)		
42 20	OUT	ODD_PWR_EN_L	Y7	SCLOCK/GPIO22		
20		PCH_GPIO24	H10	MEM_LED/GPIO24		
20		PCH_VRM_EN	AB12	GPIO27		
31 25	OUT	ISOLATE_CPU_MEM_L	V13	GPIO28 (IPU)		
		TP_PCH_STP_PCI_L	M11	STP_PCI*/GPIO34		
20	OUT	MXM_GOOD	V6	SATACLKREQ*/GPIO35		
25 20	OUT	SDCARD_RESET	AB7	SATA2GP/GPIO36		
88 25 20	OUT	JTAG_GMUX_TCK	AB13	SATA3GP/GPIO37		
88 20	IN	JTAG_GMUX_TDO	V3	SLOAD/GPIO38		
20		PCH_GPIO39	P3	SDATAOUT0/GPIO39		
74 20	OUT	WOL_EN	H3	PCIECLKRQ6*/GPIO45		
74 33 20	OUT	AP_PWR_EN	F1	PCIECLKRQ7*/GPIO46		
40 20	OUT	FW_PWR_EN	AB6	SDATAOUT1/GPIO48		
25 20	OUT	ME_TEMP_ALERT_L	AA4	SATA5GP/GPIO49		
58 48 20 6	BI	SPIROM_USE_MLB	F8	GPIO57		

OMIT
U1800
IBEX_PEAK_M
FCBGA
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GPIO

94 6		PCH_VSS_NCTF<1>	A4	VSS_NCTF1		
94 6		PCH_VSS_NCTF<2>	A49	VSS_NCTF2		
			A5	VSS_NCTF3		
			A50	VSS_NCTF4		
94 6		PCH_VSS_NCTF<5>	A52	VSS_NCTF5		
			A53	VSS_NCTF6		
94		TP_PCH_VSS_NCTF<7>	B2	VSS_NCTF7		
			B4	VSS_NCTF8		
94 6		PCH_VSS_NCTF<9>	B52	VSS_NCTF9		
			B53	VSS_NCTF10		
94 6		PCH_VSS_NCTF<11>	BE1	VSS_NCTF11		
94 6		PCH_VSS_NCTF<12>	BE53	VSS_NCTF12		
			BF1	VSS_NCTF13		
			BF53	VSS_NCTF14		
94 6		PCH_VSS_NCTF<15>	BH1	VSS_NCTF15		
			BH2	VSS_NCTF16		
94 6		PCH_VSS_NCTF<17>	BH52	VSS_NCTF17		
			BH53	VSS_NCTF18		
94 6		PCH_VSS_NCTF<19>	BJ1	VSS_NCTF19		
			BJ2	VSS_NCTF20		
94 6		PCH_VSS_NCTF<21>	BJ4	VSS_NCTF21		
94		PCH_VSS_NCTF<22>	BJ49	VSS_NCTF22		
			BJ5	VSS_NCTF23		
			BJ50	VSS_NCTF24		
94 6		PCH_VSS_NCTF<25>	BJ52	VSS_NCTF25		
			BJ53	VSS_NCTF26		
94 6		PCH_VSS_NCTF<27>	D1	VSS_NCTF27		
			D2	VSS_NCTF28		
94 6		PCH_VSS_NCTF<29>	D53	VSS_NCTF29		
			E1	VSS_NCTF30		
			E53	VSS_NCTF31		

NCTF

RSVD

MISC

		A20GATE	U2	PCH_A20GATE	
		CLKOUT_BCLK0_N/CLKOUT_PCIE8N	AM3	FSB_CLK133M_CPU_N	OUT 10 91
		CLKOUT_BCLK0_P/CLKOUT_PCIE8P	AM1	FSB_CLK133M_CPU_P	OUT 10 91
		PECI	BG10	CPU_PECI	BI 10 91
		RCIN*	T1	PCH_RCIN_L	
		PROCPWRGD	BE10	CPU_PWRGD	OUT 10 25 91
		THRMTRIP*	BD10	PCH_THRMTRIP_L	
		TP1	BA22	NC_PCH_TP1	
		TP2	AW22	NC_PCH_TP2	
		TP3	BB22	NC_PCH_TP3	
		TP4	AY45	NC_PCH_TP4	(DPL_B_MON1_N)
		TP5	AY46	NC_PCH_TP5	(DPL_B_MON1_P)
		TP6	AV43	NC_PCH_TP6	(DPL_B_MON2_N)
		TP7	AV45	NC_PCH_TP7	(DPL_B_MON2_P)
		TP8	AF13	NC_PCH_TP8	(SATA_OB_ANA)
		TP9	M18	NC_PCH_TP9	
		TP10	N18	NC_PCH_TP10	
		TP11	AJ24	NC_PCH_TP11	
		TP12	AK41	NC_PCH_TP12	(XCKPLL_MON1_N)
		TP13	AK42	NC_PCH_TP13	(XCKPLL_MON1_P)
		TP14	M32	NC_PCH_TP14	
		TP15	N32	NC_PCH_TP15	
		TP16	M30	NC_PCH_TP16	
		TP17	N30	NC_PCH_TP17	
		TP18	H12	NC_PCH_TP18	
		TP19	AA23	NC_PCH_TP19	
		NC_1	AB45	NC_PCH_NC1	
		NC_2	AB38	NC_PCH_NC2	
		NC_3	AB42	NC_PCH_NC3	
		NC_4	AB41	NC_PCH_NC4	
		NC_5	T39	NC_PCH_NC5	
(IPD)	INIT3_3V*	P6		TP_PCH_INIT3V3_L	
		TP24	C10	NC_PCH_SST	

PP3V3_S0_PCH 17 18 19 20 21 23 24 101

R2150 10K 5% 1/16W MF-LF 402 — PP3V3_S0_PCH — R2155 10K 5% 1/16W MF-LF 402

PPVTT_S0_PCH 21 23 101

R2160 56 5% 1/16W MF-LF 402

R2161 56 5% 1/16W MF-LF 402 — PM_THRMTRIP_L IN 10 47 91

PP3V3_S5_PCH 17 18 19 21 23 101
PP3V3_S3 6 7 17 31 32 33 34 35 36 49 50 51 54 55 56 72 74 88 102 103
PP3V3_S0_PCH 17 18 19 20 21 23 24 101

R2110	10K	SMC_IG_THROTTLE_L	20 25 46 47
R2111	10K	FW_PLUG_DET_L	8 20 40
R2112	20K	GMUX_INT	20 88
R2113	10K	SMC_RUNTIME_SCI_L	20 46
R2114	10K	PCH_FCIM_EN_L	20
R2115	2.2K	ENET_LOW_PWR	20 37
R2116	10K	PCH_GPIO15	20
R2120	10K	AUD_IPHS_SWITCH_EN	20 25 64
R2121	10K	LPCPLUS_GPIO	6 20 48
R2122	10K	ODD_PWR_EN_L	20 42
R2123	10K	PCH_GPIO24	20
R2124	10K	PCH_VRM_EN	20
R2130	10K	MXM_GOOD	20
R2131	10K	SDCARD_RESET	20 25
R2132	10K	JTAG_GMUX_TCK	20 25 88
R2133	10K	JTAG_GMUX_TDO	20 88
R2134	10K	PCH_GPIO39	20
R2135	10K	WOL_EN	20 74
R2136	10K	AP_PWR_EN	20 33 74
R2137	10K	FW_PWR_EN	20 40
R2138	10K	ME_TEMP_ALERT_L	20 25
R2139	100K	SPIROM_USE_MLB	6 20 48 58

All: 5% 1/16W MF-LF 402

SYNC_MASTER=K18_MLB SYNC_DATE=11/13/2009

PAGE TITLE: PCH MISC

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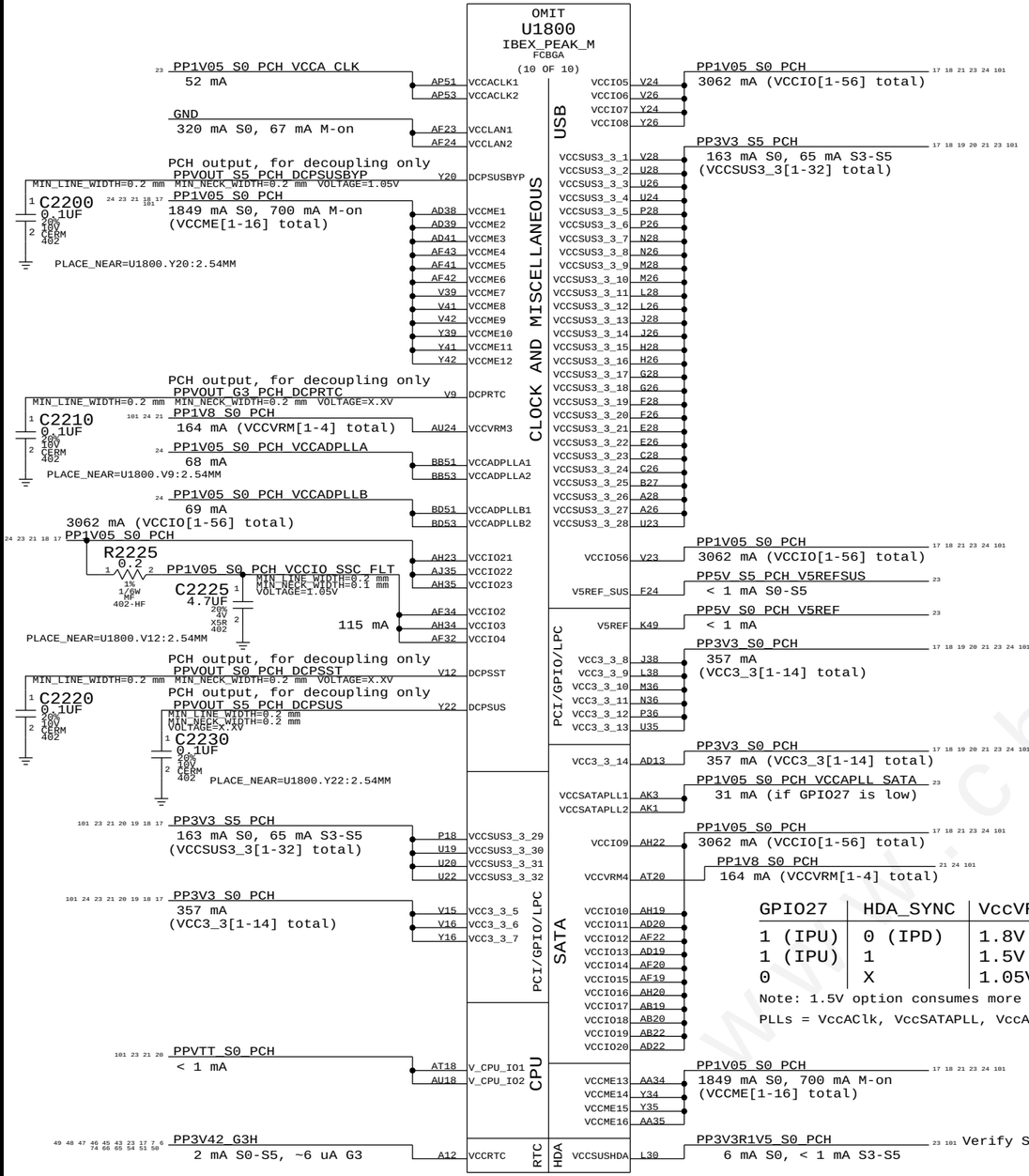

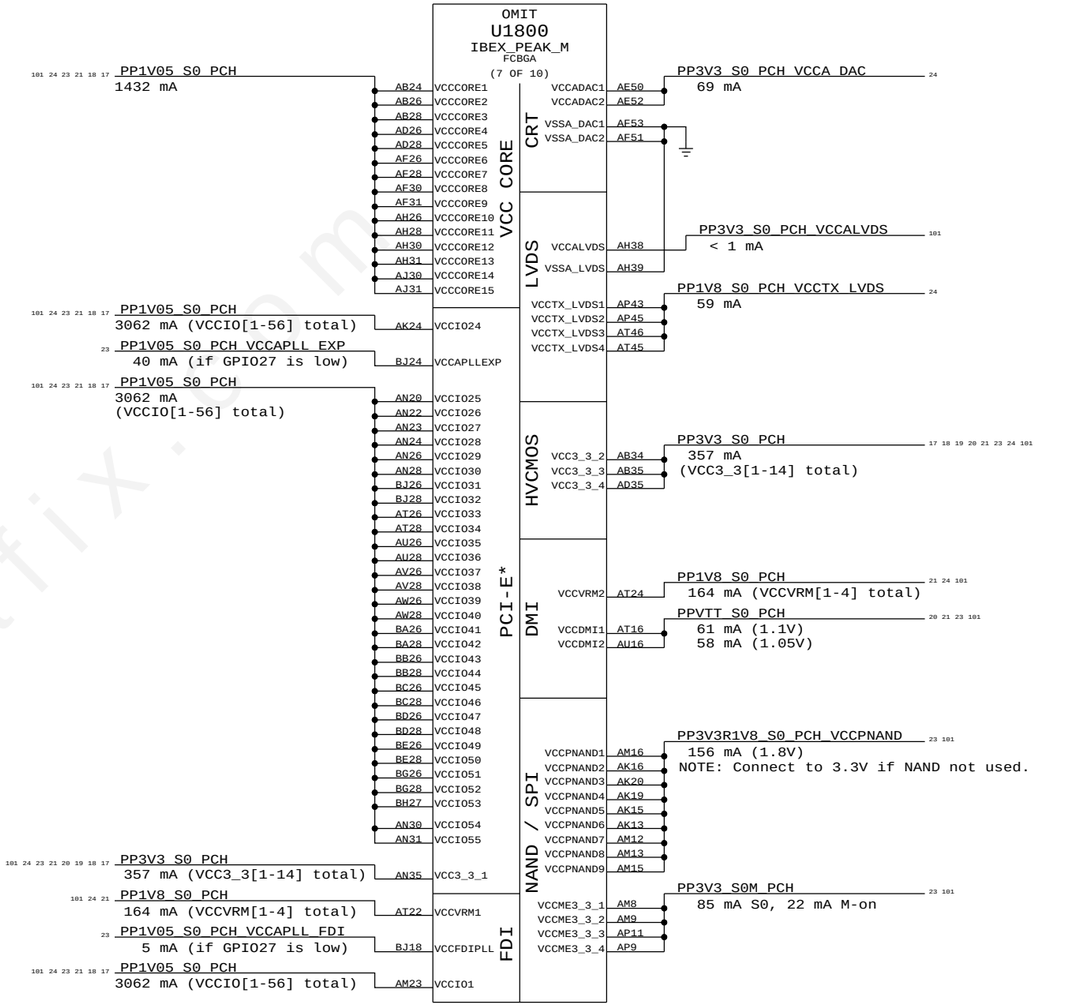

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K18_MLB SYNC_DATE=10/02/2009

PAGE TITLE: PCH Power

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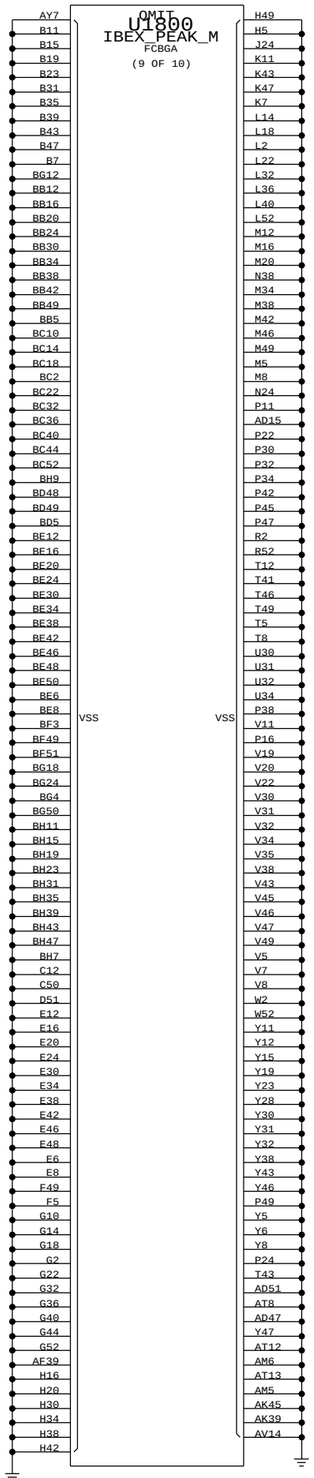

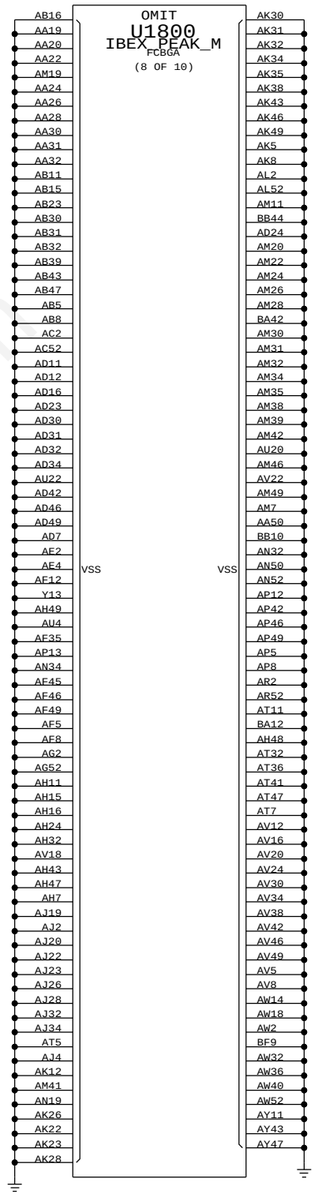

SYNC_MASTER=T22_MLB SYNC_DATE=03/26/2009

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PCH Grounds

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DRAWING NUMBER | SIZE D

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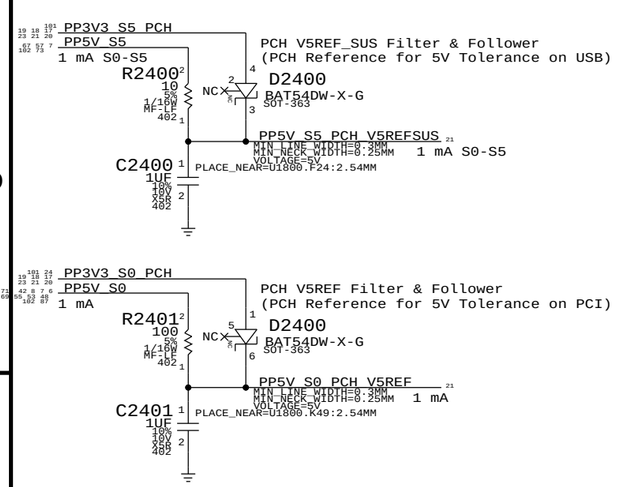

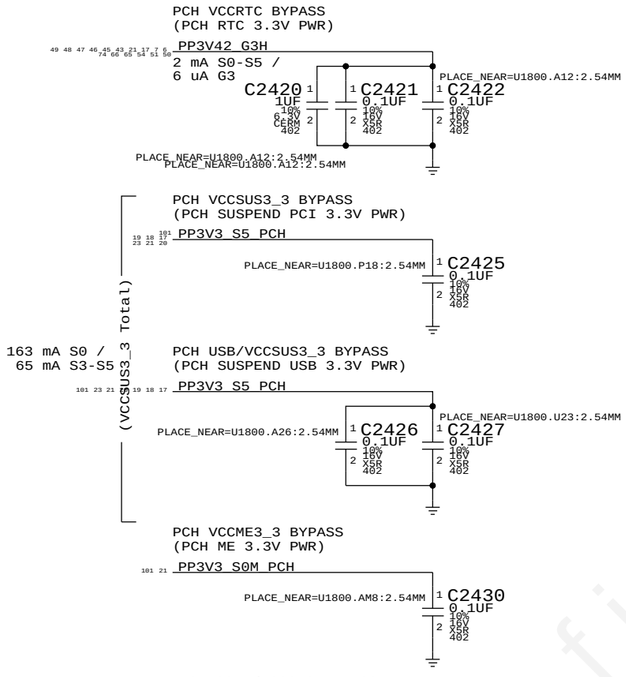

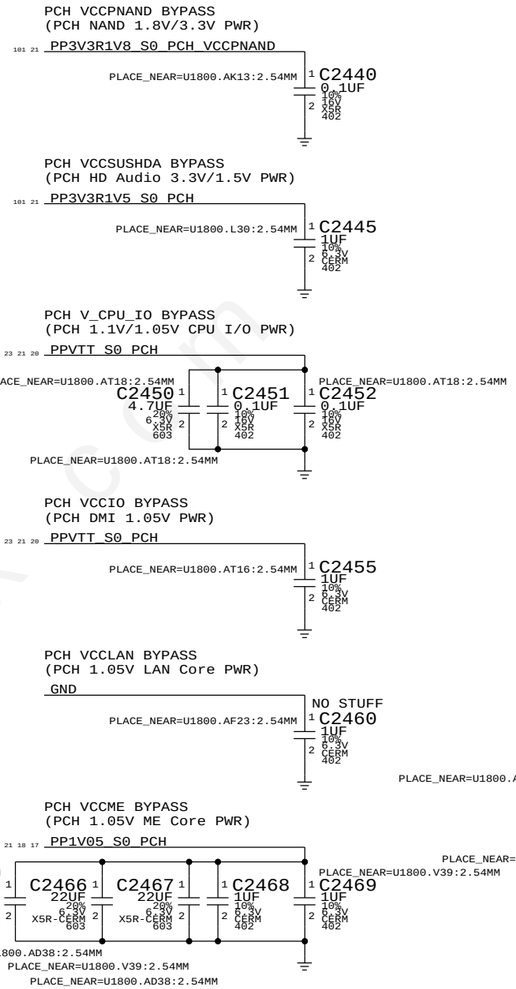

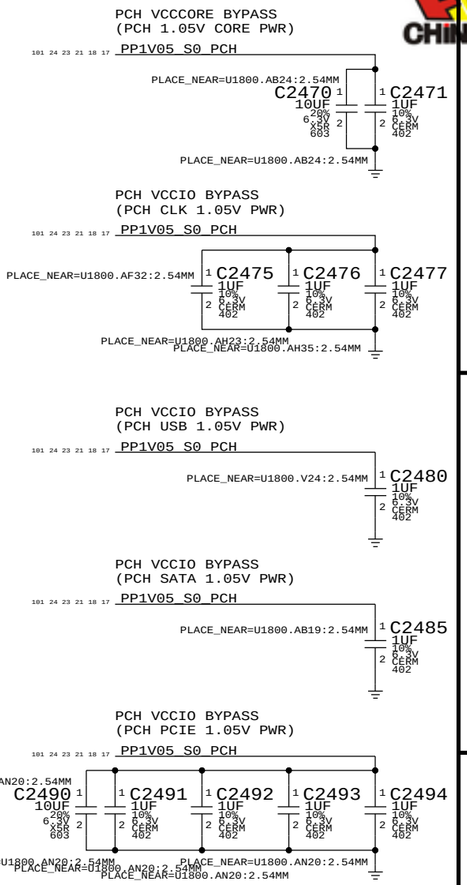

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE
PCH Non-GFX Decoupling

Apple Inc.

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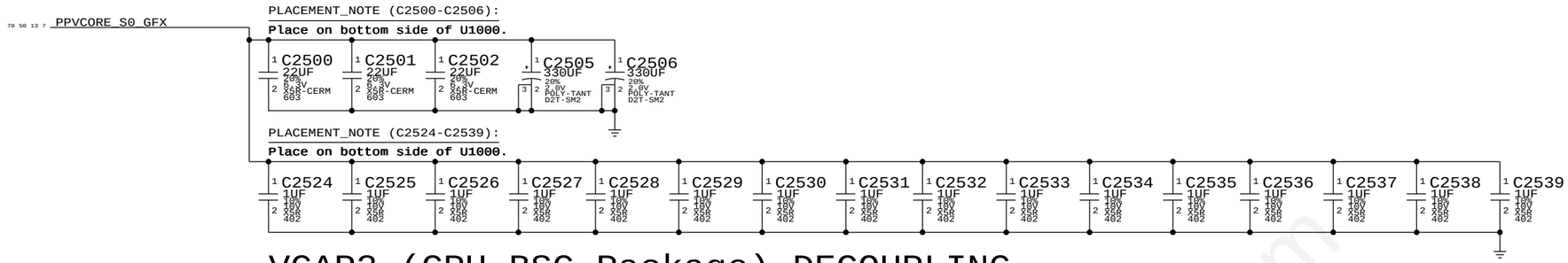
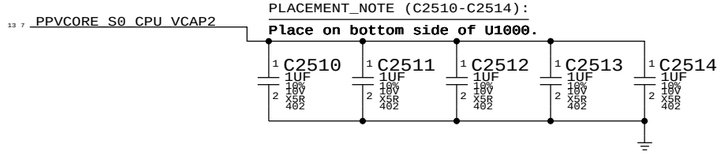
GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

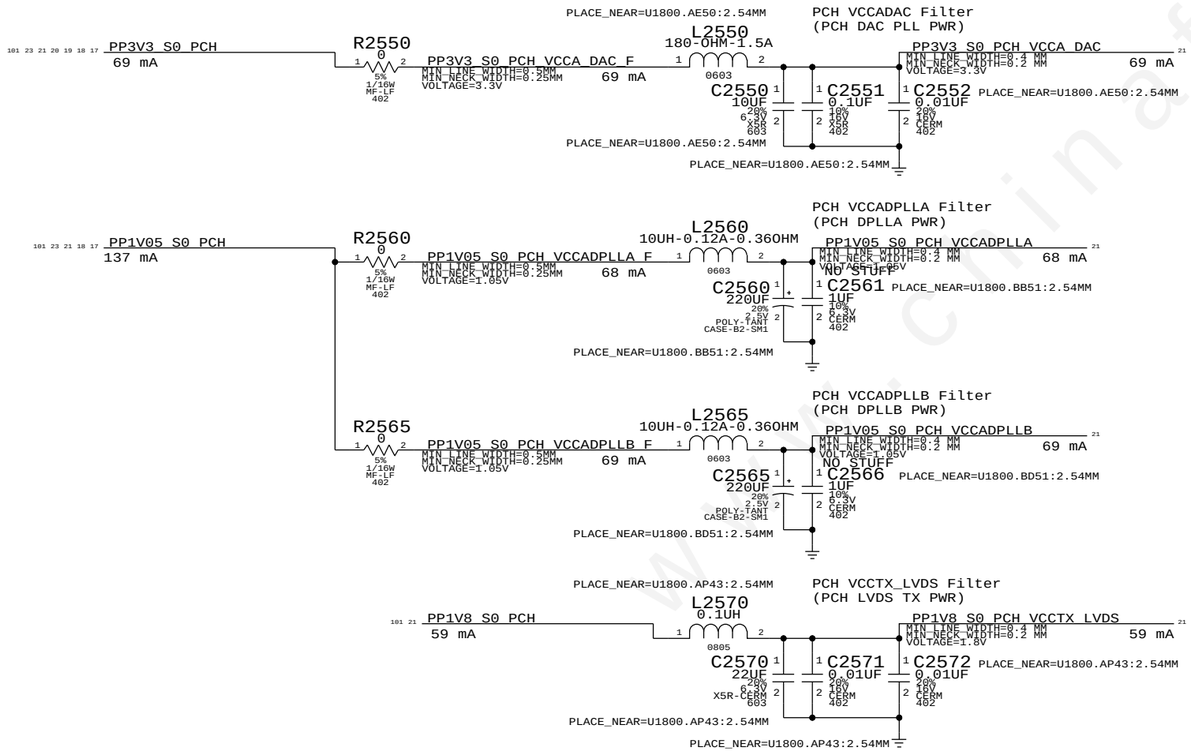


VCAP2 (CPU BSC Package) DECOUPLING

5x 1uF 0402



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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CPU/PCH GFX Decoupling

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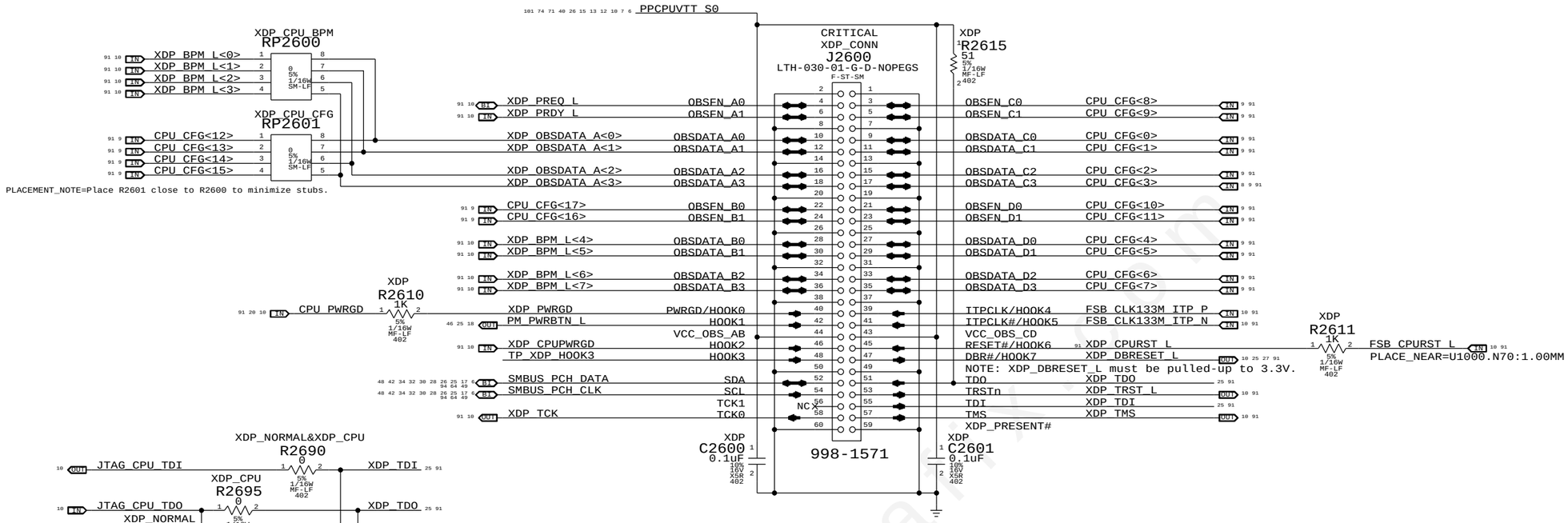
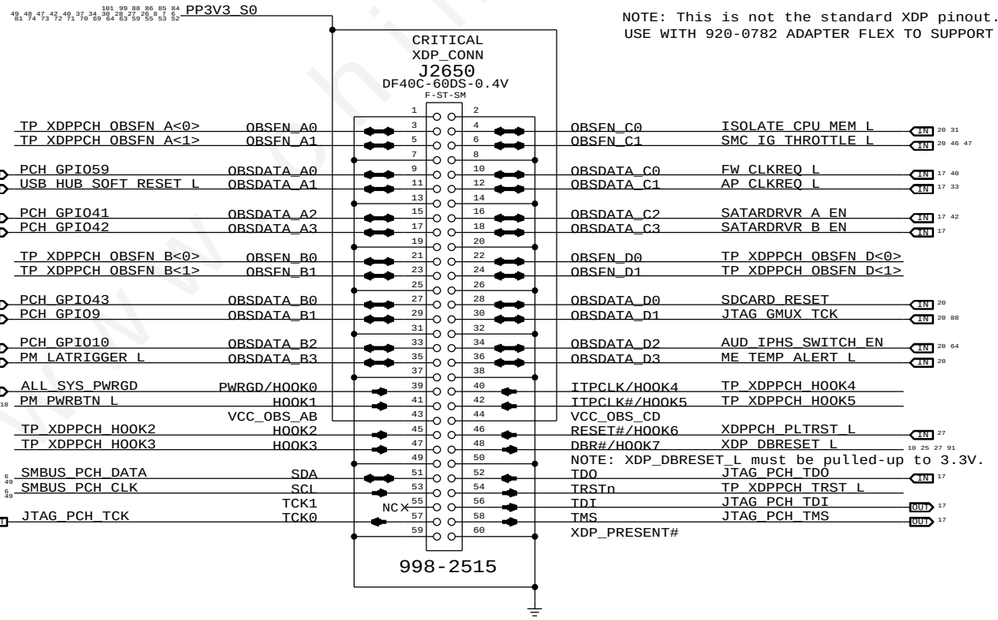
Calpella Processor mini XDP



Calpella PCH mini XDP



SYNC_MASTER=K18_MLB SYNC_DATE=06/22/2009

PAGE TITLE

eXtended Debug Port (XDP)

Apple Inc.

DRAWING NUMBER — SIZE D

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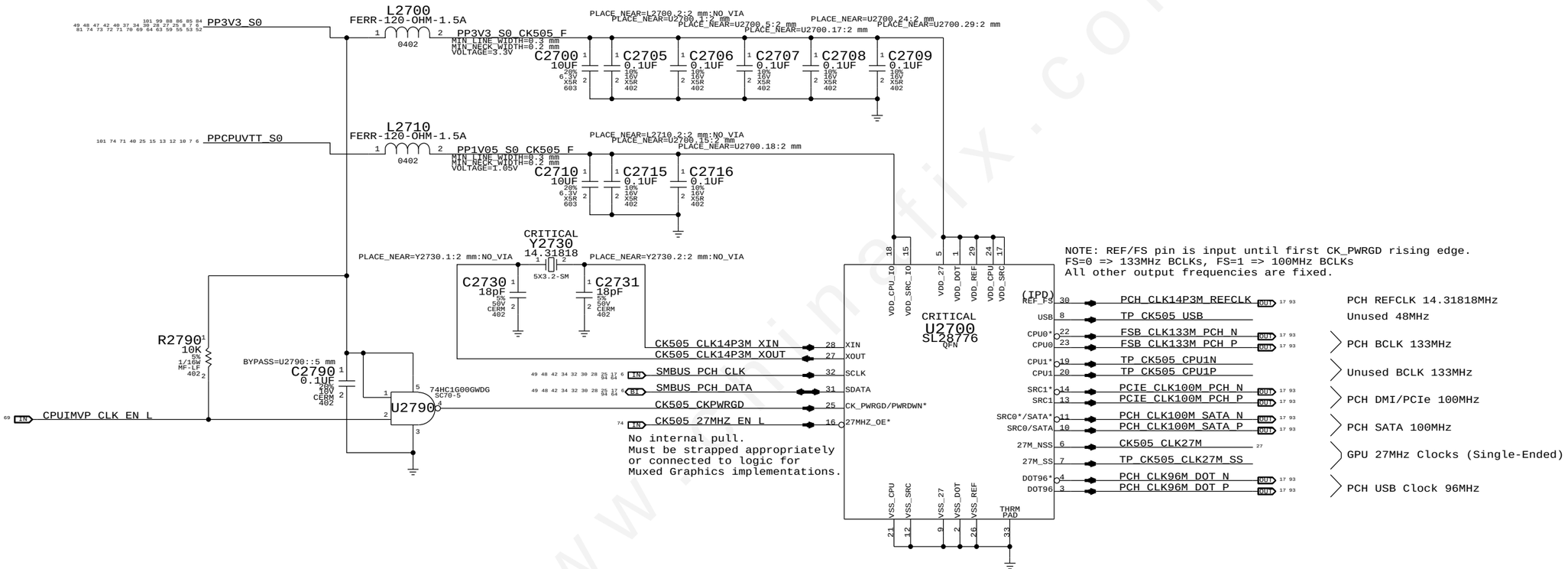

SYNC_MASTER=K17_REF SYNC_DATE=05/19/2009

PAGE TITLE

Clock (CK505)

Apple Inc.

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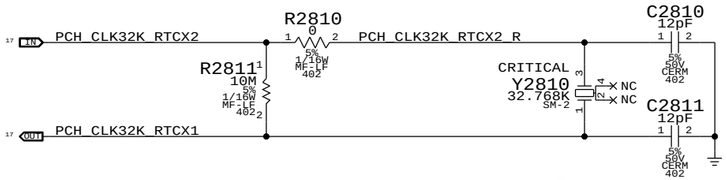
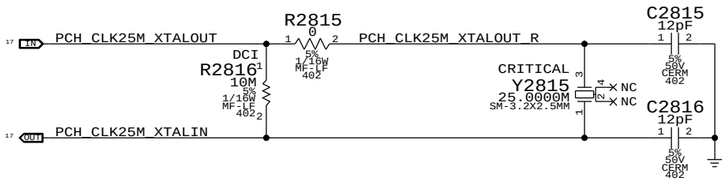
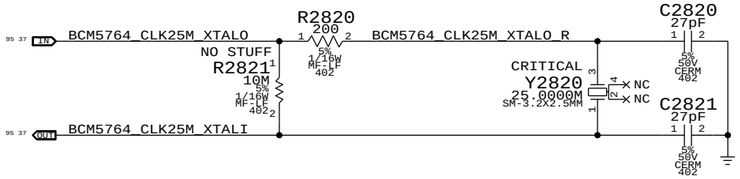
PCH RTC Crystal



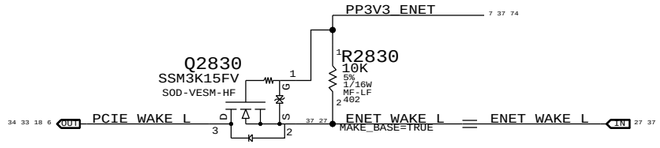
PCH 25MHz Crystal



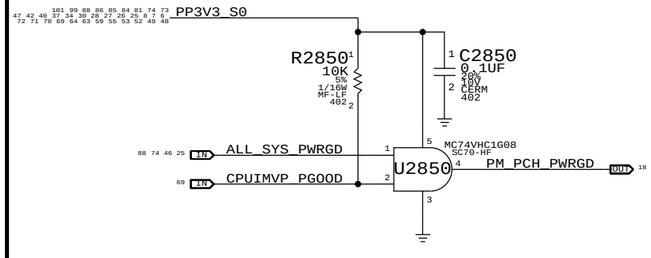
Caesar II (ENET) 25MHz Crystal



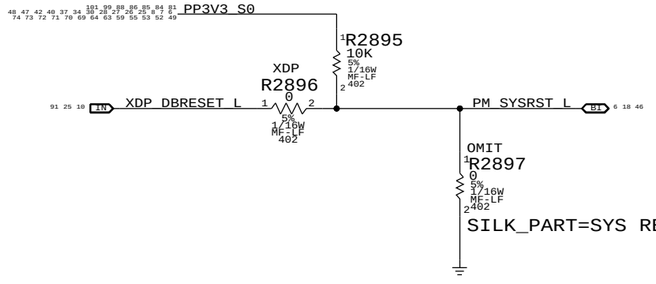
Ethernet WAKE# Isolation



PCH S0 PWRGD

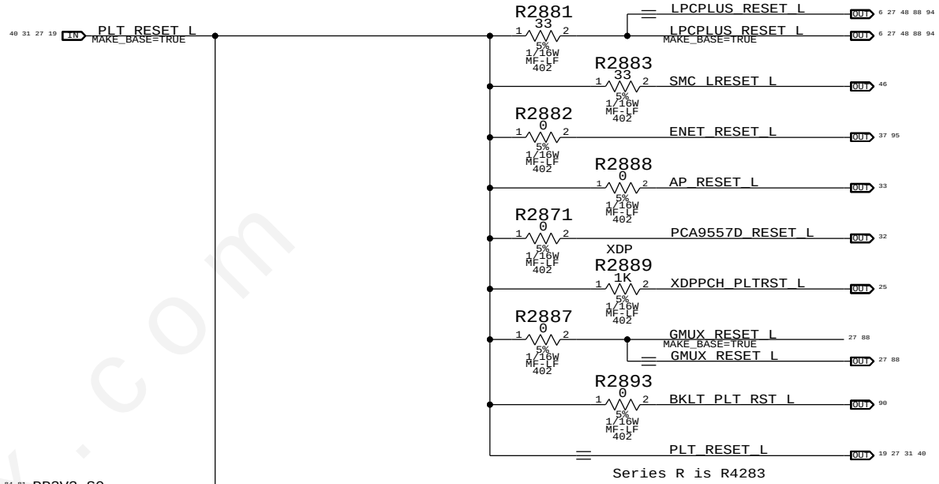


PCH Reset Button



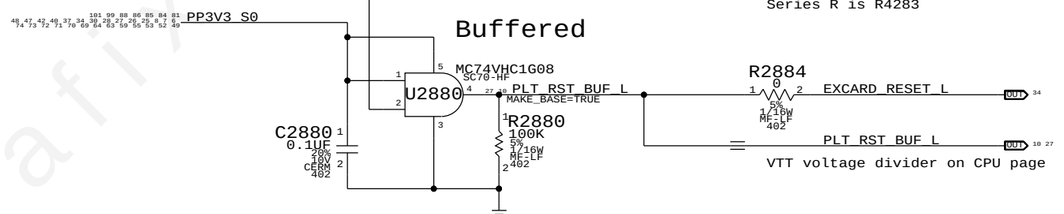
Platform Reset Connections

Unbuffered

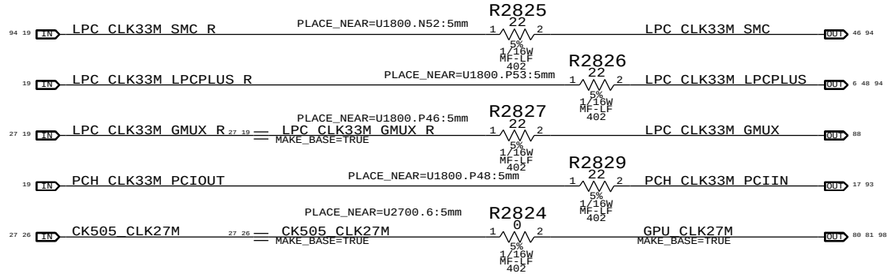


Series R is R4283

Buffered



VTT voltage divider on CPU page



SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

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Chipset Support

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PP5PD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

73 68 31 30 7 PP1V5_S3

C2900 10UF 20% 6.3V X6S 603
C2901 10UF 20% 6.3V X6S 603
C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

32 PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

KEY

NC
NC
NC
NC

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MEM_A_A<12> MEM_A_A<11>
MEM_A_A<9> MEM_A_A<7>
MEM_A_A<8> MEM_A_A<6>
MEM_A_A<5> MEM_A_A<4>
MEM_A_A<3> MEM_A_A<2>
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MEM_A_CLK_N<0> MEM_A_CLK_N<1>
MEM_A_A<10> MEM_A_BA<1>
MEM_A_BA<0> MEM_A_RAS_L
MEM_A_WE_L MEM_A_CS_L<0>
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MEM_A_CS_L<1>

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=MEM_A_DQ<43> =MEM_A_DQ<46>
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=MEM_A_DQ<58> =MEM_A_DQS_P<7>
=MEM_A_DQ<59> =MEM_A_DQ<62>
=MEM_A_DQ<63>
MEM_EVENT_A_L
SMBUS_PCH_DATA
SMBUS_PCH_CLK

J2900 F-RT-THB CRITICAL
DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2)

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

KEY

516-0229

=MEM_A_DQ<0> =MEM_A_DQ<4>
=MEM_A_DQ<1> =MEM_A_DQ<5>
MEM_A_DM<0> MEM_A_DQS_N<0>
MEM_A_DQS_P<0>
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=MEM_A_DQ<3> =MEM_A_DQ<7>
=MEM_A_DQ<8> =MEM_A_DQ<12>
=MEM_A_DQ<9> =MEM_A_DQ<13>
=MEM_A_DQS_N<1> =MEM_A_DM<1>
=MEM_A_DQS_P<1> MEM_RESET_L
=MEM_A_DQ<10> =MEM_A_DQ<14>
=MEM_A_DQ<11> =MEM_A_DQ<15>
=MEM_A_DQ<16> =MEM_A_DQ<20>
=MEM_A_DQ<17> =MEM_A_DQ<21>
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=MEM_A_DQS_P<2>
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=MEM_A_DQ<24> =MEM_A_DQ<28>
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=MEM_A_DM<3> =MEM_A_DQS_N<3>
=MEM_A_DQS_P<3>
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=MEM_A_DQ<27> =MEM_A_DQ<31>

32 PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

MEM_A_SA<0>
MEM_A_SA<1>

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

PP0V75_S0_DDRVTT

"Factory" (top) slot

SYNC_MASTER=K17_REF SYNC_DATE=05/13/2009

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

92 29 28 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_N<0>	11 28 29 92 92 30 29 11
92 29 28 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_P<0>	11 28 29 92 92 30 29 11
92 29 28 11	MEM_A_DM<0>	MAKE_BASE=TRUE	=	MEM_A_DM<0>	11 28 29 92 92 30 29 11
92 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>	28
92 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>	28
92 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>	28
92 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<0>	28
92 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>	28
92 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>	28
92 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>	28
92 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>	28

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

92 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>	28
92 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>	28
92 11	MEM_A_DM<1>	MAKE_BASE=TRUE	=	=MEM_A_DM<1>	28
92 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>	28
92 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>	28
92 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>	28
92 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>	28
92 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>	28
92 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>	28
92 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>	28
92 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=	=MEM_A_DQ<12>	28

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

92 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>	28
92 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<2>	28
92 11	MEM_A_DM<2>	MAKE_BASE=TRUE	=	=MEM_A_DM<2>	28
92 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>	28
92 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>	28
92 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>	28
92 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>	28
92 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>	28
92 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>	28
92 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<17>	28
92 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>	28

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

92 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>	28
92 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>	28
92 11	MEM_A_DM<3>	MAKE_BASE=TRUE	=	=MEM_A_DM<3>	28
92 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>	28
92 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>	28
92 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>	28
92 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<24>	28
92 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>	28
92 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>	28
92 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>	28
92 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>	28

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

92 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>	28
92 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<4>	28
92 11	MEM_A_DM<4>	MAKE_BASE=TRUE	=	=MEM_A_DM<4>	28
92 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<33>	28
92 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>	28
92 29 28 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	=	MEM_A_DQ<37>	11 28 29 92 92 30 29 11
92 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>	28
92 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>	28
92 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>	28
92 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>	28
92 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>	28

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

92 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>	28
92 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<5>	28
92 11	MEM_A_DM<5>	MAKE_BASE=TRUE	=	=MEM_A_DM<5>	28
92 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>	28
92 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>	28
92 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<45>	28
92 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>	28
92 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>	28
92 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>	28
92 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>	28
92 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>	28

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

92 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>	28
92 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<6>	28
92 11	MEM_A_DM<6>	MAKE_BASE=TRUE	=	=MEM_A_DM<6>	28
92 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>	28
92 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>	28
92 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>	28
92 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>	28
92 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>	28
92 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>	28
92 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>	28
92 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=	=MEM_A_DQ<52>	28

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

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92 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<7>	28
92 11	MEM_A_DM<7>	MAKE_BASE=TRUE	=	=MEM_A_DM<7>	28
92 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>	28
92 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>	28
92 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>	28
92 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<61>	28
92 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>	28
92 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>	28
92 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>	28
92 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>	28

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

92 29 28 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_N<0>	11 29 30 92
92 29 28 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_P<0>	11 29 30 92
92 29 28 11	MEM_B_DM<0>	MAKE_BASE=TRUE	=	MEM_B_DM<0>	11 29 30 92
92 11	MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>	30
92 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>	30
92 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>	30
92 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>	30
92 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>	30
92 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>	30
92 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>	30
92 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=	=MEM_B_DQ<0>	30

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

92 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>	30
92 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>	30
92 11	MEM_B_DM<1>	MAKE_BASE=TRUE	=	=MEM_B_DM<1>	30
92 11	MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>	30
92 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>	30
92 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>	30
92 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>	30
92 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>	30
92 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>	30
92 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>	30
92 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=	=MEM_B_DQ<9>	30

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

92 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>	30
92 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<2>	30
92 11	MEM_B_DM<2>	MAKE_BASE=TRUE	=	=MEM_B_DM<2>	30
92 11	MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>	30
92 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>	30
92 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>	30
92 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<17>	30
92 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>	30
92 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>	30
92 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>	30
92 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>	30

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

92 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>	30
92 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>	30
92 11	MEM_B_DM<3>	MAKE_BASE=TRUE	=	=MEM_B_DM<3>	30
92 11	MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>	30
92 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>	30
92 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>	30
92 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>	30
92 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>	30
92 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<29>	30
92 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>	30
92 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>	30

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

92 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>	30
92 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>	30
92 11	MEM_B_DM<4>	MAKE_BASE=TRUE	=	=MEM_B_DM<4>	30
92 11	MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>	30
92 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>	30
92 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	=	MEM_B_DQ<37>	11 29 30 92
92 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<32>	30
92 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<33>	30
92 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>	30
92 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>	30
92 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>	30

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

92 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>	30
92 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>	30
92 11	MEM_B_DM<5>	MAKE_BASE=TRUE	=	=MEM_B_DM<5>	30
92 11	MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>	30
92 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>	30
92 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>	30
92 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<41>	30
92 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>	30
92 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>	30
92 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>	30
92 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>	30

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

92 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>	30
92 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>	30
92 11	MEM_B_DM<6>	MAKE_BASE=TRUE	=	=MEM_B_DM<6>	30
92 11	MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>	30
92 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>	30
92 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>	30
92 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>	30
92 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>	30
92 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>	30
92 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>	30
92 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=	=MEM_B_DQ<52>	30

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

92 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>	30
92 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>	30
92 11	MEM_B_DM<7>	MAKE_BASE=TRUE	=	=MEM_B_DM<7>	30
92 11	MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>	30
92 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>	30
92 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>	30
92 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<56>	30
92 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>	30
92 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>	30
92 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>	30
92 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>	30

SYNC_MASTER=K18_MLB SYNC_DATE=06/19/2009

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER — SIZE D

REVISION

BRANCH

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SHEET 29 OF 103

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

73 68 31 28 7 PP1V5_S3

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

C3100 10UF 20% 6.3V X6S 603
C3101 10UF 20% 6.3V X6S 603

32 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

DDR3-SODIMM (2 OF 2)
OMIT
J3100
F-RT-BGA6
KEY

92 11 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 11 92
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 11 92
92 11 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 11 92
		81	VDD	VDD	82		
92 11 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 11 92
92 11 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 11 92
		87	VDD	VDD	88		
92 11 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 11 92
92 11 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 11 92
		93	VDD	VDD	94		
92 11 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 11 92
92 11 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 11 92
		99	VDD	VDD	100		
92 11 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 11 92
92 11 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 11 92
		105	VDD	VDD	106		
92 11 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 11 92
92 11 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 11 92
		111	VDD	VDD	112		
92 11 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 11 92
92 11 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 11 92
		117	VDD	VDD	118		
92 11 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 11 92
92 11 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
29 BI	=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>	BI 29
29 BI	=MEM_B_DQ<33>	131	DQ33	DQ37	132	=MEM_B_DQ<37>	BI 29
		133	VSS	VSS	134		
29 BI	=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	=MEM_B_DM<4>	IN 29
29 BI	=MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_B_DQ<38>	BI 29
92 29 11 BI	MEM_B_DQ<37>	141	DQ34	DQ39	142	=MEM_B_DQ<39>	BI 29
29 BI	=MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_B_DQ<44>	BI 29
29 BI	=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>	BI 29
29 BI	=MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_B_DQS_N<5>	BI 29
29 IN	=MEM_B_DM<5>	153	DM5	DQS5	154	=MEM_B_DQS_P<5>	BI 29
		155	VSS	VSS	156		
29 BI	=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>	BI 29
29 BI	=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>	BI 29
		161	VSS	VSS	162		
29 BI	=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>	BI 29
29 BI	=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>	BI 29
		167	VSS	VSS	168		
29 BI	=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	=MEM_B_DM<6>	IN 29
29 BI	=MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_B_DQ<54>	BI 29
29 BI	=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>	BI 29
29 BI	=MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_B_DQ<60>	BI 29
29 BI	=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>	BI 29
29 BI	=MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_B_DQS_N<7>	BI 29
29 IN	=MEM_B_DM<7>	187	DM7	DQS7	188	=MEM_B_DQS_P<7>	BI 29
		189	VSS	VSS	190		
29 BI	=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>	BI 29
29 BI	=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>	BI 29
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_A_L	OUT 28 46 47
		199	VDDSPD	SDA	200	SMBUS_PCH_DATA	BI 5 17 25 26 28 32 34 42 48 49 64 94
	MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_PCH_CLK	IN 5 17 25 26 28 32 34 42 48 49 64 94
		203	VTT	VTT	204		PP0V75_S0_DDRVTT 7 28 31 68
		MTG PINS					
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

516s0806
SPD ADDR=0xA4(WR)/0xA5(RD)

DDR3-SODIMM (1 OF 2)
OMIT CRITICAL
J3100
F-RT-BGA6
KEY

		1	VREFDQ	VSS	2		
29 BI	=MEM_B_DQ<0>	3	VSS	DQ4	4	=MEM_B_DQ<4>	BI 29
29 BI	=MEM_B_DQ<1>	5	DQ0	DQ5	6	=MEM_B_DQ<5>	BI 29
		7	DQ1	VSS	8		
92 29 11 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 11 29 92
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 11 29 92
		13	VSS	VSS	14		
29 BI	=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>	BI 29
29 BI	=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>	BI 29
		19	VSS	VSS	20		
29 BI	=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>	BI 29
29 BI	=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>	BI 29
		25	VSS	VSS	26		
29 BI	=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	=MEM_B_DM<1>	IN 29
29 BI	=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28 31
		31	VSS	VSS	32		
29 BI	=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>	BI 29
29 BI	=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>	BI 29
		37	VSS	VSS	38		
29 BI	=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>	BI 29
29 BI	=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>	BI 29
		43	VSS	VSS	44		
29 BI	=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	=MEM_B_DM<2>	IN 29
29 BI	=MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	=MEM_B_DQ<22>	BI 29
29 BI	=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>	BI 29
29 BI	=MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	=MEM_B_DQ<28>	BI 29
29 BI	=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>	BI 29
29 BI	=MEM_B_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	=MEM_B_DQS_N<3>	BI 29
29 IN	=MEM_B_DM<3>	63	DM3	DQS3	64	=MEM_B_DQS_P<3>	BI 29
		65	VSS	VSS	66		
29 BI	=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>	BI 29
29 BI	=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>	BI 29
		71	VSS	VSS	72		

516s0806

PP0V75_S3_MEM_VREFCA_B 32

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

R3140 10K 5% 1/16W MF-LF 402

70 69 64 63 [illegible] PP3V3_S0
53 52 49 48 47 42 38 37 34
88 86 85 84 81 74 73 72 71

C3140 2.2UF 20% 6.3V CERM 402-LF

R3141 10k 5% 1/10W MF-LF 402

"Expansion" (bottom) slot

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

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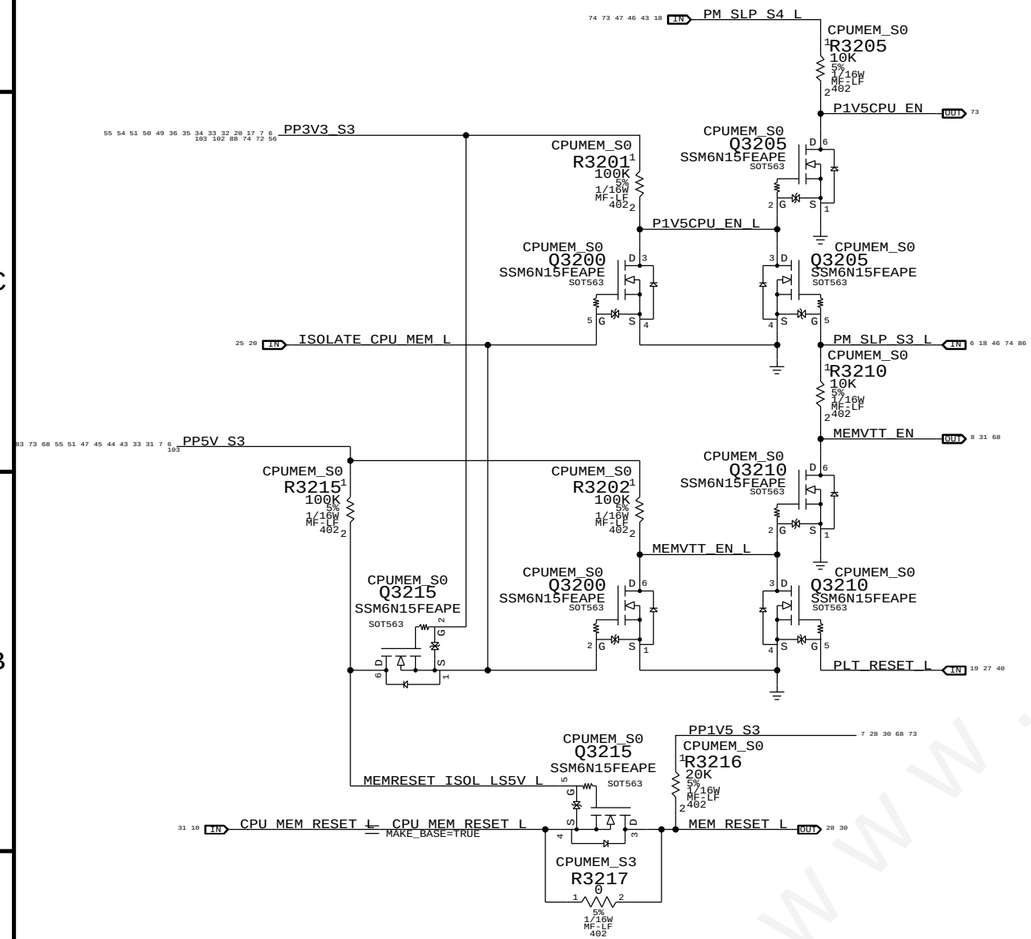
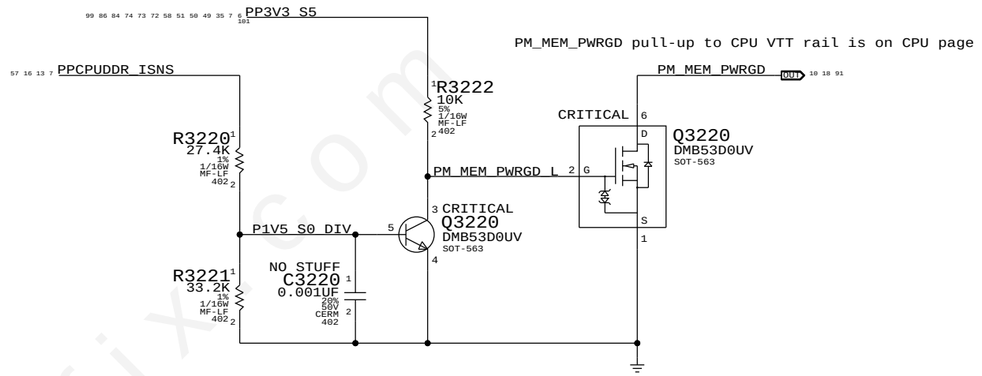
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

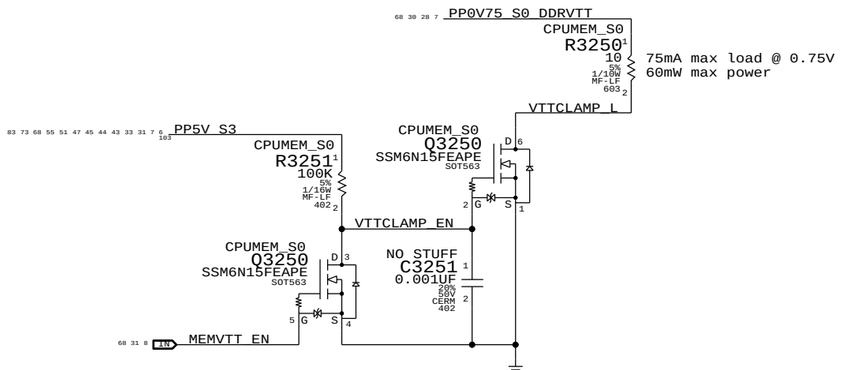


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K18_MLB SYNC_DATE=10/14/2009

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

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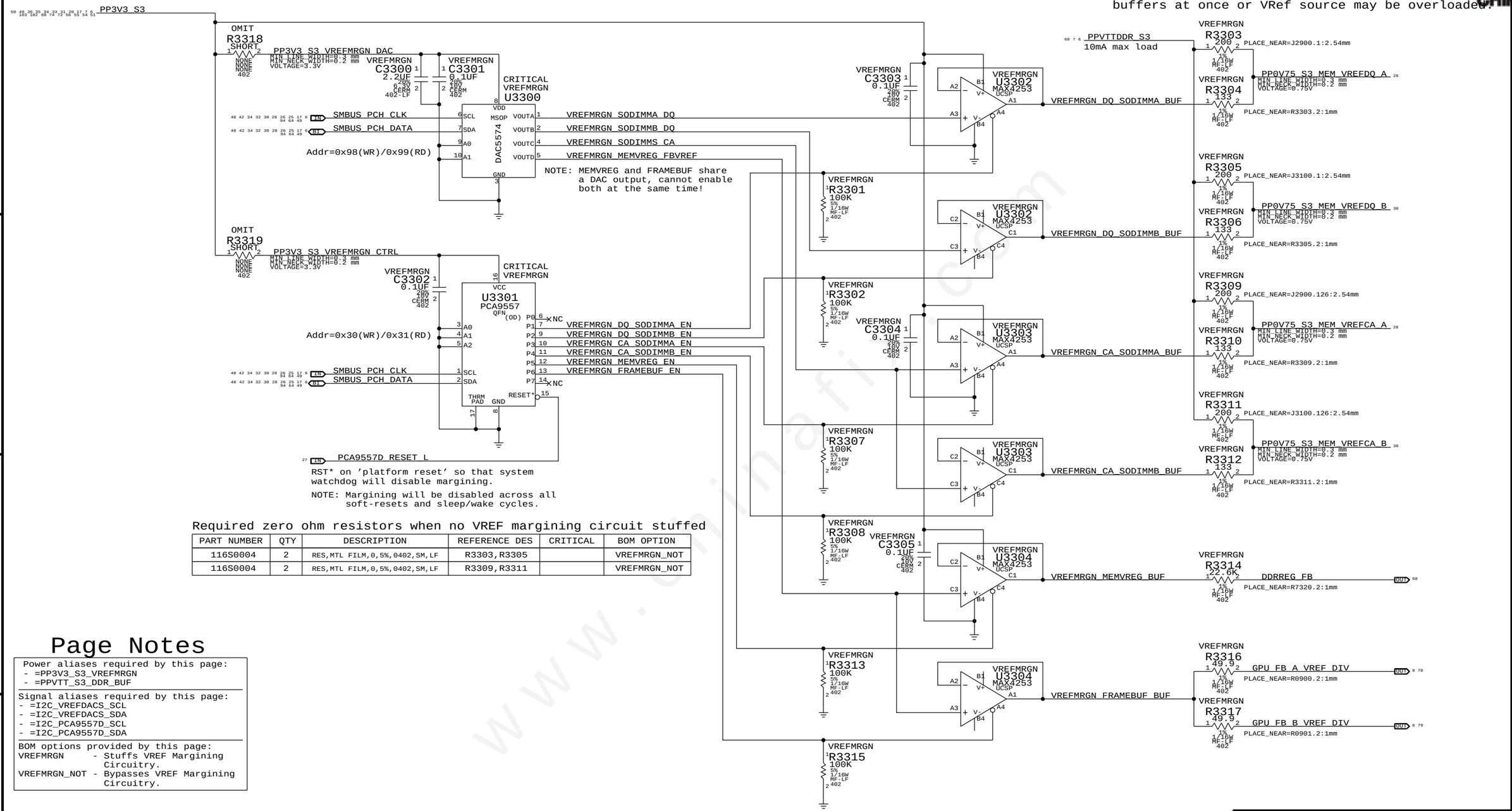

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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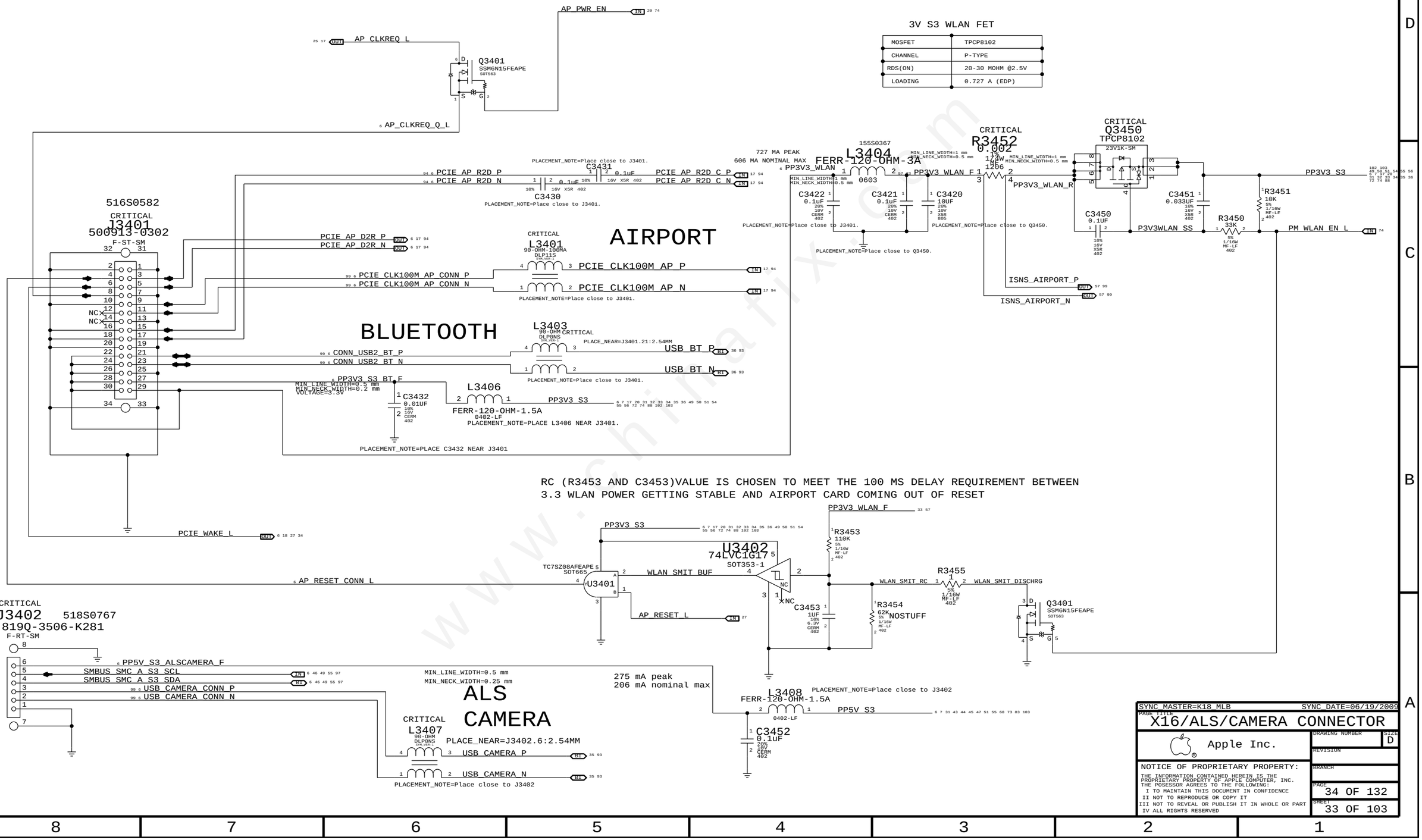
AP_PWR_EN
AP_CLKREQ_L
Q3401
SSM6N15FEAPE
SOT563
AP_CLKREQ_Q_L
3V S3 WLAN FET
MOSFET
TPCP8102
CHANNEL
P-TYPE
RDS(ON)
20-30 MOHM @2.5V
LOADING
0.727 A (EDP)
727 MA PEAK
606 MA NOMINAL MAX
155S0367
L3404
FERR-120-OHM-3A
PP3V3_WLAN
PP3V3_WLAN_F
CRITICAL
R3452
0.002
1%
1/2W
1206
PP3V3_WLAN_R
CRITICAL
Q3450
TPCP8102
23V1K-SM
PP3V3_S3
R3451
10K
5%
1/16W
MF-LF
402
C3422
0.1uF
C3421
0.1uF
C3420
10UF
C3450
0.1UF
C3451
0.033UF
R3450
33K
P3V3WLAN_SS
PM_WLAN_EN_L
PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.
516S0582
CRITICAL
J3401
500913-0302
F-ST-SM
PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
C3431
0.1uF
C3430
0.1uF
PLACEMENT_NOTE=Place close to J3401.
AIRPORT
CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PLACEMENT_NOTE=Place close to J3401.
ISNS_AIRPORT_P
ISNS_AIRPORT_N
BLUETOOTH
L3403
90-OHM CRITICAL
DLP0NS
PLACE_NEAR=J3401.21:2.54MM
CONN_USB2_BT_P
CONN_USB2_BT_N
USB_BT_P
USB_BT_N
PLACEMENT_NOTE=Place close to J3401.
PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3432
0.01UF
L3406
FERR-120-OHM-1.5A
0402-LF
PP3V3_S3
PLACEMENT_NOTE=PLACE L3406 NEAR J3401.
PLACEMENT_NOTE=PLACE C3432 NEAR J3401
PCIE_WAKE_L
RC (R3453 AND C3453)VALUE IS CHOSEN TO MEET THE 100 MS DELAY REQUIREMENT BETWEEN
3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET
PP3V3_WLAN_F
PP3V3_S3
U3402
74LVC1G17
SOT353-1
TC7SZ08AFEAPE
SOT665
U3401
WLAN_SMIT_BUF
AP_RESET_CONN_L
AP_RESET_L
R3453
110K
R3455
1
WLAN_SMIT_RC
WLAN_SMIT_DISCHRG
R3454
62K
NOSTUFF
C3453
1UF
Q3401
SSM6N15FEAPE
SOT563
CRITICAL
J3402
518S0767
819Q-3506-K281
F-RT-SM
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
ALS
CAMERA
CRITICAL
L3407
90-OHM
DLP0NS
PLACE_NEAR=J3402.6:2.54MM
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3402
275 mA peak
206 mA nominal max
L3408
FERR-120-OHM-1.5A
PLACEMENT_NOTE=Place close to J3402
PP5V_S3
C3452
0.1uF
SYNC_MASTER=K18_MLB
SYNC_DATE=06/19/2009
PAGE TITLE
X16/ALS/CAMERA CONNECTOR
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EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

PP3V3_S3
- C3530 0.1uF 20% 10V X5R CERM 402
- C3531 10uF 20% 6.3V X5R 603

PP1V5_S0
- C3534 0.1uF 20% 10V X5R CERM 402
- C3535 10uF 20% 6.3V X5R 603

L3502
90-OHM DLP0NS

USB_EXCARD_N (BI) — USB_EXCARD_N (MAKE_BASE=TRUE) — 4 — 3 — USB2_EXCARD_CONN_N
USB_EXCARD_P (BI) — USB_EXCARD_P (MAKE_BASE=TRUE) — 1 — 2 — USB2_EXCARD_CONN_P
PLACE_NEAR=J3500.3:4mm

L3503
90-OHM-100MA DLP11S

PCIE_CLK100M_EXCARD_N (IN) — 4 — 3 — PCIE_CLK100M_EXCARD_CONN_N
PCIE_CLK100M_EXCARD_P (IN) — 1 — 2 — PCIE_CLK100M_EXCARD_CONN_P
PLACE_NEAR=J3500.19:4mm

PLACE_NEAR=J3500.24:4mm

PCIE_EXCARD_R2D_C_N (IN) — C3571 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_N
PCIE_EXCARD_R2D_C_P (IN) — C3570 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_P
PLACE_NEAR=J3500.25:4mm

J3500
CRITICAL
502250-8627
F-ST-SM

PCIE_EXCARD_R2D_N	24	25	PCIE_EXCARD_R2D_P
PCIE_EXCARD_D2R_P (OUT)	22	23	
	20	21	PCIE_EXCARD_D2R_N
PCIE_CLK100M_EXCARD_CONN_N	18	19	PCIE_CLK100M_EXCARD_CONN_P
EXCARD_CLKREQ_CONN_L	16	17	EXCARD_CPPE_L
PP3V3_S0_EXCARD_SWITCH	14	15	PP3V3_S0_EXCARD_SWITCH
PP3V3_S3_EXCARD_SWITCH	12	13	PLT_RESET_SWITCH_L
PP1V5_S0_EXCARD_SWITCH	10	11	PCIE_WAKE_L (OUT)
	8	9	PP1V5_S0_EXCARD_SWITCH
SMBUS_PCH_DATA (BI)	6	7	SMBUS_PCH_CLK (BI)
NC	4	5	NC
EXCARD_CPUSB_L	2	3	USB2_EXCARD_CONN_P
USB2_EXCARD_CONN_N		1	

518S0647

OMIT_TABLE

PP3V3_S3 — OMIT R3504 SHORT — PP3V3_S3_EXCARD_R
MIN_LINE_WIDTH=0.5mm MIN_NECK_WIDTH=0.25mm VOLTAGE=3.3V

PP3V3_S0 — OMIT R3503 SHORT — PP3V3_S0_EXCARD_R
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.2mm VOLTAGE=3.3V

PP1V5_S0 — OMIT R3502 SHORT — PP1V5_S0_EXCARD_R
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.2mm VOLTAGE=1.5V

U3500
CRITICAL
TPS2231 QFN

	17 AUXIN	AUXOUT 15	VOLTAGE=3.3V MIN_LINE_WIDTH=.3mm MIN_NECK_WIDTH=0.2mm
	2 VIN3P3	VOUT3P3 3	
	12 VIN1P5	VOUT1P5 11	VOLTAGE=3.3V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
SMC_EXCARD_PWR_EN (IN)	20 SHDN*	PERST* 8	PLT_RESET_SWITCH_L
TP_EXCARD_STBY_L	1 STBY*	CPPE* 10	EXCARD_CPPE_L
EXCARD_RESET_L (IN)	6 SYSRST* (IPU)	CPUSB* 9 (IPU)	EXCARD_CPUSB_L
EXCARD_OC_L (IN)	19 OC*		VOLTAGE=1.5V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.11mm
NC	4 NC0	RCLKEN (IPU) 18	EXCARD_RCLKEN
NC	5 NC1		
NC	13 NC2		
NC	14 NC3		
NC	16 NC4	THRML_PAD 21	
		GND 7	

All pull-ups to AUXIN rail

PP3V3_S3_EXCARD_SWITCH
- C3500 0.1uF 20% 10V X5R CERM 402
- C3503 10uF 20% 6.3V X5R 603

PP3V3_S0_EXCARD_SWITCH
- C3501 0.1uF 20% 10V X5R CERM 402
- C3504 10uF 20% 6.3V X5R 603

PP1V5_S0_EXCARD_SWITCH
- C3502 0.1uF 20% 10V X5R CERM 402
- C3505 10uF 20% 6.3V X5R 603

OUTPUT DECOUPLING

PP3V3_S3
- C3550 0.1uF 20% 10V X5R CERM 402

SMC_EXCARD_NOT
- R3550 0 5% 1/16W MF-LF 402

SMC_EXCARD
- R3551 0 5% 1/16W MF-LF 402 — SMC_EXCARD_CP (OUT)

U3551 74HC1G00GWDG SC70-5
- EXCARD_CPUSB_L
- EXCARD_CPPE_L
- EXCARD_CP

PP3V3_S0
- R3561 100K 1% 1/16W MF-LF 402 — EXCARD_CLKREQ_CONN_L
- U3561 SN74LVC1G04YZPR BGA — EXCARD_RCLKEN
- C3560 0.1uF 20% 10V X5R CERM 402

U3560 74HC1G00GWDG SC70-5
- EXCARD_CLKREQ_CONN
- EXCARD_CLKREQ_L (OUT)

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: ExpressCard Connector

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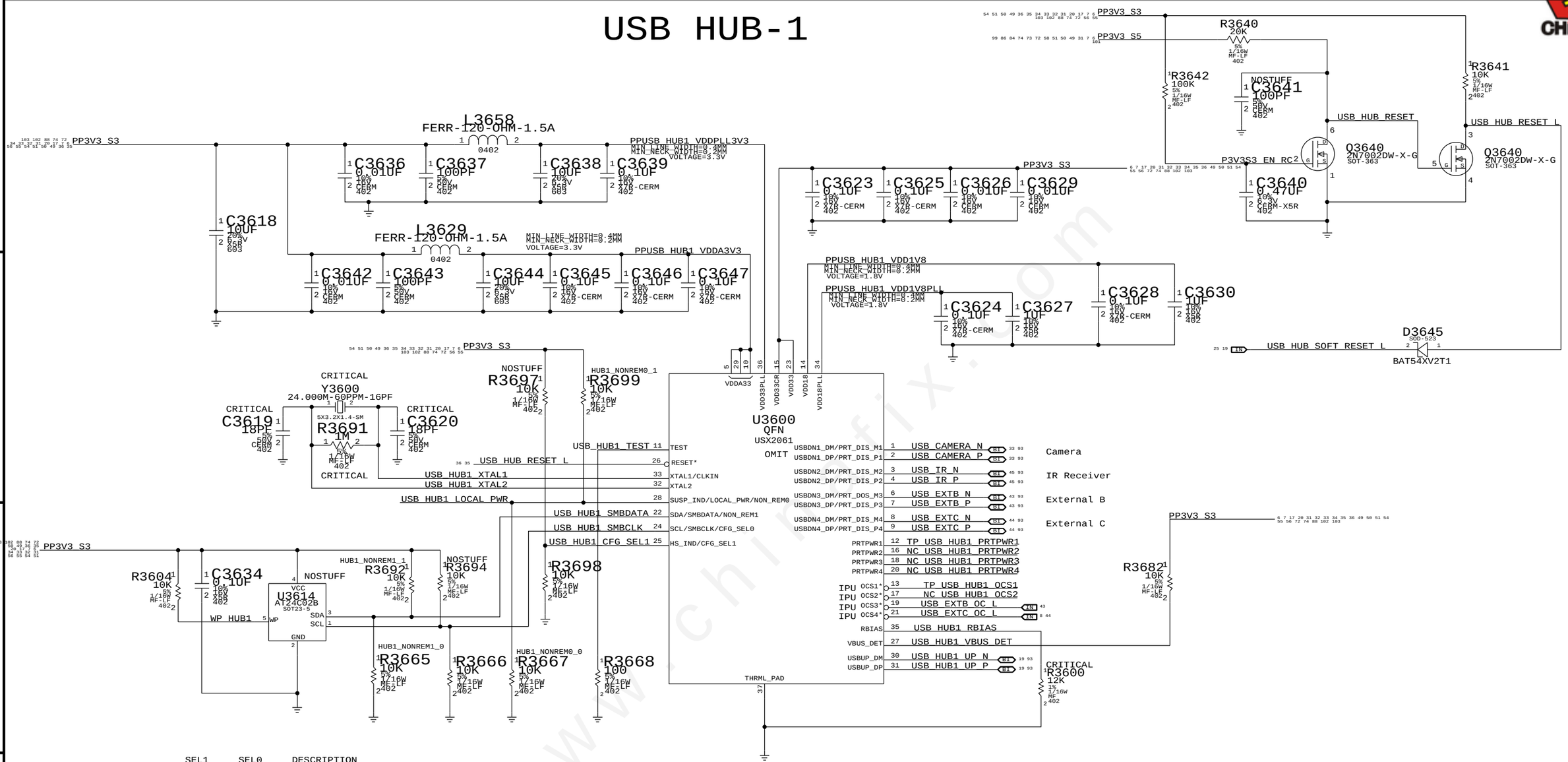
USB HUB-1



SEL1	SEL0	DESCRIPTION
0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	IC,ASSP,USB2.0,HUB CNTROL,4 PRT,36QFN	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	IC,USB2514B,USB 2.0,HUB CNTRL,4 PRT,36QFN	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	IC,USX2061,USB 2.0,HUB CNTRL,4 PRT,36QFN	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC MASTER=K18 MLB SYNC DATE=10/07/2009

PAGE TITLE: USB HUB 1

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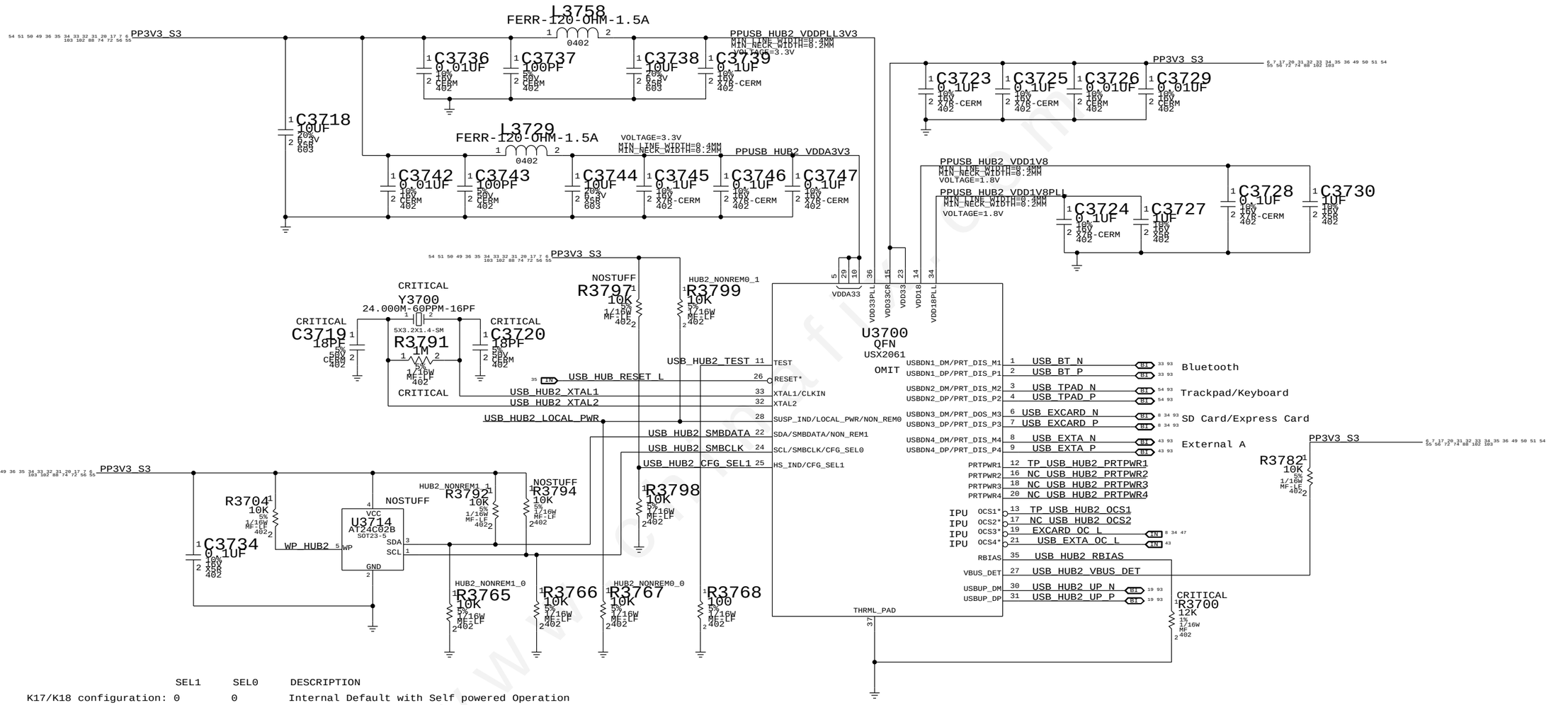
USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

SYNC MASTER=K18_MLB SYNC DATE=10/09/2009

PAGE TITLE: USB HUB 2

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BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

PP3V3_ENET
86mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-0.5A
CRITICAL L3905 FERR-600-OHM-0.5A
CRITICAL L3910 FERR-600-OHM-0.5A

PP3V3_ENET_PHY_XTALVDDH
PP3V3_ENET_PHY_BIASVDDH
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

BCM57765 R3915 0 5% 1/16W MF-LF 402
BCM57765 R3900 0 5% 1/16W MF-LF 402
C3900 0.1UF 10% 16V X7R-CERM 402
C3905 0.1UF 10% 16V X7R-CERM 402
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDO_PIN20
BCM57765_XTALVDDH
BCM57765_SR_LX
BCM57765_SR_VFB

CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_AVDDL
PP1V2_ENET
396mA (1000base-T, Caesar II)
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402
C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

BCM57765 R3940 4.7K 5% 1/16W MF-LF 402
BCM57765 R3941 4.7K 5% 1/16W MF-LF 402

AVDDH BIASVDDH VDDC VDDIO XTALVDDH VDDIO VDDIO VDDC REGCTL12 VDDIO WAKE* AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC VDDC

PP3V3_S0
BCM57765 R3942 1K 5% 1/16W MF-LF 402

C3950 0.1uF
C3951 0.1uF
C3955 0.1uF
C3956 0.1uF

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

BCM57765 R3943 0 5% 1/16W MF-LF 402
ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT (IPD)
PCIE_ENET_D2R_C_N → PCIE_TXD_N
PCIE_ENET_D2R_C_P → PCIE_TXD_P
PCIE_ENET_R2D_P → PCIE_RXD_P
PCIE_ENET_R2D_N → PCIE_RXD_N
PCIE_CLK100M_ENET_P → PCIE_REFCLK_P
PCIE_CLK100M_ENET_N → PCIE_REFCLK_N
ENET_RESET_L → PERST* (IPD)
ENET_CLKREQ_L → CLKREQ* (OD)
BCM57765_WAKE_L → LINKLED* (OD)
ENET_LOW_PWR → LOW_PWR (IPD)
BCM57765_SMB_CLK → VDDC
BCM57765_SMB_DATA → UART_MODE (IPD-BCM5764M)
BCM5764_SCLK → SCLK
BCM5764_MISO → SI
BCM5764_MOSI → SO
BCM5764_CS_L → CS* (IPD)
TP_BCM5764_SPD100LED_L → SPD100LED*
TP_BCM5764_TRAFFICLED_L → TRAFFICLED*
BCM5764_CLK25M_XTALI → XTALI
BCM5764_CLK25M_XTALO → XTALO
BCM5764_RDAC → RDAC

CRITICAL OMIT U3900 BCM5764M QFN-8X8 VERSION 2

THRM_PAD 69

BCM57765 R3965 1.24K 1% 1/16W MF-LF 402

ENET_MDI_P<0> 84
ENET_MDI_N<0> 84
ENET_MDI_P<1> 84
ENET_MDI_N<1> 84
ENET_MDI_P<2> 84
ENET_MDI_N<2> 84
ENET_MDI_P<3> 84
ENET_MDI_N<3> 84

CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.
BCM57765 C3970 4.7UF 10% 6.3V X5R-CERM 603
BCM57765 C3971 0.1UF 10% 16V X7R-CERM 402
BCM57765 C3972 0.1UF 10% 16V X7R-CERM 402

PP3V3R1V8_SW_SD_VIO
BCM57765_MEDIA_SENSE
R3972 0 5% 1/16W MF-LF 402
ENET_ENERGY_DET

BCM57765_CR_CMD
BCM57765_CR_DATA<5>
BCM57765_CR_DATA<6>
BCM57765_CR_DATA<7>
BCM57765_CE_L_MS_INS_L
BCM57765_CR_LED
TP_BCM57765_XD_DET

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
U3990 AT45DB011D SOIC-8S1 OMIT
C3990 0.1UF 10% 16V X7R-CERM 402
BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO
BCM57765 R3990 4.7K 5% 1/16W MF-LF 402
BCM5764M R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function

60-ENERGY_DET	BCM57765_CR_LED	R3980	0	ENET_ENERGY_DET
13-WAKE*	BCM57765_SR_VFB	R3981	0	ENET_WAKE_L (See note)
53-VMAIN_PRSNT	BCM57765_CR_DATA<5>	R3982	1K	PP3V3_S0
59-SMB_CLK	BCM57765_CE_L_MS_INS_L	R3983	4.7K	PP3V3_ENET
58-SMB_DATA	BCM57765_VMAIN_PRSNT	R3984	4.7K	
54-VAUX_PRSNT	BCM57765_CR_DATA<6>	R3985	1K	
16-VDDIO	BCM57765_SR_LX	R3986	0	
20-XTALVDDH	BCM57765_VDDO_PIN20	R3987	0	PP3V3_ENET_PHY_XTALVDDH
55-VDDC	BCM57765_CR_DATA<7>	R3988	0	PP1V2_ENET
17-VDDC	BCM57765_XTALVDDH	R3989	0	
14-VDDC	BCM57765_SR_VDD	R3998	0	
06-VDDC	BCM57765_SMB_CLK	R3999	0	

All resistors: 5% 1/16W MF-LF 402

L3999 FERR-600-OHM-0.5A SM CRITICAL
26-PCIE_VDDL — BCM57765_CR_CMD — PLACE_NEAR=U3900.26:4 mm
Keep net short, with no stubs.
BCM5764M C3999 0.1UF 10% 16V X7R-CERM 402 — PLACE_NEAR=U3900.26:4 mm
BCM5764M C3998 4.7UF 10% 6.3V X5R-CERM 603 — PLACE_NEAR=L3999.1:4 mm

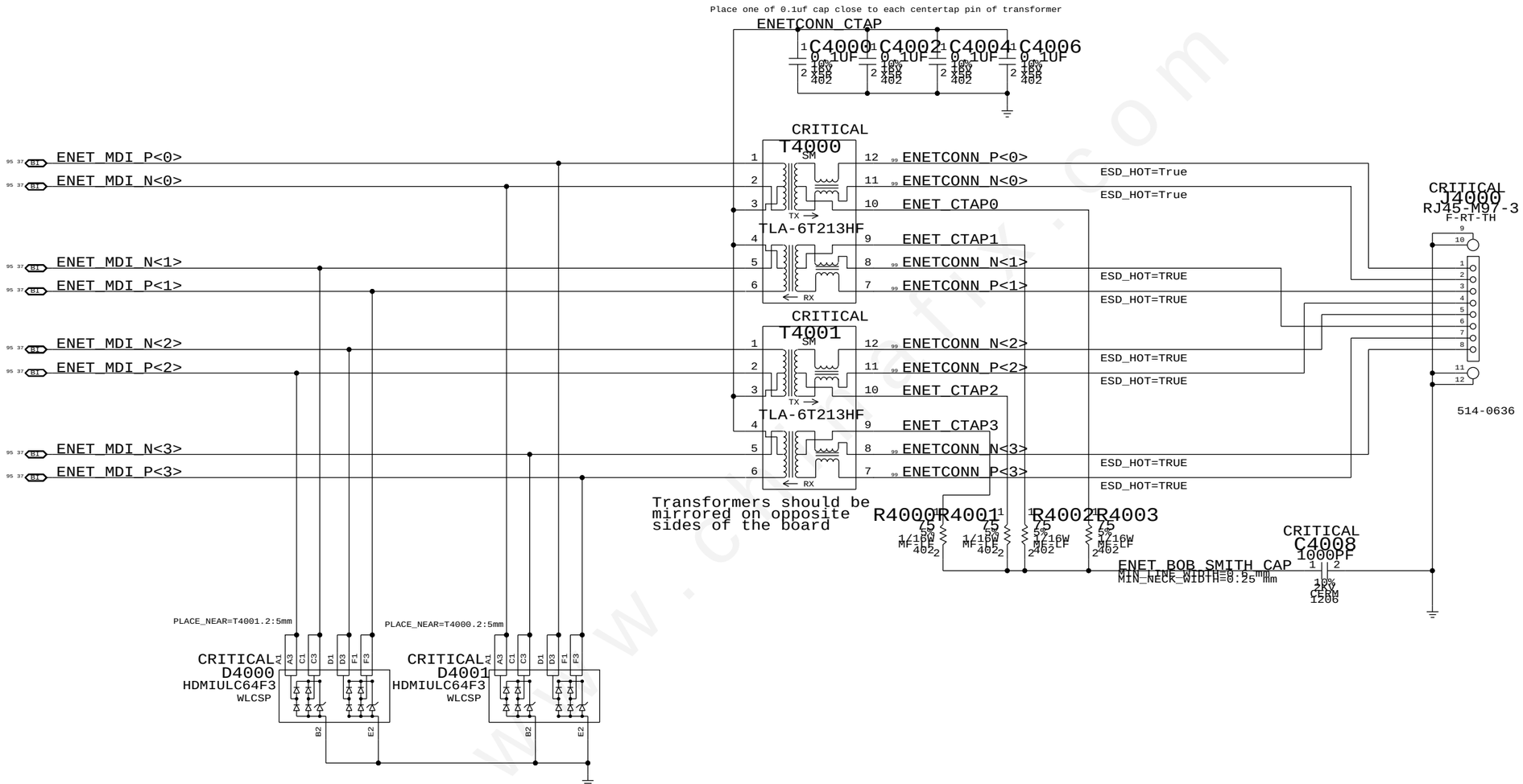
SYNC_MASTER=K18_MLB SYNC_DATE=10/28/2009
PAGE TITLE: Ethernet PHY (Caesar II/IV)
Apple Inc.
DRAWING NUMBER — SIZE D
REVISION
BRANCH
PAGE 39 OF 132
SHEET 37 OF 103

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

SYNC_MASTER=K17 WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

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BRANCH

PAGE: 40 OF 132

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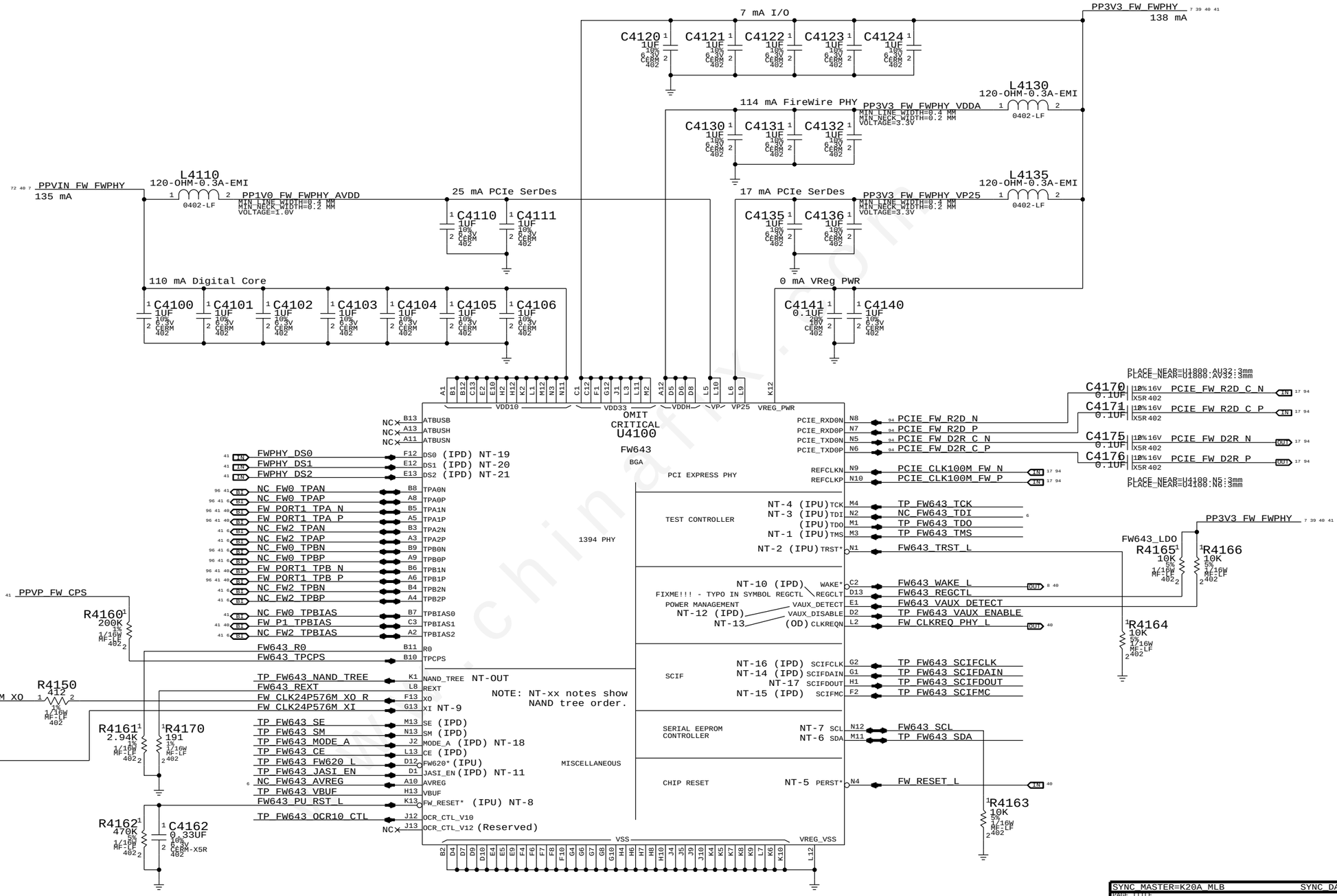

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

3.3V FW FET

I(max) = 1.7A (85C)

PP3V3_S0 → C4201 1UF 10% 6.3V CERM 402 → U4201 TPS22924 CSP (A2, B2, VIN, C2, ON, GND, C1; A1, B1, VOUT) CRITICAL → PP3V3_FW_FWPHY

FW_PWR_EN (IN) → C2

1.05V FW FET

PPCPUVTT_S0 → C4202 1UF 10% 6.3V CERM 402 → U4202 TPS22924 CSP (A2, B2, VIN, C2, ON, GND, C1; A1, B1, VOUT) CRITICAL → PP1V0_FW

FW_CLKREQ_L (OUT) → Q4261 SSM6N15FEAPE SOT563 (D3, G5, S4) → FW_CLKREQ_PHY_L (IN) → FW_CLKREQ_PHY_L (MAKE_BASE=TRUE)

FireWire Port Power Switch

PP3V3_S0 → R4281 100K 5% 1/16W MF-LF 402 → Q4299 DMB53D0UV SOT-563 (CRITICAL)

PPVIN_FW_FWPHY → R4280 10K 1% 1/16W MF-LF 402 → P1V0_FW_RC → Q4299

C4281 1UF 10% 16V 0.1X CERM 402

P1V0_RESET_GATE → R4283 10K 5% 1/16W MF-LF 402 → PLT_RESET_L (IN)

Q4299 DMB53D0UV SOT-563 (CRITICAL) → FW_RESET_L (OUT)

PP1V05_FW PGOOD/FW_RESET_L

PP3V3_FW_FWPHY → R4277 10K 5% 1/16W MF-LF 402

R4276 100K 5% 1/16W MF-LF 402 → FW_PLUG_DET_L (OUT)

FW_WAKE → Q4276 DMB53D0UV SOT-563 (CRITICAL)

NOSTUFF C4276 0.1UF 10% 16V X5R 402

FW643_WAKE_L (BI) → Q4276

Late-VG Protection

PP3V3_S0 → C4200 0.1UF 10% 16V X5R 402 (PLACE_NEAR=U4200.1:4mm)

Q4262 BSS8402DW SOT-363 (SYM-VER1)

U4200 TPD4S1394 LLP (CRITICAL, PLACE_NEAR=J4310.4:4mm)

FW_PORT1_TPA_P (BI) → D1+
FW_PORT1_TPA_N (BI) → D1-
FW_PORT1_TPB_P (BI) → D2+
FW_PORT1_TPB_N (BI) → D2-

VCLMP → TP_FW_LATEVG_VCLMP

FWPWR_EN → R4201 100K 5% 1/16W MF-LF 402

PPBUS_G3H → R4260 470K 5% 1/16W MF-LF 402 → FWPWR_EN_L_DIV

C4260 0.1UF 10% 25V X5R 402

Q4260 NDS9407 SOI-HF (CRITICAL) → PPBUS_FW_FWBOOST

R4262 10K 5% 1/16W MF-LF 402 → FWPWR_EN_TRI

R4263 10 5% 1/16W MF-LF 402 → FWPWR_EN_TRI_R

Q4262 BSS8402DW SOT-363 → R4261 330K 5% 1/16W MF-LF 402 → FWPWR_EN_L

Q4261 SSM6N15FEAPE SOT563

NOSTUFF C4261 0.1UF 10% 16V X5R 402

PP10V_FW → F4260 1.5A-24V 1812L15024HF (CRITICAL) → PP10V_FW_D (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=10V) → D4260 CRS08-1.5A-30V (CRITICAL) → PPVP_FW

PPCPUVTT_S0 → R4275 1K 5% 1/16W MF-LF 402 → FW_PWR_EN_L

R4270 330K 5% 1/16W MF-LF 402 → FW_DET_MIRROR

R4271 56K 5% 1/16W MF-LF 402 → FW_PLUG_DET

Q4270 BC847CDXV6TXG SOT563 (CRITICAL)

C4270 0.1UF 10% 16V X5R 402

FW_PLUG_DET_L (OUT) ← Q4275 DMB53D0UV SOT-563 (CRITICAL)

FW_P1_TPBIAS_R

R4272 1K 5% 1/16W MF-LF 402

R4273 12K 5% 1/16W MF-LF 402 (PLACE_NEAR=C4360.1:4mm)

FW_PWR_EN (IN) → Q4275

FW_P1_TPBIAS (IN)

SYNC_MASTER=K20A_MLB	SYNC_DATE=03/26/2009
PAGE TITLE	FireWire Port Power
Apple Inc.	DRAWING NUMBER: D; SIZE: D
	REVISION:
	BRANCH:
	PAGE: 42 OF 132
	SHEET: 40 OF 103

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain
the necessary aliases to map the
FireWire TPA/TPB pairs to their
appropriate connectors and/or to
properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT
constrained on this page. It is
assumed that FireWire PHY page will
provide the appropriate constraints
to apply to entire TPA/TPB XNets.

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

41 40 39 7 PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

41 39 FWPHY_DS0 — MAKE_BASE=TRUE — FWPHY_DS0 39 41

41 39 FWPHY_DS2 — MAKE_BASE=TRUE — FWPHY_DS2 39 41

41 39 FWPHY_DS1 — MAKE_BASE=TRUE — FWPHY_DS1 39 41

R4381 10K 1% 1/10W MF-LF 402

41 39 NC_FW0_TPBIAS — NC_FW0_TPBIAS MAKE_BASE=TRUE 39 41

41 39 6 NC_FW2_TPBIAS — NC_FW2_TPBIAS MAKE_BASE=TRUE 6 39 41

96 41 39 NC_FW0_TPAN — NC_FW0_TPAN MAKE_BASE=TRUE 39 41 96

96 41 39 6 NC_FW0_TPAP — NC_FW0_TPAP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPAN — NC_FW2_TPAN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPAP — NC_FW2_TPAP MAKE_BASE=TRUE 6 39 41

96 41 39 6 NC_FW0_TPBN — NC_FW0_TPBN MAKE_BASE=TRUE 6 39 41 96

96 41 39 6 NC_FW0_TPBP — NC_FW0_TPBP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPBN — NC_FW2_TPBN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPBP — NC_FW2_TPBP MAKE_BASE=TRUE 6 39 41

Termination

Place close to FireWire PHY

40 39 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 16V CERM-X5R 402

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.A5:2mm

PLACE_NEAR=U4100.B5:2mm

96 41 40 39 FW_PORT1_TPA_P — MAKE_BASE=TRUE — 39 40 41 96

96 41 40 39 FW_PORT1_TPA_N — MAKE_BASE=TRUE — 39 40 41 96

96 41 40 39 FW_PORT1_TPB_P — MAKE_BASE=TRUE — 39 40 41 96

96 41 40 39 FW_PORT1_TPB_N — MAKE_BASE=TRUE — 39 40 41 96

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.B6:4mm

PLACE_NEAR=U4100.A6:4mm

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

41 40 7 6 PPVP_FW

R4311 470K 5% 1/16W MF-LF 402

Q4300 BSS8402DW SOT-363 (SYM-VER1)

41 39 PPVP_FW_CPS MAKE_BASE=TRUE — PPVP_FW_CPS 39 41

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

41 40 39 7 PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

Cable Power

41 40 7 6 PPVP_FW

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

96 41 40 39 FW_PORT1_TPB_N — ESD_HOT=TRUE

96 41 40 39 FW_PORT1_TPB_P — ESD_HOT=TRUE

96 41 40 39 FW_PORT1_TPA_N — ESD_HOT=TRUE

96 41 40 39 FW_PORT1_TPA_P — ESD_HOT=TRUE

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

1 TPB- TPB(R) 9 TPB<R> 2 TPB+ VP 8 VP

NC 7 VPC/NC

6 VG 3 TPA- VG 5 TPA<R> 4 TPA+ TPA(R)

OUTPUT

INPUT

10 11 12 13 CHASSIS GND

C4319 0.1uF 10% 50V X7R 603-1

PLACE_NEAR=J4310.5:3mm

R4319 1M 5% 1/16W MF-LF 402

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

SYNC_MASTER=K18_MLB SYNC_DATE=07/08/2009

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: — SIZE: D

REVISION:

BRANCH:

PAGE: 43 OF 132

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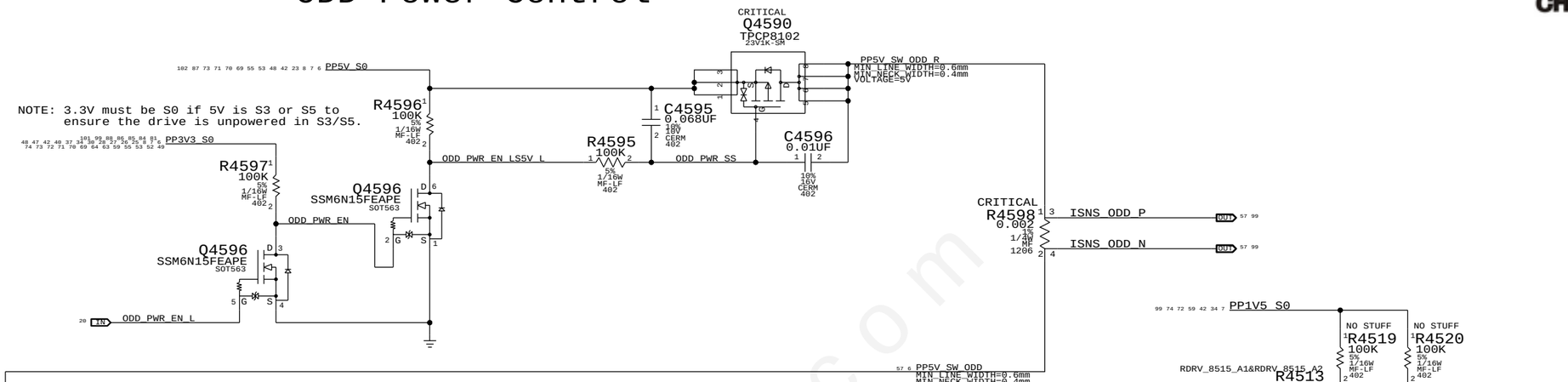
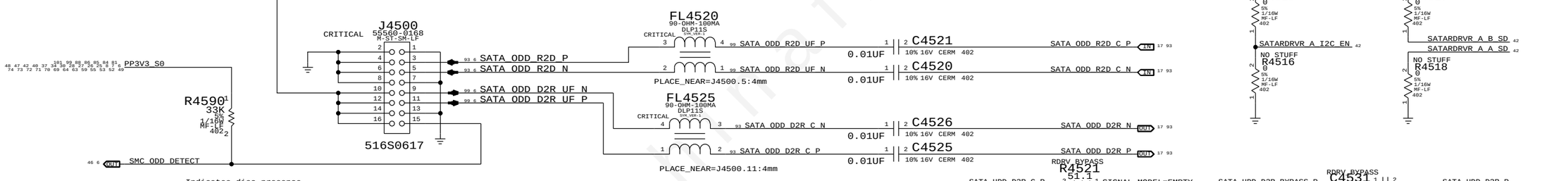
ODD Power Control



SATA ODD Port



SATA HDD Port

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8515_A1
338S0848	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8515_A2

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: D

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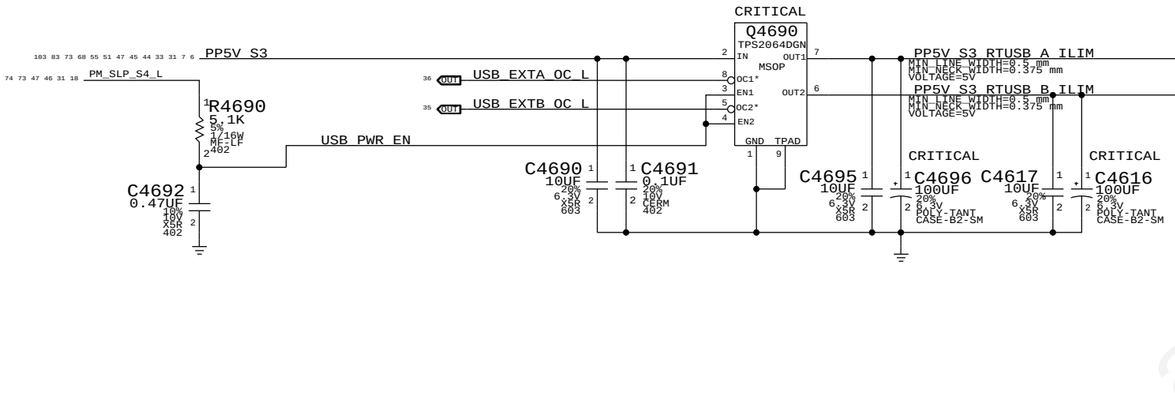
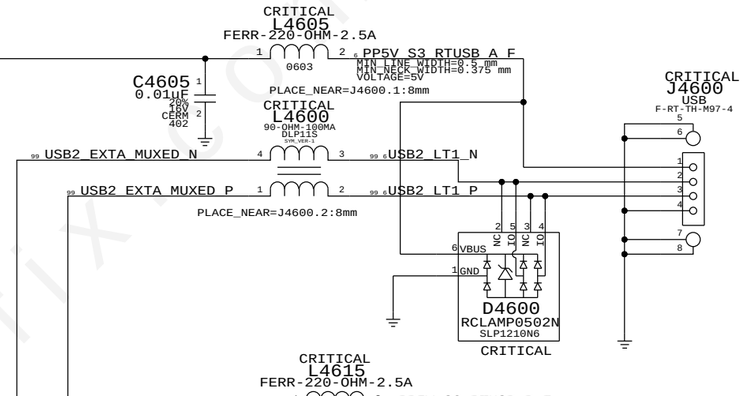
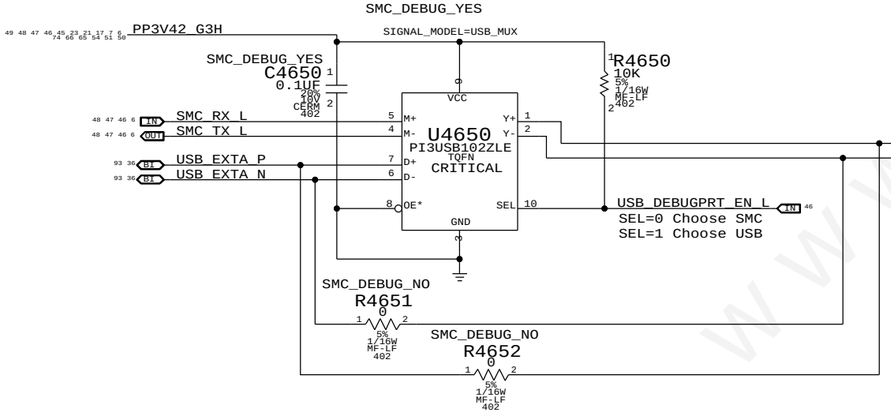
Port Power Switch



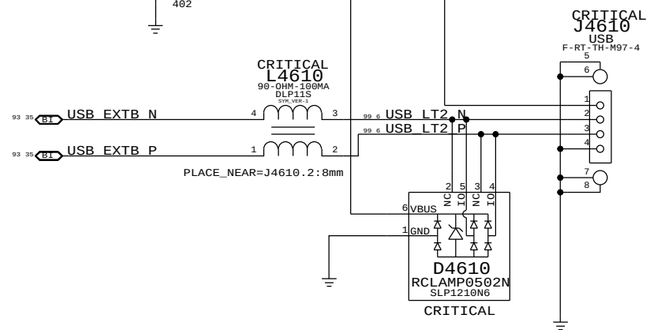
Left USB Port A



USB/SMC Debug Mux



Left USB Port B



SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER | SIZE: D

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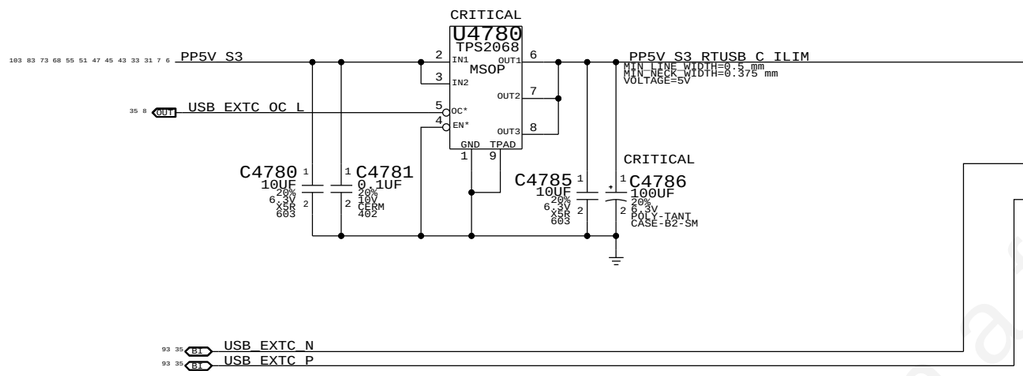
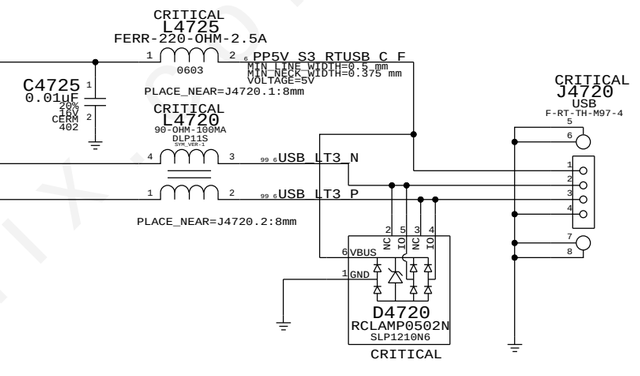
Port Power Switch

ENABLE TIED LOW SO INPUT POWER SOURCE MUST BE S3!!!



LEFT USB PORT C



SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE
PROJECT SPECIFIC CONNS

Apple Inc.

DRAWING NUMBER | SIZE D
REVISION
BRANCH
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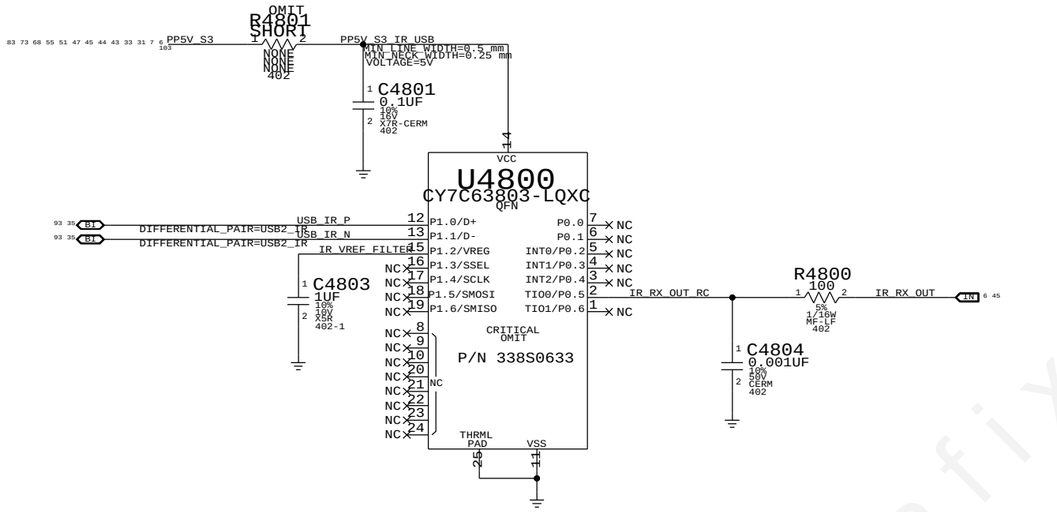

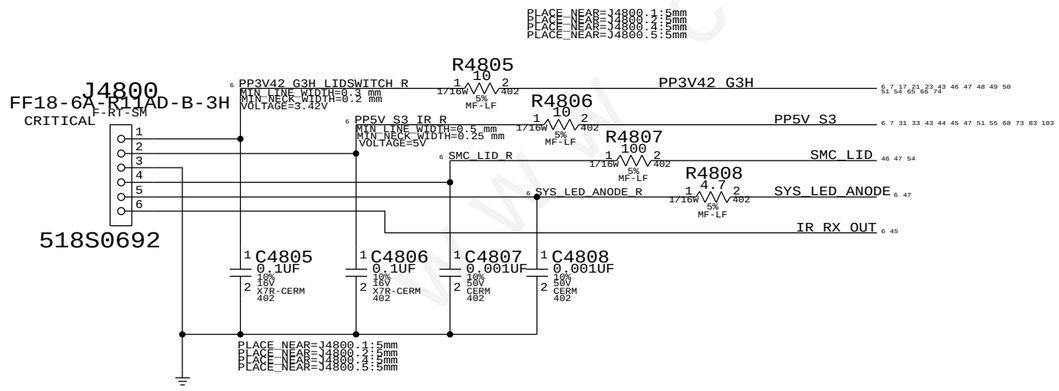

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: Front Flex Support

Apple Inc.

DRAWING NUMBER | SIZE: D

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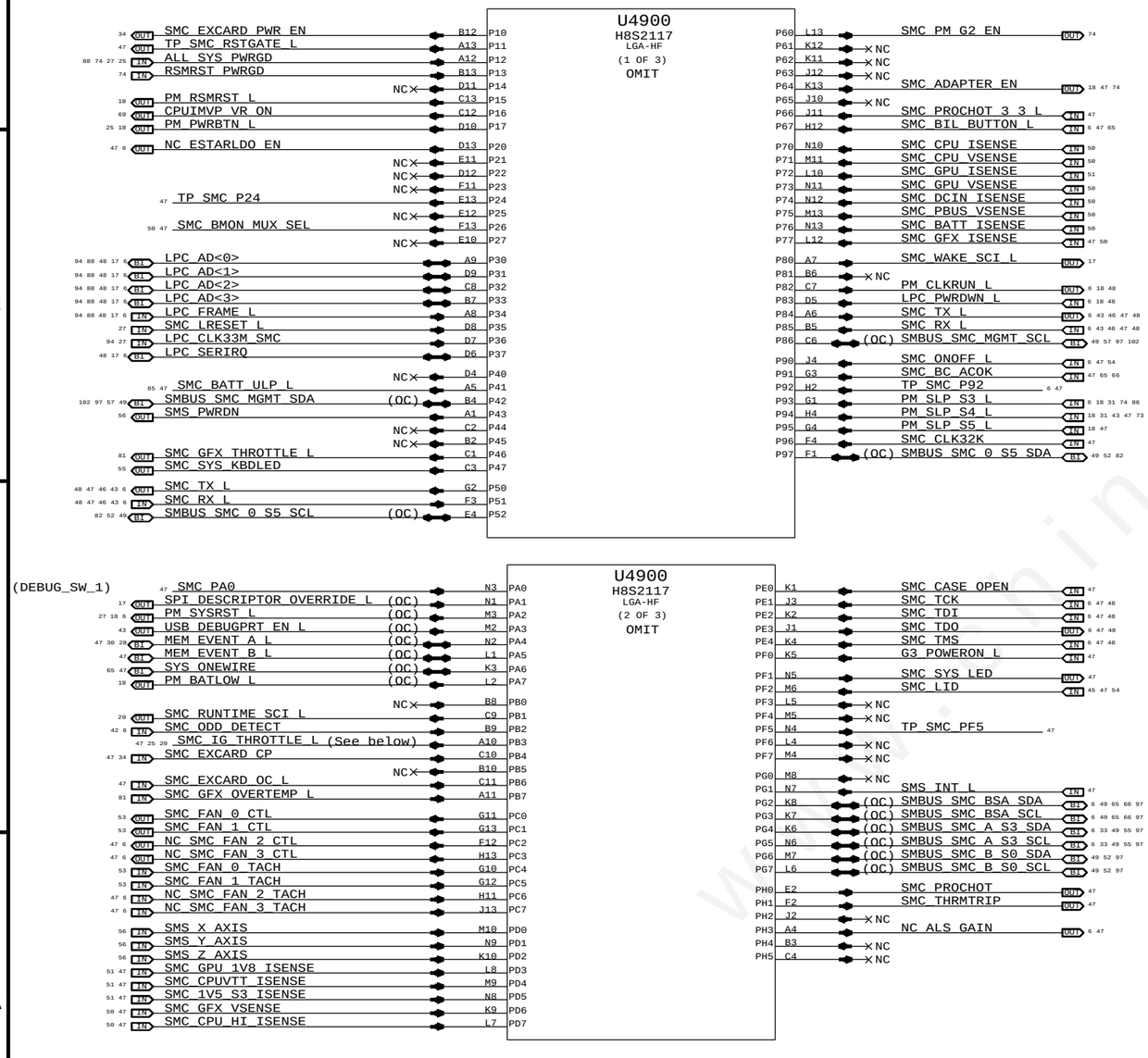
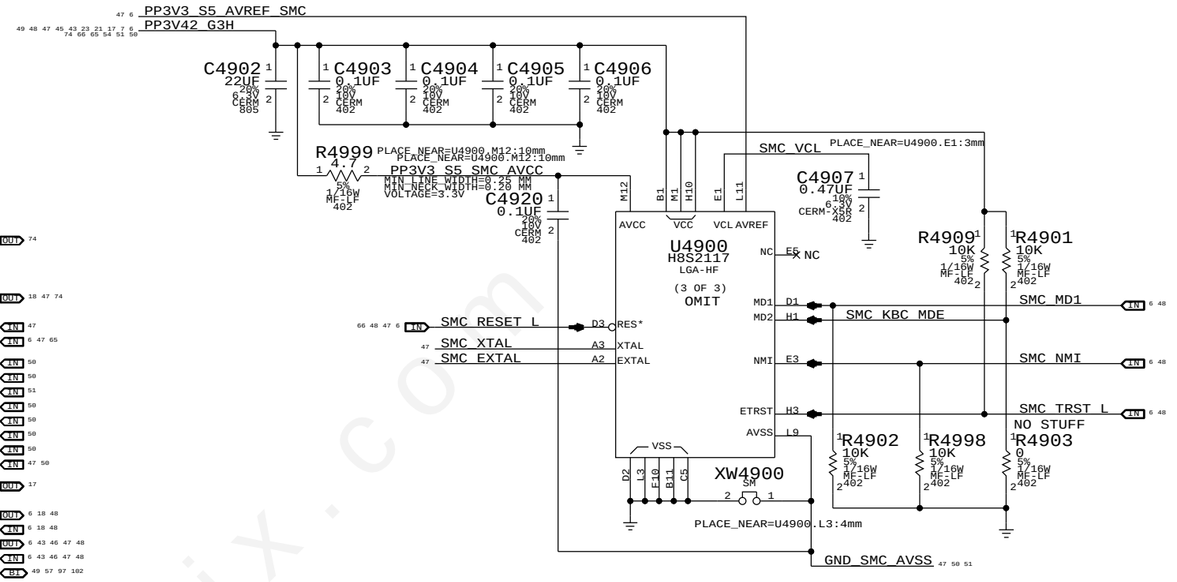
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER | SIZE: D

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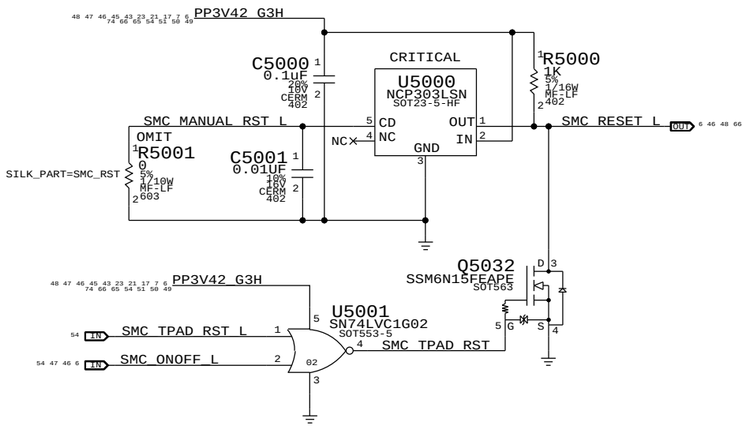
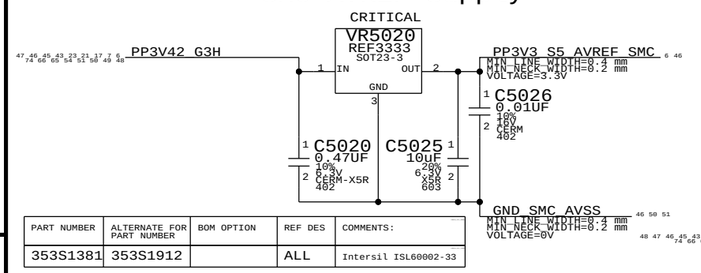
SMC Reset "Button" / Brownout Detect

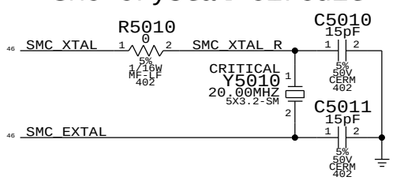


SMC AVREF Supply

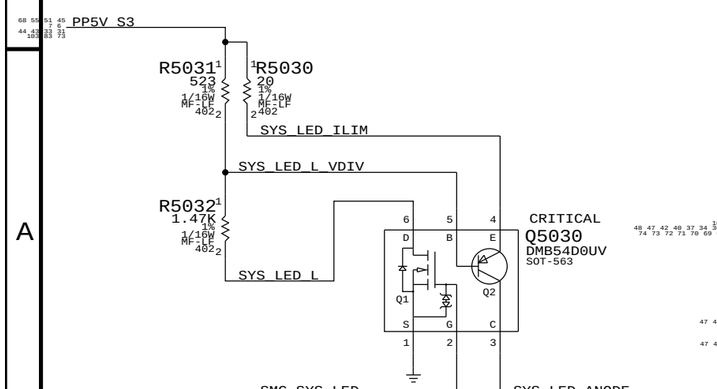


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

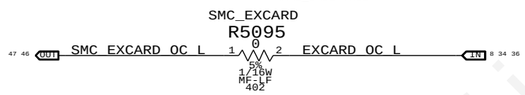
SMC Crystal Circuit



System (Sleep) LED Circuit

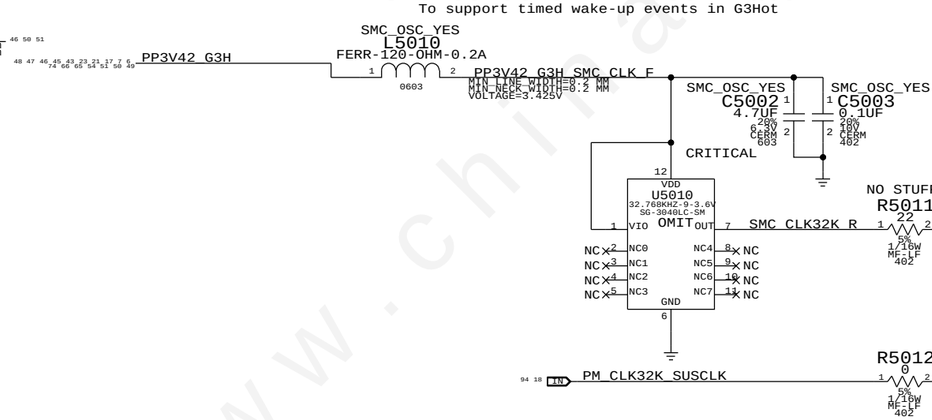


SMC_EXCARD

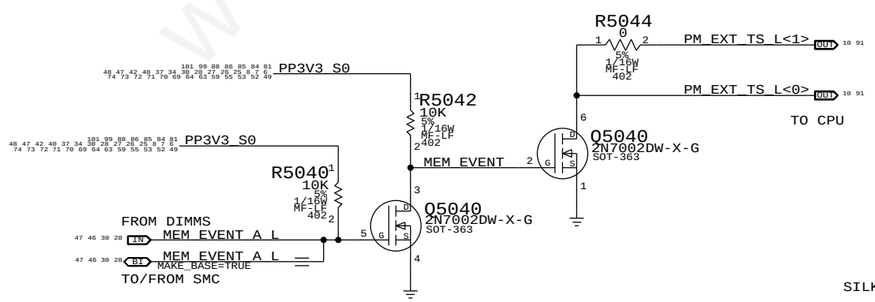


SMC G3Hot 32kHz Oscillator

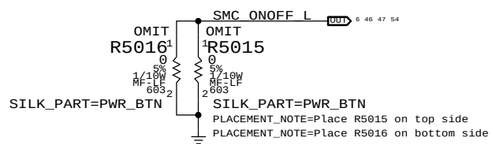
To support timed wake-up events in G3Hot



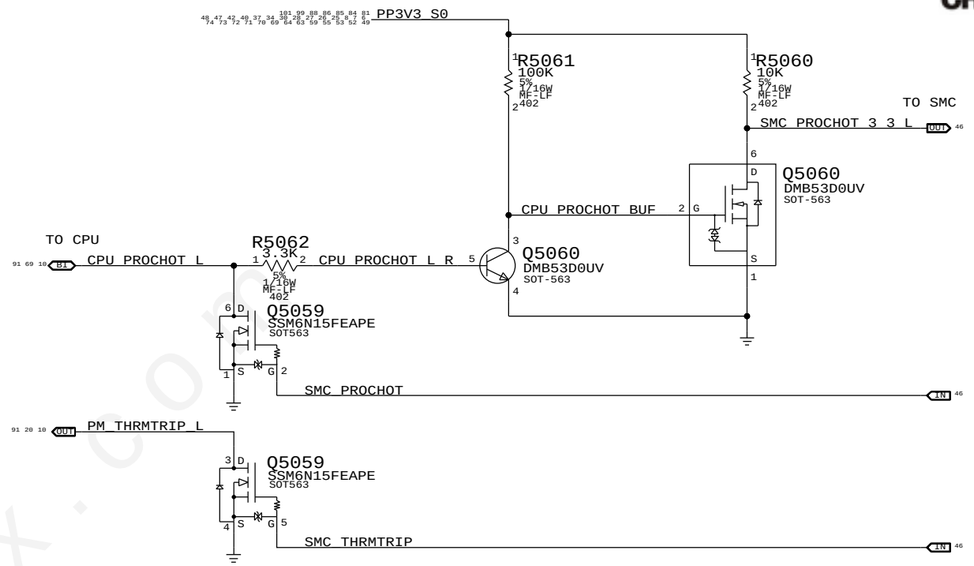
CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting



Debug Power "Buttons"



SMC FSB to 3.3V Level Shifting



SMC_ONOFF_L	R5070	10K	5% 1/16W MF-LF 402	PP3V42_G3H
G3_POWERON_L	R5072	10K	5% 1/16W MF-LF 402	
SMC_LID	R5071	100K	5% 1/16W MF-LF 402	
SMC_TX_L	R5073	10K	5% 1/16W MF-LF 402	
SMC_RX_L	R5074	100K	5% 1/16W MF-LF 402	
SYS_ONEWIRE_NO_STUFF	R5075	2.0K	5% 1/16W MF-LF 402	
SMC_TMS	R5077	10K	5% 1/16W MF-LF 402	
SMC_TDO	R5078	10K	5% 1/16W MF-LF 402	
SMC_TDI	R5079	10K	5% 1/16W MF-LF 402	
SMC_TCK	R5080	10K	5% 1/16W MF-LF 402	
SMC_BIL_BUTTON_L	R5081	10K	5% 1/16W MF-LF 402	
SMC_BC_ACOK	R5087	470K	5% 1/16W MF-LF 402	
SMS_INT_L	R5093	10K	5% 1/16W MF-LF 402	
SMC_BATT_ULP_L	R5096	100K	5% 1/16W MF-LF 402	
SMC_PA0	R5091	100K	5% 1/16W MF-LF 402	
SMC_EXCARD_OC_L	R5092	100K	5% 1/16W MF-LF 402	SMC_EXCARD_NOT
SMC_ADAPTER_EN	R5085	10K	5% 1/16W MF-LF 402	
SMC_CASE_OPEN	R5086	10K	5% 1/16W MF-LF 402	
SMC_EXCARD_CP	R5088	10K	5% 1/16W MF-LF 402	
PM_SLP_S5_L	R5090	100K	5% 1/16W MF-LF 402	
PM_SLP_S4_L	R5094	100K	5% 1/16W MF-LF 402	
MEM_EVENT_B_L	R5089	10K	5% 1/16W MF-LF 402	PP3V3_S0

SYNC_MASTER=K17_REF	SYNC_DATE=06/17/2009
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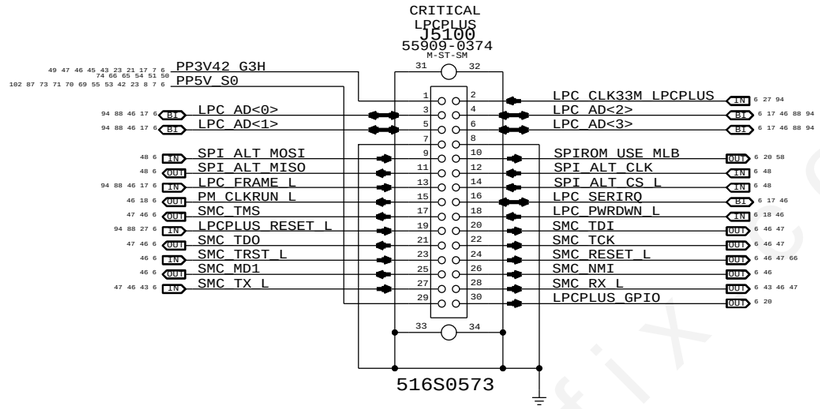
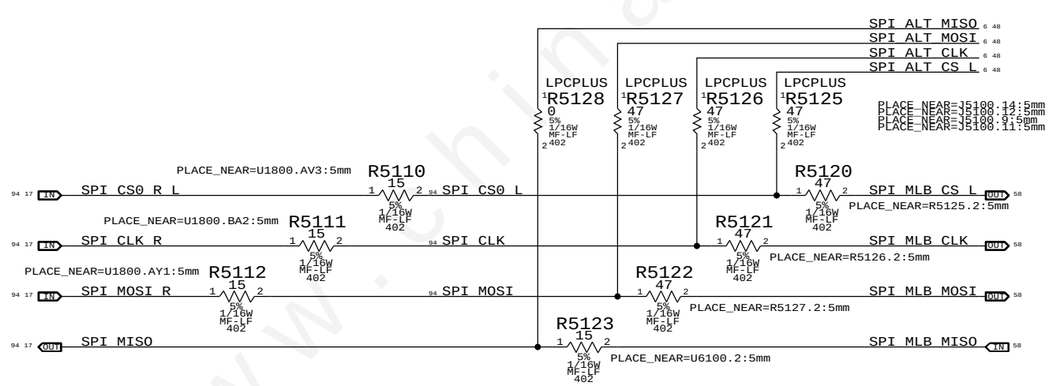
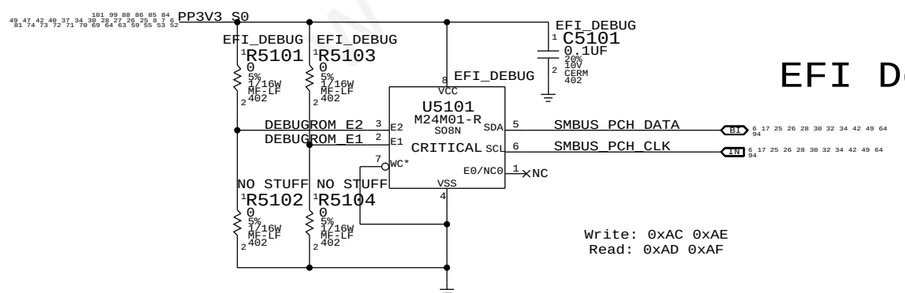
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=T22_MLB SYNC_DATE=03/30/2009

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 1/16W MF-LF 402 — R5201 1K 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U2900
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2901
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

CK505 (Clock)
U2700
(Write: 0xD2 Read: 0xD3)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

EFI Debug Serial
U5101
(Write: 0xAC 0xAE)
(Read: 0xAD 0xAF)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

ExpressCard Slot
J3500
(Address via ARP)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2600 & J2650
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6800
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDD Re-driver Control
U4510
(Write: 0x94 Read: 0x95)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 1/16W MF-LF 402 — R5211 8.2K 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF R5220 8.2K 1/16W MF-LF 402 — NO STUFF R5221 8.2K 1/16W MF-LF 402

R5223 0 1/16W MF-LF 402

R5222 0 1/16W MF-LF 402

Ibex Peak-M
U1800
(Write: 0x90 Read: 0x91)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 1/16W MF-LF 402 — R5251 4.7K 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S5_SCL
- SMBUS_SMC_0_S5_SDA
MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S5_SCL
- SMBUS_SMC_0_S5_SDA

GPU Temp (Int)
GT216: U8000
(Write: 0x9E Read: 0x9F)
- SMBUS_SMC_0_S5_SCL
- SMBUS_SMC_0_S5_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 1/16W MF-LF 402 — R5271 1K 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x72 Read: 0x73)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 1/16W MF-LF 402 — R5261 4.7K 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

CPU Temp
EMC1414: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 2.0K 1/16W MF-LF 402 — R5281 2.0K 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S5

R5290 4.7K 1/16W MF-LF 402 — R5291 4.7K 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

Sensor ADC B
UC210
(Write: 0x32 Read: 0x33)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

SYNC_MASTER=K17_WFERRY SYNC_DATE=05/20/2009

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K17 SMBus Connections

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CPU Voltage Sense / Filter

PPVCORE_S0_CPU → XW5309 (SM) → CPUVSENSE_IN → R5309 4.53K (PLACE_NEAR=U4900.M11:10mm, 1% 1/16W MF-LF 402) → SMC_CPU_VSENSE (OUT 46)

Place short near U1000 center

C5309 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.M11:10mm

GND_SMC_AVSS 46 47 50 51

GPU Voltage Sense / Filter

PPVCORE_GPU → XW5359 (SM) → GPUVSENSE_IN → R5359 4.53K (PLACE_NEAR=U4900.N11:10mm, 1% 1/16W MF-LF 402) → SMC_GPU_VSENSE (OUT 46)

Place short near U8000 center

C5359 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.N11:10mm

GND_SMC_AVSS 46 47 50 51

GFX Voltage Sense / Filter

PPVCORE_S0_GFX → XW5399 (SM) → GFXVSENSE_IN → R5399 4.53K (PLACE_NEAR=U4900.K9:10mm, 1% 1/16W MF-LF 402) → SMC_GFX_VSENSE (OUT 46 47)

PLACEMENT_NOTE=Place near U1000

C5399 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.K9:10mm

GND_SMC_AVSS 46 47 50 51

PBUS Voltage Sense & Filter

PPBUS_G3H → Q5315 FDG6332CG SC70-6 (P-CHN) → PPBUS_G3H_VSENSE (MIN_LINE_WIDTH=0.20 mm, MIN_NECK_WIDTH=0.20 mm, VOLTAGE=6V)

R5315 100K (5% 1/16W MF-LF 402) → PBUSVSENS_EN_DIV

R5316 100K (5% 1/16W MF-LF 402) → PBUSVSENS_EN_L

R5385 12.7K (1% 1/16W MF-LF 402) PLACE_NEAR=U4900.M13:10mm

Rthevenin = 4504 ohms

SMC_PBUS_VSENSE (OUT 46)

R5386 6.98K (1% 1/16W MF-LF 402)

C5385 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.M13:10mm

PLACE_NEAR=U4900.M13:10mm

GND_SMC_AVSS 46 47 50 51

PM_SLP_S3_L_R → Q5315 FDG6332CG SC70-6 (N-CHN)

Enables PBUS VSense divider when high.

DCIN Current Sense Filter

PLACE_NEAR=U4900.N12:10mm

CHGR_AMON (IN 66) → R5380 4.53K (1% 1/16W MF-LF 402) → SMC_DCIN_ISENSE (OUT 46)

C5380 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.N12:10mm

GND_SMC_AVSS 46 47 50 51

CPU VCore High Side Current Sensor

PP3V42_G3H

PPBUS_CPU_IMVP_ISNS (OUT 69 7 6)

OMIT R5388 0.001 (1% 1W MF 1206) → ISNS_CPU_N / ISNS_CPU_P

U5388 INA213 SC70: IN- IN+ V+ GND REF OUT → CPUVCORE_HISIDE_IOUT

GAIN: 50X

C5388 0.1UF (20% 10V CERM 402)

PLACE_NEAR=U4900.L7:10mm

R5335 4.53K (1% 1/16W MF-LF 402) → SMC_CPU_HI_ISENSE (OUT 46 47)

C5335 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.L7:10mm

GND_SMC_AVSS 46 47 50 51

PPBUS_G3H (IN 83 71 70 68 67 66 50 40 8 7 6 87)

CRITICAL C5300 100UF (20% 16V TANT D-HF)

CRITICAL C5301 100UF (20% 16V TANT D-HF)

CRITICAL C5302 68UF (20% 16V POLY-TANT CASE-D2E-SM)

CRITICAL C5303 68UF (20% 16V POLY-TANT CASE-D2E-SM)

CRITICAL C5304 68UF (20% 16V POLY-TANT CASE-D2E-SM)

CRITICAL C5305 68UF (20% 16V POLY-TANT CASE-D2E-SM)

CRITICAL C5306 68UF (20% 16V POLY-TANT CASE-D2E-SM)

BMON Current Sense - Entire circuit must be near SMC (U4900)

PP3V42_G3H

REGULATOR SIDE:

BMON_ENG → C5318 0.1uF (20% 10V CERM 402)

U5323 INA214 SC70: IN- IN+ V+ GND OUT

CHGR_CSO_R_P (OUT 99 66) → IN-

CHGR_CSO_R_N (IN 99 66) → IN+

LOAD SIDE:

REF → GND

GAIN: 100X

Monitors battery discharge current from battery to PBUS

U5313 NC7SB3157P6XG SC70: B1 GND B0 VCC A SEL

BMON_INA_OUT → B1

CHGR_BMON (IN 66) → B0

BMON_AMUX_OUT → A

SMC_BMON_MUX_SEL (IN 46 47)

BMON_PROD: R5330 0 (5% 1/16W MF-LF 402)

R5371 100K (5% 1/16W MF-LF 402)

R5391 45.3K (1% 1/16W MF-LF 402) → SMC_BATT_ISENSE (OUT 46)

C5369 0.1uF (20% 10V CERM 402)

C5390 0.022UF (10% 16V CERM-X5R 402)

PLACE_NEAR=U4900.N13:10mm

PLACE_NEAR=U4900.N13:10mm

GND_SMC_AVSS 46 47 50 51

INA214 has gain of 100V/V
U5303 only senses current up to 6.6A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
102S0858	1	RES,1/2W,1%,0.010 OHM,SMD	R5388		

CPU VCore Load Side Current Sense / Filter

PP3V3_S3

CPUIMVP_IMON (IN 91 69 12) → R5350 6.65K (1% 1/16W MF-LF 402) → CPUISENS_P

R5351 10K (1% 1/16W MF-LF 402) → CPUISENS_N

U5350 OPA333DCKG4 SC70-5: V+ V- → CPUVCORE_IOUT

Gain: 3x

C5354 0.1UF (20% 10V CERM 402)

R5353 4.53K (1% 1/16W MF-LF 402) PLACE_NEAR=U4900.N10:5mm → SMC_CPU_ISENSE (OUT 46)

C5353 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.N10:5mm

GND_SMC_AVSS 46 47 50 51

R5352 20.0K (1% 1/16W MF-LF 402) SIGNAL_MODEL=EMPTY

C5357 470PF (10% 50V CERM 402) NO STUFF SIGNAL_MODEL=EMPTY

GFX/AXG Current Sense

PP3V3_S3

GFXIMVP_CS_R_P (IN 99 70) → R5342 6.65K (1% 1/16W MF-LF 603) → GFX_ISNS_R_P

GFXIMVP_CS_R_N (IN 99 70) → R5341 6.65K (1% 1/16W MF-LF 603) → GFX_ISNS_R_N

U5340 OPA333DCKG4 SC70-5: V+ V- → GFXIMVP_ISNS_IOUT

GAIN: 150X

C5344 0.1UF (20% 10V CERM 402) PLACE_NEAR=U4900.L12:10mm

R5379 4.53K (1% 1/16W MF-LF 402) → SMC_GFX_ISENSE (OUT 46 47)

C5379 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=U4900.L12:10mm

NO STUFF C5340 470PF (10% 50V CERM 402) SIGNAL_MODEL=EMPTY

R5340 1M (1% 1/16W MF-LF 402) SIGNAL_MODEL=EMPTY

R5343 1M (1% 1/16W MF-LF 402) NO STUFF SIGNAL_MODEL=EMPTY

C5343 470PF (10% 50V CERM 402)

PCH VCore Current Sense

PP3V3_S5

DEBUG_ADC → C5320 0.1UF (20% 10V CERM 402)

CRITICAL U5305 INA210 SC70: IN- IN+ V+ GND OUT

NC_ISNS_P1V05S0PCH_N (IN 99 8) → IN-

NC_ISNS_P1V05S0PCH_P (IN 99 8) → IN+

REF → GND

GAIN: 200X

PCH VCore Current Sense Filter

PLACE_NEAR=UC210.23:10mm

PCHCORE_IOUT → R5370 4.53K (1% 1/16W MF-LF 402) → ADC2_CH1 (OUT 102)

DEBUG_ADC → C5370 0.22UF (20% 6.3V X5R 402) PLACE_NEAR=UC210.23:10mm

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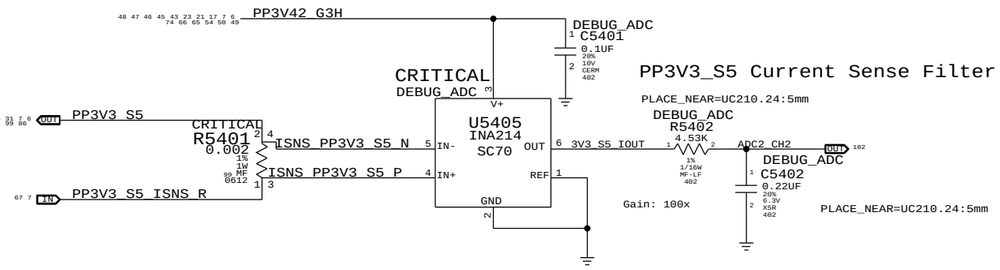
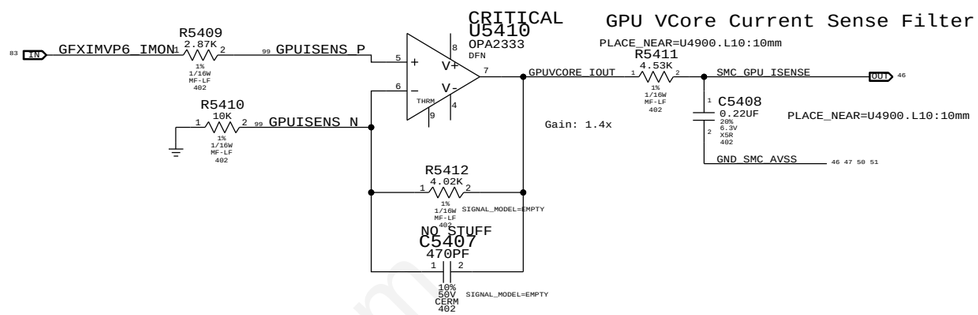
PP3V3_S5 Current Sense

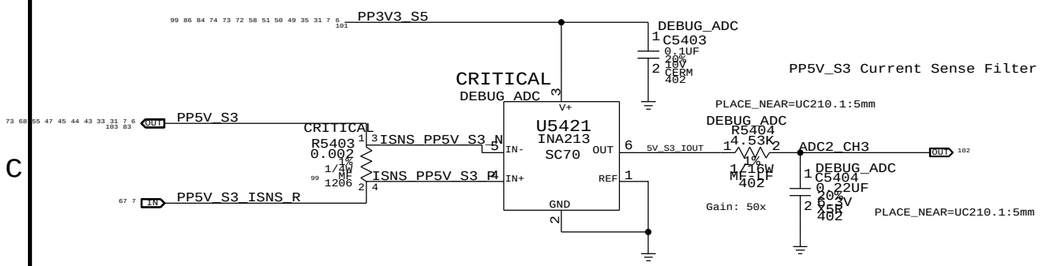


GPU VCore Current Sense

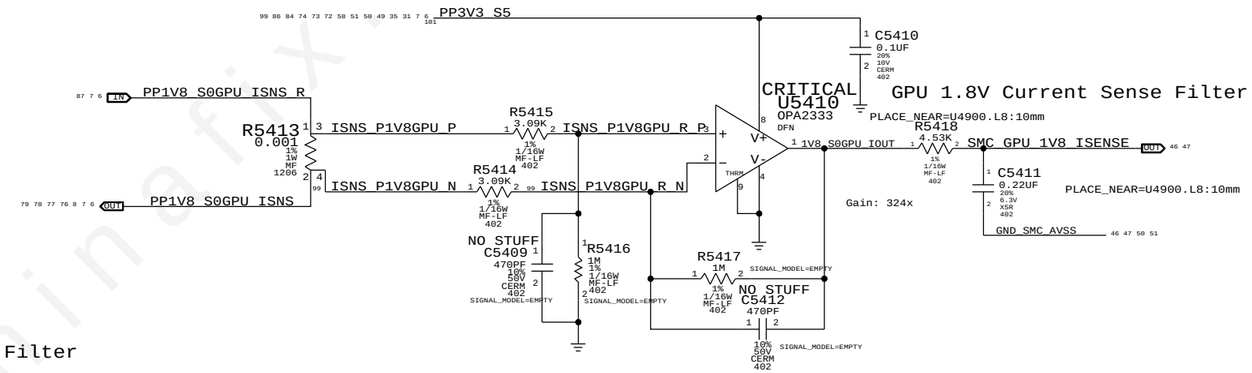


GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

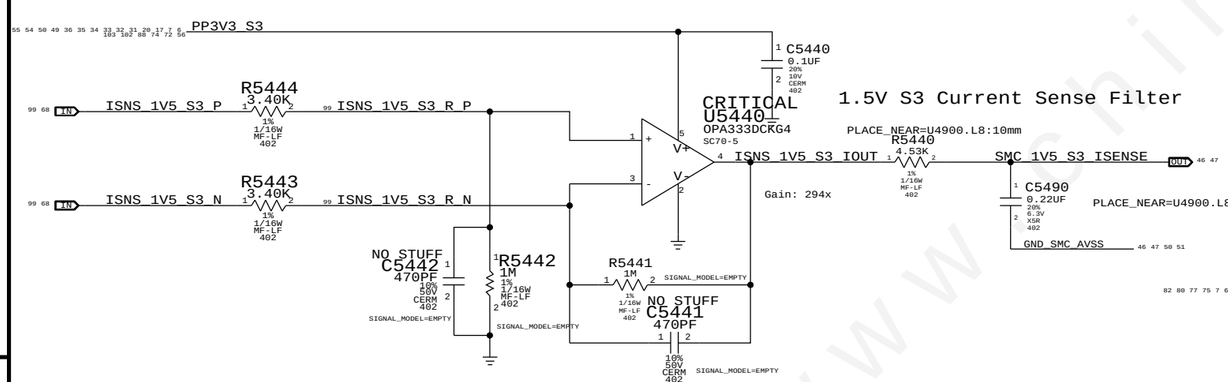
PP5V_S3 Current Sense



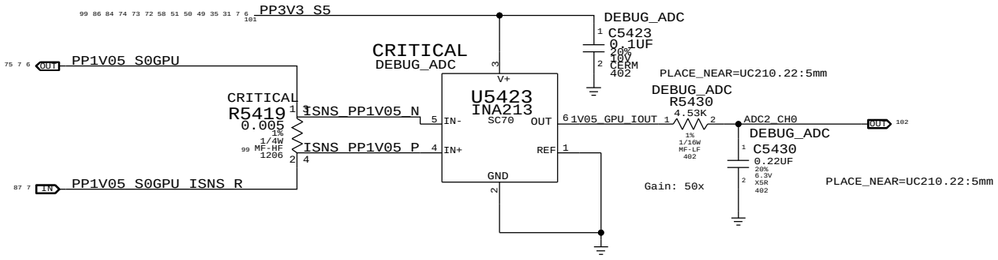
GPU 1.8V Current Sense



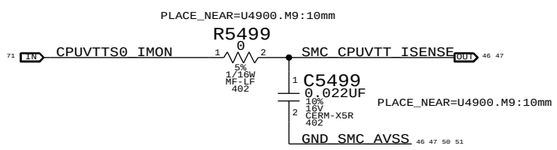
1.5V S3 Current Sense



GPU 1.05V Current Sense



CPUVTT 1.05V Current Sense



SYNC_MASTER=K17_CHENGD SYNC_DATE=06/04/2009

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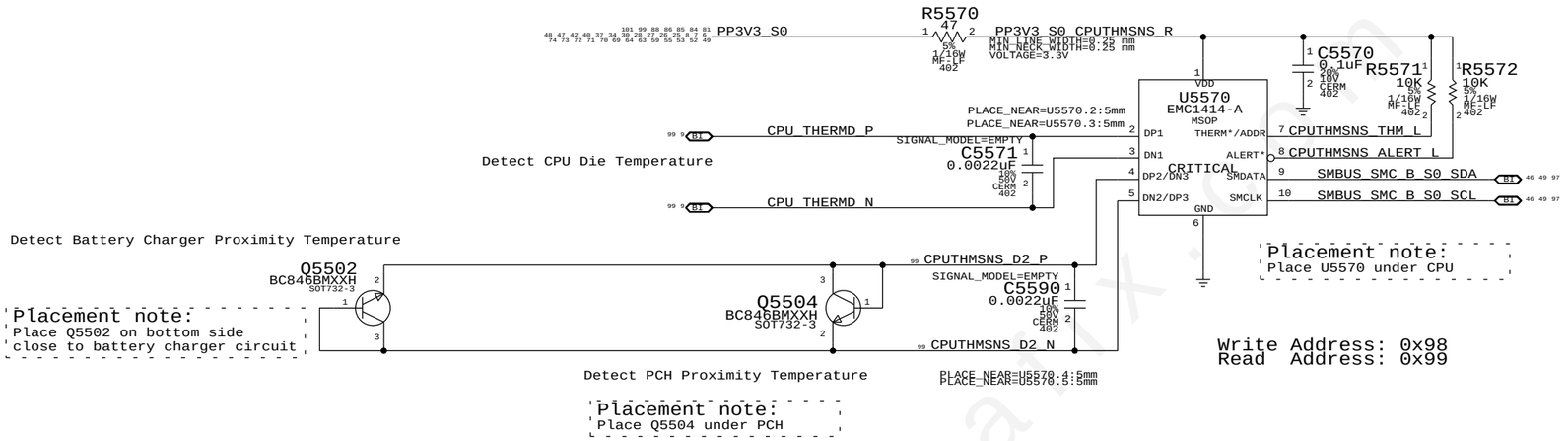
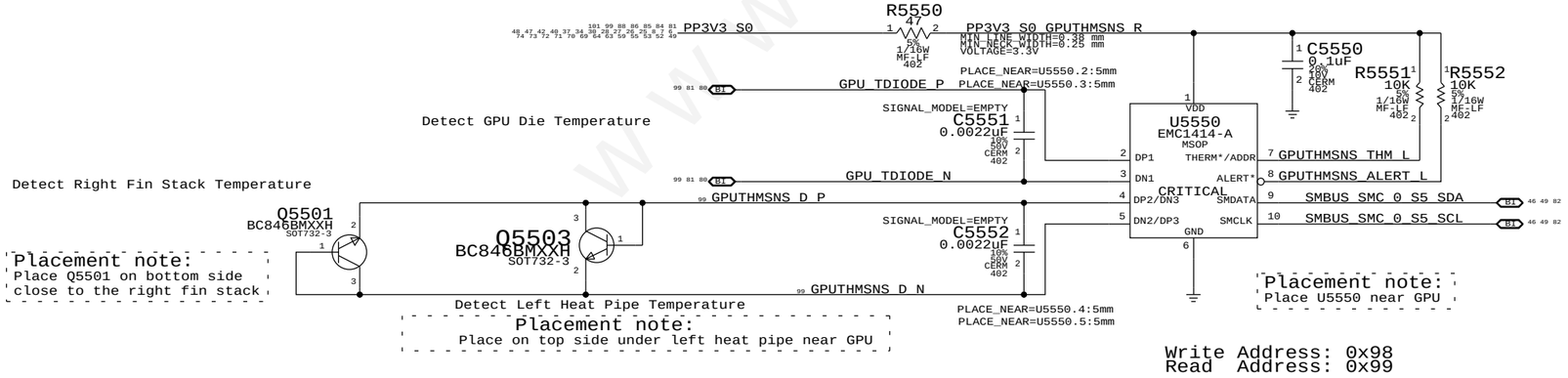
CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



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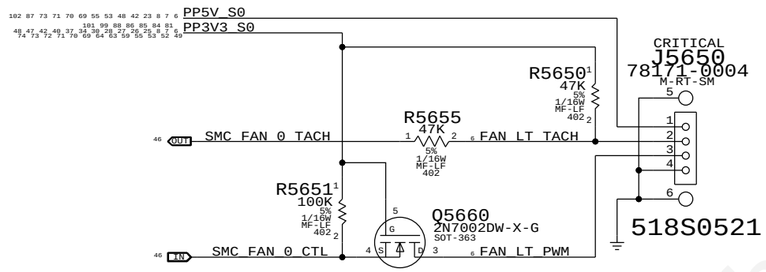
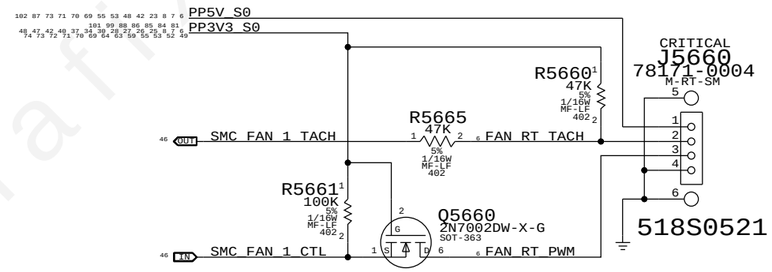
Left Fan



Right Fan



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Fan Connectors

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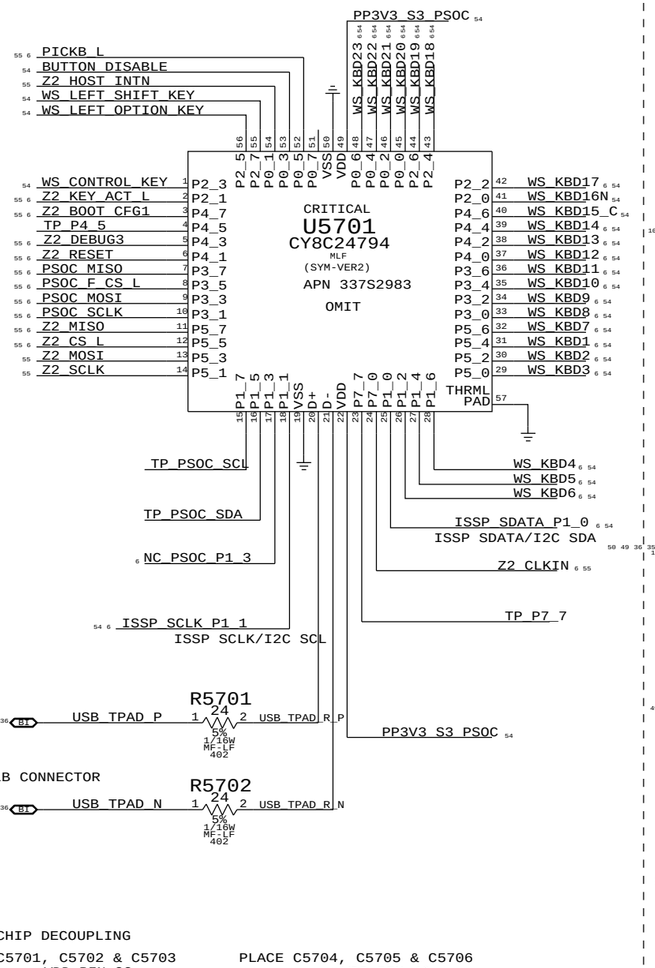
PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

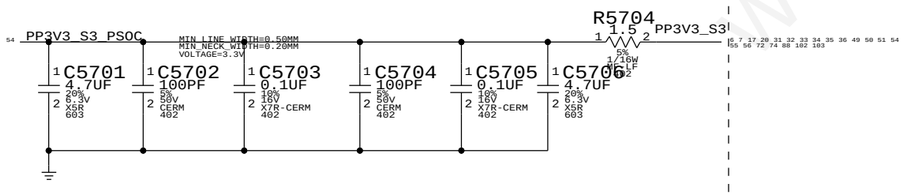
TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

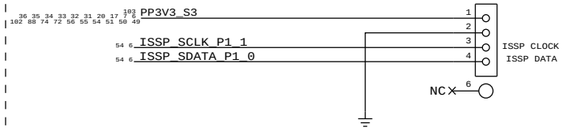


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

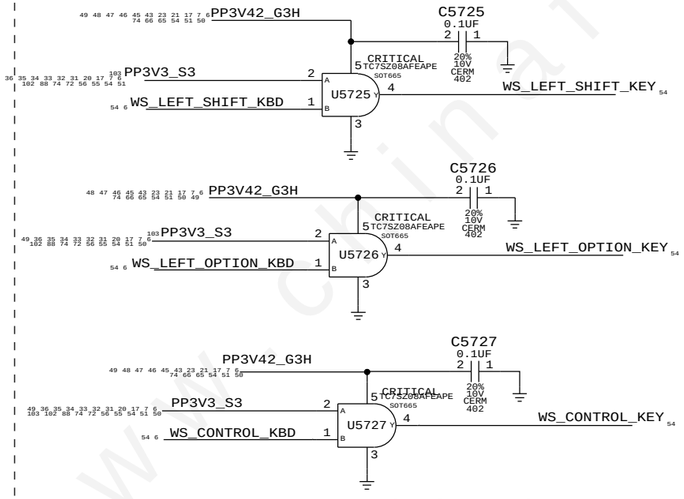
PSOC PROGRAMMING CONNECTOR

TEST POINTS ARE FOR ON BOARD PROGRAMMING

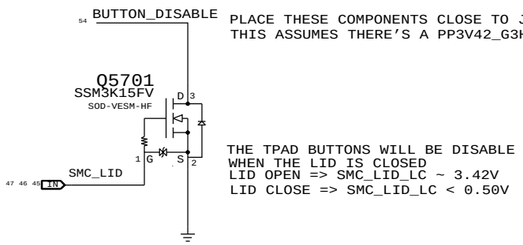
TPAD_DEBUG
CRITICAL
APN 518S0430
J5702
FH19C-4S-0.5SH25
F-RT-SM1



ISOLATION CIRCUIT



TPAD BUTTONS DISABLE

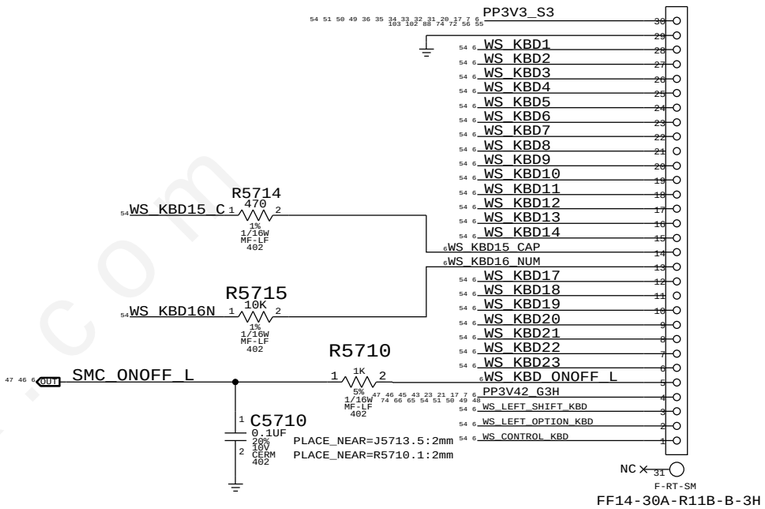


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

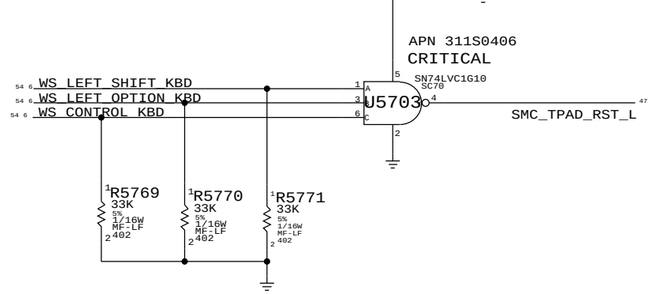
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR

CRITICAL
J5713
APN 518S0637

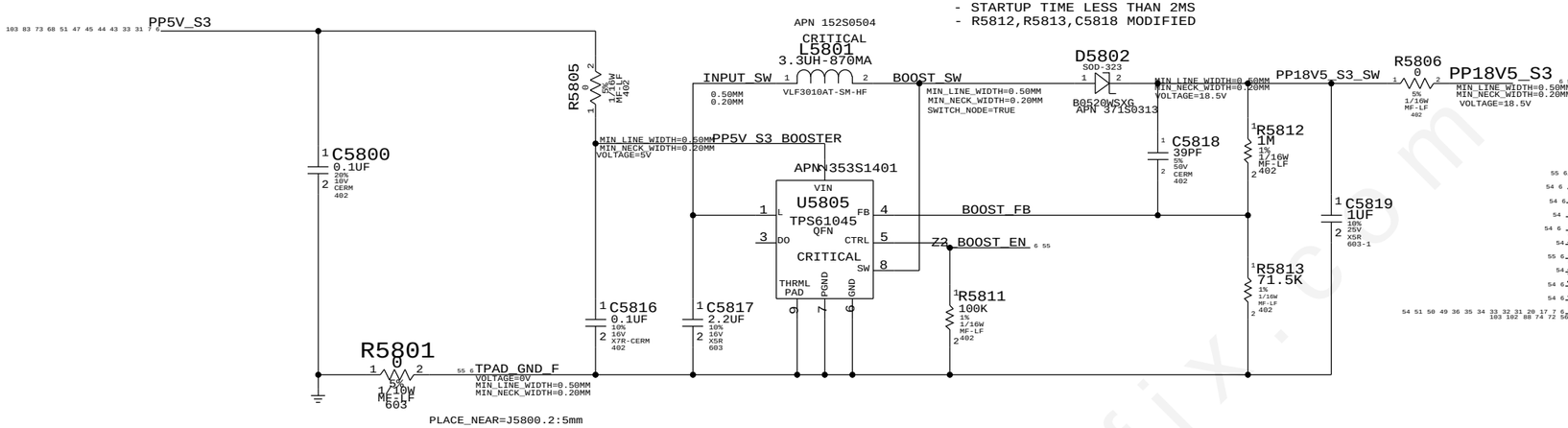


SMC_MANUAL_RESET LOGIC

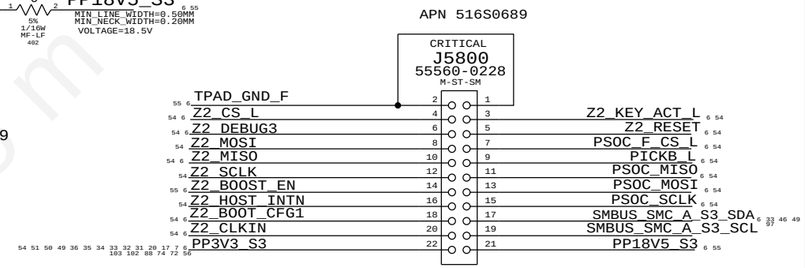


BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



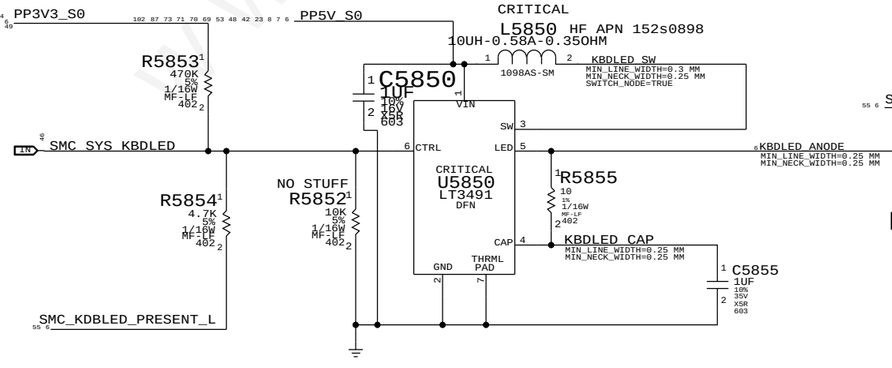
IPD FLEX CONNECTOR

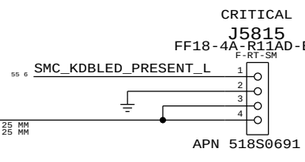


Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

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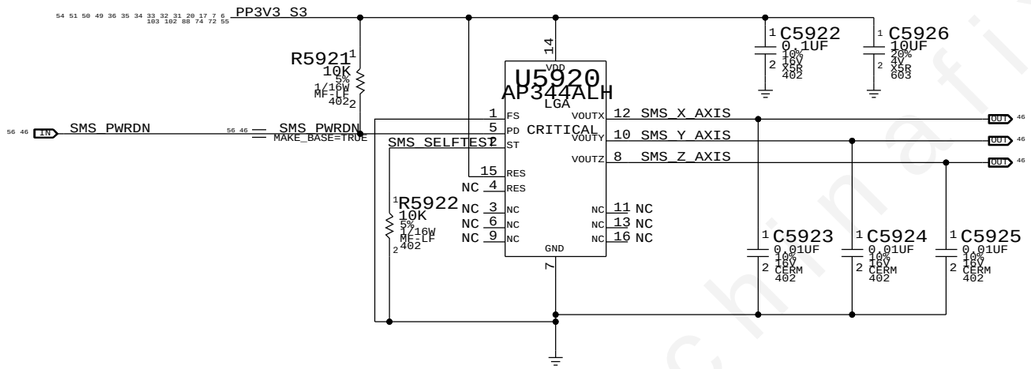
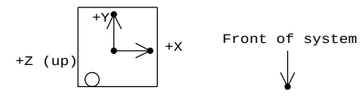
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE
Sudden Motion Sensor (SMS)

Apple Inc.

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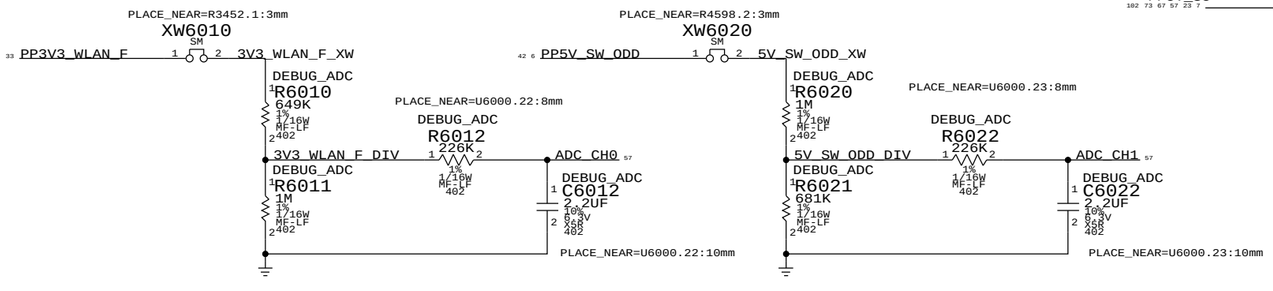

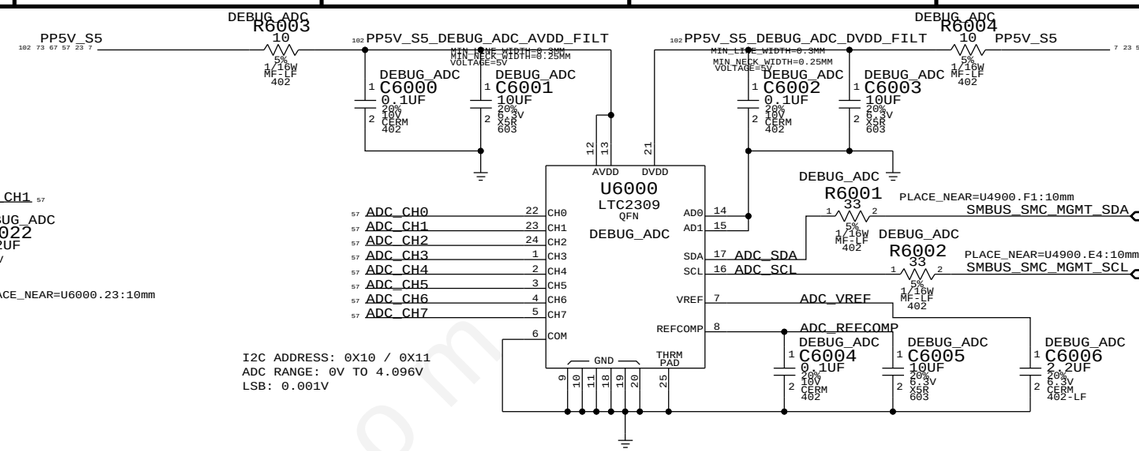

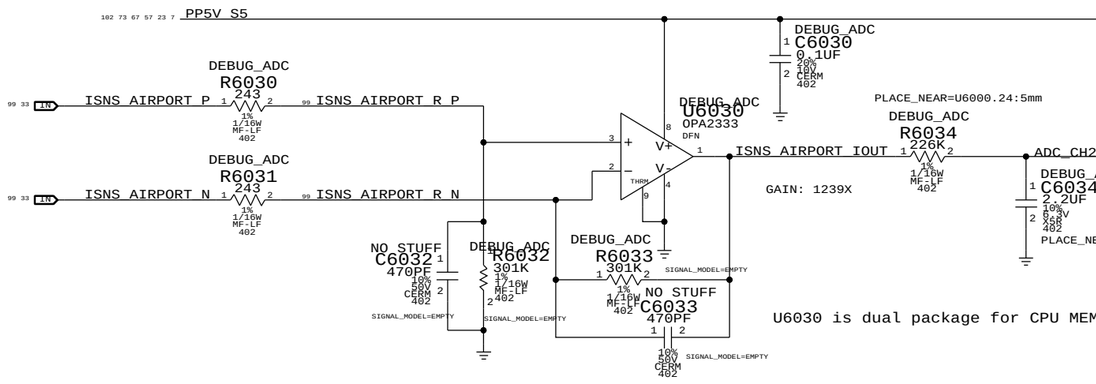

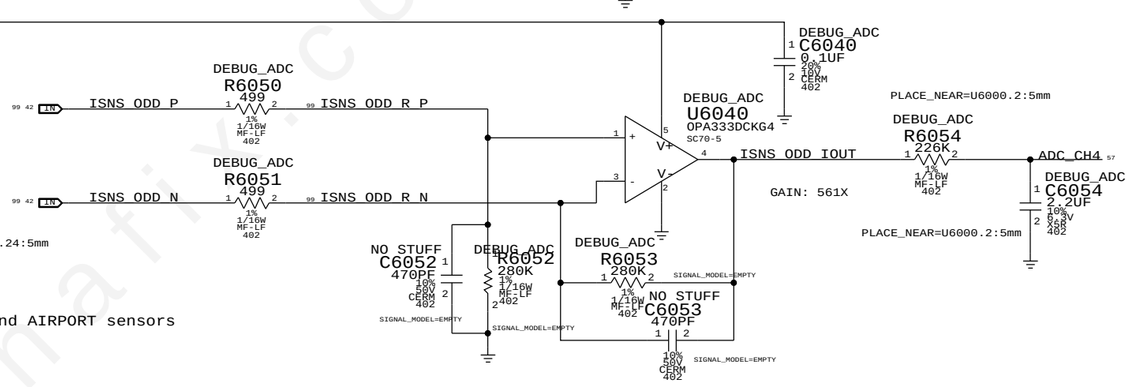

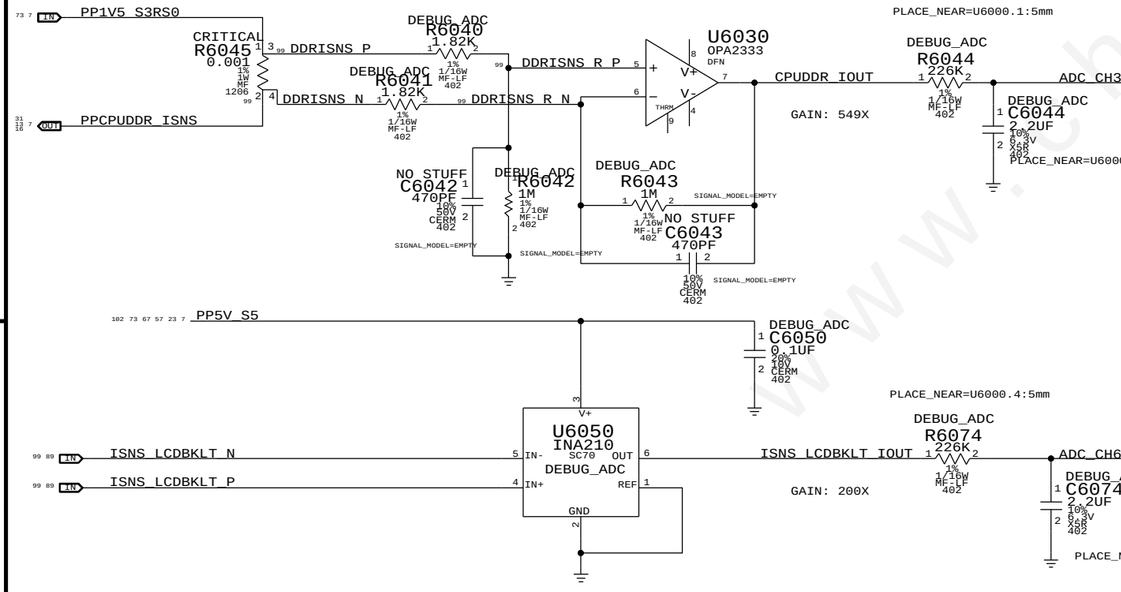

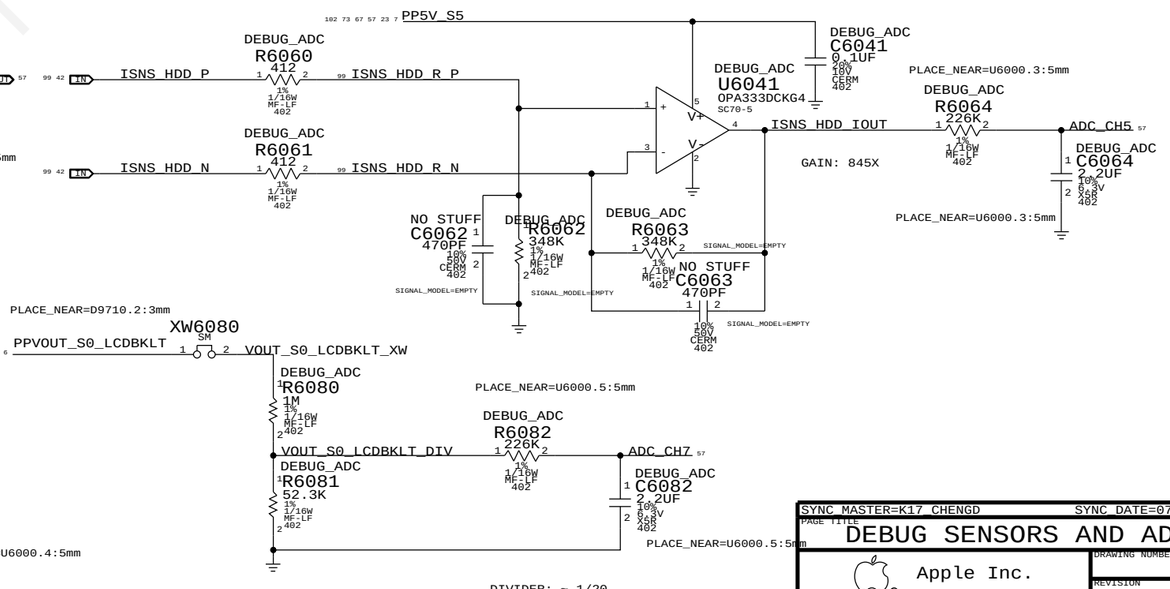

SYNC_MASTER=K17_CHENGD SYNC_DATE=07/08/2009

PAGE TITLE

DEBUG SENSORS AND ADC

Apple Inc.

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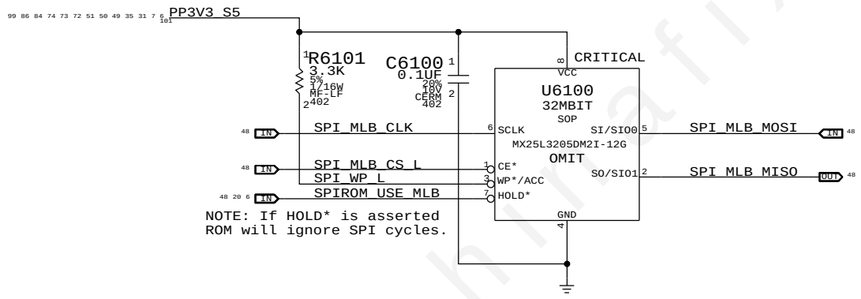

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

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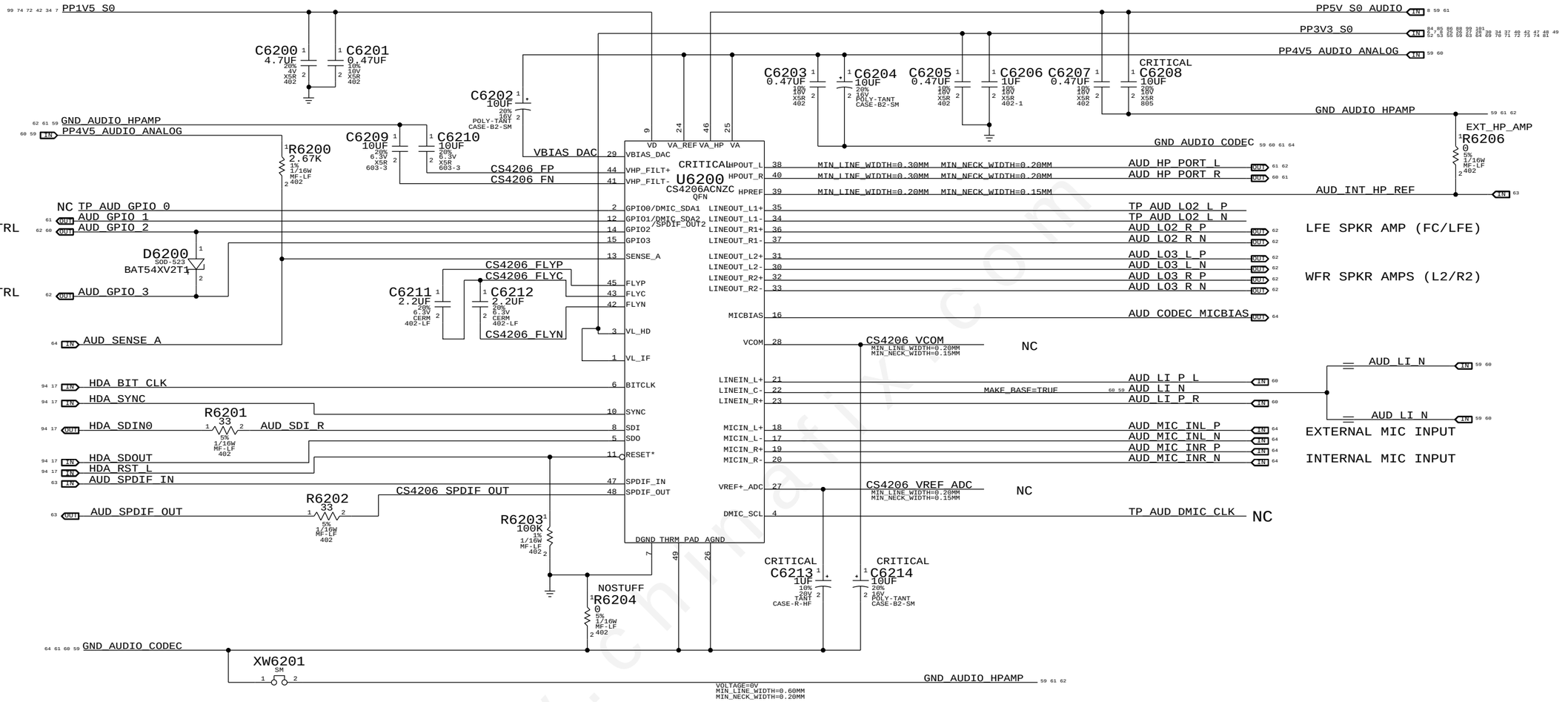
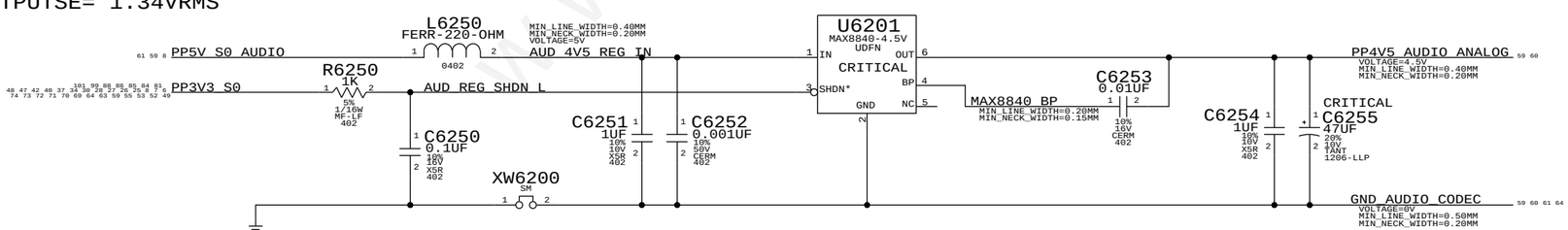
AUDIO CODEC
APPLE P/N 353S2592



DIFF_FSINPUT= 2.45VRMS
SE_FSINPUT= 1.22VRMS
DAC1_FSOUTPUT= 1.34VRMS
DAC2/3_FSOUTPUTDIFF= 2.67VRMS
DAC2/3_FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234



SYNC_MASTER=K17_REF	SYNC_DATE=05/30/2009
PAGE TITLE	AUDIO:CODEC
Apple Inc.	DRAWING NUMBER: SIZE: D
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	BRANCH:
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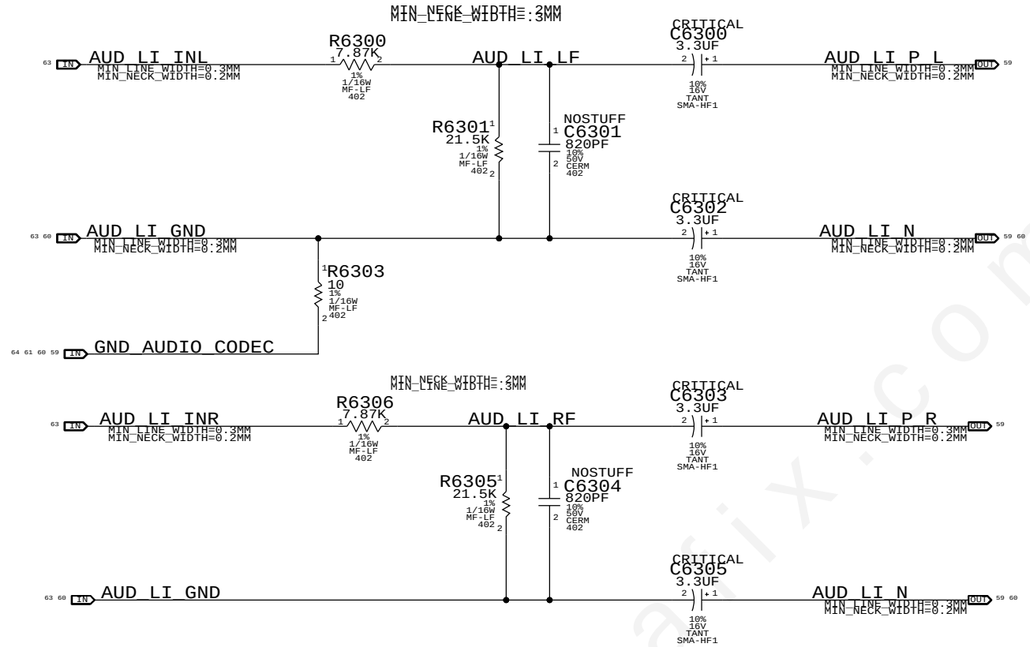
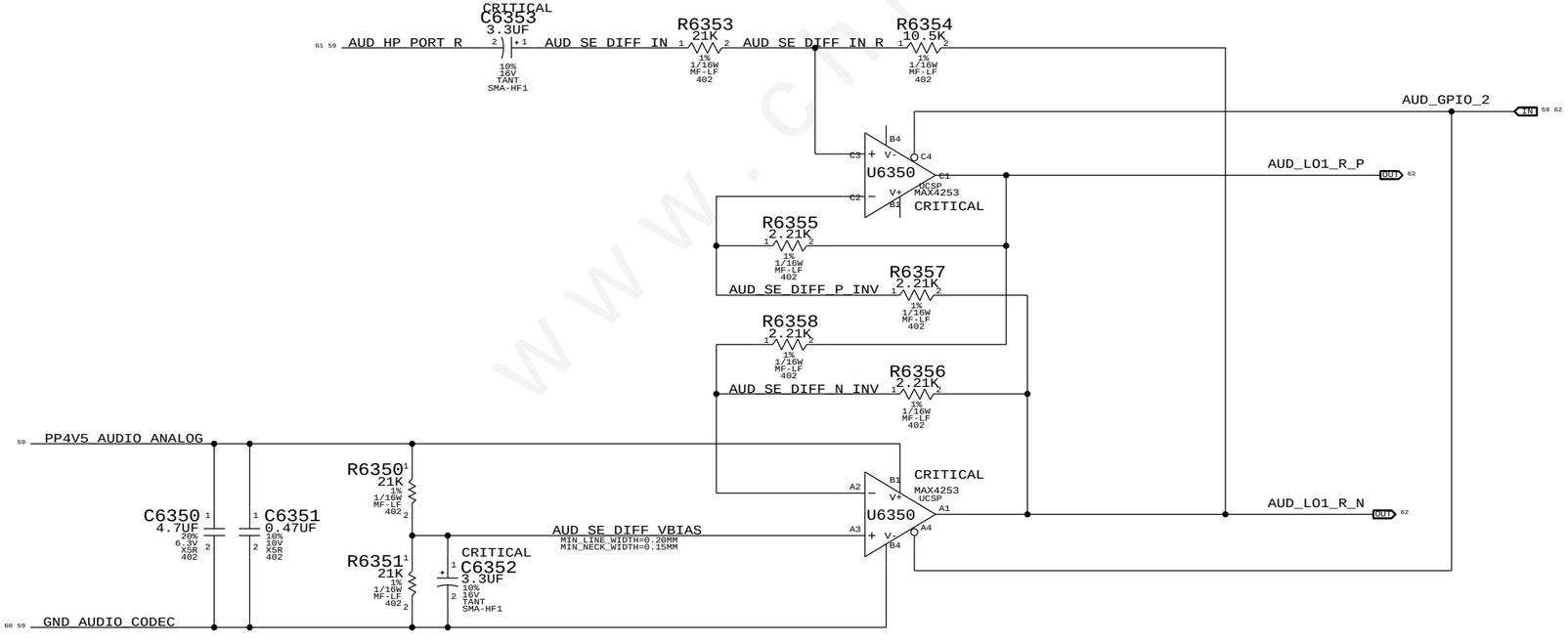
CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SE-TO-DIFF CONVERTER



SYNC_MASTER=K17_REF SYNC_DATE=05/30/2009

PAGE TITLE
AUDIO: LINE IN

Apple Inc.

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SIZE D
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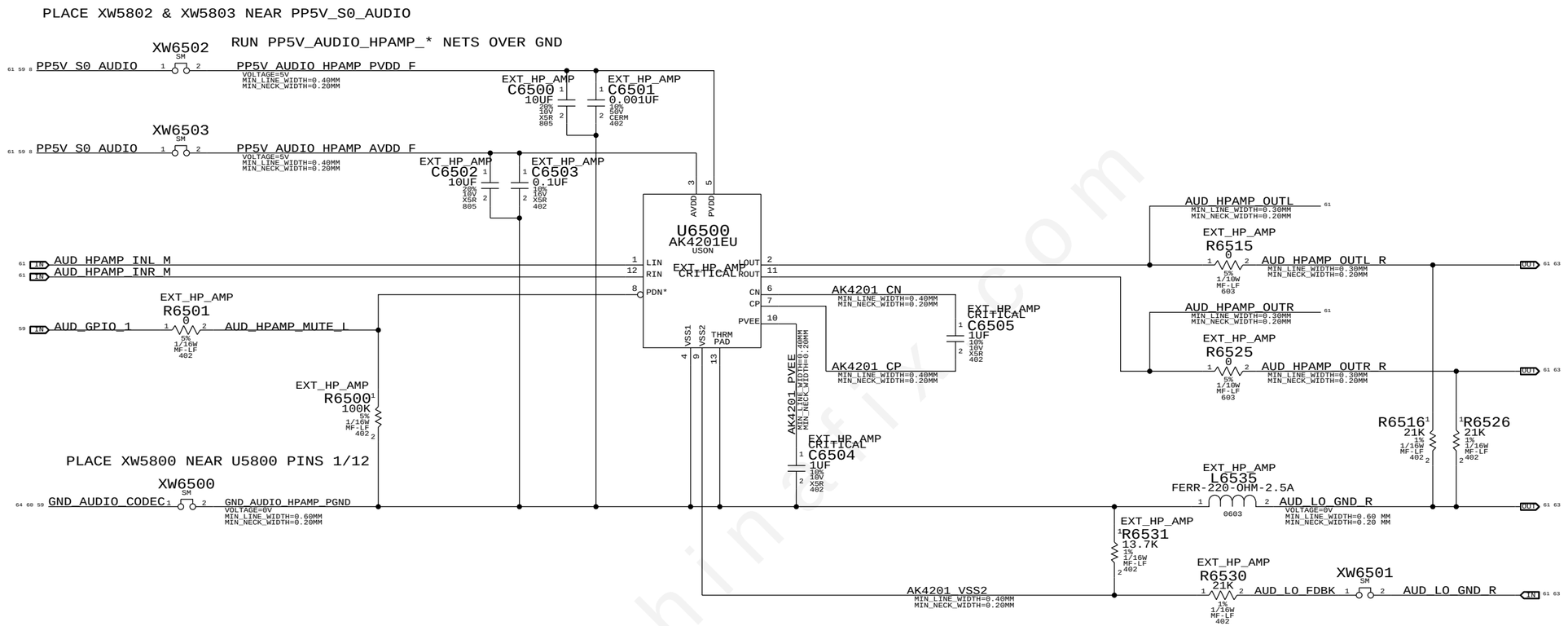
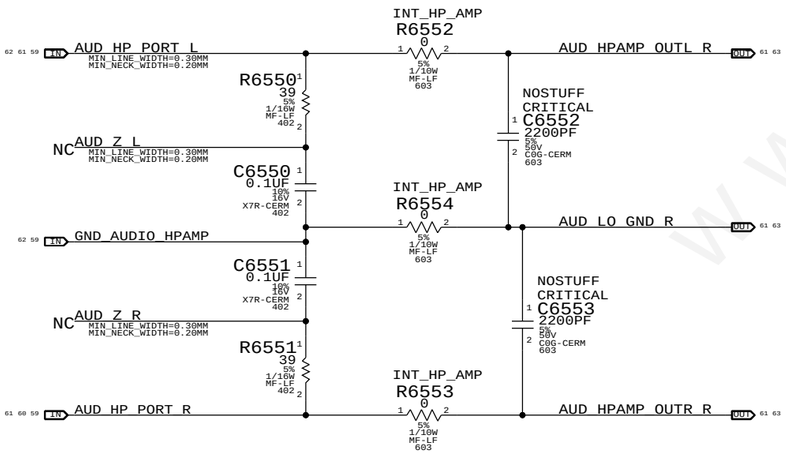
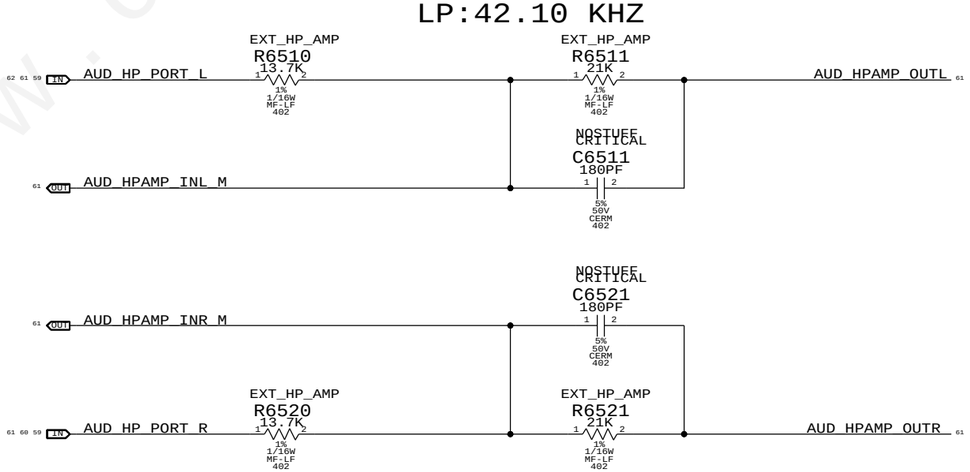
HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53



CS4206A HP OUT ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



1ST ORDER DAC FILTER LP:42.10 KHZ



SYNC_MASTER=K17_REF SYNC_DATE=05/30/2009

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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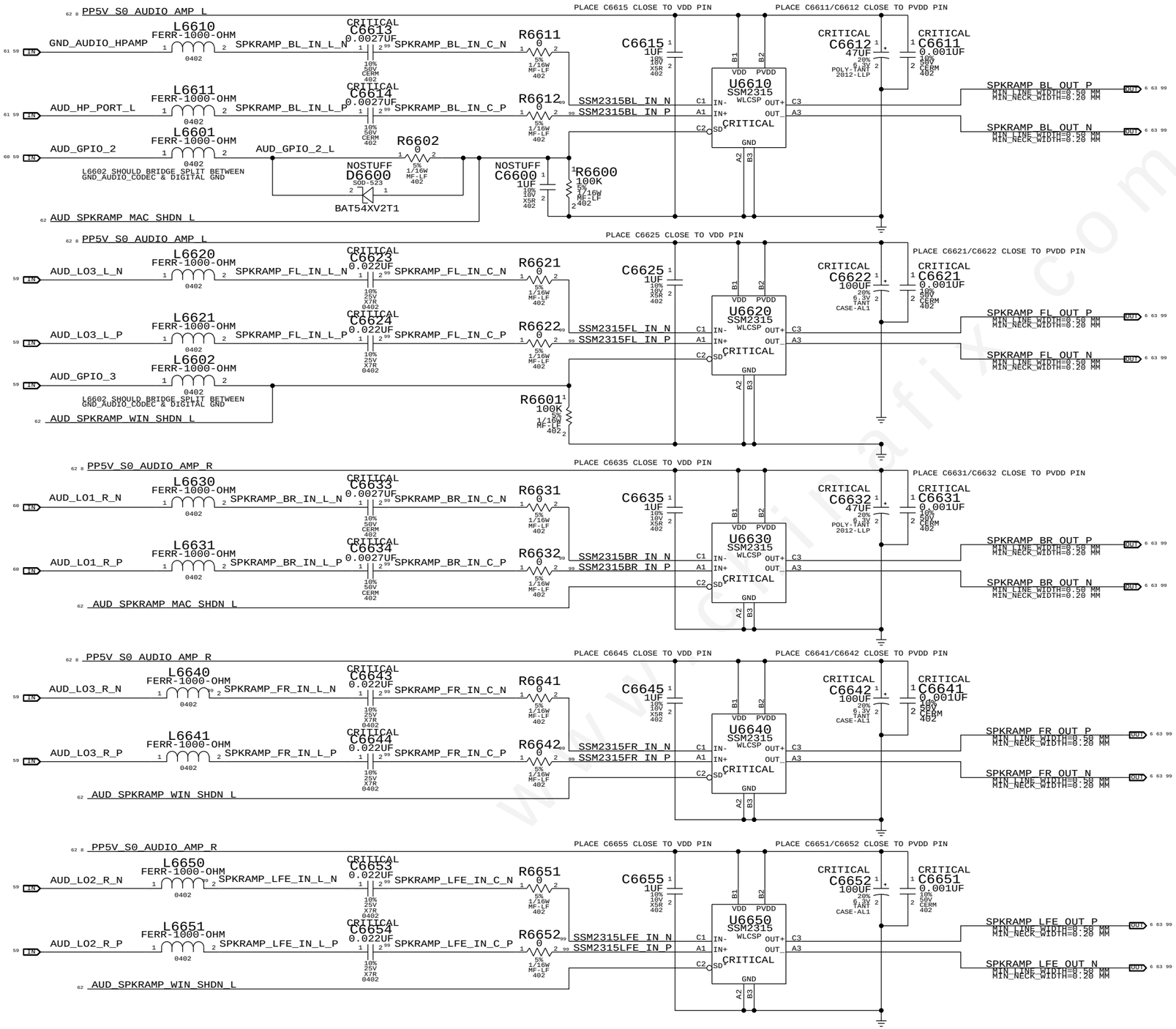
5X MONO SPEAKER AMPLIFIERS (SSM2315)

APN: 353S2500
GAIN = +6 DB

FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ



SYNC MASTER=K17 REF SYNC DATE=05/30/2009

PAGE TITLE

AUDIO:SPEAKER AMP

Apple Inc.

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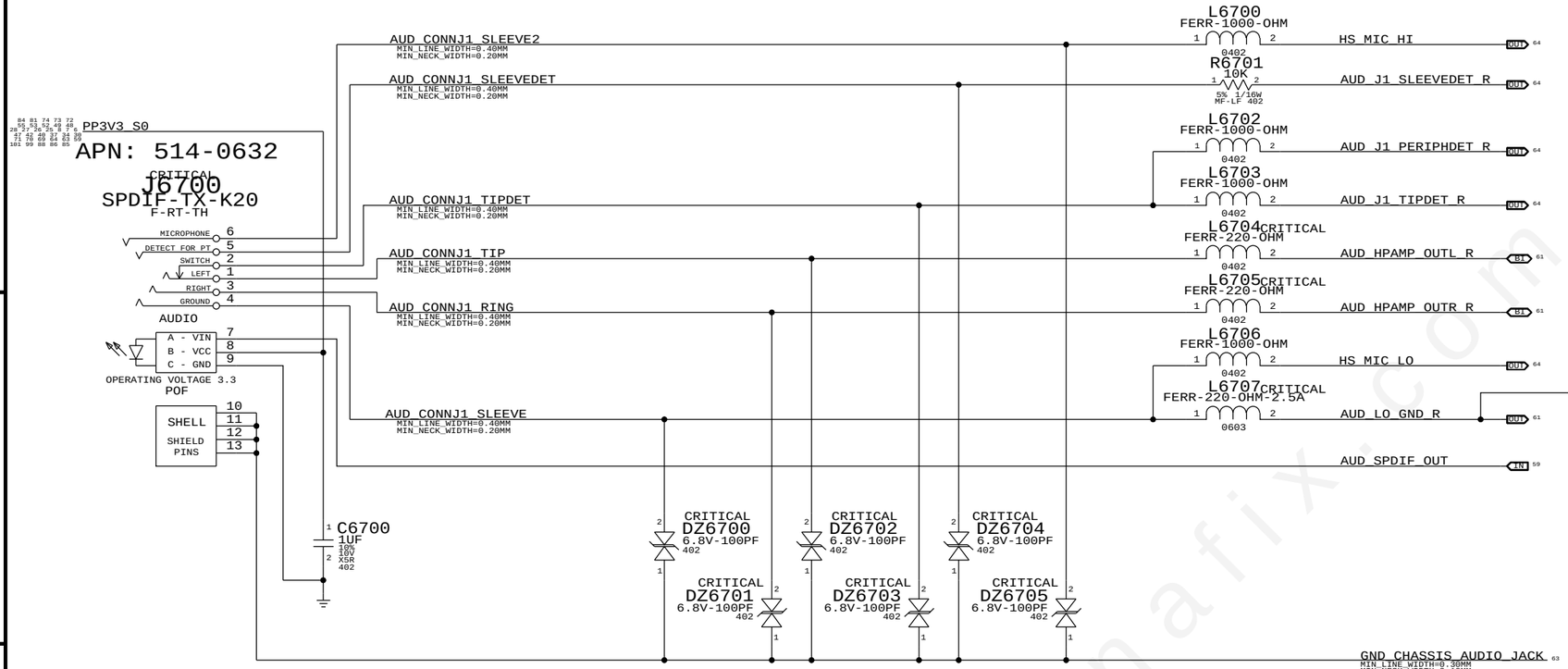
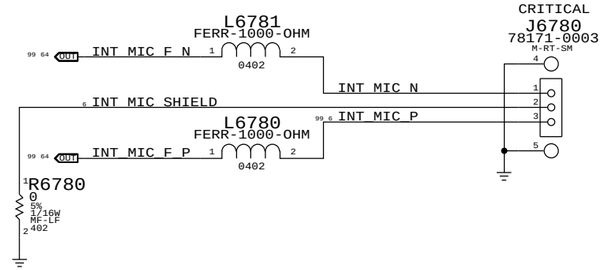
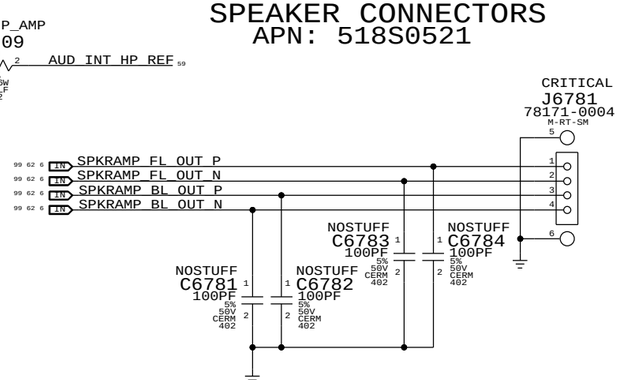
AUDIO JACK 1 LO/HP JACK, SPDIF TX



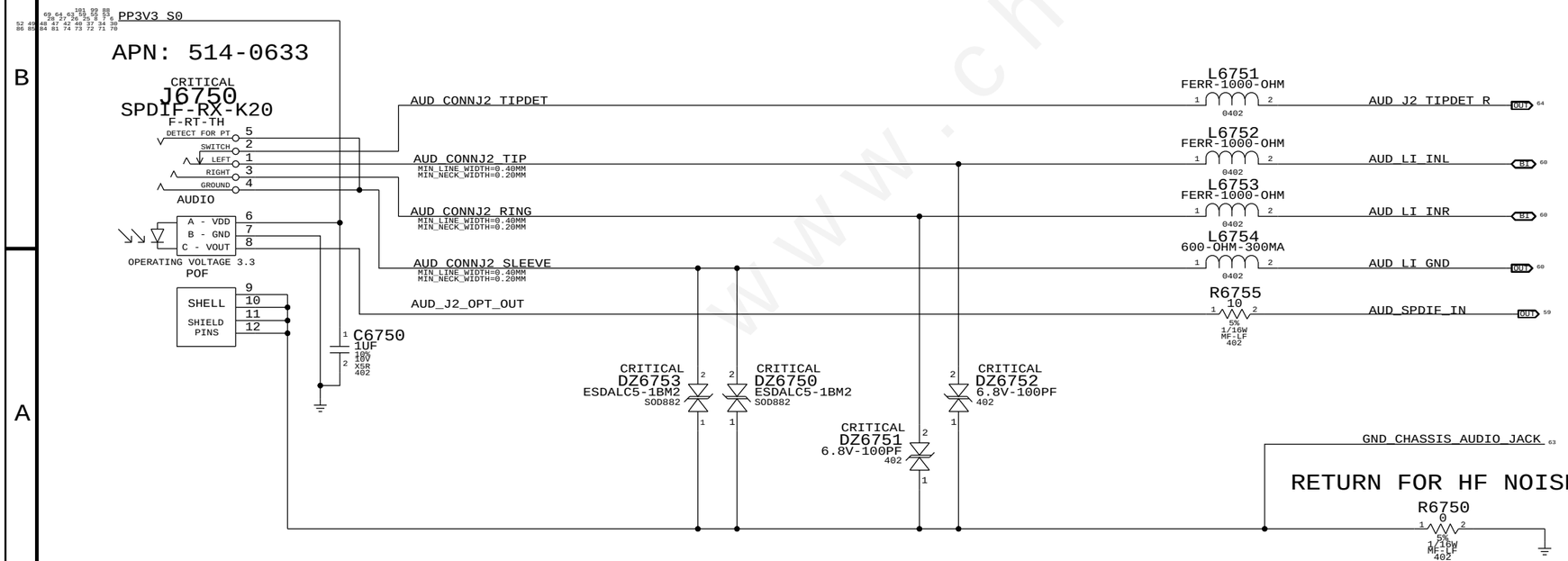
MIC CONNECTOR
APN: 518S0520



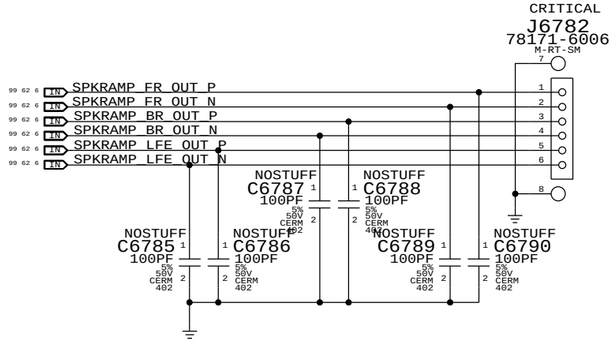
SPEAKER CONNECTORS
APN: 518S0521



AUDIO JACK 2 LINE IN JACK, SPDIF RX



APN: 518S0672



SYNC_MASTER=K17_LENGO SYNC_DATE=11/24/2009

PAGE TITLE: AUDIO: JACKS

Apple Inc.

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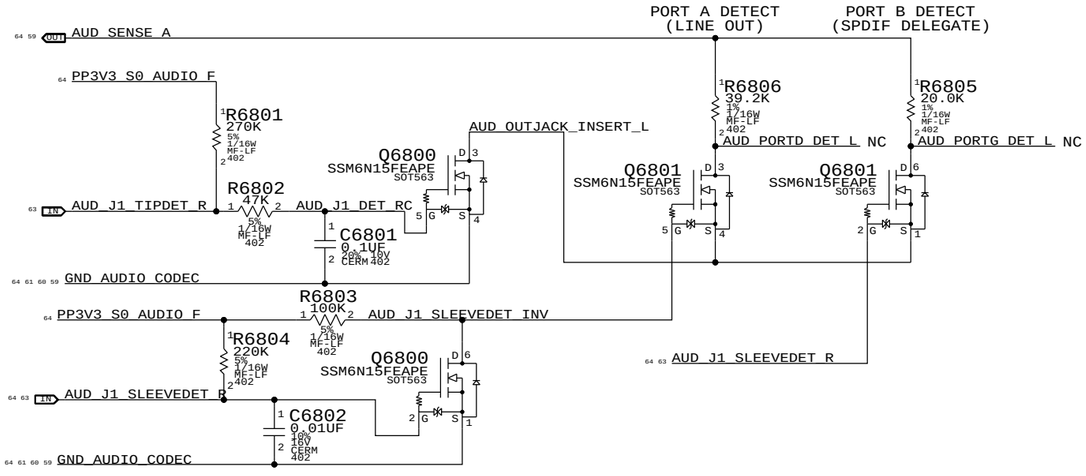
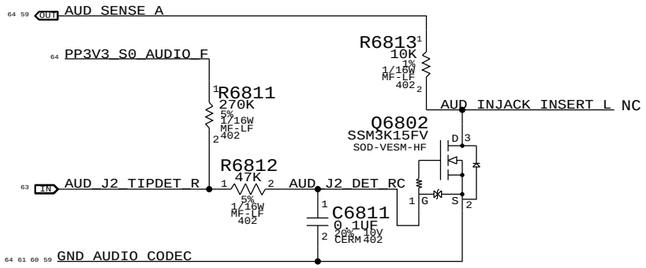
CODEC OUTPUT SIGNAL PATHS

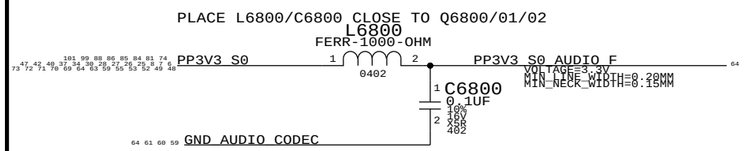
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (B)

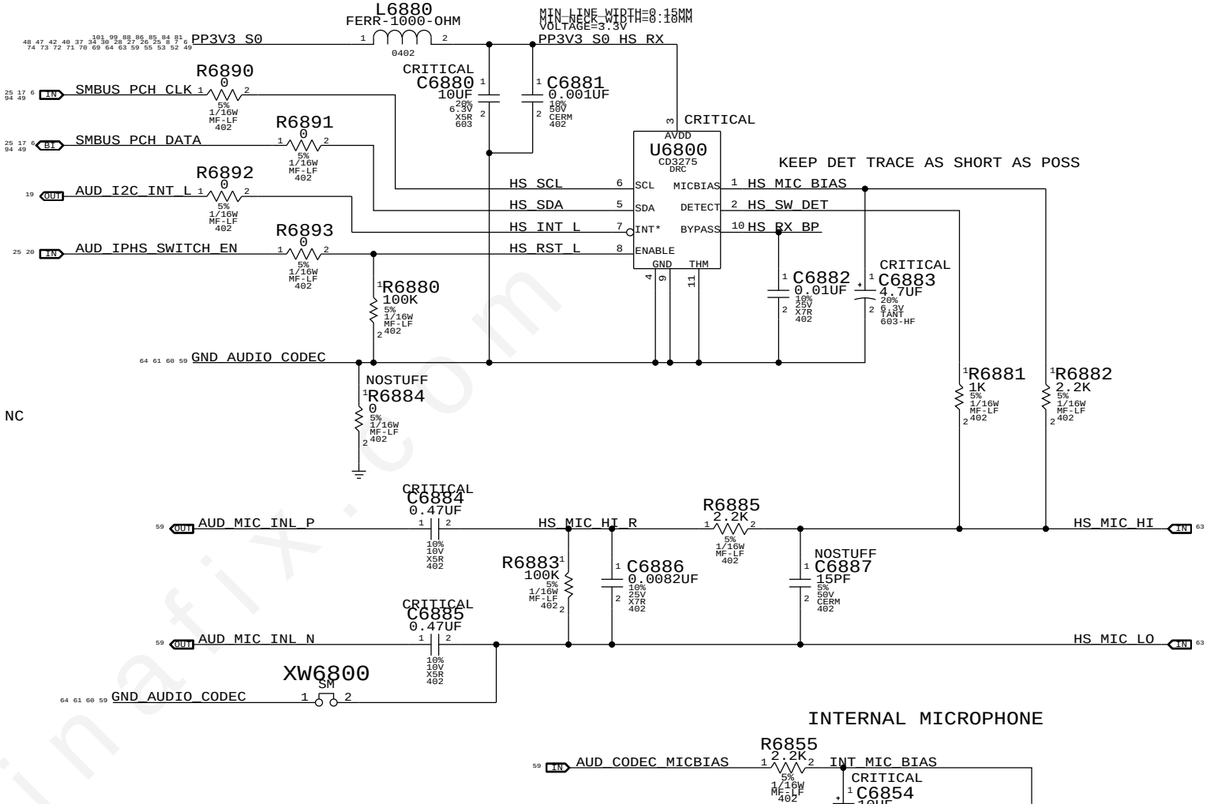
CODEC INPUT SIGNAL PATHS

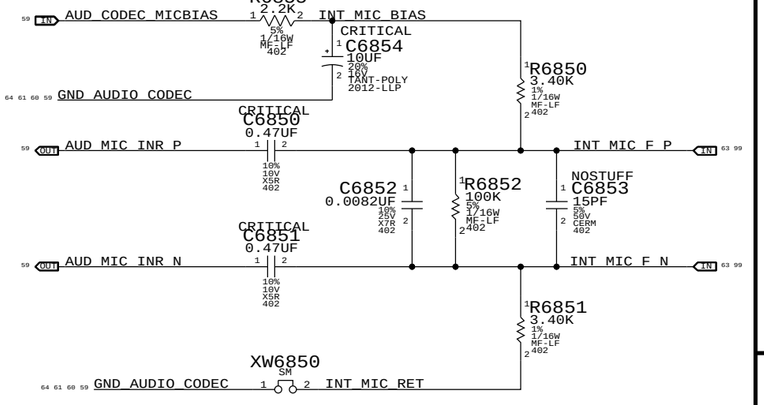
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

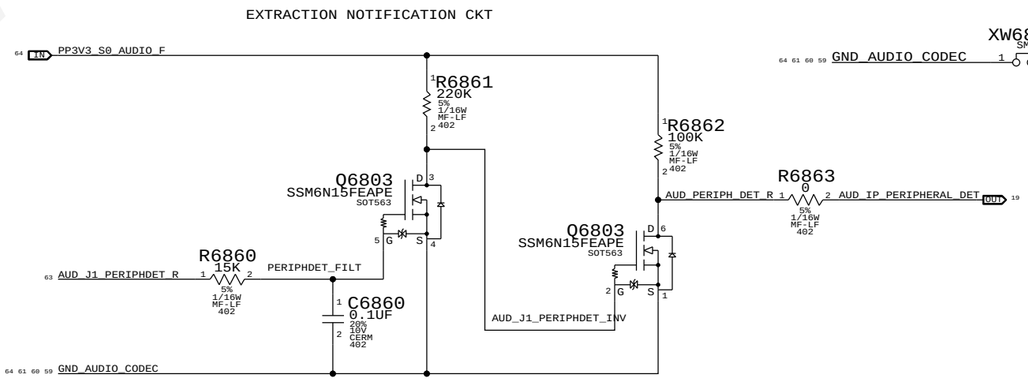












SYNC_MASTER=K17_REF SYNC_DATE=05/30/2009

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

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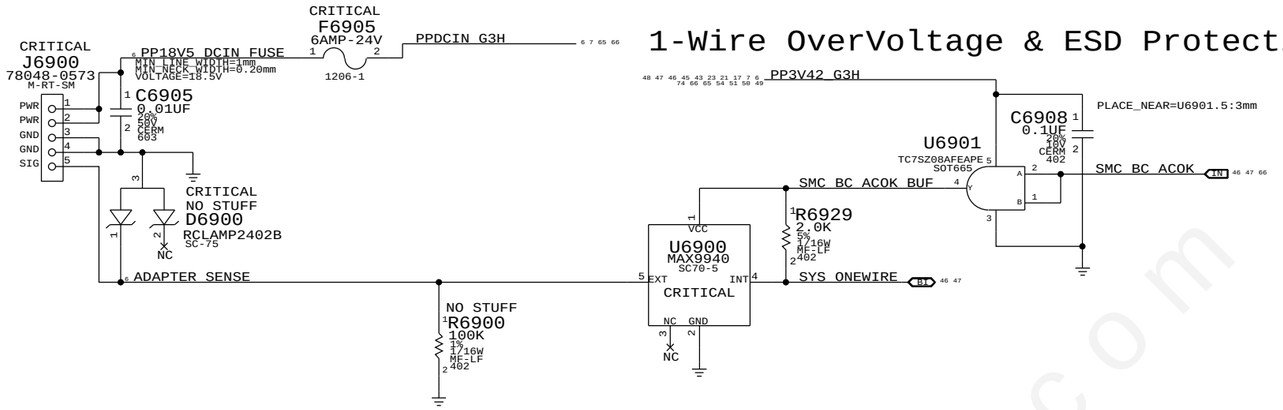
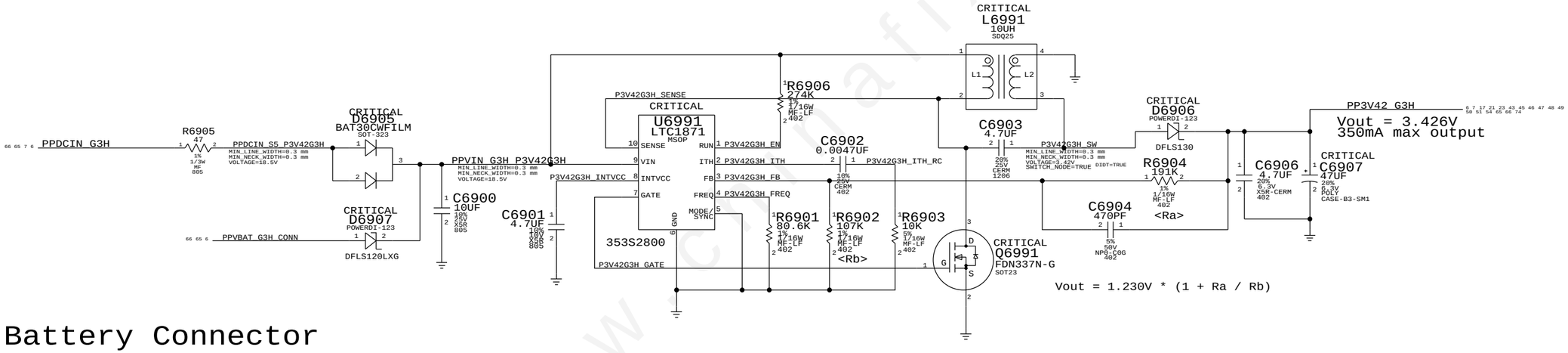
MagSafe DC Power Jack



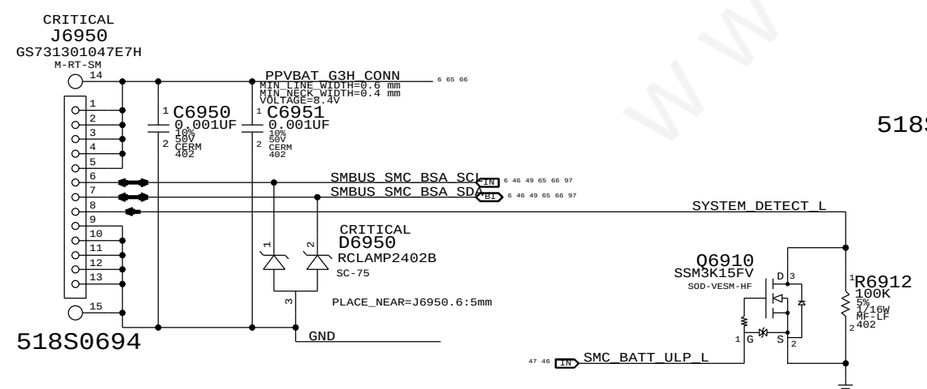
1-Wire OverVoltage & ESD Protection

3.425V "G3Hot" Supply

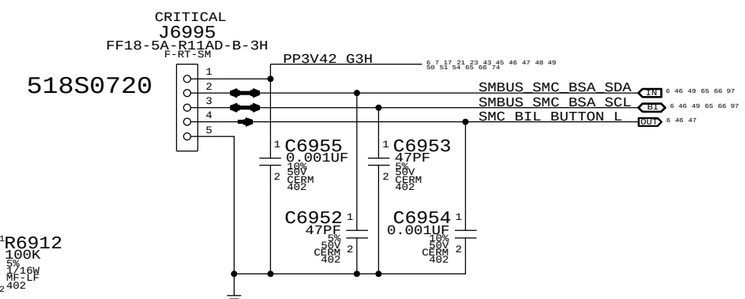
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Battery Connector



BIL Connector



SYNC_MASTER=K17_REF SYNC_DATE=04/29/2009

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

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Reverse-Current Protection

Inrush Limiter

FROM ADAPTER

PPDCIN_G3H

CRITICAL Q7080 HAT1128R01 SOI

CRITICAL Q7085 HAT1128R01 SOI

PPDCIN_G3H_OR_PBUS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

R7080 100K 5% 1/16W MF-LF 402

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7081 62K 1% 1/16W MF-LF 402

R7086 332K 1% 1/16W MF-LF 402

CRITICAL D7005 BAT30CWFILM SOT-323

R7003 20 5% 1/16W MF-LF 402 CHGR_DCIN_R

(CHGR_SGATE)

(CHGR_AGATE)

(CHGR_DCIN)

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.55V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

PP3V42_G3H

R7010 30.1K 1% 1/16W MF-LF 402

NO STUFF R7002 100K 5% 1/16W MF-LF 402

R7000 0 5% 1/16W MF-LF 402

SMC_RESET_L

CHGR_RST_L
SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA
CHGR_VFRQ
CHGR_CELL

Float CELL for 1S

CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N

U7000 ISL6259HRTZ TQFN

12	VHST	DCIN	2
13	SMB_RST_N	SGATE	26
11	SCL	AGATE	1
10	SDA	CSIP	28
4	VFRQ	CSIN	27
6	CELL	BOOT	25
3	ACIN	UGATE	24
5	ICOMP	PHASE	23
7	VCOMP	LGATE	21
8	VNEG	BGATE	16
18	CSOP	20V/V AMON	9
17	CSON	36V/V BMON	15
		(OD) ACOK	14
29	(AGND) THRM_PAD	PGND	22

CHGR_DCIN
CHGR_SGATE
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE DIDT=TRUE
CHGR_PHASE GATE_NODE=TRUE DIDT=TRUE
CHGR_LGATE GATE_NODE=TRUE DIDT=TRUE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
SMC_BC_ACOK

353S2392

R7011 9.31K 1% 1/16W MF-LF 402

R7013 100 1% 1/16W MF-LF 402

R7015 220K 5% 1/16W MF-LF 402

C7050 1UF 10% 16V X5R 402

CHGR_VCOMP_R

C7015 470PF 10% 50V CERM 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V CERM 402

XW7000 SM

(GND)

PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

C7042 0.068UF 10% 10V CERM 402

C7002 1UF 10% 10V X5R 402

C7011 0.01UF 10% 16V CERM 402

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 20% 25V CERM 805

C7026 0.001UF 10% 50V CERM 402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

R7021 10 5% 1/10W MF-LF 402

R7022 10 5% 1/10W MF-LF 402

CHGR_CSI_R_P

CHGR_CSI_R_N

CRITICAL R7020 0.020 0.5% 1W MF-LF 0612

C7020 0.047UF 10% 10V CERM 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7032 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7033 22UF 20% 25V POLY-TANT CASE-D2-SM

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

CRITICAL Q7031 RJK0305DPB LFPAK-HF

CRITICAL Q7030 RJK0305DPB LFPAK-HF

C7025 0.22UF 10% 10V CERM 402

Max Current = 15A
(L7030/L7031 limit)
f = 400 kHz

CRITICAL L7030 2.2UH-20A-5.5M-OHM SM

CRITICAL L7031 2.2UH-20A-5.5M-OHM SM

CHGR_PHASE_MID
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

CRITICAL F7040 8AMP-24V 1206

CRITICAL F7041 8AMP-24V 1206

TO SYSTEM

PPBUS_G3H

NO STUFF R7039 10 5% 1/10W MF-LF 603

CRITICAL Q7036 RJK0305DPB LFPAK-HF

CRITICAL Q7035 RJK0305DPB LFPAK-HF

CHGR_PHASE_RC DIDT=TRUE

NO STUFF C7039 0.001UF 10% 50V X7R 402

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

CRITICAL C7040 33UF 20% 16V POLY-TANT CASED2E-SM

CRITICAL C7041 33UF 20% 16V POLY-TANT CASED2E-SM

C7045 0.001UF 10% 50V X7R 402

TO/FROM BATTERY

PPVBAT_G3H_CONN

CRITICAL R7050 0.005 1% 1W MF 0612

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

CRITICAL Q7055 SI7137DP SO-8

CRITICAL Q7056 SI7137DP SO-8

PPVBAT_G3H_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

C7055 1UF 10% 25V X5R 603-1

C7056 0.1UF 10% 16V X5R 402

C7057 0.01UF 10% 16V CERM 402

C7058 1UF 10% 16V X5R 402

R7058 1M 1% 1/16W MF-LF 402

BATT_POS_GATE

R7059 20K 5% 1/16W MF-LF 402

GND

R7051 2.2 5% 1/16W MF-LF 402 CHGR_CSO_R_P

R7052 0 5% 1/16W MF-LF 402 CHGR_CSO_R_N

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

R7092 1K 5% 1/16W MF-LF 402 CHGR_BGATE_R

R7093 220K 5% 1/16W MF-LF 402 CHGR_OVP_G_C

PLACE_NEAR=Q7055.4:1mm

CRITICAL SOT-363 ASMCC0178 U7090

CHGR_OVP_A

R7094 1K 5% 1/16W MF-LF 402 CHGR_OVP_B

C7090 100PF 5% 50V CERM 402

R7090 20K 5% 1/16W MF-LF 402

PLACE_NEAR=U7090.5:1mm

SYNC_MASTER=K17_REF SYNC_DATE=04/29/2009

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

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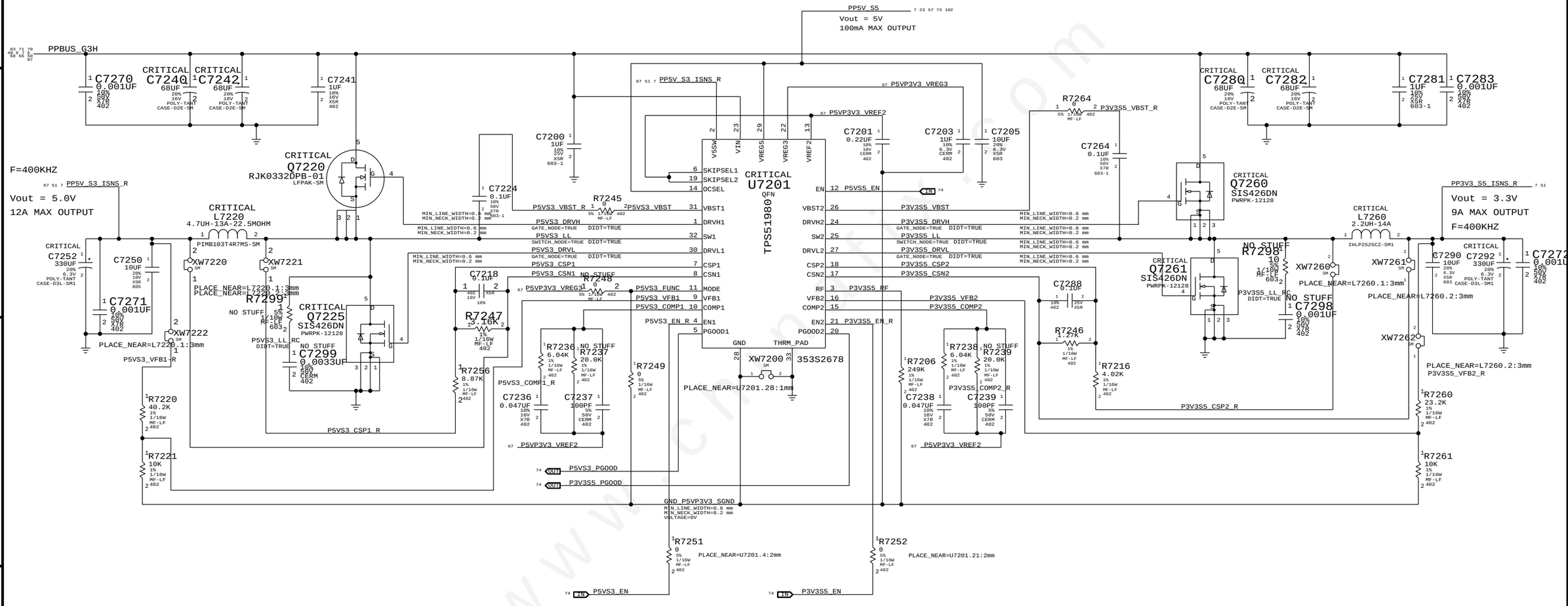

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER — SIZE D

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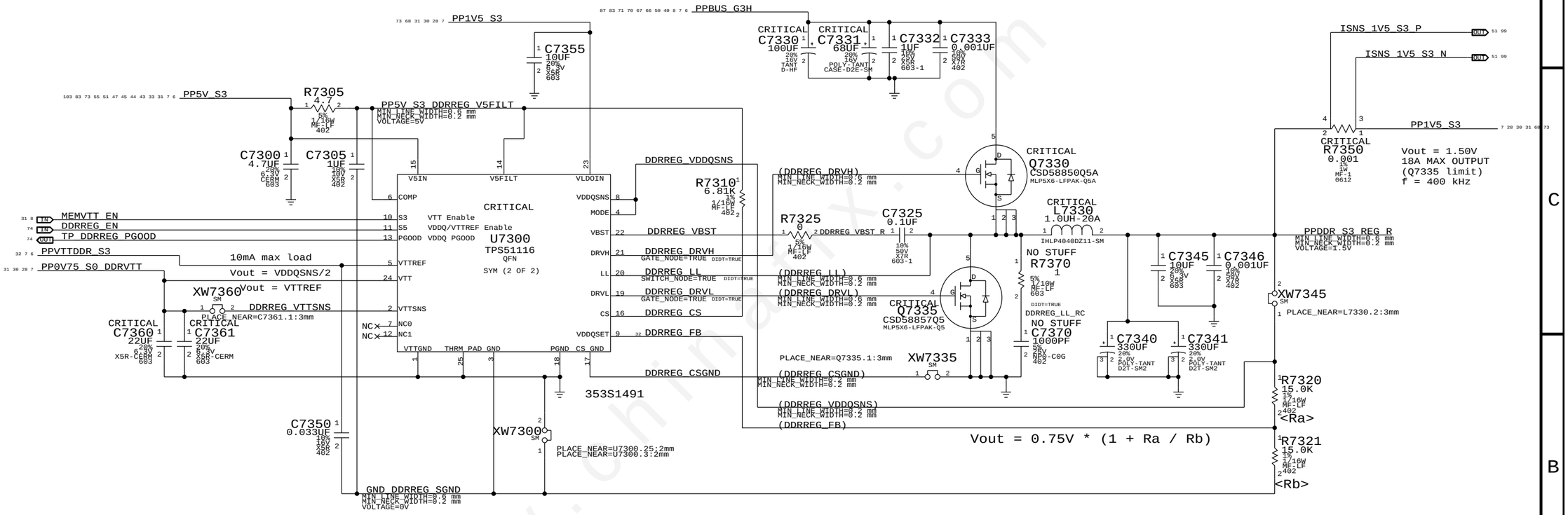

SYNC_MASTER=K17_REF SYNC_DATE=06/24/2009

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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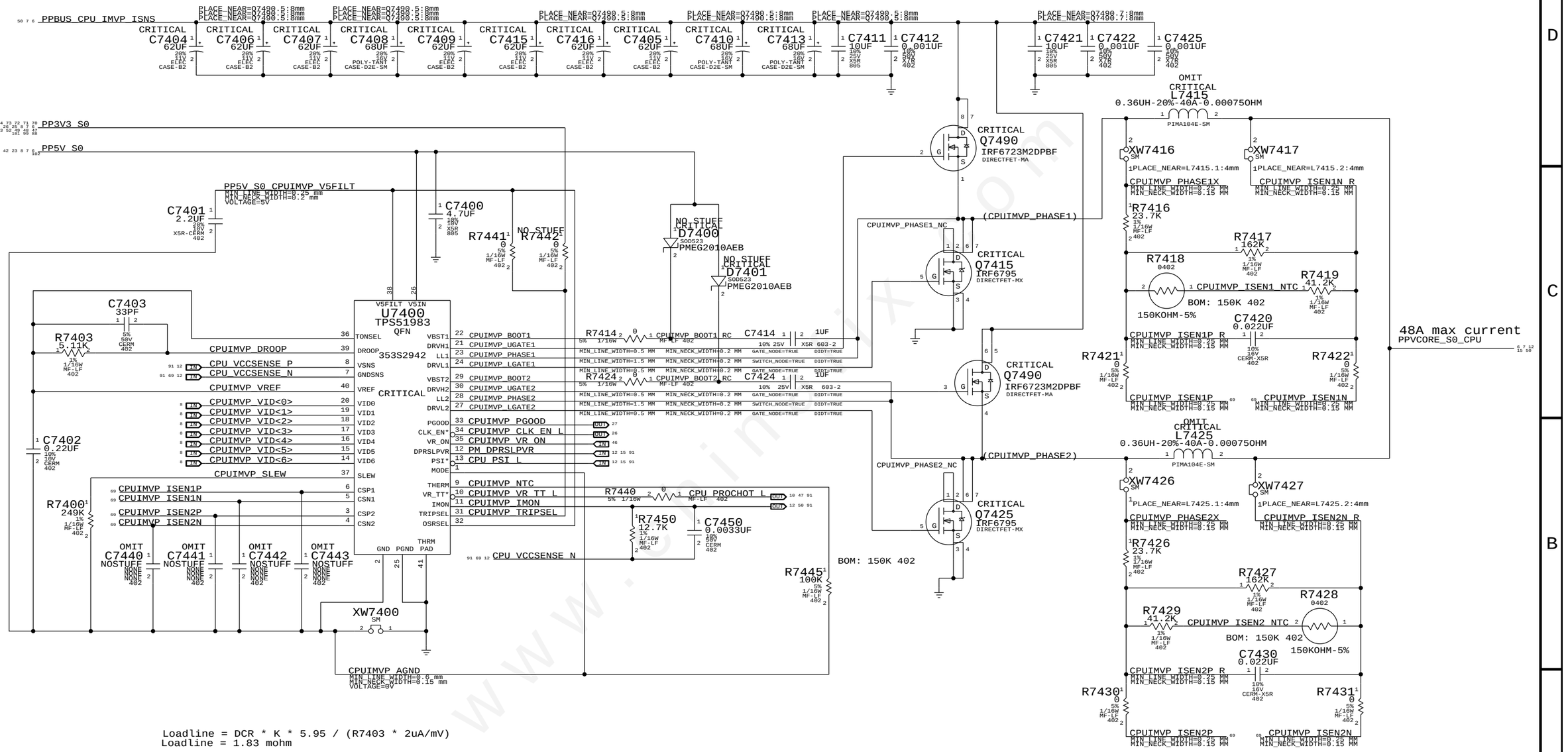

Loadline = DCR * K * 5.95 / (R7403 * 2uA/mV)
Loadline = 1.83 mohm

VIMON = Io * DCR * K * 2uA/mV * R7450
50 A = 1.049 V

K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.787

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1177	2	IND,PWR,0.36uH,1.05MO,12x10x4mm	L7415,L7425	CRITICAL	

SYNC_MASTER=K18_POWER SYNC_DATE=06/29/2009

PAGE TITLE: CPU IMVP VCore Regulator

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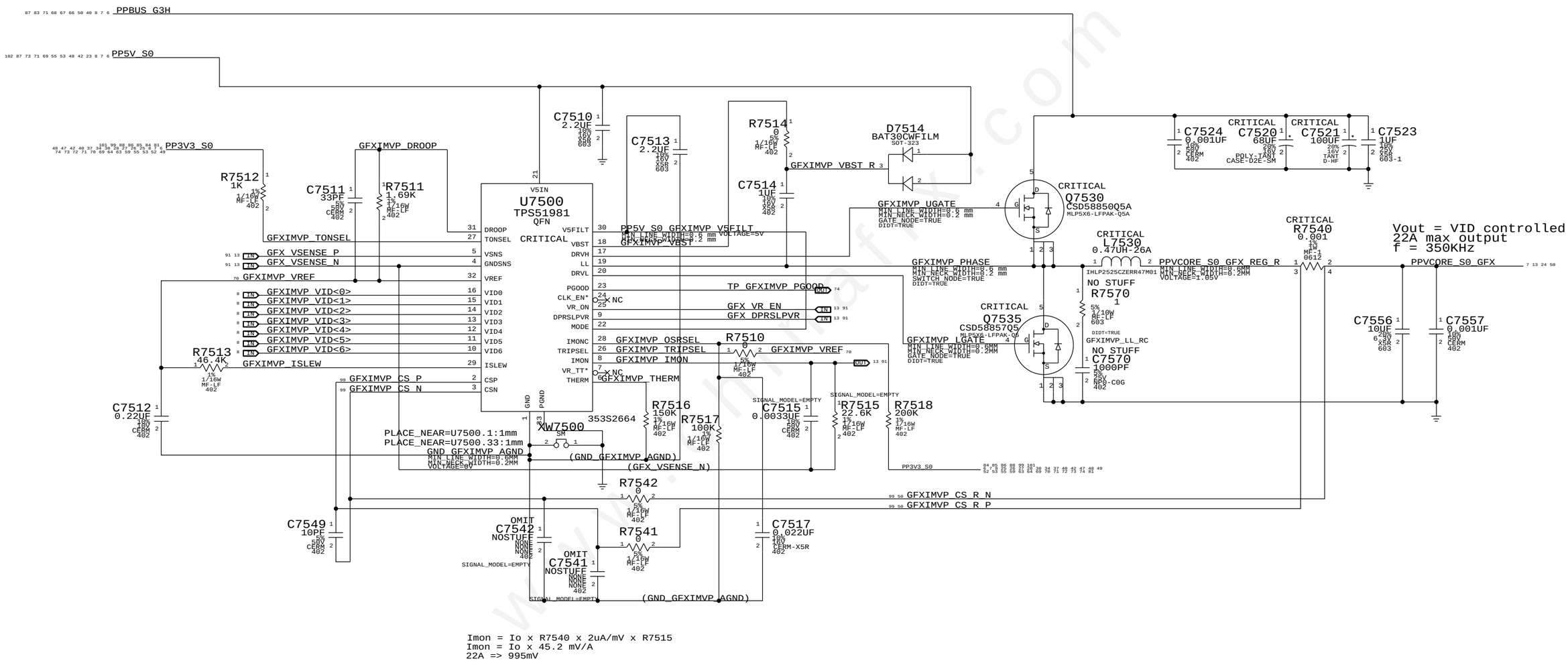

SYNC_MASTER=T22_MLB	SYNC_DATE=03/26/2009
PAGE TITLE	GFX IMVP VCore Regulator
Apple Inc.	DRAWING NUMBER / SIZE: D
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	BRANCH
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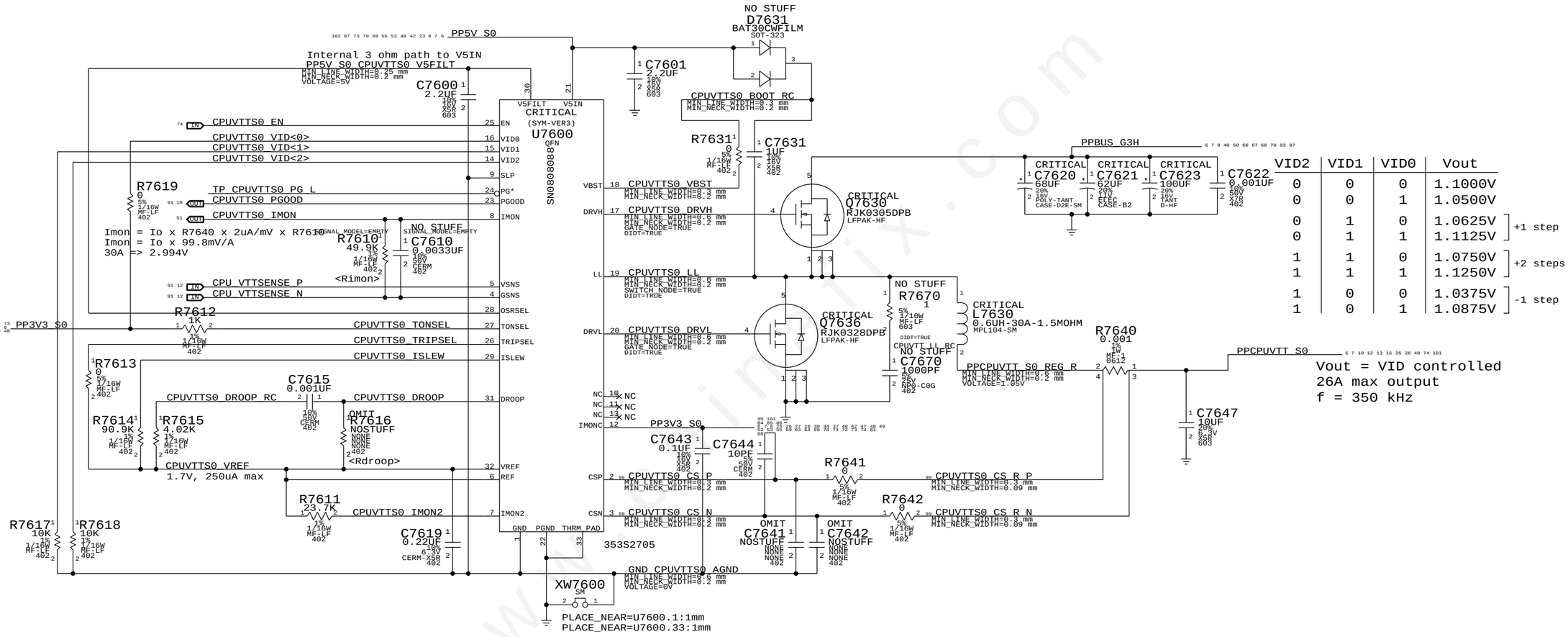
CPU VTT (1.05V S0) Regulator



VID2	VID1	VID0	Vout	
0	0	0	1.1000V	
0	0	1	1.0500V	
0	1	0	1.0625V	+1 step
0	1	1	1.1125V	
1	1	0	1.0750V	+2 steps
1	1	1	1.1250V	
1	0	0	1.0375V	-1 step
1	0	1	1.0875V	

SYNC_MASTER=T22_MLB SYNC_DATE=03/26/2009

PAGE TITLE: CPUVTT (1.05V) Power Supply

Apple Inc.

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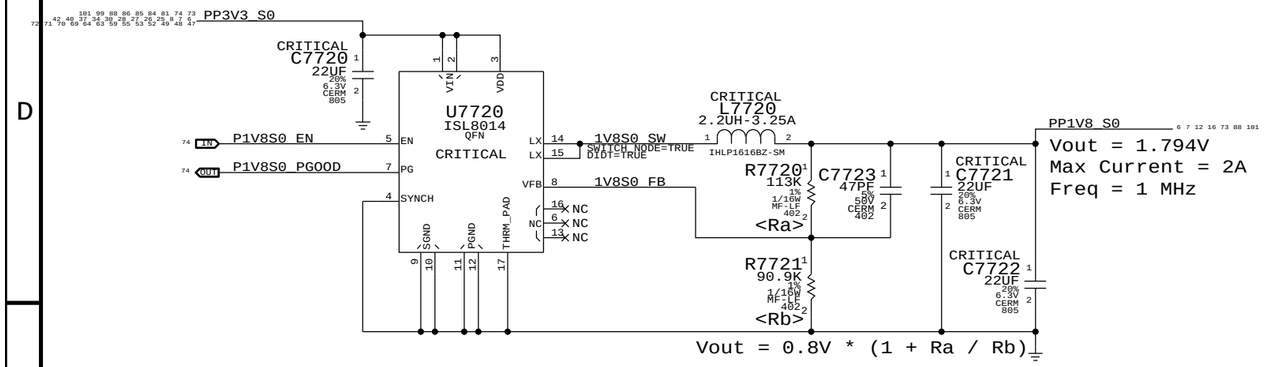
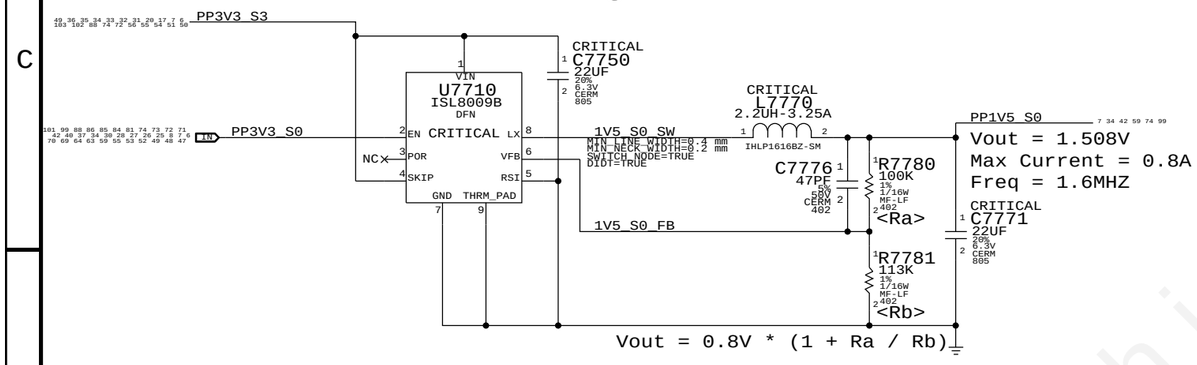
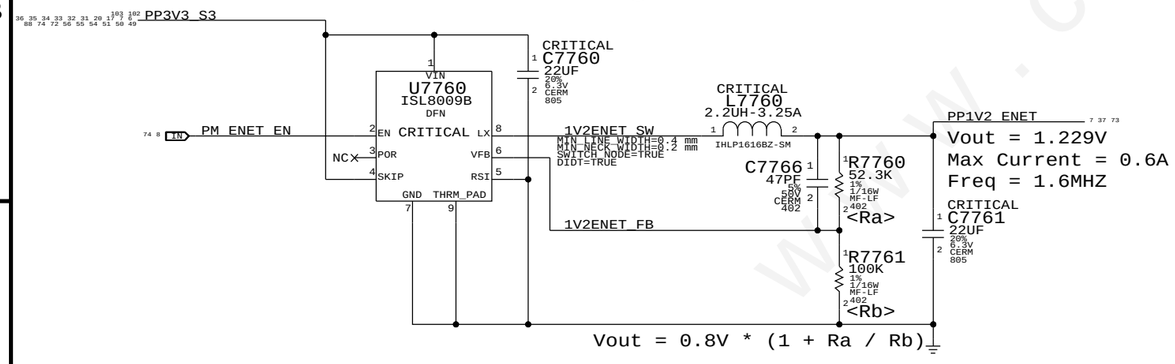
1.8V S0 Regulator



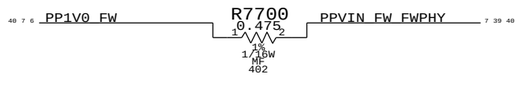
1.5V S0 Regulator



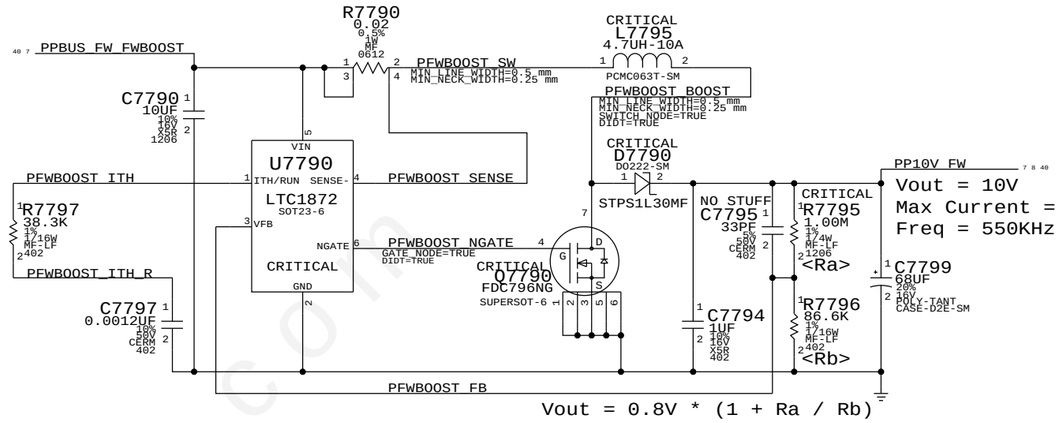
1.2V ENET Regulator



1.05V to 1.0V FW Drop

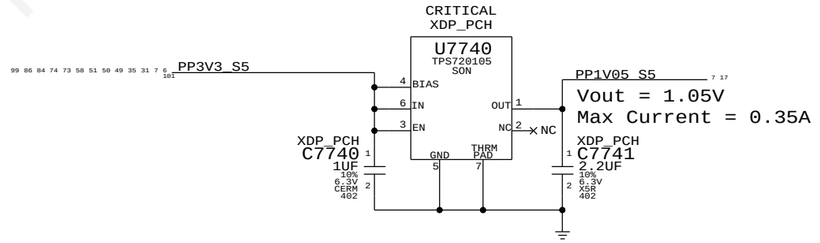


FW 10V Boost Regulator



1.05V S5 LDO

Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Misc Power Supplies

Apple Inc.

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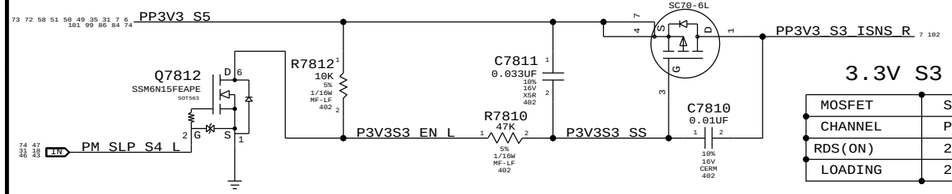
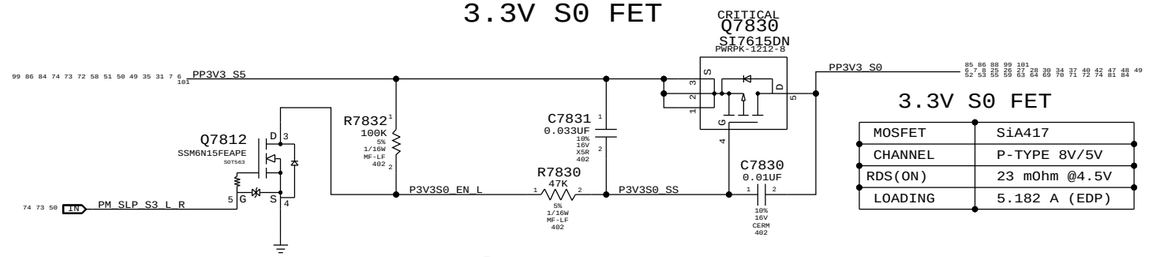
3.3V S3 FET



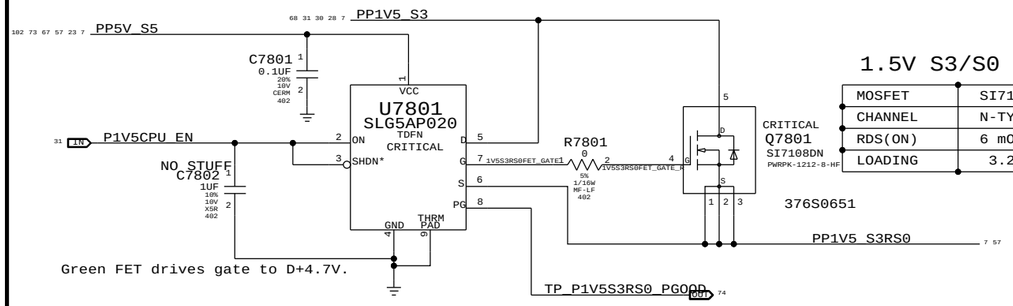
3.3V S3 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	2.096 A (EDP)

3.3V S0 FET



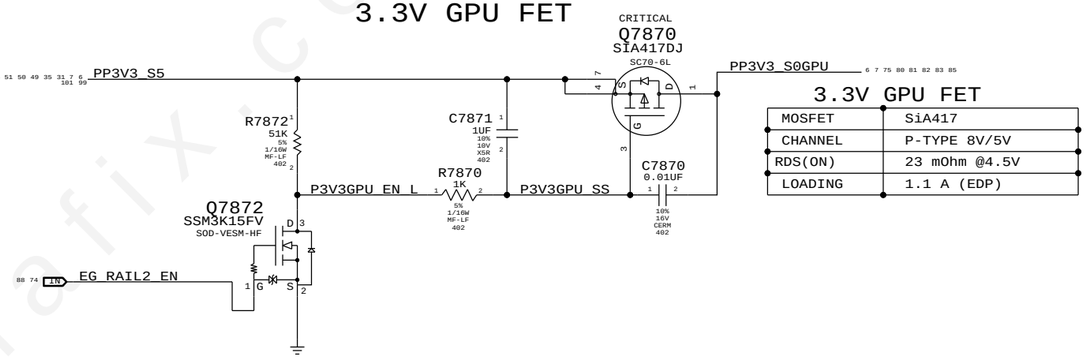
3.3V S0 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	5.182 A (EDP)

1.5V S3/S0 FET



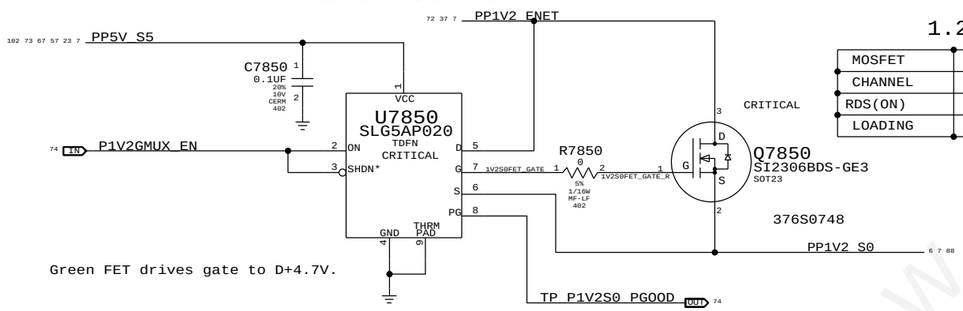
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	3.2A (EDP)

3.3V GPU FET



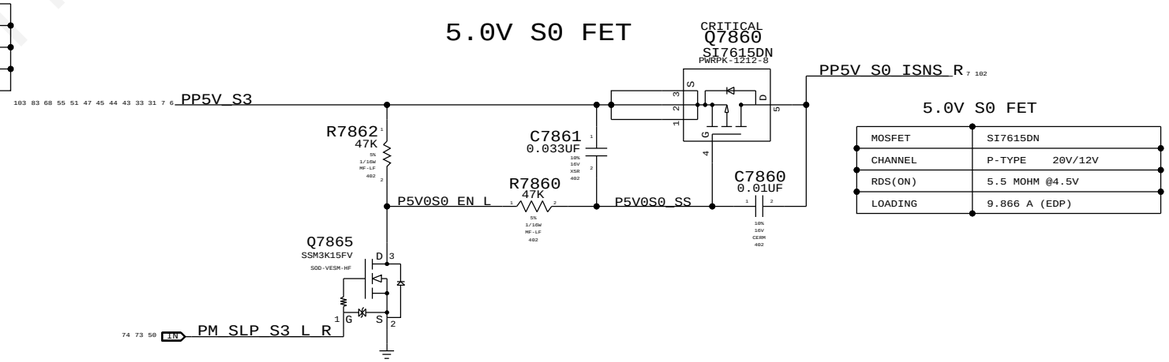
3.3V GPU FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	1.1 A (EDP)

1.2V S0 FET



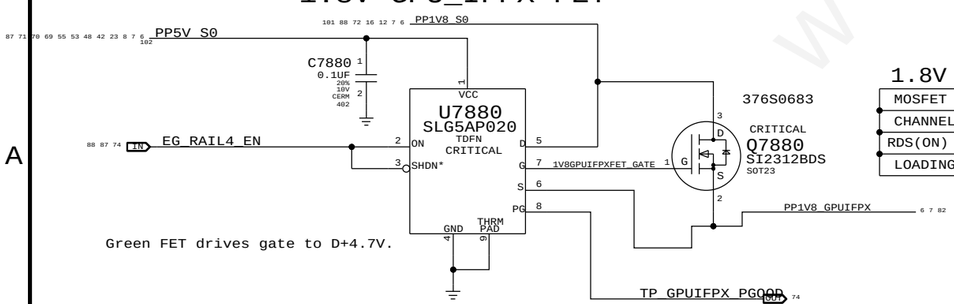
1.2V S0 FET	
MOSFET	SI2306BDS-GE3
CHANNEL	N-TYPE
RDS(ON)	65 mOhm @4.5V
LOADING	0.124 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	9.866 A (EDP)

1.8V GPU_IFPX FET



1.8V GPU_IFPX FET	
MOSFET	SI2312BDS
CHANNEL	N-TYPE
RDS(ON)	31 mOhm @4.5V
LOADING	0.3 A (EDP)

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Power FETs

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State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.3V S5 ENABLE

SMC_PM_G2_EN → R7902 100 → P3V3S5_EN
R7958 100K (PLACE_NEAR=U4900.L13:3mm)
C7902 NO STUFF 0.068UF (PLACE_NEAR=R7252.2:2mm)
R7901 100 → P5VS5_EN
C7901 NO STUFF 0.068UF
P3V3S5_PGOOD → R7941 0 → RSMRST_PWRGD
PP3V42_G3H → R7940 100K
OMIT C7941 NOSTUFF

S5 rail PWRGD

Unused PGOOD signal

TP_P1V2S0_PGOOD
TP_GPUIFPX_PGOOD
TP_P1V5S3RS0_PGOOD
TP_GFXIMVP_PGOOD
TP_DDRREG_PGOOD

3.3V,5V S3 ENABLE

PM_SLP_S4_L (PM_S4_STATE_L) PM_SLP_S4_L
R7911 5.1K (PLACE_NEAR=U7300.11:3mm)
R7912 0 (PLACE_NEAR=R7251.2:3mm)
P5VS3_EN
DDRREG_EN
C7910 0.47UF
C7912 NO STUFF 0.47UF (PLACE_NEAR=R7251.2:3mm)

S0 ENABLE

(PM_SLP_S3_L)
PM_SLP_S3_L → R7978 100
PM_SLP_S4_L
R7979 100K (PLACEMENT_NOTE=Near U1800)
VFRQ_SLPS4 R7933 0
VFRQ_SLPS3 R7932 0
PP3V42_G3H
R7931 10K
CHGR VFRQ Generation
CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF
NO STUFF R7935 0
VFRQ_EN_GATE
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

PM_SLP_S3_L_R
R7981 33K (PLACE_NEAR=U7600.25:6mm)
R7985 10K (PLACE_NEAR=U7850.1:6mm)
R7986 5.1K (PLACE_NEAR=U7720.5:6mm)
C7981 C7985 C7986 0.47UF
PM_SLP_S3_L_R
P1V8S0_EN
P1V2GMUX_EN
CPUVTTS0_EN

Other S0 RAILS

PP3V3_S0
R7992 10K
PM_ALL_GFX_PGOOD
PM_ALL_GPU_PGOOD
R7995 100 ← S0PGOOD_PWROK
R7996 100 ← P1V8S0_PGOOD
R7997 100 ← P5VS3_PGOOD
S0_PWR_PGOOD
R7994 0 (PLACE_NEAR=U7980.1:4mm)
R7991 100 ← PM_ALL_GPU_PGOOD, ALL_GFX_PGOOD_R
U7980 TC7SZ08AFEAPE SOT665
ALL_SYS_PWRGD
C7989 0.1UF
PP3V3_S5

27MHZ OE EN Generation

PP3V3_S0
R7999 10K
Q7995 SSM3K15FV SOD-VESM-HF
CK505_27MHZ_EN_L

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R7920 & Q7920, MUST BE S3 RAIL.

3.3V ENET FET

EXT GPU PWRGD Pullup

PP3V3_S0
R7990 100K
PM_ALL_GPU_PGOOD ×3 → PM_ALL_GPU_PGOOD (MAKE_BASE=TRUE)

PP3V3_S3
R7920 10K → PM_ENET_EN
C7920 0.22UF
Q7921 2N7002DW-X-G SOT-363 → PM_ENET_EN_L
R7921 10K
R7922 100K → P3V3ENET_SS
C7921 0.033UF
C7922 0.01UF
Q7922 NTR4101P SOT-23-HF CRITICAL → PP3V3_ENET

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_SLP_S3_L → Q7921 2N7002DW-X-G SOT-363 → PM_WLAN_EN_L
WOL_EN → Q7920 2N7002DW-X-G SOT-363
Q7925 2N7002DW-X-G SOT-363 ← AP_PWR_EN
AC_EN_L → (AC_EN_L)
SMC_ADAPTER_EN → Q7920 2N7002DW-X-G SOT-363
Q7925 2N7002DW-X-G SOT-363 ← (PM_SLP_S3_L)

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

PP3V3_S0
RAIL_MON
U7971 ISL88042IRTJJZ TDFN CRITICAL
V2MON
V3MON
V4MON
PP1V5_S0
PPCPUVTT_S0
MR* → NC
RST* → S0PGOOD_PWROK
C7971 0.1uF (PLACE_NEAR=U7971.7:2mm)
V2MON THRESHOLD IS 2.866V
V3MON THRESHOLD IS 0.6V
V4MON THRESHOLD IS 0.6V

GPU Rail Sequencing

GT216 GPU requires rails to come up in the following order:
1) 1.1V
2) GPU_3.3V
3) GPUVcore
4) GDDR3 1.8V

EG_RAIL1_EN
EG_RAIL2_EN
EG_RAIL3_EN
EG_RAIL4_EN

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU

PEX 1.05V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8018 10UF 20% 6.3V X5R 603
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

L8015 100NH-700MA-0.140OHM 0603

120 mA: GT216 A01 DG v3 01/09

PP1V05_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V

C8017 1UF 10% 6.3V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

OMIT

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H32	PEX_IOVDD1	AK16
M7	PEX_IOVDD2	AK17
P6	PEX_IOVDD3	AK21
A5	PEX_IOVDD4	AK24
U7	PEX_IOVDD5	AK27
V6		
AB7		
AD6		
AF6	PEX_IOVDDQ1	AG11
AG6	PEX_IOVDDQ2	AG12
AJ5	PEX_IOVDDQ3	AG13
AK15	PEX_IOVDDQ4	AG15
AL7	PEX_IOVDDQ5	AG16
E7	PEX_IOVDDQ6	AG17
A2	PEX_IOVDDQ7	AG18
A7	PEX_IOVDDQ8	AG22
B7	PEX_IOVDDQ9	AG23
C5	PEX_IOVDDQ10	AG24
C7	PEX_IOVDDQ11	AG25
D5	PEX_IOVDDQ12	AG26
D6	PEX_IOVDDQ13	AJ14
D7	PEX_IOVDDQ14	AJ15
E5	PEX_IOVDDQ15	AJ19
E4	PEX_IOVDDQ16	AJ21
G5	PEX_IOVDDQ17	AJ22
J18	PEX_IOVDDQ18	AJ24
J19	PEX_IOVDDQ19	AJ25
J25	PEX_IOVDDQ20	AJ27
J26	PEX_IOVDDQ21	AK18
AA4	PEX_IOVDDQ22	AK20
AB4	PEX_IOVDDQ23	AK23
AC5	PEX_IOVDDQ24	AK26
Y4	PEX_IOVDDQ25	AL16
AG20		
D35		
P7	VDD_SENSE	AG14
E35		
R7	GND_SENSE	VDD_SENSE AD20
A4	BUFRST*	GND_SENSE AD19

NC

GPU_VDD_SENSE 83
GPU_GND_SENSE 83

NC_GPU_BUFRST_L OUT 6

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PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19	PEX_RX1*	
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PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29	PEX_RX11*	
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PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32	PEX_RX14*	
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PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34	PEX_RX15*	

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PEG_CLK100M_P
PEG_CLK100M_N
EG_RESET_L R8020 0 5% 1/16W MF-LF 402 GPU_RESET_R_L
PEX_CLKREQ_L

PP3V3_S0GPU
R8021 10K 5% 1/16W MF-LF 402

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PEX_REFCLK	AR16	PEX_REFCLK			
PEX_REFCLK*	AR17	PEX_REFCLK*			
PEX_RST*	AM16	PEX_RST*			
PEX_CLKREQ*	AR13	PEX_CLKREQ*			
PEX_TX0	AL17	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>	
PEX_TX0*	AM17	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>	
PEX_TX1	AM18	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>	
PEX_TX1*	AM19	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>	
PEX_TX2	AL19	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>	
PEX_TX2*	AK19	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>	
PEX_TX3	AL20	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>	
PEX_TX3*	AM20	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>	
PEX_TX4	AM21	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>	
PEX_TX4*	AM22	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4>	
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PEX_TX5*	AK22	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5>	
PEX_TX6	AL23	PEG_D2R_C_P<6>	C8067 0.1uF	PEG_D2R_P<6>	
PEX_TX6*	AM23	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6>	
PEX_TX7	AM24	PEG_D2R_C_P<7>	C8069 0.1uF	PEG_D2R_P<7>	
PEX_TX7*	AM25	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7>	
PEX_TX8	AL25	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8>	
PEX_TX8*	AK25	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8>	
PEX_TX9	AL26	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9>	
PEX_TX9*	AM26	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9>	
PEX_TX10	AM27	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10>	
PEX_TX10*	AM28	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10>	
PEX_TX11	AL28	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11>	
PEX_TX11*	AK28	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11>	
PEX_TX12	AK29	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12>	
PEX_TX12*	AL29	PEG_D2R_C_N<12>	C8080 0.1uF	PEG_D2R_N<12>	
PEX_TX13	AM29	PEG_D2R_C_P<13>	C8081 0.1uF	PEG_D2R_P<13>	
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PEX_TX14*	AM32	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14>	
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PEX_TX15*	AP32	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>	

10%16V X5R 402

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK_P
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK_N
PEX_TERMP AG21 PEX_TERMP_PD R8050 2.49K 1% 1/16W MF-LF 402
PEX_SVDD_3V3 AG19 F7

NO STUFF R8060 200 1% 1/16W MF-LF 402

C8013 4.7UF 10% 6.3V X5R-CERM 603
C8012 0.1UF 10% 16V X5R 402

PP1V05_S0GPU
NO STUFF R8012 0 5% 1/16W MF-LF 402
R8013 0 5% 1/16W MF-LF 402
PP3V3R1V05_GPU_PEX_SVDD
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

SYNC_MASTER=K18_MLB SYNC_DATE=06/29/2009

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NV GT216 PCI-E

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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

7 83 9 50 PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 10% 16V X5R 402
C8101 0.22UF 10% 6.3V CERM-X5R 402
C8102 0.22UF 10% 6.3V CERM-X5R 402
C8103 0.1UF 10% 16V X7R-CERM 402
C8104 0.047UF 10% 16V X7R 402
C8105 0.047UF 10% 16V X7R 402
C8106 0.047UF 10% 16V X7R 402
C8107 0.022UF 10% 16V CERM-X5R 402
C8108 0.022UF 10% 16V CERM-X5R 402
C8109 0.022UF 10% 16V CERM-X5R 402
C8110 0.015UF 10% 16V X7R 402
C8111 0.015UF 10% 16V X7R 402
C8112 0.01UF 10% 25V X7R 402
C8113 0.01UF 10% 25V X7R 402
C8114 0.01UF 10% 25V X7R 402
C8115 0.01UF 10% 25V X7R 402
C8116 0.01UF 10% 25V X7R 402
C8117 0.01UF 10% 25V X7R 402
C8118 0.0068UF 10% 25V CERM 402
C8119 0.0047UF 10% 25V CERM 402

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VDD: L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17

VDD: V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20

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GND: B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16

GND: V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30 K9 AK14

79 78 77 51 8 7 6 PP1V8_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8156 4.7UF 20% 6.3V CERM 603
C8157 0.1UF 10% 16V CERM 402
C8158 0.1UF 10% 16V CERM 402
C8159 0.1UF 10% 16V CERM 402
C8160 0.047UF 10% 16V X7R 402
C8162 0.047UF 10% 16V X7R 402
C8163 0.047UF 10% 16V X7R 402
C8164 0.01UF 10% 25V X7R 402
C8165 0.01UF 10% 25V X7R 402
C8166 0.01UF 10% 25V X7R 402

OMIT

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FBVDDQ: B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16

FBVDDQ: J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31

SYNC_MASTER=GT216 SYNC_DATE=03/26/2009

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NV GT216 CORE/FB POWER

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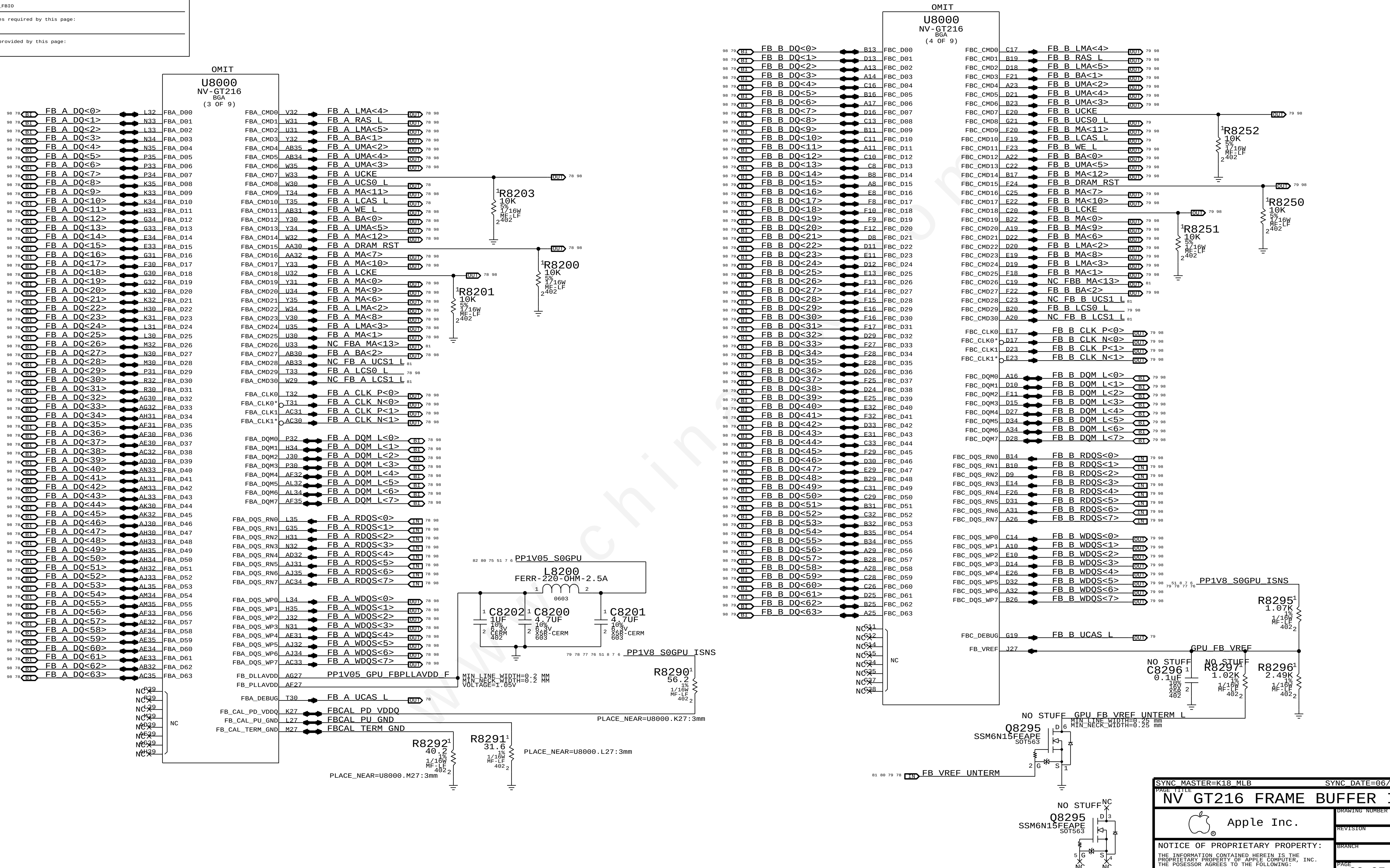
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K18_MLB SYNC_DATE=06/29/2009

PAGE TITLE

NV GT216 FRAME BUFFER I/F

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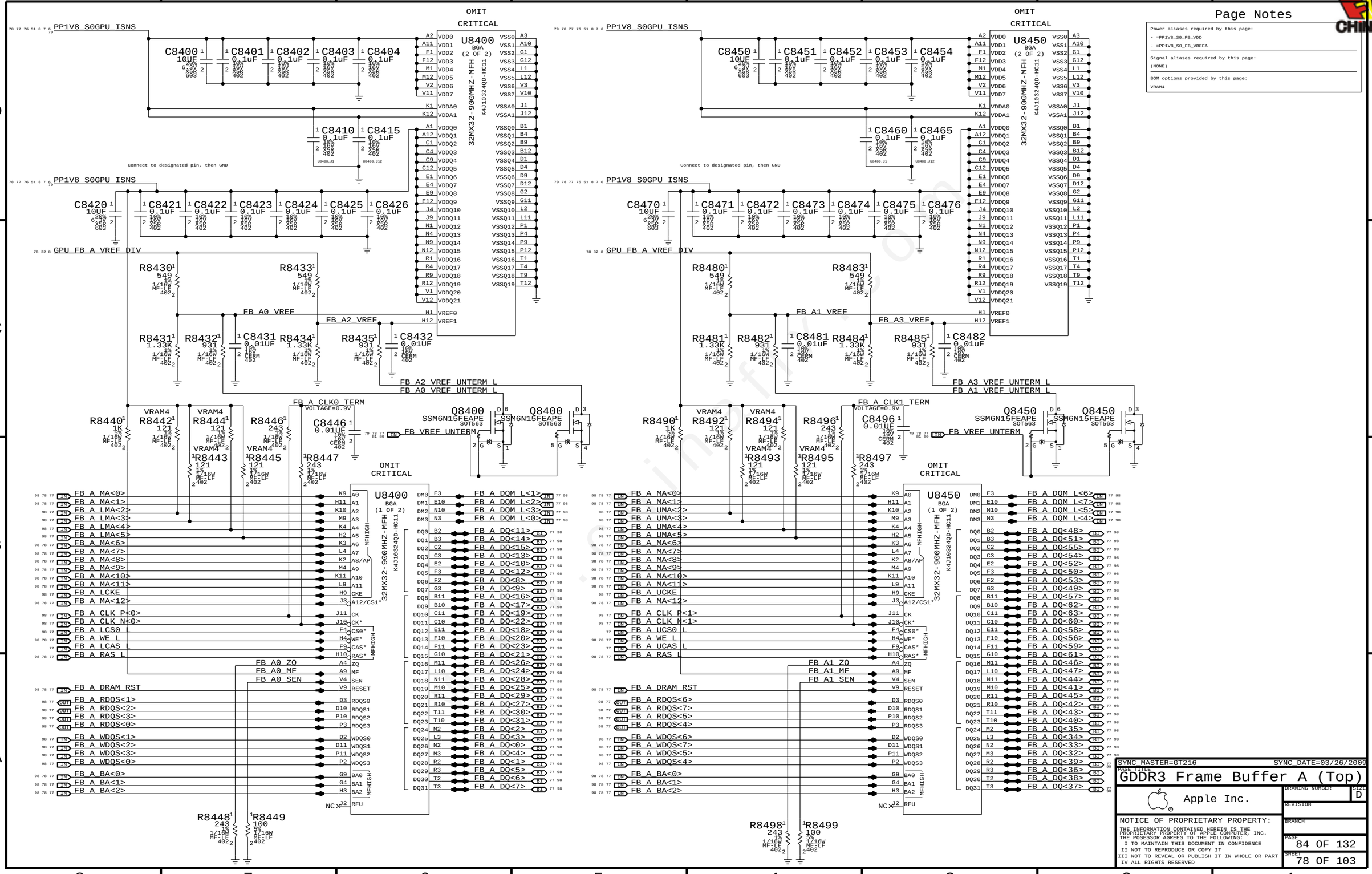
OMIT
CRITICAL
U8400
BGA
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32MX32-900MHZ-MFH
K4J10324QD-HC11
PP1V8_S0GPU_ISNS
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C8401 0.1UF 10% 16V X5R 402
C8402 0.1UF 10% 16V X5R 402
C8403 0.1UF 10% 16V X5R 402
C8404 0.1UF 10% 16V X5R 402
C8410 0.1UF 10% 16V X5R 402
C8415 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
C8420 10UF 20% 6.3V X5R 603
C8421 0.1UF 10% 16V X5R 402
C8422 0.1UF 10% 16V X5R 402
C8423 0.1UF 10% 16V X5R 402
C8424 0.1UF 10% 16V X5R 402
C8425 0.1UF 10% 16V X5R 402
C8426 0.1UF 10% 16V X5R 402
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R8430 549 1% 1/16W MF-LF 402
R8433 549 1% 1/16W MF-LF 402
FB_A0_VREF
FB_A2_VREF
R8431 1.33K 1% 1/16W MF-LF 402
R8432 931 1% 1/16W MF-LF 402
C8431 0.01UF 10% 16V CERM 402
R8434 1.33K 1% 1/16W MF-LF 402
R8435 931 1% 1/16W MF-LF 402
C8432 0.01UF 10% 16V CERM 402
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FB_A0_VREF_UNTERM_L
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VOLTAGE=0.9V
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FB_VREF_UNTERM
R8440 1K 1% 1/16W MF-LF 402
R8442 121 1% 1/16W MF-LF 402
R8444 121 1% 1/16W MF-LF 402
R8446 243 1% 1/16W MF-LF 402
R8443 121 1% 1/16W MF-LF 402
R8445 121 1% 1/16W MF-LF 402
R8447 243 1% 1/16W MF-LF 402
Q8400 SSM6N15FEAPE SOT563
Q8400 SSM6N15FEAPE SOT563
OMIT
CRITICAL
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FB_A0_ZQ
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FB_A0_SEN
FB_A_DRAM_RST
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_RDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_WDQS<0>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
R8448 243 1% 1/16W MF-LF 402
R8449 100 5% 1/16W MF-LF 402
PP1V8_S0GPU_ISNS
C8450 10UF 20% 6.3V X5R 603
C8451 0.1UF 10% 16V X5R 402
C8452 0.1UF 10% 16V X5R 402
C8453 0.1UF 10% 16V X5R 402
C8454 0.1UF 10% 16V X5R 402
C8460 0.1UF 10% 16V X5R 402
C8465 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
C8470 10UF 20% 6.3V X5R 603
C8471 0.1UF 10% 16V X5R 402
C8472 0.1UF 10% 16V X5R 402
C8473 0.1UF 10% 16V X5R 402
C8474 0.1UF 10% 16V X5R 402
C8475 0.1UF 10% 16V X5R 402
C8476 0.1UF 10% 16V X5R 402
GPU_FB_A_VREF_DIV
R8480 549 1% 1/16W MF-LF 402
R8483 549 1% 1/16W MF-LF 402
FB_A1_VREF
FB_A3_VREF
R8481 1.33K 1% 1/16W MF-LF 402
R8482 931 1% 1/16W MF-LF 402
C8481 0.01UF 10% 16V CERM 402
R8484 1.33K 1% 1/16W MF-LF 402
R8485 931 1% 1/16W MF-LF 402
C8482 0.01UF 10% 16V CERM 402
FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L
FB_A_CLK1_TERM
VOLTAGE=0.9V
C8496 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
R8490 1K 1% 1/16W MF-LF 402
R8492 121 1% 1/16W MF-LF 402
R8494 121 1% 1/16W MF-LF 402
R8496 243 1% 1/16W MF-LF 402
R8493 121 1% 1/16W MF-LF 402
R8495 121 1% 1/16W MF-LF 402
R8497 243 1% 1/16W MF-LF 402
Q8450 SSM6N15FEAPE SOT563
Q8450 SSM6N15FEAPE SOT563
OMIT
CRITICAL
FB_A_MA<0>
FB_A_MA<1>
FB_A_UMA<2>
FB_A_UMA<3>
FB_A_UMA<4>
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FB_A_MA<11>
FB_A_UCKE
FB_A_MA<12>
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_UCS0_L
FB_A_WE_L
FB_A_UCAS_L
FB_A_RAS_L
FB_A_DQM_L<6>
FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<4>
FB_A_DQ<48>
FB_A_DQ<51>
FB_A_DQ<55>
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FB_A_DQ<37>
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
FB_A_DRAM_RST
FB_A_RDQS<6>
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FB_A_RDQS<5>
FB_A_RDQS<4>
FB_A_WDQS<6>
FB_A_WDQS<7>
FB_A_WDQS<5>
FB_A_WDQS<4>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
R8498 243 1% 1/16W MF-LF 402
R8499 100 5% 1/16W MF-LF 402
Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4
SYNC_MASTER=GT216
SYNC_DATE=03/26/2009
PAGE TITLE
GDDR3 Frame Buffer A (Top)
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
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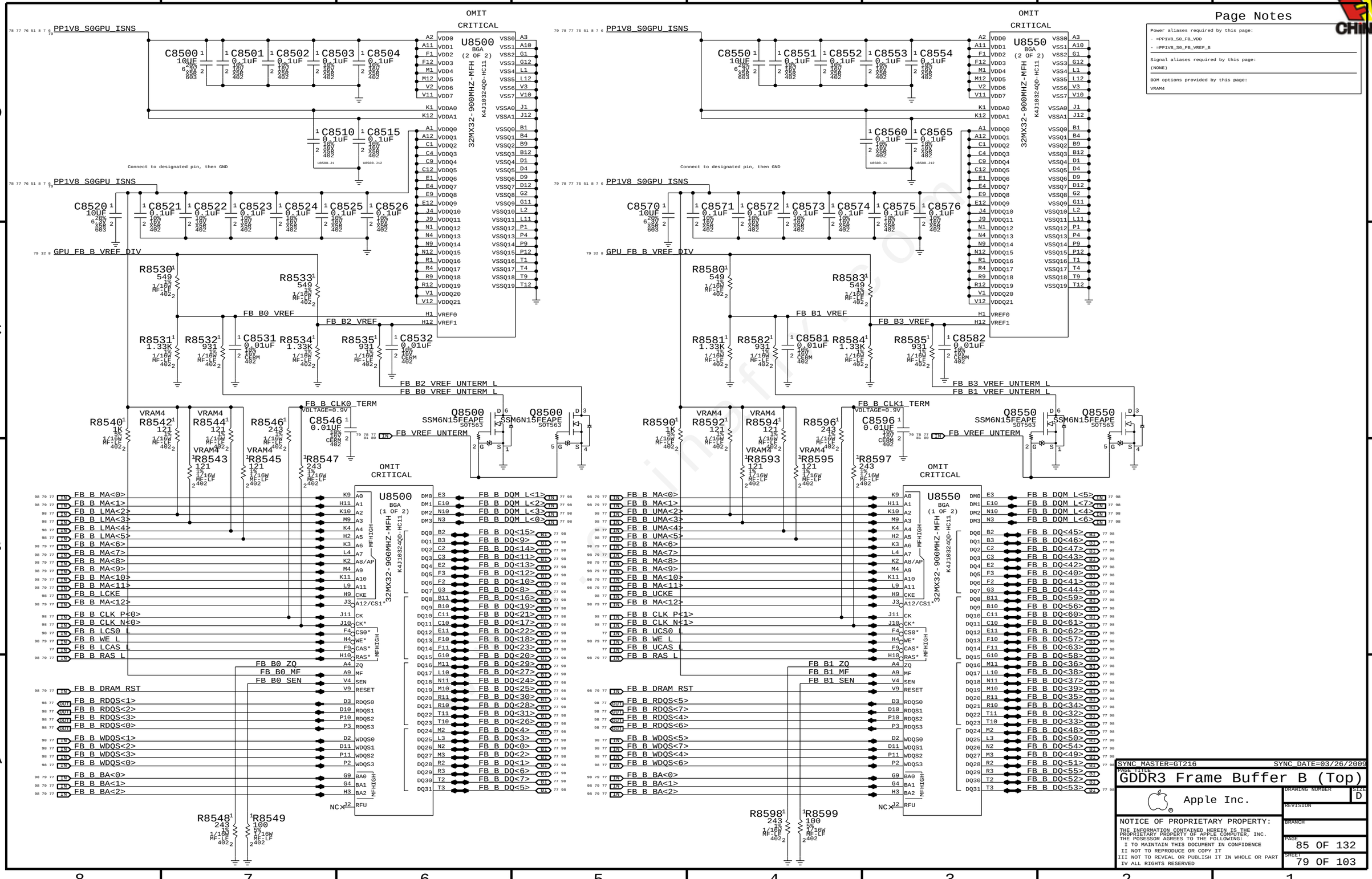
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CRITICAL
U8500
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
PP1V8_S0GPU_ISNS
C8500 10UF 20% 6.3V X5R 603
C8501 C8502 C8503 C8504 0.1UF 10% 16V X5R 402
C8510 C8515 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
C8520 10UF 20% 6.3V X5R 603
C8521 C8522 C8523 C8524 C8525 C8526 0.1UF 10% 16V X5R 402
GPU_FB_B_VREF_DIV
R8530 549 1% 1/16W MF-LF 402
R8533 549 1% 1/16W MF-LF 402
FB_B0_VREF
FB_B2_VREF
R8531 1.33K 1% 1/16W MF-LF 402
R8532 931 1% 1/16W MF-LF 402
C8531 0.01UF 10% 16V CERM 402
R8534 1.33K 1% 1/16W MF-LF 402
R8535 931 1% 1/16W MF-LF 402
C8532 0.01UF 10% 16V CERM 402
FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L
FB_B_CLK0_TERM
VOLTAGE=0.9V
C8546 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
Q8500 SSM6N15FEAPE SOT563
R8540 1K 1% 1/16W MF-LF 402
R8542 121 1% 1/16W MF-LF 402
R8544 121 1% 1/16W MF-LF 402
R8546 243 1% 1/16W MF-LF 402
R8543 121 1% 1/16W MF-LF 402
R8545 121 1% 1/16W MF-LF 402
R8547 243 1% 1/16W MF-LF 402
OMIT
CRITICAL
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FB_B_WE_L
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FB_B_RAS_L
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FB_B_RDQS<1>
FB_B_RDQS<2>
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FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
R8548 243 1% 1/16W MF-LF 402
R8549 100 5% 1/16W MF-LF 402
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FB_B_DQ<5>
U8550
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
PP1V8_S0GPU_ISNS
C8550 10UF 20% 6.3V X5R 603
C8551 C8552 C8553 C8554 0.1UF 10% 16V X5R 402
C8560 C8565 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
C8570 10UF 20% 6.3V X5R 603
C8571 C8572 C8573 C8574 C8575 C8576 0.1UF 10% 16V X5R 402
GPU_FB_B_VREF_DIV
R8580 549 1% 1/16W MF-LF 402
R8583 549 1% 1/16W MF-LF 402
FB_B1_VREF
FB_B3_VREF
R8581 1.33K 1% 1/16W MF-LF 402
R8582 931 1% 1/16W MF-LF 402
C8581 0.01UF 10% 16V CERM 402
R8584 1.33K 1% 1/16W MF-LF 402
R8585 931 1% 1/16W MF-LF 402
C8582 0.01UF 10% 16V CERM 402
FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L
FB_B_CLK1_TERM
VOLTAGE=0.9V
C8596 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
Q8550 SSM6N15FEAPE SOT563
R8590 1K 1% 1/16W MF-LF 402
R8592 121 1% 1/16W MF-LF 402
R8594 121 1% 1/16W MF-LF 402
R8596 243 1% 1/16W MF-LF 402
R8593 121 1% 1/16W MF-LF 402
R8595 121 1% 1/16W MF-LF 402
R8597 243 1% 1/16W MF-LF 402
OMIT
CRITICAL
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R8599 100 5% 1/16W MF-LF 402
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Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4
SYNC_MASTER=GT216
SYNC_DATE=03/26/2009
PAGE TITLE
GDDR3 Frame Buffer B (Top)
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
BRANCH
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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U8000
NV-GT216
BGA
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PP3V3_S0GPU → C8694 0.1UF, C8696 1UF, C8698 4.7UF → J9, J10, J11, J12, J13 (VDD33)

GPU_TESTMODE_PD → AP35 TESTMODE
GPU_MIOA_VREF → N5 MIOA_VREF
GPU_MIOB_VREF → AF1 MIOB_VREF
GPU_MIOA_PD_VDDQ → U5 MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND → T5 MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ → AA7 MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND → AA6 MIOB_CAL_PU_GND

AF9 SP_PLLVDD
AE9 PLLVDD (65mA)
AD9 VID_PLLVDD

PP1V05_S0GPU → L8635 100NH-700MA-0.14OHM → PP1V05_GPU_H_PLLVDD_F (25mA) → C8637 4.7UF, C8635 4.7UF, C8636 1UF
PP1V05_S0GPU → L8640 100NH-700MA-0.14OHM → PP1V05_GPU_VID_PLLVDD_F (50mA) → C8643 4.7UF, C8640 4.7UF, C8641 1UF, C8631 0.1UF

GPU_CLK27M → B1 XTAL_IN
NC_GPU_XTALOUT → B2 XTAL_OUT
GPU_XTALOUTBUFF → D1 XTAL_OUTBUFF
GPU_CLK27M_SS → D2 XTAL_SSIN

NC_GPU_ROM_CS_L → C3 ROM_CS*
GPU_ROM_SCLK → D4 ROM_SCLK
GPU_ROM_SI → D3 ROM_SI
GPU_ROM_SO → C4 ROM_SO

R8696 40.2K, R8697 40.2K
GPU_STRAP_REF_3V3_PD → N9 MULTI_STRAP_REF0_GND
GPU_STRAP_REF_MIOB_PD → P9 MULTI_STRAP_REF1_GND

PP3V3_S0GPU → C8610 1UF, C8611 1UF
P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4

R8620 49.9, R8621 49.9 → GPU_MIOA_PD_VDDQ, GPU_MIOB_PD_VDDQ
R8622 49.9, R8623 49.9 → GPU_MIOA_PU_GND, GPU_MIOB_PU_GND
R8616 10K, R8618 10K, R8617 10K, C8617 0.1UF, R8619 10K, C8619 0.1UF, R8660 10K

GPIO0 K1 GPU_VCORE_VID3
GPIO1 K2 DP_EG_HPD
GPIO2 K3 GPU_VCORE_VID4
GPIO3 H3 EG_LCD_PWR_EN
GPIO4 H2 EG_BKLT_EN
GPIO5 H1 GPU_VCORE_VID0
GPIO6 H4 GPU_VCORE_VID1
GPIO7 H5 GPU_VCORE_VID2
GPIO8 H6 SMC_GFX_OVERTEMP_R_L
GPIO9 J7 TP_GPU_GSTATE<0>
GPIO10 K4 FB_VREF_UNTERM
GPIO11 K5 GPU_GPIO_11
GPIO12 H7 SMC_GFX_THROTTLE_R_L
GPIO13 J4 FBVDD_ALTVO
GPIO14 J6 NC_GPU_GPIO_14
GPIO15 L1 NC_GPU_GPIO_15
GPIO16 L2 GPU_GPIO_16
GPIO17 L4 NC_GPU_GPIO_17
GPIO18 M4 NC_GPU_GPIO_18
GPIO19 L7 NC_GPU_GPIO_19
GPIO20 L5 NC_GPU_GPIO_20
GPIO21 K6 NC_GPU_GPIO_21
GPIO22 L6 NC_GPU_GPIO_22
GPIO23 M6 NC_GPU_GPIO_23

JTAG_TCK AP14 TP_GPU_JTAG_TCK
JTAG_TDI AN14 TP_GPU_JTAG_TDI
JTAG_TDO AN16 TP_GPU_JTAG_TDO
JTAG_TMS AR14 TP_GPU_JTAG_TMS
JTAG_TRST* AP16 TP_GPU_JTAG_TRST_L
MIOA_CLKIN N4 NC_GPU_MIOA_CLKIN
MIOA_CLKOUT R4 NC_GPU_MIOA_CLKOUT
MIOA_CLKOUT* T4 NC_GPU_MIOA_CLKOUT_L
MIOA_CTL3 P5 NC_GPU_MIOA_CTL3
MIOA_DE N2 TP_GPU_MIOA_DE
MIOA_D0 N1 TP_GPU_MIOA_D<0>
MIOA_D1 P4 TP_GPU_MIOA_D<1>
MIOA_D2 P1 TP_GPU_MIOA_D<2>
MIOA_D3 P2 TP_GPU_MIOA_D<3>
MIOA_D4 P3 TP_GPU_MIOA_D<4>
MIOA_D5 T3 TP_GPU_MIOA_D<5>
MIOA_D6 T2 TP_GPU_MIOA_D<6>
MIOA_D7 T1 TP_GPU_MIOA_D<7>
MIOA_D8 U4 TP_GPU_MIOA_D<8>
MIOA_D9 U1 TP_GPU_MIOA_D<9>
MIOA_D10 U2 GPU_MIOA_D<10>
MIOA_D11 U3 GPU_MIOA_D<11>
MIOA_D12 R6 GPU_MIOA_D<12>
MIOA_D13 T6 GPU_MIOA_D<13>
MIOA_D14 N6 GPU_MIOA_D<14>
MIOA_HSYNC N3 NC_GPU_MIOA_HSYNC
MIOA_VSYNC L3 NC_GPU_MIOA_VSYNC
MIOB_CLKIN AE1 NC_GPU_MIOB_CLKIN
MIOB_CLKOUT V4 NC_GPU_MIOB_CLKOUT
MIOB_CLKOUT* W4 NC_GPU_MIOB_CLKOUT_L
MIOB_CTL3 W3 NC_GPU_MIOB_CTL3
MIOB_DE Y5 NC_GPU_MIOB_DE
MIOB_D0 Y1 NC_GPU_MIOB_D<0>
MIOB_D1 Y2 NC_GPU_MIOB_D<1>
MIOB_D2 Y3 NC_GPU_MIOB_D<2>
MIOB_D3 AB3 NC_GPU_MIOB_D<3>
MIOB_D4 AB2 NC_GPU_MIOB_D<4>
MIOB_D5 AB1 NC_GPU_MIOB_D<5>
MIOB_D6 AC4 NC_GPU_MIOB_D<6>
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MIOB_D9 AC3 NC_GPU_MIOB_D<9>
MIOB_D10 AE3 NC_GPU_MIOB_D<10>
MIOB_D11 AE2 NC_GPU_MIOB_D<11>
MIOB_D12 U6 NC_GPU_MIOB_D<12>
MIOB_D13 W6 NC_GPU_MIOB_D<13>
MIOB_D14 Y6 NC_GPU_MIOB_D<14>
MIOB_HSYNC W1 NC_GPU_MIOB_HSYNC
MIOB_VSYNC W2 NC_GPU_MIOB_VSYNC
THERMDP B5 GPU_TDIODE_P
THERMDN B4 GPU_TDIODE_N

GPU_STRAP<0> W5 STRAP0
GPU_STRAP<1> W7 STRAP1
GPU_STRAP<2> V7 STRAP2

SYNC_MASTER=K18_MLB SYNC_DATE=06/29/2009

PAGE TITLE
NV GT216 GPIO/MIO/MISC

Apple Inc.

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REVISION:
BRANCH:
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GPIOs

GPU_VCORE_VID3	GP		GPU_VCORE_VID3	OUT	MAKE_BASE=TRUE
DP_EG_HPD	HPDC		DP_EG_HPD	IN	MAKE_BASE=TRUE
GPU_VCORE_VID4	LCD0_BL_PWM		GPU_VCORE_VID4	OUT	MAKE_BASE=TRUE
EG_LCD_PWR_EN	LCD0_VDD		EG_LCD_PWR_EN		MAKE_BASE=TRUE
EG_BKLT_EN	LCD0_BL_EN		EG_BKLT_EN		MAKE_BASE=TRUE
GPU_VCORE_VID0	VID0		GPU_VCORE_VID0	OUT	MAKE_BASE=TRUE
GPU_VCORE_VID1	VID1		GPU_VCORE_VID1	OUT	MAKE_BASE=TRUE
GPU_VCORE_VID2	VID2/MEM_VID		GPU_VCORE_VID2	OUT	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_R_L	THERM		SMC_GFX_OVERTEMP_R_L		MAKE_BASE=TRUE
TP_GPU_GSTATE<0>	FAN_PWM		TP_GPU_GSTATE<0>		MAKE_BASE=TRUE
FB_VREF_UNTERM	MEM_VREF		FB_VREF_UNTERM		MAKE_BASE=TRUE
GPU_GPIO_11	SLI_SYNC		TP_GPU_GSTATE<1>	OUT	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_R_L	PWR_CTL		SMC_GFX_THROTTLE_R_L	OUT	MAKE_BASE=TRUE
FBVDD_ALTVO	PWR_CTL0		FBVDD_ALTVO	OUT	MAKE_BASE=TRUE
NC_GPU_GPIO_14	PWR_CTL1		NC_GPU_GPIO_14		MAKE_BASE=TRUE NO_TEST=TRUE

GPIOs

NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15		MAKE_BASE=TRUE NO_TEST=TRUE
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET		
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17		MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18		MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19		MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20		MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21		MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22		MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23		MAKE_BASE=TRUE NO_TEST=TRUE

Renamed signals

GPU_CLK27M		GPU_CLK27M
GPU_CLK27M_SS		GPU_CLK27M_SS
GPU_TDIODE_P		GPU_TDIODE_P
GPU_TDIODE_N		GPU_TDIODE_N
LVDS_EG_DDC_CLK		LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA		LVDS_EG_DDC_DATA
DP_EG_DDC_CLK		DP_EG_DDC_CLK
DP_EG_DDC_DATA		DP_EG_DDC_DATA

Unused signals

TP_GPU_JTAG_TCK		TP_GPU_JTAG_TCK
TP_GPU_JTAG_TDI		TP_GPU_JTAG_TDI
TP_GPU_JTAG_TDO		TP_GPU_JTAG_TDO
TP_GPU_JTAG_TMS		TP_GPU_JTAG_TMS
TP_GPU_JTAG_TRST_L		TP_GPU_JTAG_TRST_L
NC_FBA_MA<13>	NO_TEST=TRUE	NC_FBA_MA<13>
NC_FBB_MA<13>	NO_TEST=TRUE	NC_FBB_MA<13>

Unused I2C Buses

NC_GPU_I2CC_SCL	NO_TEST=TRUE	NC_GPU_I2CC_SCL
NC_GPU_I2CC_SDA	NO_TEST=TRUE	NC_GPU_I2CC_SDA
NC_GPU_I2CH_SCL	NO_TEST=TRUE	NC_GPU_I2CH_SCL
NC_GPU_I2CH_SDA	NO_TEST=TRUE	NC_GPU_I2CH_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

NC_FB_B_UCS1_L	NO_TEST=TRUE	NC_FB_B_UCS1_L
NC_FB_B_LCS1_L	NO_TEST=TRUE	NC_FB_B_LCS1_L
NC_GPU_ROM_CS_L	NO_TEST=TRUE	NC_GPU_ROM_CS_L
NC_FB_A_UCS1_L	NO_TEST=TRUE	NC_FB_A_UCS1_L
NC_FB_A_LCS1_L	NO_TEST=TRUE	NC_FB_A_LCS1_L
TP_LVDS_EG_B_CLK_P		TP_LVDS_EG_B_CLK_P
TP_LVDS_EG_B_CLK_N		TP_LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3>	NO_TEST=TRUE	NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>	NO_TEST=TRUE	NC_LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3>	NO_TEST=TRUE	NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>	NO_TEST=TRUE	NC_LVDS_EG_B_DATA_N<3>

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUTP	NO_TEST=TRUE	NC_GPU_MIOA_CLKOUTP
NC_GPU_MIOA_CLKOUTN	NO_TEST=TRUE	NC_GPU_MIOA_CLKOUTN
NC_GPU_MIOA_CTL3	NO_TEST=TRUE	NC_GPU_MIOA_CTL3
TP_GPU_MIOA_DE		TP_GPU_MIOA_DE
TP_GPU_MIOA_D<9..0>		GPU_MIOA_D<9..0>
NC_GPU_MIOA_CLKIN	NO_TEST=TRUE	NC_GPU_MIOA_CLKIN
NC_GPU_MIOA_D<14..10>	NO_TEST=TRUE	GPU_MIOA_D<14..10>
NC_GPU_MIOA_HSYNC	NO_TEST=TRUE	NC_GPU_MIOA_HSYNC
NC_GPU_MIOA_VSYNC	NO_TEST=TRUE	NC_GPU_MIOA_VSYNC
NC_GPU_MIOB_CLKIN	NO_TEST=TRUE	NC_GPU_MIOB_CLKIN
NC_GPU_MIOB_CLKOUTP	NO_TEST=TRUE	NC_GPU_MIOB_CLKOUTP
NC_GPU_MIOB_CLKOUTN	NO_TEST=TRUE	NC_GPU_MIOB_CLKOUTN
NC_GPU_MIOB_CTL3	NO_TEST=TRUE	NC_GPU_MIOB_CTL3
NC_GPU_MIOB_DE	NO_TEST=TRUE	NC_GPU_MIOB_DE
NC_GPU_MIOB_D<14..0>	NO_TEST=TRUE	GPU_MIOB_D<14..0>
NC_GPU_MIOB_VSYNC	NO_TEST=TRUE	NC_GPU_MIOB_VSYNC
NC_GPU_MIOB_HSYNC	NO_TEST=TRUE	NC_GPU_MIOB_HSYNC

Config Straps

PP3V3_S0GPU

OMIT	NO STUFF	NO STUFF	
R8707[1] 2.0K 5% 1/10W MF-LF 402	R8709[1] 4.99K 1% 1/10W MF-LF 402	R8711[1] 15.0K 1% 1/10W MF-LF 402	
GPU_ROM_SI	OUT		
GPU_ROM_SO	IN		
GPU_ROM_SCLK	IN		
OMIT			
R8708[1] 45.3K 1% 1/10W MF-LF 402	R8710[1] 10K 1% 1/10W MF-LF 402	R8712[1] 15.0K 1% 1/10W MF-LF 402	

PP3V3_S0GPU

R8701[1] 45.3K 1% 1/10W MF-LF 402	R8703[1] 34.8K 1% 1/10W MF-LF 402	R8705[1] 10K 1% 1/10W MF-LF 402	
GPU_STRAP<0>	BI		
GPU_STRAP<1>	BI		
GPU_STRAP<2>	BI		
NO STUFF	NO STUFF	NO STUFF	
R8702[1] 2.0K 5% 1/10W MF-LF 402	R8704[1] 10K 1% 1/10W MF-LF 402	R8706[1] 24.9K 1% 1/10W MF-LF 402	

Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0]	PU/PD	Rval
0	0000	PD 5k
1	0001	PD 10k
2	0010	PD 15k
3	0011	PD 20k
4	0100	PD 25k
5	0101	PD 30k
6	0110	PD 35k
7	0111	PD 45k

Strap S1/S2 Bit[3:0]	PU/PD	Rval
8	1000	PU 5k
9	1001	PU 10k
A	1010	PU 15k
B	1011	PU 20k
C	1100	PU 25k
D	1101	PU 30k
E	1110	PU 35k
F	1111	PU 45k

PCI_DEVID[4:0]=0x14

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0353	1	RES,MTL FILM,1/16W,24.9K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX

PP3V3_S0

PP3V3_S0GPU

R8750[1] 2.2K 5% 1/10W MF-LF 402	R8751[1] 2.2K 5% 1/10W MF-LF 402	R8752[1] 4.7K 5% 1/10W MF-LF 402	R8753[1] 4.7K 5% 1/10W MF-LF 402	
DP_EG_DDC_CLK	IN			
DP_EG_DDC_DATA	BI			
DP_IG_DDC_CLK	IN			
DP_IG_DDC_DATA	BI			

PP3V3_S0GPU

DP_CA_DET_EG_FET

DP_CA_DET_EG_FET Q8742 SOD-VESM-HF SSM3K15FV

R8742[1] 100K 5% 1/10W MF-LF 402

EG_DP_CA_DET — DP_CA_DET (IN)

R8743 0 5% 1/10W MF-LF 402 — DP_CA_DET_EG (IN)

DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

PP3V3_S0GPU

R8796[1] 2.2K 5% 1/10W MF-LF 402	R8797[1] 2.2K 5% 1/10W MF-LF 402			
SMC_GFX_OVERTEMP_R_L		R8798 0 5% 1/10W MF-LF 402	NO STUFF	SMC_GFX_OVERTEMP_L (OUT)
SMC_GFX_THROTTLE_R_L		R8799 0 5% 1/10W MF-LF 402		SMC_GFX_THROTTLE_L (OUT)
				EG_LCD_PWR_EN (OUT)
				EG_BKLT_EN (OUT)
				FBVDD_ALTVO (OUT)
				FB_VREF_UNTERM (OUT)
R8792[1] 10K 5% 1/10W MF-LF 402	R8793[1] 10K 5% 1/10W MF-LF 402	R8794[1] 10K 5% 1/10W MF-LF 402	R8795[1] NO STUFF 10K 5% 1/10W MF-LF 402	

Unused Clocks

GPU_CLK27M_SS			
GPU_XTALOUTBUFF		GPU_SS_INT	
		R8780[1] 10K 5% 1/10W MF-LF 402	R8781[1] 10K 5% 1/10W MF-LF 402

SYNC_MASTER=K18_MLB SYNC_DATE=07/01/2009

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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

PP1V8_GPUIFPX → L8800 FERR-220-OHM-2.5A (0603)
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402 — Place at AG9
C8803 0.1UF 20% 10V CERM 402 — Place at AG10
→ PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

PP1V05_S0GPU → L8805 180-OHM-1.5A (0603)
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 1UF 20% 6.3V CERM 402
→ PP1V05_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

GPU_IFPEF_RSET
GPU_IFPC_RSET
GPU_IFPAB_RSET
GPU_IFPD_RSET
R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402
R8858 1K 1% 1/16W MF-LF 402

PP1V05_S0GPU → L8810 180-OHM-1.5A (0603)
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402 — Place at AJ8
C8813 0.1UF 20% 10V CERM 402 — Place at AK8
→ PP1V05_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

PP3V3_S0GPU → L8815 FERR-220-OHM-2.5A (0603)
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 1UF 10% 6.3V CERM 402
→ PP3V3_GPU_IFPC_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V05_GPU_IFPEF_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V

PP1V8_GPU_IFPEF_PLLVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

GPU_DACA_VDD
GPU_DACB_VDD
PP1V8_GPU_IFPD_PLLVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

OMIT

U8000 NV-GT216 BGA (5 OF 9)

AG9	IFPA_IOVDD	IFPA_TXC	AM11	LVDS_EG_A_CLK_P	OUT 88 98
AG10	IFPB_IOVDD	IFPA_TXC*	AM12	LVDS_EG_A_CLK_N	OUT 88 98
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8	LVDS_EG_A_DATA_P<0>	OUT 88 98
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8	LVDS_EG_A_DATA_N<0>	OUT 88 98
AE7	IFPE_IOVDD	IFPA_TXD1	AM10	LVDS_EG_A_DATA_P<1>	OUT 88 98
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9	LVDS_EG_A_DATA_N<1>	OUT 88 98
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10	LVDS_EG_A_DATA_P<2>	OUT 88 98
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10	LVDS_EG_A_DATA_N<2>	OUT 88 98
AJ9	IFPC_PLLVDD	IFPA_TXD3	AK11	NC_LVDS_EG_A_DATA_P<3>	OUT 81 98
AK7	IFPC_RSET	IFPA_TXD3*	AL11	NC_LVDS_EG_A_DATA_N<3>	OUT 81 98
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13	TP_LVDS_EG_B_CLK_P	OUT 6 81
AL1	IFPEF_RSET	IFPB_TXC*	AN13	TP_LVDS_EG_B_CLK_N	OUT 6 81
		IFPB_TXD4	AN8	LVDS_EG_B_DATA_P<0>	OUT 88 98
		IFPB_TXD4*	AP8	LVDS_EG_B_DATA_N<0>	OUT 88 98
		IFPB_TXD5	AP10	LVDS_EG_B_DATA_P<1>	OUT 88 98
		IFPB_TXD5*	AN10	LVDS_EG_B_DATA_N<1>	OUT 88 98
		IFPB_TXD6	AR11	LVDS_EG_B_DATA_P<2>	OUT 88 98
		IFPB_TXD6*	AR10	LVDS_EG_B_DATA_N<2>	OUT 88 98
		IFPB_TXD7	AN11	NC_LVDS_EG_B_DATA_P<3>	OUT 81 98
		IFPB_TXD7*	AP11	NC_LVDS_EG_B_DATA_N<3>	OUT 81 98
		IFPC_AUX_I2CW_SCL	AP2	DP_EG_AUX_CH_P	OUT 85 98
		IFPC_AUX_I2CW_SDA*	AN3	DP_EG_AUX_CH_N	OUT 85 98
		IFPC_L0	AM7	DP_EG_ML_P<0>	OUT 85 98
		IFPC_L0*	AM6	DP_EG_ML_N<0>	OUT 85 98
		IFPC_L1	AL5	DP_EG_ML_P<1>	OUT 85 98
		IFPC_L1*	AM5	DP_EG_ML_N<1>	OUT 85 98
		IFPC_L2	AM3	DP_EG_ML_P<2>	OUT 85 98
		IFPC_L2*	AM4	DP_EG_ML_N<2>	OUT 85 98
		IFPC_L3	AP1	DP_EG_ML_P<3>	OUT 85 98
		IFPC_L3*	AR2	DP_EG_ML_N<3>	OUT 85 98
		IFPD_AUX_I2CX_SCL	AP4	NC	
		IFPD_AUX_I2CX_SDA*	AN4	NC	
		IFPD_L0	AP6	NC	
		IFPD_L0*	AP7	NC	
		IFPD_L1	AP5	NC	
		IFPD_L1*	AN5	NC	
		IFPD_L2	AN6	NC	
		IFPD_L2*	AR5	NC	
		IFPD_L3	AR6	NC	
		IFPD_L3*	AR7	NC	
		IFPE_AUX_I2CY_SCL	AE4	NC	
		IFPE_AUX_I2CY_SDA*	AD4	NC	
		IFPE_L0	AH6	NC	
		IFPE_L0*	AH5	NC	
		IFPE_L1	AH4	NC	
		IFPE_L1*	AG4	NC	
		IFPE_L2	AE5	NC	
		IFPE_L2*	AE6	NC	
		IFPE_L3	AF6	NC	
		IFPE_L3*	AF5	NC	
		IFPF_AUX_I2CZ_SCL	AF3	NC	
		IFPF_AUX_I2CZ_SDA*	AE3	NC	
		IFPF_L0	AL2	NC	
		IFPF_L0*	AL3	NC	
		IFPF_L1	AJ3	NC	
		IFPF_L1*	AJ2	NC	
		IFPF_L2	AJ1	NC	
		IFPF_L2*	AH1	NC	
		IFPF_L3	AH2	NC	
		IFPF_L3*	AH3	NC	
AJ12	DACA_VDD	DACA_RED	AM15	NC	
		DACA_GREEN	AM14	NC	
		DACA_BLUE	AL14	NC	
AK12	DACA_VREF	DACA_HSYNC	AM13	NC	
NC	NC	NC	NC	NC	
AK13	DACA_RSET	DACA_VSYNC	AL13	NC	
AG7	DACB_VDD	DACB_RED	AK1	NC	
		DACB_GREEN	AL4	NC	
		DACB_BLUE	AJ4	NC	
AK6	DACB_VREF	NC	NC	NC	
NC	NC	CEC	AB5	NC	
AK7	DACB_RSET				
AC6	IFPD_PLLVDD				
		DACB_HSYNC	AM2	NC	
AB6	IFPD_RSET	DACB_VSYNC	AM1	NC	

R8861 1K 5% 1/10W MF-LF 402 — NO STUFF
R8860 1K 5% 1/10W MF-LF 402 — NO STUFF

DP_EG_DDC_CLK → I2CB_SCL
DP_EG_DDC_DATA → I2CB_SDA
LVDS_EG_DDC_CLK → I2CA_SCL
LVDS_EG_DDC_DATA → I2CA_SDA
NC_GPU_I2CC_SCL → I2CC_SCL
NC_GPU_I2CC_SDA → I2CC_SDA
SMBUS_SMC_0_S5_SCL → I2CS_SCL
SMBUS_SMC_0_S5_SDA → I2CS_SDA
NC_GPU_I2CH_SDA → I2CH_SCL
NC_GPU_I2CH_SCL → I2CH_SDA

GPU_IFPD_RSET → IFPD_RSET

SYNC_MASTER=K18_MLB SYNC_DATE=06/29/2009
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NV GT216 VIDEO INTERFACES
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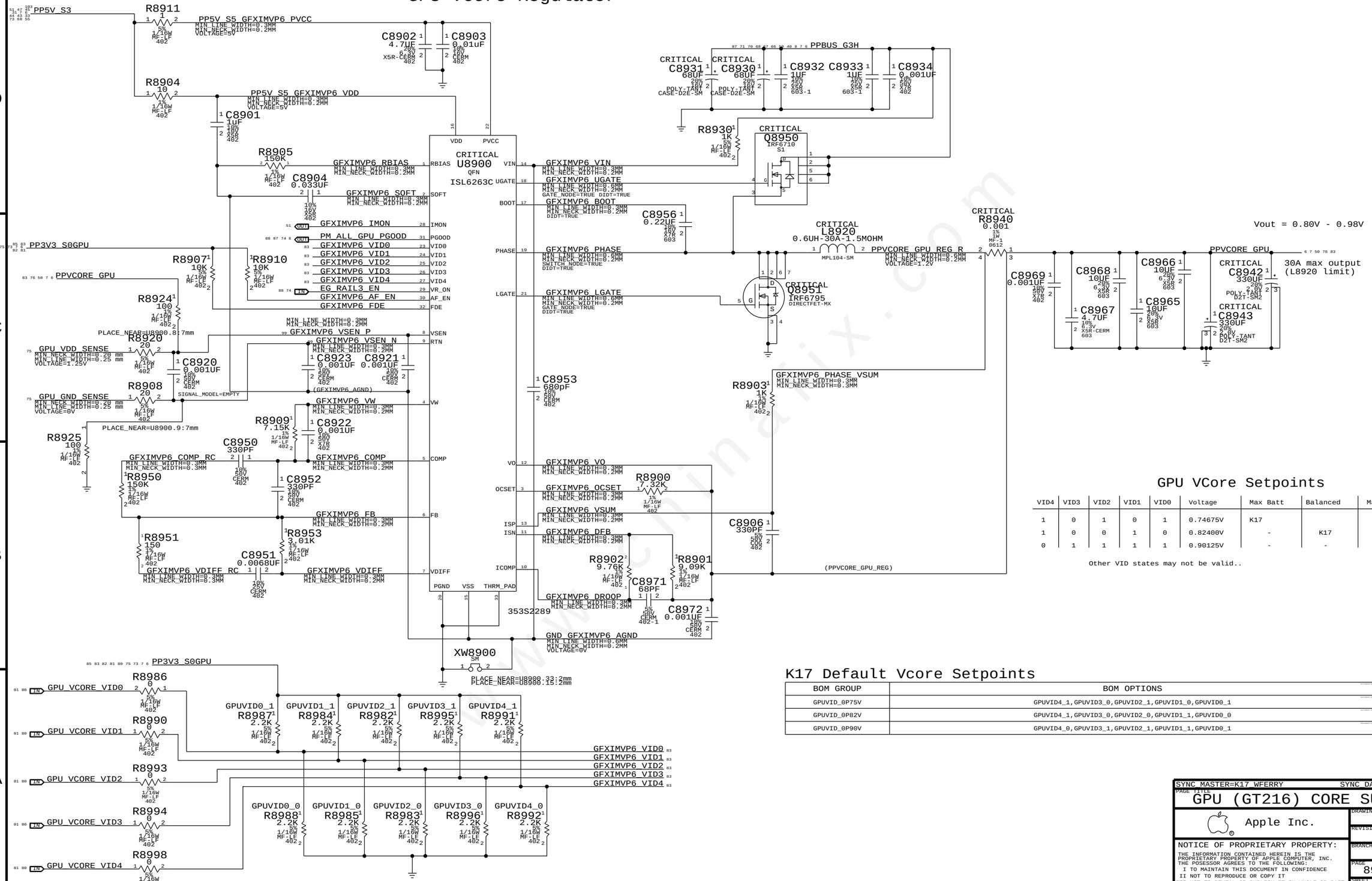
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K17		-
1	0	0	1	0	0.82400V	-	K17	-
0	1	1	1	1	0.90125V	-	-	K17

Other VID states may not be valid..

K17 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1,GPUVID3_0,GPUVID2_1,GPUVID1_0,GPUVID0_1
GPUVID_0P82V	GPUVID4_1,GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_0P90V	GPUVID4_0,GPUVID3_1,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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GPU (GT216) CORE SUPPLY

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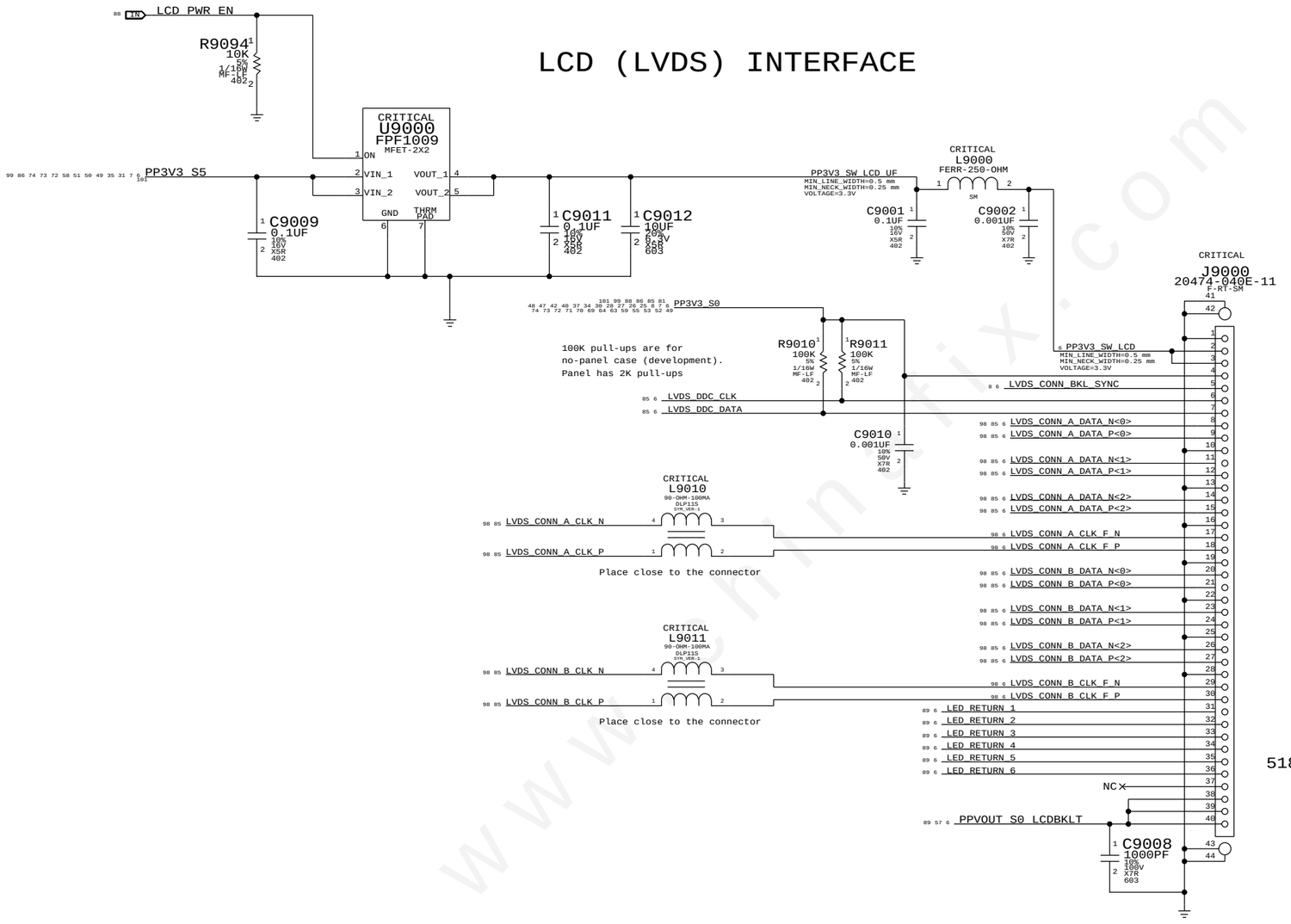
LCD (LVDS) INTERFACE



518S0651

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

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LVDS Display Connector

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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9320 357 1% 1/10W MF-LF 402
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9322 357 1% 1/10W MF-LF 402
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

PLACE_NEAR=U9600.A8:7mm
R9325 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>

PLACE_NEAR=U9600.B9:7mm
R9327 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

PLACE_NEAR=U9600.A9:7mm
R9330 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>

PLACE_NEAR=U9600.C10:7mm
R9332 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

PLACE_NEAR=U9600.B10:7mm
R9335 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>

PLACE_NEAR=U9600.A10:7mm
R9337 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

PLACE_NEAR=U9600.C8:7mm
R9340 357 1% 1/10W MF-LF 402
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P

PLACE_NEAR=U9600.C9:7mm
R9342 357 1% 1/10W MF-LF 402
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

PLACE_NEAR=U9600.A2:7mm
R9345 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>

PLACE_NEAR=U9600.A3:7mm
R9347 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

PLACE_NEAR=U9600.A1:7mm
R9350 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>

PLACE_NEAR=U9600.B3:7mm
R9352 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

PLACE_NEAR=U9600.C5:7mm
R9355 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>

PLACE_NEAR=U9600.A5:7mm
R9357 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>

DisplayPort Mux

PP3V3_S0

U9320 CBTL06141EE BGA CRITICAL

DP_IG_ML_P<0> → DIN1_0+ (B4) → DOUT_0+ (B2) → DP_ML_P<0>
DP_IG_ML_N<0> → DIN1_0- (A4) → DOUT_0- (B1) → DP_ML_N<0>
DP_IG_ML_P<1> → DIN1_1+ (B5) → DOUT_1+ (D2) → DP_ML_P<1>
DP_IG_ML_N<1> → DIN1_1- (A5) → DOUT_1- (D1) → DP_ML_N<1>
DP_IG_ML_P<2> → DIN1_2+ (B6) → DOUT_2+ (E2) → DP_ML_P<2>
DP_IG_ML_N<2> → DIN1_2- (A6) → DOUT_2- (E1) → DP_ML_N<2>
DP_IG_ML_P<3> → DIN1_3+ (A8) → DOUT_3+ (F2) → DP_ML_P<3>
DP_IG_ML_N<3> → DIN1_3- (A9) → DOUT_3- (F1) → DP_ML_N<3>

DP_IG_AUX_CH_P → C9330 0.1uF 10% 16V X5R 402 → DAUX1+ (H9) → AUX+ (H2) → DP_AUX_CH_C_P
DP_IG_AUX_CH_N → C9331 0.1uF 10% 16V X5R 402 → DAUX1- (J9) → AUX- (H1) → DP_AUX_CH_C_N

DP_IG_DDC_CLK → DDC_CLK1 (H8)
DP_IG_DDC_DATA → DDC_DAT1 (J8)

DP_IG_HPD → R9304 100K 5% 1/10W MF-LF 402 → HPD_1 (J2)

DP_EG_ML_P<0> → DIN2_0+ (B8)
DP_EG_ML_N<0> → DIN2_0- (B9)
DP_EG_ML_P<1> → DIN2_1+ (D8)
DP_EG_ML_N<1> → DIN2_1- (D9)
DP_EG_ML_P<2> → DIN2_2+ (E8)
DP_EG_ML_N<2> → DIN2_2- (E9)
DP_EG_ML_P<3> → DIN2_3+ (F8)
DP_EG_ML_N<3> → DIN2_3- (F9)

DP_EG_AUX_CH_P → C9335 0.1uF 10% 16V X5R 402 → DAUX2+ (H6)
DP_EG_AUX_CH_N → C9336 0.1uF 10% 16V X5R 402 → DAUX2- (J6)

DP_EG_DDC_CLK → DDC_CLK2 (H5)
DP_EG_DDC_DATA → DDC_DAT2 (J5)

DP_EG_HPD → R9305 100K 5% 1/10W MF-LF 402 → HPD_2 (H3)

LO=PORT1 HI=PORT2

DP_MUX_SEL_EG → GPU_SEL (A1)
DP_MUX_XSD_L → XSD* (B7)

LO=AUX_CH HI=DDC
DDC_AUX_SEL (C2) → DP_CA_DET

TST0 (G2)

HPDIN (J1) ← DP_HPD_R ← R9307 1K 5% 1/10W MF-LF 402 ← DP_HOTPLUG_DET

DPMUX_EN_HPD → R9301 10K 5% 1/10W MF-LF 402 → PP3V3_S0
DPMUX_EN_HPD → C9301 1UF 10% 6.3V CERM-X5R 402 → GND

PP3V3_S0 → DPMUX_EN_S0&DPMUX_EN_PLD → R9302 10K 1% 1/10W MF-LF 402 → DPMUX_EN_PLD
DPMUX_EN_PLD → R9303 0 5% 1/10W MF-LF 402 → DP_MUX_EN

DP_HOTPLUG_DET (OUT) MAKE_BASE=TRUE

VDD: C9320 0.1UF 20% 16V CERM 402; C9321 0.1UF 20% 16V CERM 402

PLACE_NEAR=U9320.J1:3mm

LVDS DDC MUX

PP3V3_S0GPU

R9370 20K 5% 1/10W MF-LF 402
R9371 20K 5% 1/10W MF-LF 402
R9372 20K 5% 1/10W MF-LF 402
R9373 20K 5% 1/10W MF-LF 402

C9370 0.1UF 20% 16V CERM 402

U9370 SN74LV4066A QFN1

LVDS_DDC_SEL_EG → C1
LVDS_DDC_SEL_IG → C2
C3
C4
GND THRM

A1 ↔ LVDS_EG_DDC_CLK
B1 ↔ LVDS_DDC_CLK
A2 ↔ LVDS_IG_DDC_CLK
B2 ↔ LVDS_EG_DDC_DATA
A3 ↔ LVDS_IG_DDC_DATA
B3 ↔ LVDS_DDC_DATA
A4
B4

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Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23

PP3V3_S5 → IN
PM_SLP_S3_L → EN
OC* → TP_DPPWR_OC_L
GND

PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

L9400
FERR-120-OHM-3A
0603

PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

C9400 0.01UF 20% 50V CERM 603

C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 16V CERM 402
C9485 0.1UF 20% 16V CERM 402
CRITICAL
C9486 22UF 20% 6.3V X5R 603
CRITICAL
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

R9420 100K 5% 1/16W MF-LF 402

ESD_HOT=TRUE
HDMI_CEC

R9425 1M 5% 1/16W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402

CRITICAL
FL9403
12-OHM-100MA
TCM1210-4SM

DP_ML_P<3> → C9414 0.1uF → DP_ML_C_P<3>
DP_ML_N<3> → C9415 0.1uF → DP_ML_C_N<3>
DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
	HOT_PLUG_DETECT	GND
	CONFIG1	ML_LANE0P
	CONFIG2	ML_LANE0N
	GND	GND
	ML_LANE3P	ML_LANE1P
	ML_LANE3N	ML_LANE1N
	GND	GND
	AUX_CHP	ML_LANE2P
	AUX_CHN	ML_LANE2N
	DP_PWR	RETURN

SHIELD PINS
514-0637

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402
R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402

CRITICAL
FL9400
12-OHM-100MA
TCM1210-4SM

FL9401
12-OHM-100MA
TCM1210-4SM

CRITICAL
FL9402
12-OHM-100MA
TCM1210-4SM

DP_ML_CONN_P<0> → DP_ML_C_P<0> → C9410 0.1uF → DP_ML_P<0>
DP_ML_CONN_N<0> → DP_ML_C_N<0> → C9411 0.1uF → DP_ML_N<0>
DP_ML_CONN_P<1> → DP_ML_C_P<1> → C9412 0.1uF → DP_ML_P<1>
DP_ML_CONN_N<1> → DP_ML_C_N<1> → C9413 0.1uF → DP_ML_N<1>
DP_ML_CONN_P<2> → DP_ML_C_P<2> → C9416 0.1uF → DP_ML_P<2>
DP_ML_CONN_N<2> → DP_ML_C_N<2> → C9417 0.1uF → DP_ML_N<2>

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

PP3V3_S0

R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

R9421 100K 5% 1/16W MF-LF 402

R9422 1M 5% 1/16W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

PP3V3_S0

R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HOTPLUG_DET
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/16W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

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DisplayPort Connector

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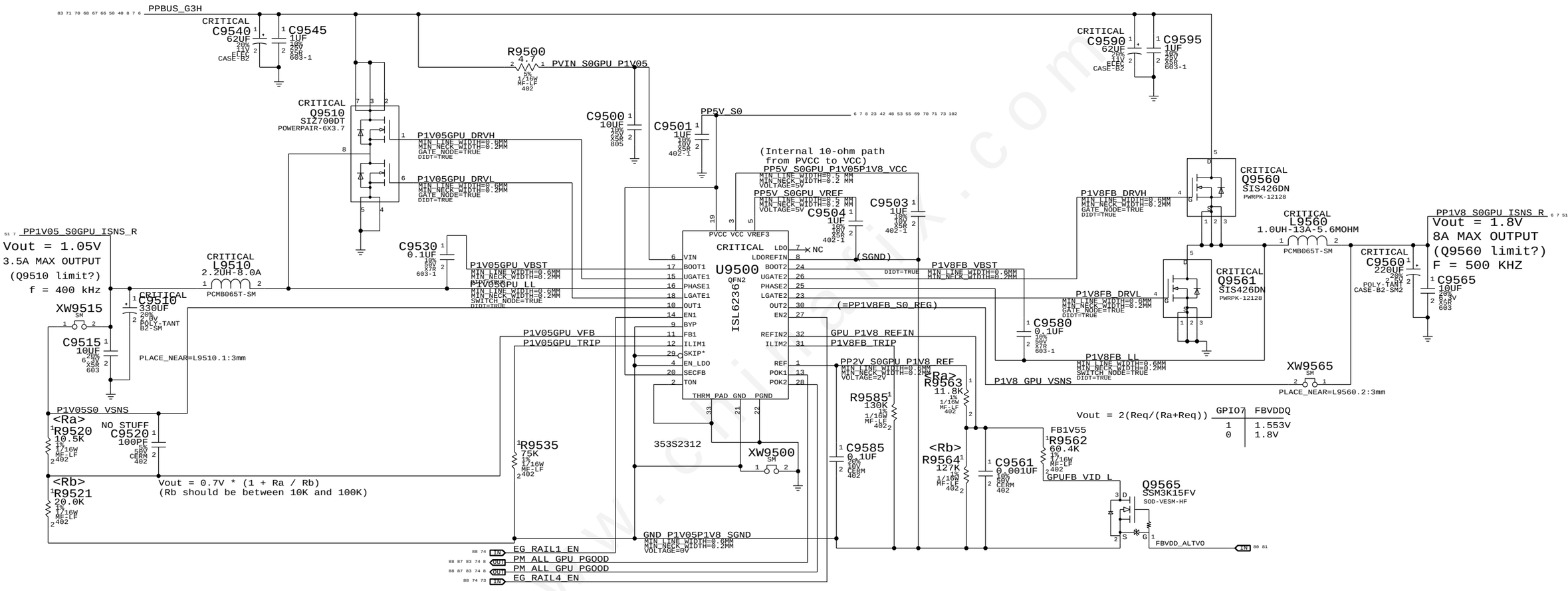

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0362	1	RES,1/16W,30.9K,1%,0402,LF	R9562		FB1V35

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GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.E12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

All: 1% 1/16W MF-LF 402

Required Pullups

SIGNAL_MODEL=EMPTY

PP3V3_S0

EG_PWRSEQ_EN	R9684	1K	5% 1/16W MF-LF 402
GMUX_DEBUG_RESET_L	R9680	1K	5% 1/16W MF-LF 402

NO STUFF
R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402
EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

PP3V3_S0 → R9600 0 5% 1/16W MF-LF 402

C9610 0.1UF 20% 10V X5R 402
C9621 0.1UF 20% 10V CERM 402
C9622 0.1UF 20% 10V CERM 402
C9623 0.1UF 20% 10V CERM 402
C9624 0.1UF 20% 10V CERM 402
C9625 0.1UF 20% 10V CERM 402
C9626 0.1UF 20% 10V CERM 402
C9627 0.1UF 20% 10V CERM 402
C9628 0.1UF 20% 10V CERM 402
C9629 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

PP1V8_S0 → R9610 0 5% 1/16W MF-LF 402

C9611 0.1UF 20% 10V X5R 402
C9612 0.1UF 20% 10V CERM 402
C9613 0.1UF 20% 10V CERM 402
C9614 0.1UF 20% 10V CERM 402
C9615 0.1UF 20% 10V CERM 402
C9616 0.1UF 20% 10V CERM 402
C9617 0.1UF 20% 10V CERM 402

PP1V8_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=1.8V

PP1V2_S0

C9600 4.7UF 20% 10V X5R 402
C9604 0.1UF 20% 10V CERM 402
C9605 0.1UF 20% 10V CERM 402
C9606 0.1UF 20% 10V CERM 402
C9607 0.1UF 20% 10V CERM 402
C9608 0.1UF 20% 10V CERM 402
C9609 0.1UF 20% 10V CERM 402

PP3V3_S0 → R9640 10K 1% 1/16W MF-LF 402
PP3V3_S0 → R9645 10K 1% 1/16W MF-LF 402

NO STUFF R9641 10K 1% 1/16W MF-LF 402
NO STUFF R9646 10K 1% 1/16W MF-LF 402

CRITICAL
J9600 1909782 M-RT-SM
GMUX_JTAG_CONN

1	PP3V3_S0
2	JTAG_GMUX_TDO
3	JTAG_GMUX_TDI
4	JTAG_GMUX_TMS
6	JTAG_GMUX_TCK

NO STUFF R9647 10K 1% 1/16W MF-LF 402

PP1V8_S0 → R9611 0 5% 1/16W MF-LF 402 → PP3V3R1V8_S0_GMUX
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

GMUXPLL_3V3
PP3V3_S0 → R9612 0 5% 1/16W MF-LF 402

L9621 FERR-220-OHM 0402
PP3V3R1V8_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C9631 0.1UF 20% 10V CERM 402

L9620 FERR-220-OHM 0402
PP3V3R1V8_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C9630 0.1UF 20% 10V CERM 402

U9600 XP25-5 CSBGA
OMIT CRITICAL

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO06 B5
VCCIO01 B7
VCCIO02 A12
VCCIO03 C14
VCCIO04 F13
VCCIO05 M12
VCCIO06 M9
VCCIO07 M3
VCCJ N5
ULC_VCCPLL M1
LRC_VCCPLL C3
K12 F2
A4
P11

JTAG_GMUX_TCK	K14	TCK
JTAG_GMUX_TDI	L13	TDI
JTAG_GMUX_TDO	K13	TDO
JTAG_GMUX_TMS	L12	TMS
GMUX_TOE	K2	TOE
GMUX_CFG0	K1	CFG0

BANK5

OUT LCD_BKLT_EN	P2	PB7A
OUT LCD_BKLT_PWM	N2	PB7B
OUT LVDS_DDC_SEL_EG	P4	PB14A
OUT LVDS_DDC_SEL_IG	N4	PB14B
OUT DP_MUX_EN	N3	PB15A (OD)
OUT DP_MUX_SEL_EG	M4	PB15B
OUT EG_RESET_L	P5	PB16A
OUT EG_RAIL1_EN	M5	PB16B
OUT EG_RAIL2_EN	P6	PB17A
OUT EG_RAIL3_EN	M6	PB17B
OUT EG_RAIL4_EN	P7	PB18A
OUT PEG_CLKREQ_L	M7	PB18B (OD)
OUT DP_CA_DET_EG	N7	PB19A
OUT LCD_PWR_EN	N8	PB19B

BANK4

OUT LPC_AD<0>	P9	PB20A
OUT LPC_AD<1>	N9	PB20B
OUT LPC_AD<2>	P10	PB26A
OUT LPC_AD<3>	M10	PB26B
IN LPC_FRAME_L	P12	PB27A
IN LPCPLUS_RESET_L	P13	PB27B
IN LPC_CLK33M_GMUX	N12	PB28A
OUT GMUX_INT	P14	PB28B

BANK7

IN LVDS_IG_B_DATA_P<2>	B1	PL2A
IN LVDS_IG_B_DATA_N<2>	B2	PL2B
GMUX_PL6A	C2	PL6A
TP_GMUX_PL6B	D3	PL6B
IN LVDS_IG_A_DATA_P<0>	D1	PL7A
IN LVDS_IG_A_DATA_N<0>	E1	PL7B
IN LVDS_IG_A_DATA_P<1>	D2	PL8A
IN LVDS_IG_A_DATA_N<1>	E3	PL8B
IN LVDS_IG_A_DATA_P<2>	F1	PL9A
IN LVDS_IG_A_DATA_N<2>	G1	PL9B
IN LVDS_IG_B_DATA_P<0>	F3	PL10A
IN LVDS_IG_B_DATA_N<0>	G2	PL10B
IN LVDS_IG_B_DATA_P<1>	H2	PL11A
IN LVDS_IG_B_DATA_N<1>	G3	PL11B
IN LVDS_IG_A_CLK_P	H1	PL12A
IN LVDS_IG_A_CLK_N	H3	PL12B
OUT TP_LVDS_MUX_SEL_EG	L1	PL14A
TP_GMUX_PL14B	L3	PL14B
GMUX_RESET_L	K3	PL15A
OUT GMUX_VSYNC	L2	PL15B
PM_ALL_GPU_PGOOD	N1	PL25A
IN PEX_CLKREQ_L	P1	PL25B

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

BANK6

PT7A	A2	LVDS_B_DATA_P<0>
PT7B	A3	LVDS_B_DATA_N<0>
PT8A	A1	LVDS_B_DATA_P<1>
PT8B	B3	LVDS_B_DATA_N<1>
PT9A	C5	LVDS_B_DATA_P<2>
PT9B	A5	LVDS_B_DATA_N<2>
PT14A	B6	EG_PWRSEQ_EN
PT14B	C7	GMUX_DEBUG_RESET_L
PT15A	A6	LVDS_A_CLK_P
PT15B	A7	LVDS_A_CLK_N
PT16A	C8	LVDS_B_CLK_P
PT16B	C9	LVDS_B_CLK_N
PT17A	A8	LVDS_A_DATA_P<0>
PT17B	B9	LVDS_A_DATA_N<0>
PT18A	A9	LVDS_A_DATA_P<1>
PT18B	C10	LVDS_A_DATA_N<1>
PT19A	B10	LVDS_A_DATA_P<2>
PT19B	A10	LVDS_A_DATA_N<2>
PT20A	A11	GND
PT20B	B12	GND
PT28A	B13	GND
PT28B	A13	GND

BANK1

BANK2

PR2A	A14	DP_CA_DET
PR2B	B14	DP_HOTPLUG_DET
PR6A	D12	LVDS_EG_A_DATA_P<0>
PR6B	D13	LVDS_EG_A_DATA_N<0>
PR7A	D14	LVDS_EG_A_DATA_P<1>
PR7B	E14	LVDS_EG_A_DATA_N<1>
PR8A	E12	LVDS_EG_A_DATA_P<2>
PR8B	F12	LVDS_EG_A_DATA_N<2>
PR9A	F14	LVDS_EG_B_DATA_P<0>
PR9B	G14	LVDS_EG_B_DATA_N<0>
PR10A	G12	LVDS_EG_B_DATA_P<1>
PR10B	G13	LVDS_EG_B_DATA_N<1>
PR11A	H13	LVDS_EG_B_DATA_P<2>
PR11B	H12	LVDS_EG_B_DATA_N<2>
PR12A	H14	LVDS_EG_A_CLK_P
PR12B	J12	LVDS_EG_A_CLK_N

BANK3

PR14A	L14	LVDS_IG_PANEL_PWR
PR14B	M13	EG_LCD_PWR_EN
PR24A	N14	LVDS_IG_BKL_ON
PR24B	N13	EG_BKLT_EN

GND: J1 B8 C6 C12 C13 G13 M14 N10 N6 P3 M2 C1 E2 B4 M11

GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PP3V3_S3 → R9676 100K 5% 1/16W MF-LF 2402 → GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563

ALL_SYS_PWRGD

EG_RAIL1_EN
EG_RAIL2_EN
EG_RAIL3_EN
EG_RAIL4_EN
LCD_PWR_EN

R9678 4.7K 5% 1/16W MF-LF 402
R9671 4.7K 5% 1/16W MF-LF 2402
R9672 4.7K 5% 1/16W MF-LF 2402
R9673 4.7K 5% 1/16W MF-LF 2402
R9674 4.7K 5% 1/16W MF-LF 2402

GMUX_S3_PD_GND

NO STUFF R9675 0 5% 1/16W MF-LF 2402

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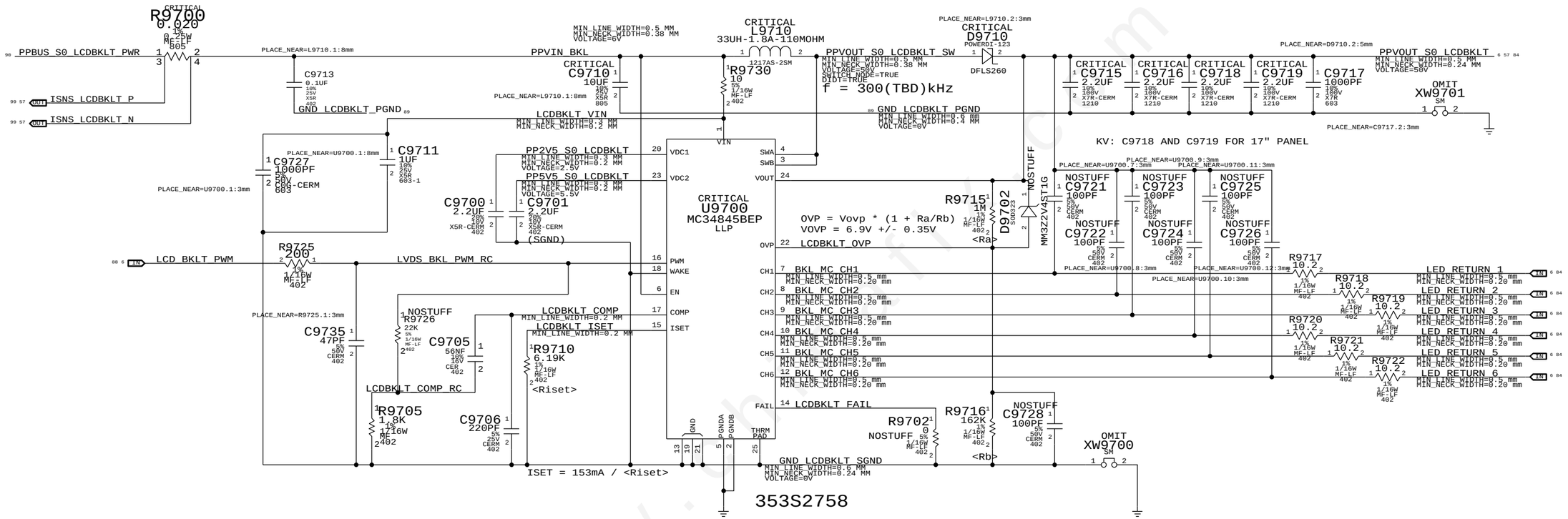

17 Inch Panel (14 LEDs per string)

Target: ISET = 25mA, OVP = 50V
ACTUAL: ISET = 24.7mA, OVP = 49.5V

KV: WAKE AND EN WIRING CHANGED FROM REF SCHEMATIC AS QFET IS PRESENT ON P.98

PLACEMENT_NOTE=PLACE XW9700 FAR FROM THE NOISY PINS 3 AND 4

SYNC_MASTER=K17_VEMURI SYNC_DATE=12/16/2009

PAGE TITLE: LCD Backlight Driver (MC34845)

Apple Inc.

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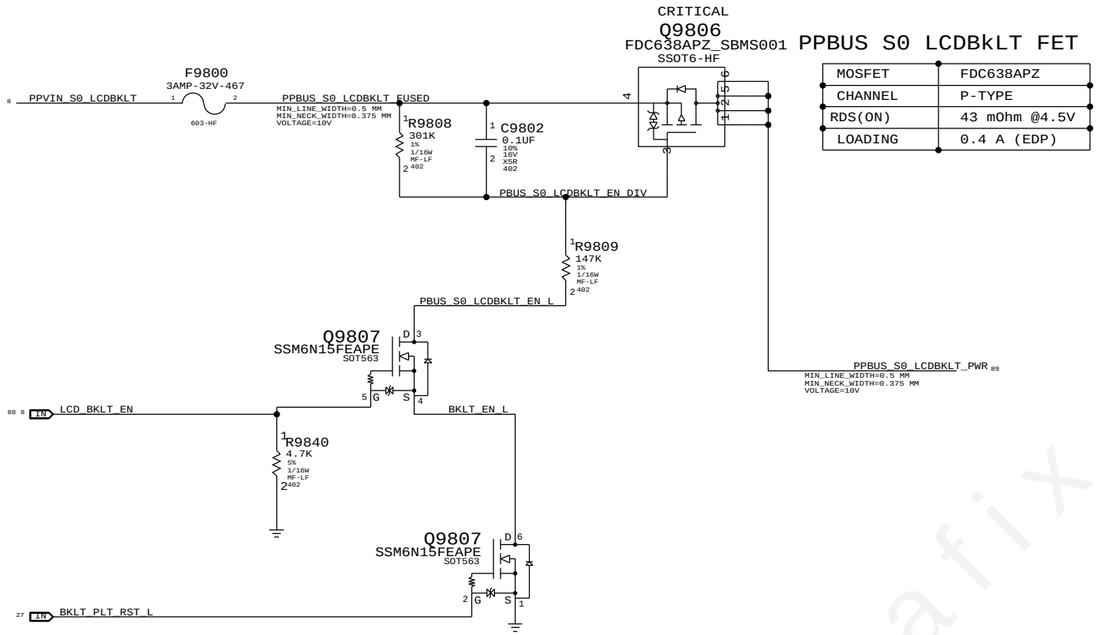

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTS0_PGOOD	10 71
XDP_XPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 47
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 47
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 47 69
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 47
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 69
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	12 15 69
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 70
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	13 70
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 70
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 70
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	75
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	75
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 75
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 9 75
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	75
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	75

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0> 11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4> 11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7> 11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 11 29 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0> 11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4> 11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7> 11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 11 29

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Memory Constraints

Apple Inc.

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8 85
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 18 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 18 85
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 88
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAP<3>	8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAN<3>	8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 42
	SATA_90D	SATA	SATA_HDD_D2R_N	17 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	17 42
	SATA_90D	SATA	SATA_ODD_D2R_N	17 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	42
SATA_EXTA_R2D	SATA_90D	SATA	TP_SATA_EXTA_R2D_C_P	8 17
	SATA_90D	SATA	TP_SATA_EXTA_R2D_C_N	8 17
SATA_EXTA_D2R	SATA_90D	SATA	TP_SATA_EXTA_D2R_P	8 17
	SATA_90D	SATA	TP_SATA_EXTA_D2R_N	8 17
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATA_ICOMP	
USB_EXTA	USB_85D	USB	USB_EXTA_P	36 43
	USB_85D	USB	USB_EXTA_N	36 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	35 43
	USB_85D	USB	USB_EXTB_N	35 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	35 44
	USB_85D	USB	USB_EXTC_N	35 44
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	19 36
	USB_85D	USB	USB_HUB2_UP_N	19 36
USB_MINI	USB_85D	USB	NC_USB_MINIP	6
	USB_85D	USB	NC_USB_MININ	6
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	19 35
	USB_85D	USB	USB_HUB1_UP_N	19 35
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	33 35
	USB_85D	USB	USB_CAMERA_N	33 35
USB_BT	USB_85D	USB	USB_BT_P	33 36
	USB_85D	USB	USB_BT_N	33 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	36 54
	USB_85D	USB	USB_TPAD_N	36 54
USB_IR	USB_85D	USB	USB_IR_P	35 45
	USB_85D	USB	USB_IR_N	35 45
USB_EXCARD	USB_85D	USB	USB_EXCARD_P	8 34 36
	USB_85D	USB	USB_EXCARD_N	8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	19 103
	USB_85D	USB	USB_BRCRYPT_N	19 103
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	19
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17 26
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17 26
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17 26
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 46 48 88
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 46 48 88
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 48 88
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 46
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 48
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	6 17 25 26 28 30 32 34 42 48 49 64
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	6 17 25 26 28 30 32 34 42 48 49 64
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 49
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 49
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 49
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 49
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 59
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 59
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 59
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 59
	HDA_50S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 59
	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 47
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 48
	SPI_55S	SPI	SPI_CLK	48
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 48
	SPI_55S	SPI	SPI_MOSI	48
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 48
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 48
	SPI_55S	SPI	SPI_CS0_L	48
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_P	6 34
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_N	6 34
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	17 34
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	17 34
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 17 34
	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 17 34
MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 75
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 75
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 34
1231	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20
1232	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20
1237	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20
1238	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20
1239	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
1240	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
1241	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20
1242	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20
1243	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20
1244	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20
1245	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20
1246	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20
1247	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	20
1248	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20
1249	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20
1250	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20
1251 PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
1252	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
1253 PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
1254	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	27 37
	ENET_50S	ENET_3X	ENET_RESET_L	27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP 6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP 6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN 6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P 39 40 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N 39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P 39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N 39 40 41
Port 2 Not Used			

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 33 46 49 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 33 46 49 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 46 49 52
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 46 49 52
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 46 49 65 66
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 46 49 65 66
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 46 49 57 102
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 46 49 57 102

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 66
	1TO1_DIFFPAIR		CHGR_CSI_N 66
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 66
	1TO1_DIFFPAIR		CHGR_CSO_N 66

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE
U20G FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE
U20G FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DATA0)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>
U20F LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>
U20H LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>
U20H LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_P<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_N<3..0>
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_N

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J14G LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P
J14G LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N
J15G LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>
J15G LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>
J15F LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P
J15F LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N
J20F LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>
J20G LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>
J13J	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P
J13J	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N
J13K	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P
J13K	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N
J13G	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P
J13F	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N
J13D	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>
J13C	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>
J13H	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P
J13G	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N
J13E	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>
J13D	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>
J15J DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_P<3..0>
J15G	DP_85D	DISPLAYPORT	DP_ML_C_N<3..0>
J15J DP_ML	DP_85D	DISPLAYPORT	DP_ML_P<3..0>
J15J	DP_85D	DISPLAYPORT	DP_ML_N<3..0>
J20G DP_ML	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>
J20F	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>
J15H DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_P
J15H DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K17 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
	SATA_90D	SATA	SATA_ODD_R2D_UF_P	42
	SATA_90D	SATA	SATA_ODD_R2D_UF_N	42
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_R2D_UF_P	42
	SATA_90D	SATA	SATA_HDD_R2D_UF_N	42
L30D	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P	42
L30C	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N	42
L30F	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P	42
L30E	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N	42
L30H	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P	42
L31D	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N	42
L31F	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P	42
L31E	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N	42
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	52
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	52
L28J	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 52
L28K	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 52
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	52
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	52
	THERM_1TO1_55S	THERM	GPU_TDIODE_P	52 80 81
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	52 80 81
	SENSE_1TO1_55S	THERM	ISNS_3V3_S3_R_P	102
	SENSE_1TO1_55S	THERM	ISNS_3V3_S3_R_N	102
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	33 57 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	33 57 99
	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	57
	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	57
	SENSE_1TO1_55S	SENSE	GPUISENS_P	51
	SENSE_1TO1_55S	SENSE	GPUISENS_N	51
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	33 57 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	33 57 99
	SENSE_1TO1_55S	SENSE	DDRISNS_P	57
	SENSE_1TO1_55S	SENSE	DDRISNS_N	57
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	51
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	51
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	50
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	51
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	51
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	42 57
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	42 57
L24J	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	57
L25C	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	57
L24F	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	57
L25E	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	57
L25F	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	42 57
L25G	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	42 57
L25K	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	57 89
L25L	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	57 89
L23K	SENSE_1TO1_55S	SENSE	NC_ISNS_P1V05S0PCH_P	8 50
L24C	SENSE_1TO1_55S	SENSE	NC_ISNS_P1V05S0PCH_N	8 50
L23H	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	71
L23J	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	71
L23G	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_R_P	71
L23F	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_R_N	71
L23D	SENSE_1TO1_55S	SENSE	NC_ISNS_P3V3S0MPCH_P	8 102
L23E	SENSE_1TO1_55S	SENSE	NC_ISNS_P3V3S0MPCH_N	8 102
L25B	SENSE_1TO1_55S	SENSE	ISNS_P3V3S0MPCH_R_P	102
L26C	SENSE_1TO1_55S	SENSE	ISNS_P3V3S0MPCH_R_N	102
L29J	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_P	70
L29K	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_N	70
L29F	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_P	50 70
L29H	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_N	50 70
L27J	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_R_P	102
L27K	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_R_N	102
L27G	SENSE_1TO1_55S	SENSE	NC_ISNS_PVTTS0PCH_P	8 102
L27H	SENSE_1TO1_55S	SENSE	NC_ISNS_PVTTS0PCH_N	8 102
L27E	SENSE_1TO1_55S	SENSE	ISNS_PVTTS0PCH_R_P	102
L27D	SENSE_1TO1_55S	SENSE	ISNS_PVTTS0PCH_R_N	102
L27J	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_P	51
L27K	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_N	51
L27B	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	102
L28C	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	102
L28B	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_P	51
L28D	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_N	51
L28F	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_P	102
L28G	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_N	102
L28H	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_P	51
L28K	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_N	51
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	51 68
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	51 68
	SENSE_1TO1_55S	THERM	ISNS_1V5_S3_R_P	51
	SENSE_1TO1_55S	THERM	ISNS_1V5_S3_R_N	51
L29J	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	57
L29K	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	57
L30J	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	83
L30K	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	83
L30D	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_P	50
L30C	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_N	50

K17 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 33
	1TO1_DIFFPAIR		CHGR_CSI_R_P	66
	1TO1_DIFFPAIR		CHGR_CSI_R_N	66
	1TO1_DIFFPAIR		CHGR_CSO_R_P	59 66
	1TO1_DIFFPAIR		CHGR_CSO_R_N	59 66
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 43
(USB_EXTD)	USB_85D	USB	USB_BRCRYPT_CONN_P	
(USB_EXTD)	USB_85D	USB	USB_BRCRYPT_CONN_N	
(USB_CAMERA)	USB_85D	USB	USB_CAMERA_CONN_P	6 33
(USB_CAMERA)	USB_85D	USB	USB_CAMERA_CONN_N	6 33
	USB_85D	USB	CONN_USB2_BT_P	6 33
	USB_85D	USB	CONN_USB2_BT_N	6 33
	USB_85D	USB	USB_LT2_P	6 43
	USB_85D	USB	USB_LT2_N	6 43
	USB_85D	USB	USB2_EXCARD_CONN_P	6 34
	USB_85D	USB	USB2_EXCARD_CONN_N	6 34
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	85
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	85
L31C	USB_85D	USB	USB_BRCRYPT_R_P	
L31B	USB_85D	USB	USB_BRCRYPT_R_N	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	6 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	6 34
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_FL_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_FL_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_BL_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_BL_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_FR_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_FR_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_BR_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_BR_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	6 62 63
L41C	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_C_P	62
L41B	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_C_N	62
L41F	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_C_P	62
L41E	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_C_N	62
L41G	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_C_P	62
L42J	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_C_N	62
L42H	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_C_P	62
L42G	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_C_N	62
L42D	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_C_P	62
L42C	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_C_N	62
L42K	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_L_P	62
L42L	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_L_N	62
L42F	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_L_P	62
L42E	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_L_N	62
L43K	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_L_P	62
L43J	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_L_N	62
L43H	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_L_P	62
L43G	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_L_N	62
L43D	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_L_P	62
L43C	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_L_N	62
L43F	DIFFPAIR	AUDIO	SSM2315FL_IN_P	62
L43E	DIFFPAIR	AUDIO	SSM2315FL_IN_N	62
L43J	DIFFPAIR	AUDIO	SSM2315FR_IN_P	62
L43H	DIFFPAIR	AUDIO	SSM2315FR_IN_N	62
L43K	DIFFPAIR	AUDIO	SSM2315BR_IN_P	62
L43L	DIFFPAIR	AUDIO	SSM2315BR_IN_N	62
L44K	DIFFPAIR	AUDIO	INT_MIC_F_P	63 64
L44J	DIFFPAIR	AUDIO	INT_MIC_F_N	63 64
L44F	DIFFPAIR	AUDIO	INT_MIC_P	6 63
L44E	DIFFPAIR	AUDIO	INT_MIC_N	6 63
L44G	DIFFPAIR	AUDIO	SSM2315BL_IN_P	62
L44D	DIFFPAIR	AUDIO	SSM2315BL_IN_N	62
L44J	DIFFPAIR	AUDIO	SSM2315LFE_IN_P	62
L44H	DIFFPAIR	AUDIO	SSM2315LFE_IN_N	62
	USB_85D	USB	USB_TPAD_R_P	54
	USB_85D	USB	USB_TPAD_R_N	54
	USB_85D	USB	USB_LT3_P	6 44
	USB_85D	USB	USB_LT3_N	6 44
		SB_POWER	PP3V3_S5	84 85 101 6 7 31 35 49 50 51 58 72 73 74
		SB_POWER	PP3V3_S0	69 70 71 72 73 74 81 84 85 86 6 7 8 25 26 27 28 30 34 37 40 42 47 48 49 52 53 55 59 63 64 80 101
		SB_POWER	PP1V5_S0	34 42 59 72 74
		GND	GND	

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Project Specific Constraints

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K17 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.190 MM	0.190 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?

NOTE: From T18 MLB, changed to reflect K17 mlb stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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PCH "S0" Rails

XWC100 SM
PPCPUVTT_S0 4759 mA
PP1V05_S0_PCH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0_PCH 128 mA (0 mA if PCH_VRM_YES?)
PP1V05_S0_PCH 1432 mA
PP1V05_S0_PCH 137 mA
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH 3062 mA
PP1V05_S0_PCH 1849 mA S0, 700 mA M-on

PCH "S0M" Rails

XWC110 SM
PPCPUVTT_S0 62 mA
PPVTT_S0_PCH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE OR 1.1V
PPVTT_S0_PCH < 1 mA
PPVTT_S0_PCH 61 mA (1.1V)
PPVTT_S0_PCH 58 mA (1.05V)

XWC120 SM
PP1V8_S0 250 mA
PP1V8_S0_PCH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0_PCH 59 mA
PP1V8_S0_PCH 35 mA
PCH_NAND_1V8
RC125 0 5% 1/10W MF-LF 603
PP3V3R1V8_S0_PCH_VCCPNAND
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE OR 1.8V
PP3V3R1V8_S0_PCH_VCCPNAND 156 mA (1.8V)
??? mA (3.3V)
WF: Estimate 300 mA for budget purposes
PCH_NAND_3V3
RC126 0 5% 1/10W MF-LF 603

XWC130 SM
PP3V3_S0 729 mA
PP3V3_S0_PCH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0_PCH < 1 mA
PP3V3_S0_PCH < 1 mA
PP3V3_S0_PCH
PP3V3_S0_PCH
PP3V3_S0_PCH
PP3V3_S0_PCH
PP3V3_S0_PCH
PP3V3_S0_PCH 357 mA
PP3V3_S0_PCH 69 mA

XWC135 SM
NO STUFF
RC136 0 5% 1/16W MF-LF 402
PP3V3_S0_PCH_VCCALVDS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0_PCH_VCCALVDS < 1 mA

XWC140 SM
PP3V3_S0 6 mA
PP3V3R1V5_S0_PCH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE OR 3.3V
PP3V3R1V5_S0_PCH 6 mA (3.3V)

PCH "S5" Rail

XWC150 SM
PP3V3_S5 165 mA
PP3V3_S5_PCH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5_PCH ≤1 mA S0-S5
PP3V3_S5_PCH ≤1 mA S0-S5
PP3V3_S5_PCH 163 mA S0 /
PP3V3_S5_PCH 65 mA S3-S5

XWC170 SM
PP3V3_S0 85 mA
PP3V3_S0M_PCH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0M_PCH 85 mA S0, 22 mA M-on

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

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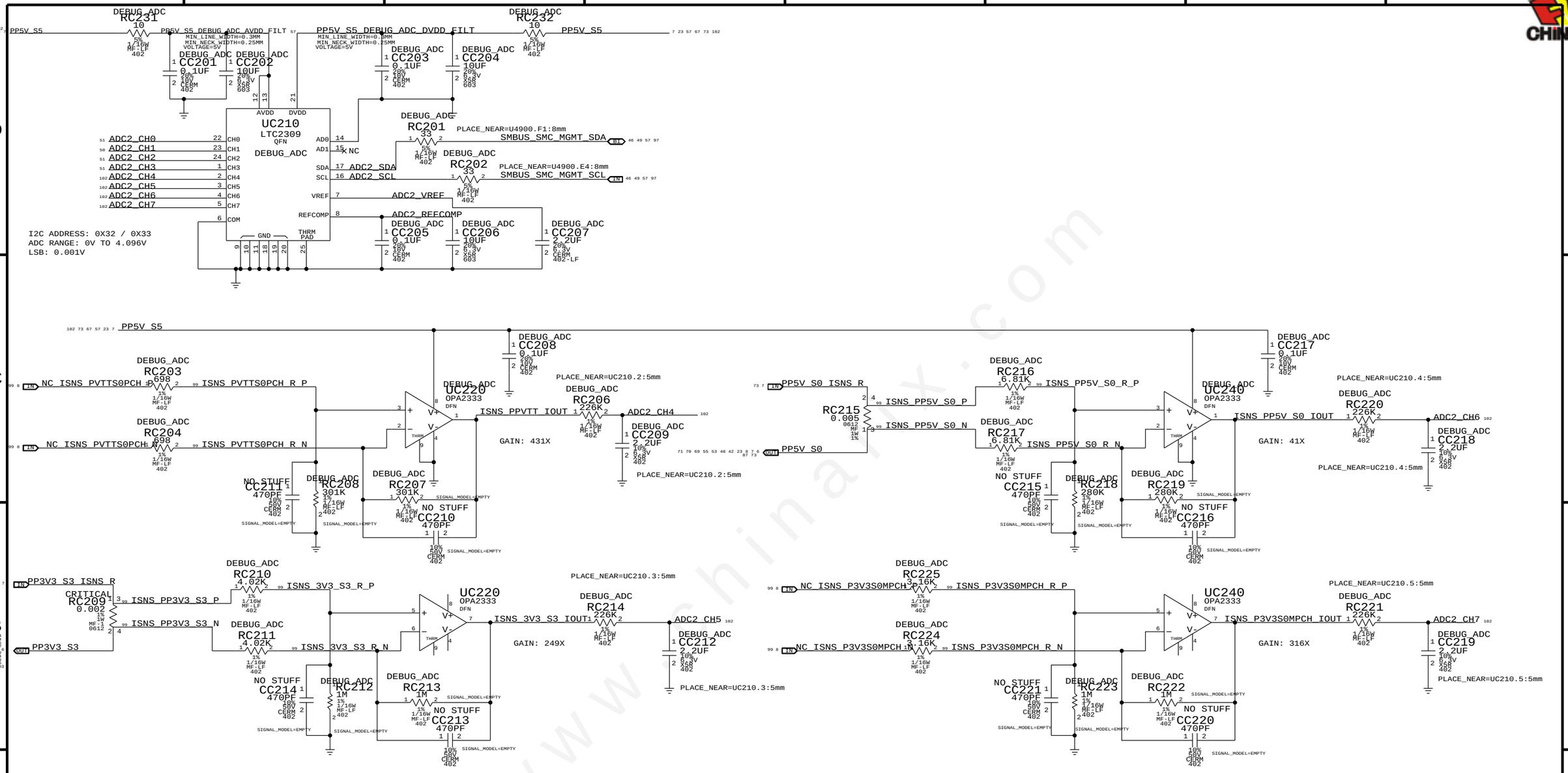

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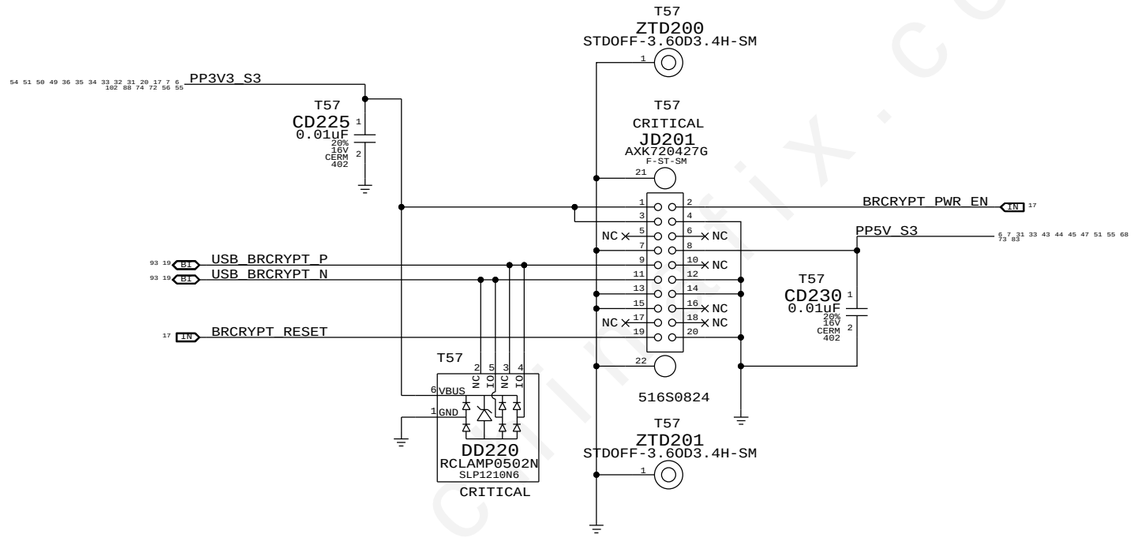

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