

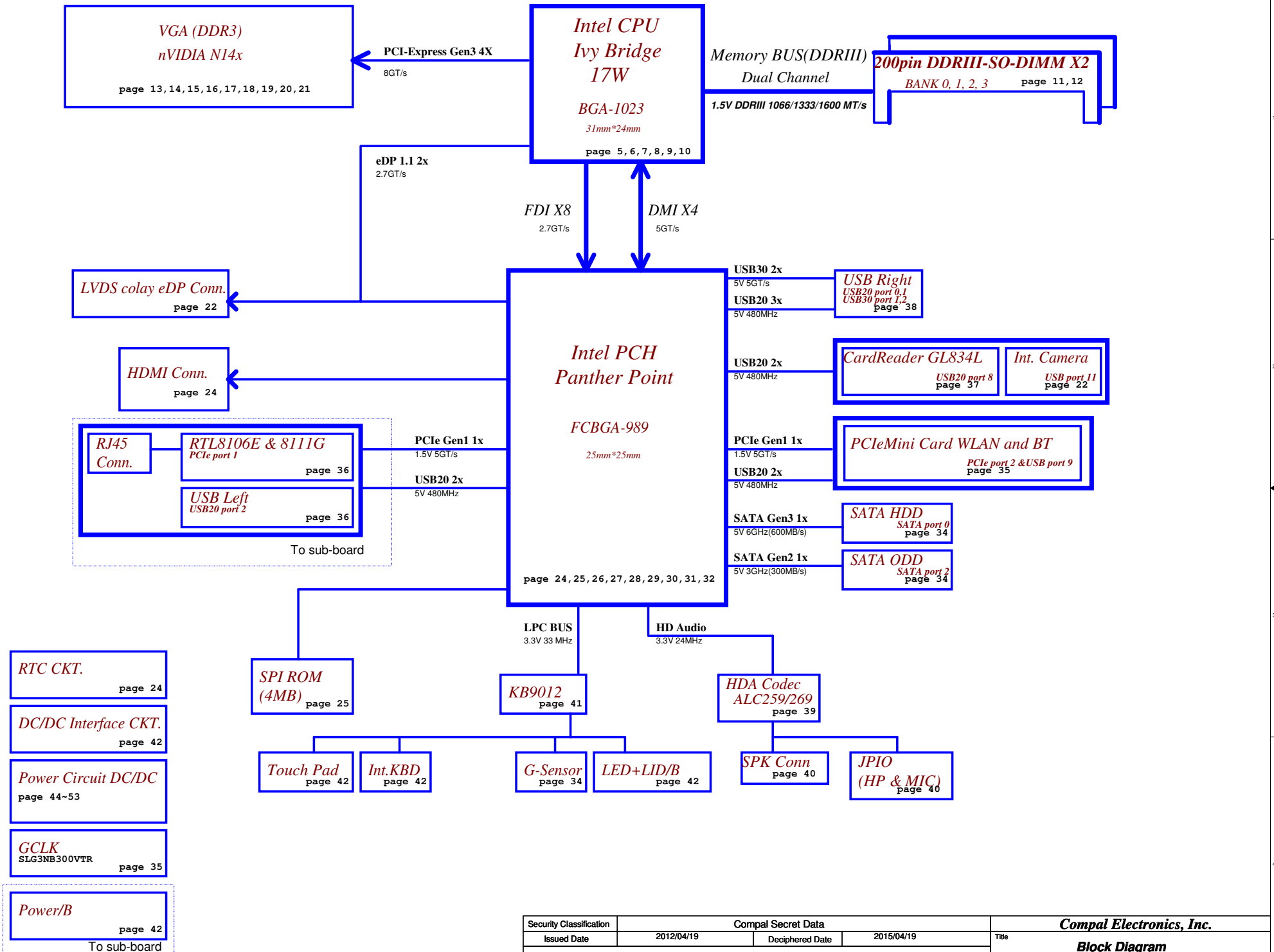
# VFKTA

## Rosetta 10FTG

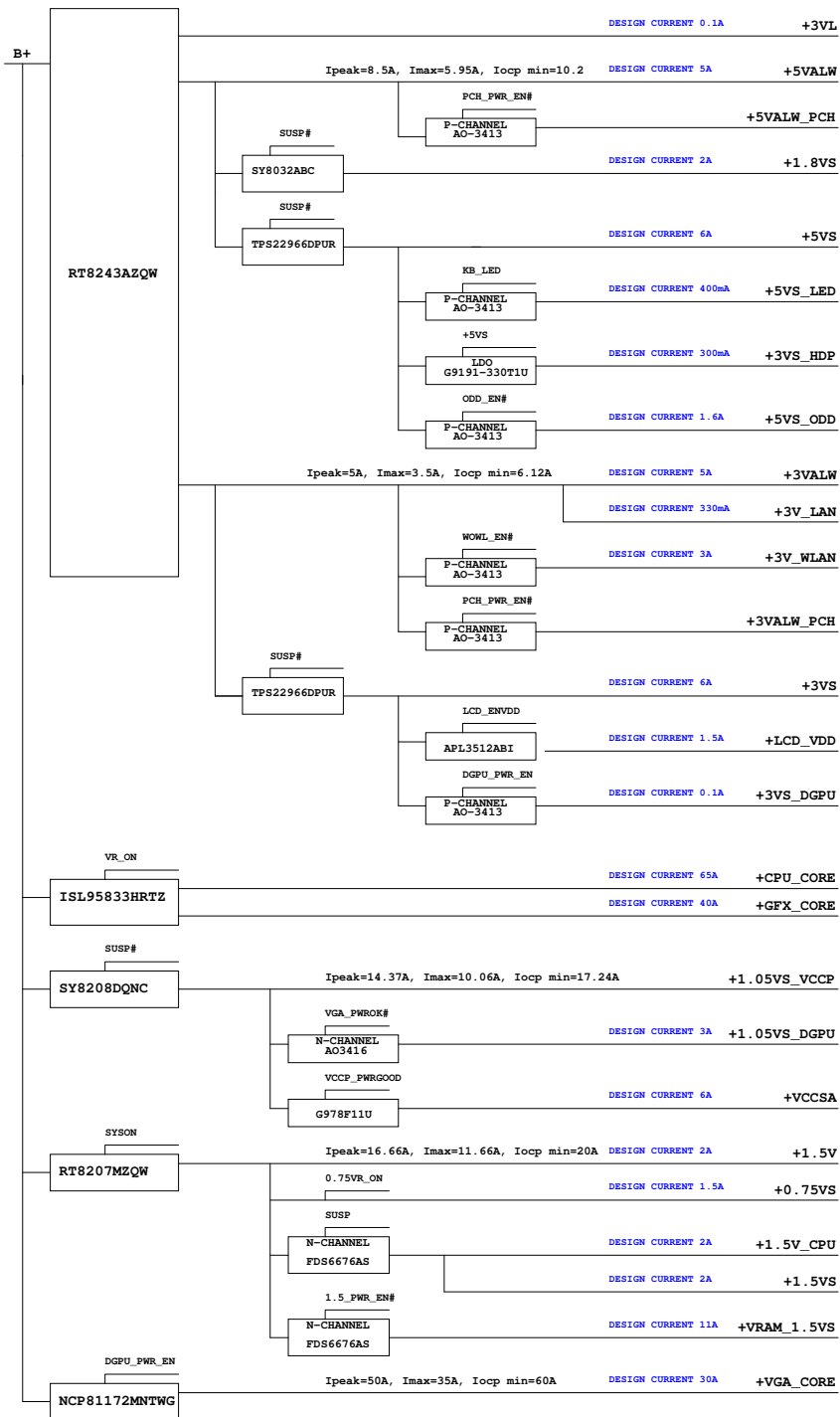
# LA-9861P REV 1.0 Schematic

Intel Processor (Ivy Bridge/Sandy Bridge)+  
PCH(Panther Point)  
2013-02-19 Rev 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	<b>Cover Page</b>
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				VFKTA	1.0
				Date: Monday, March 11, 2013	Sheet 1 of 56



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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Block Diagram	
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				VFKTA	1.0
Date: Monday, March 11, 2013				Sheet	2 of 56



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Size	1.0	Rev	1.0	Sheet 3 of 61

### Voltage Rails

( O MEANS ON X MEANS OFF )

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

### PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

### EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b
+3VL	USB S&C 14640	35 H	0011 0101 b

### EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

### BTO Option Table

Function	CPU					
description	IVB i7 3537U	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847
explain	IVB i7 3537U	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847
BTO	CPUI73537UR1@	CPUI53337UR1@	CPUI3227UR1@	CPUI32375MR1@	CPUP2117UR1@	CPUC847R1@
	CPUI73537UR3@	CPUI53337UR3@	CPUI3227UR3@	CPUI32375MR3@	CPUP2117UR3@	CPUC847R3@

Function	SKU	PCH		GPU		VRAM	EC	
description	Optimus	Panther Point		N14M-GL	N14P-GV2	Dual Rank	EC	
explain	Optimus	HM76	HM70	N14M-GL	N14P-GV2	Dual Rank	KB9012	NPCE885N
BTO	OPT@	HM76R1@	HM70R1@	N14MGL@	N14PGV2@	DRANK@	9012@	885@
		HM76R3@	HM70R3@	N14MGLR1@ N14MGLR3@	N14PGV2R1@ N14PGV2R3@			

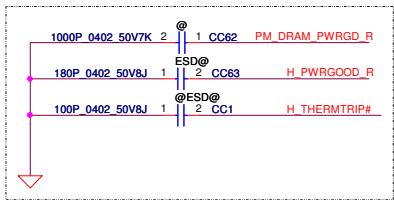
Function	LVDS-eDP		Camera & Mic	USB S&C		CRT		Touch Screen
description	LVDS-eDP		Camera & Mic	14640	14641	CRT		Touch Screen
explain	LVDS	eDP	Camera & Mic	14640	14641	w/ CRT	w/o CRT	Touch Screen
BTO	LVDS@	IEDP@	CAM_EMI@	14640@	14641@	CRT@	CRT_EMI@	NOCRT@ TOUCH_EMI@

Function	WOWL		G-SENSOR	ZPODD		GCLK		VRAM SKU for GV2
description	WOWL		G-SENSOR	ZPODD		GCLK	non-GCLK	Single Rank
explain	w/	w/o	G-SENSOR	w/	w/o	GCLK	non-GCLK	Single Rank
BTO	WOWL@	NOWOWL@	GSENSOR@	ZPODD@	NONZP@	GCLK@	NOGCLK@	GVSR@

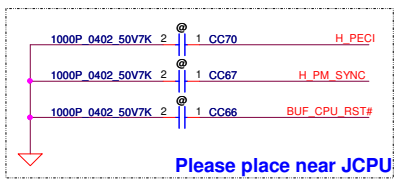
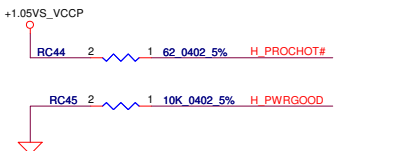
Function	Sleep & Music		KB Light	EMI/ESD part	
description	Sleep & Music		KB Light	EMI/ESD part	
explain	w/ S&M	w/o S&M	KB Light	EMI/ESD part	
BTO	269@	259@	KBL@	EMI@	ESD@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

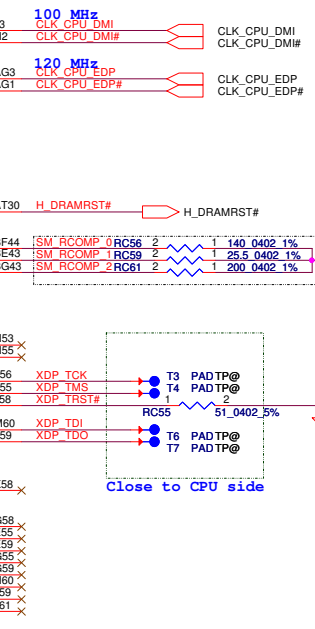
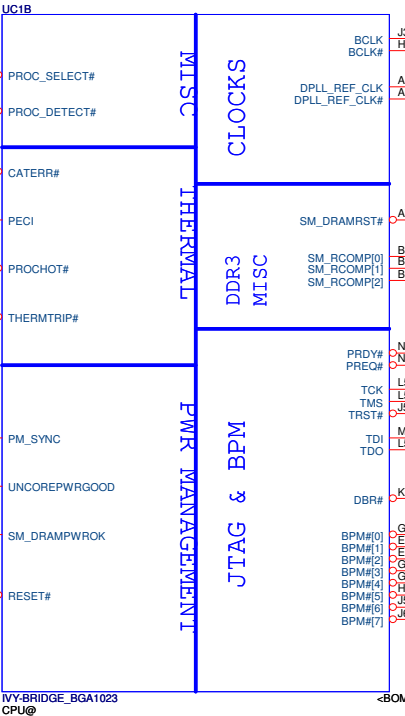
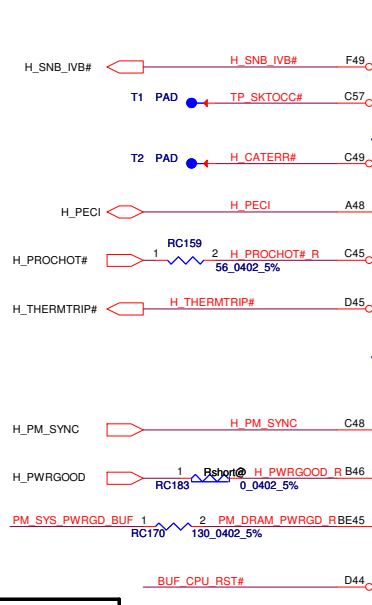
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				Notes List		
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				VFKTA	1.0	
				Date: Monday, March 11, 2013	Sheet 4 of 56	



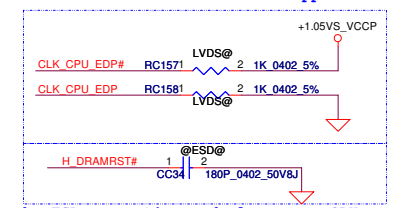
by ESD request and place near CPU



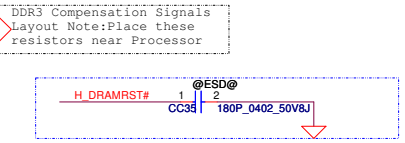
Please place near JCPU



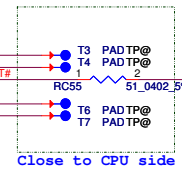
Stuff RC158&RC157 if do not support eDP



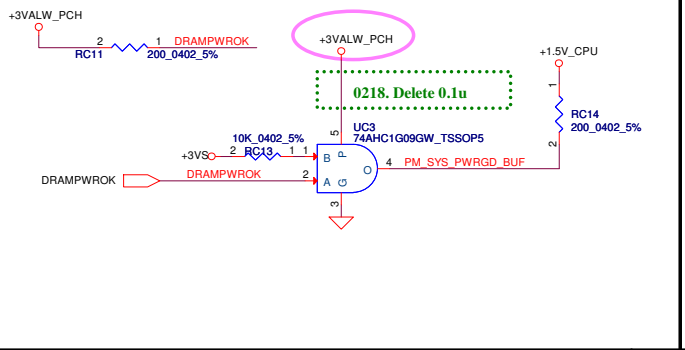
by ESD request and place near CPU



Routed as a single daisy chain

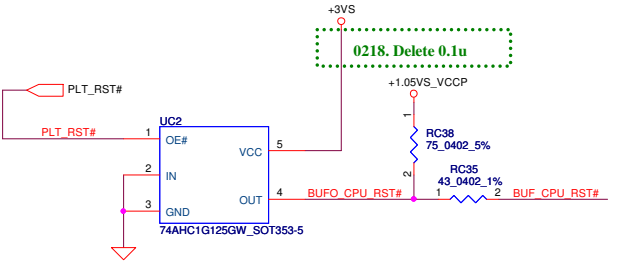


Close to CPU side



0218. Delete 0.1u

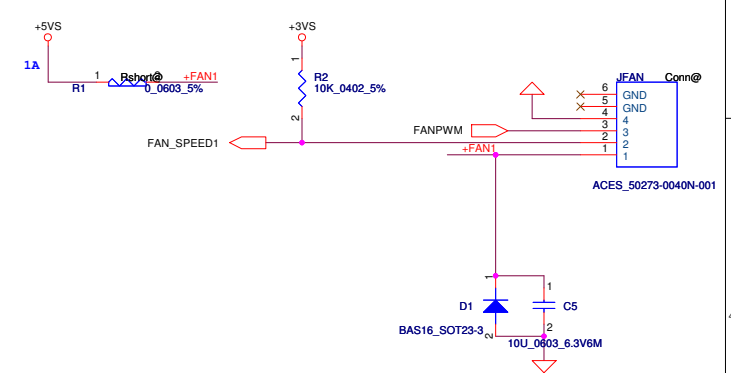
### Buffered Rest to CPU



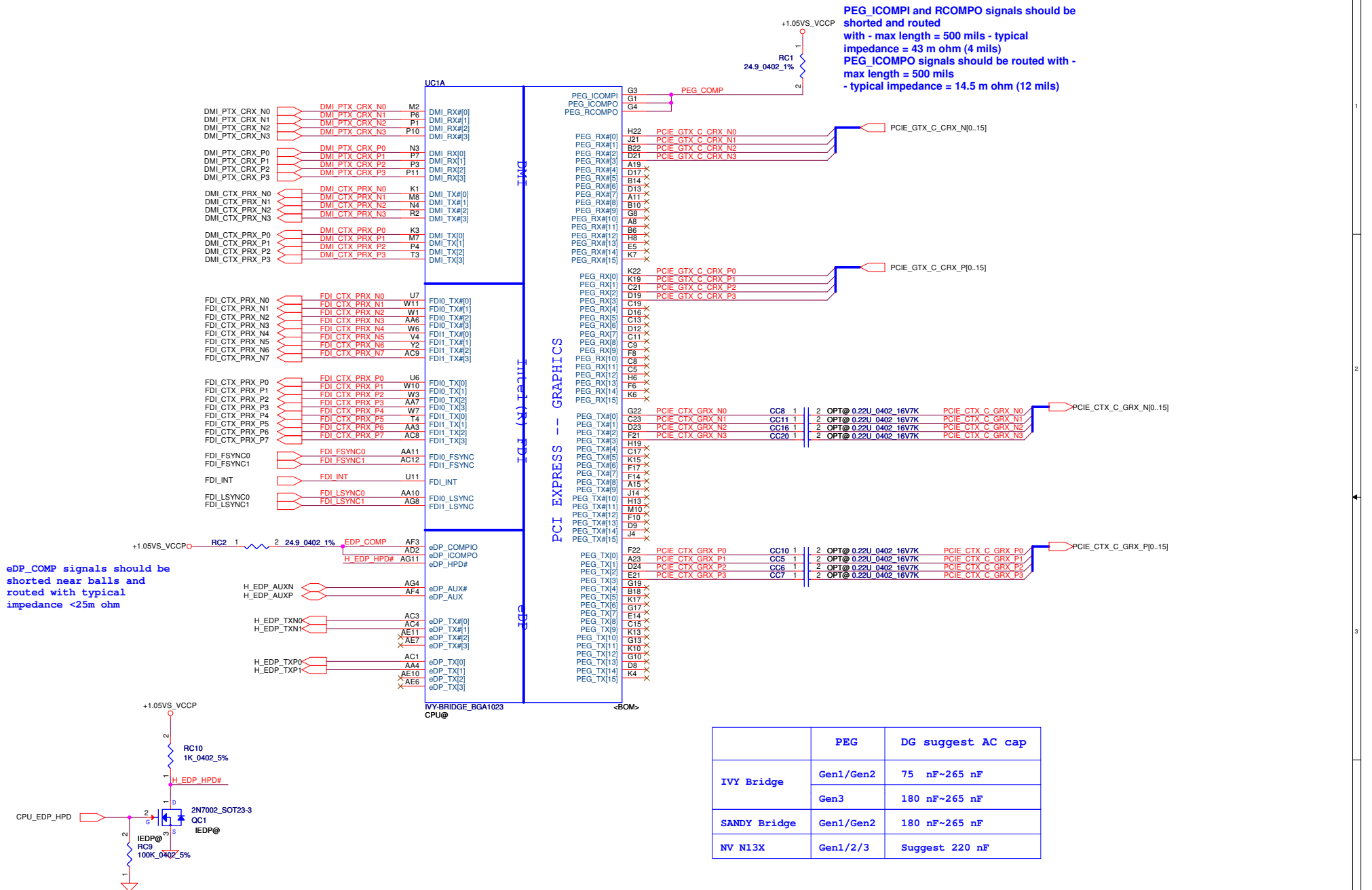
0218. Delete 0.1u

### XDP Connector

### FAN Control Circuit



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Date:	Monday, March 11, 2013	Sheet	5	of	56



	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N13X	Gen1/2/3	Suggest 220 nF

DDR\_A\_D[0..63]

DDR\_B\_D[0..63]

UC1C

UC1D

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

IVY-BRIDGE\_BGA1023 CPU@

IVY-BRIDGE\_BGA1023 CPU@

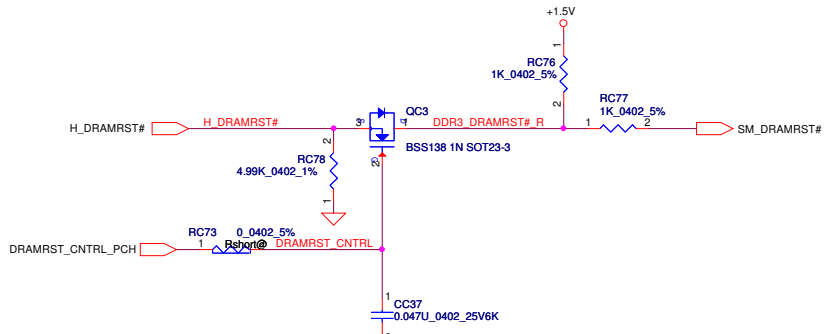
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 SA\_CK[1] AV36 DDRA\_CLK1#  
 SA\_CK[2] AY26 DDRA\_CKE0  
 SA\_CK[3] AT40 DDRA\_CLK1  
 SA\_CK[4] AU40 DDRA\_CLK1#  
 SA\_CK[5] BB26 DDRA\_CKE1  
 SA\_CS#0 BB40 DDRA\_SCS0#  
 SA\_CS#1 BC41 DDRA\_SCS1#  
 SA\_ODT[0] AY40 DDRA\_ODT0  
 SA\_ODT[1] BA41 DDRA\_ODT1  
 SA\_DQS#0 AL11 DDR\_A\_DQS#0  
 SA\_DQS#1 AR8 DDR\_A\_DQS#1  
 SA\_DQS#2 AV11 DDR\_A\_DQS#2  
 SA\_DQS#3 AT17 DDR\_A\_DQS#3  
 SA\_DQS#4 AV45 DDR\_A\_DQS#4  
 SA\_DQS#5 AY51 DDR\_A\_DQS#5  
 SA\_DQS#6 AT55 DDR\_A\_DQS#6  
 SA\_DQS#7 AK55 DDR\_A\_DQS#7  
 SA\_DQS#0 AJ11 DDR\_A\_DQS#0  
 SA\_DQS#1 AR10 DDR\_A\_DQS#1  
 SA\_DQS#2 AY11 DDR\_A\_DQS#2  
 SA\_DQS#3 AU17 DDR\_A\_DQS#3  
 SA\_DQS#4 AW45 DDR\_A\_DQS#4  
 SA\_DQS#5 AV51 DDR\_A\_DQS#5  
 SA\_DQS#6 AT56 DDR\_A\_DQS#6  
 SA\_DQS#7 AK54 DDR\_A\_DQS#7  
 SA\_MA[0] BG35 DDR\_A\_MA0  
 SA\_MA[1] BB34 DDR\_A\_MA1  
 SA\_MA[2] BE35 DDR\_A\_MA2  
 SA\_MA[3] BD35 DDR\_A\_MA3  
 SA\_MA[4] AT34 DDR\_A\_MA4  
 SA\_MA[5] AU34 DDR\_A\_MA5  
 SA\_MA[6] BB32 DDR\_A\_MA6  
 SA\_MA[7] AT32 DDR\_A\_MA7  
 SA\_MA[8] AY32 DDR\_A\_MA8  
 SA\_MA[9] AV32 DDR\_A\_MA9  
 SA\_MA[10] BE37 DDR\_A\_MA10  
 SA\_MA[11] BA30 DDR\_A\_MA11  
 SA\_MA[12] BC30 DDR\_A\_MA12  
 SA\_MA[13] AW41 DDR\_A\_MA13  
 SA\_MA[14] AY28 DDR\_A\_MA14  
 SA\_MA[15] AU26 DDR\_A\_MA15

SB\_CK[0] AL4 DDR\_B\_D0  
 SB\_CK[1] AR11 DDR\_B\_D1  
 SB\_CK[2] AN3 DDR\_B\_D2  
 SB\_CK[3] AR4 DDR\_B\_D3  
 SB\_CK[4] AK4 DDR\_B\_D4  
 SB\_CK[5] AK3 DDR\_B\_D5  
 SB\_CK[6] AN4 DDR\_B\_D6  
 SB\_CK[7] AR1 DDR\_B\_D7  
 SB\_CK[8] AU4 DDR\_B\_D8  
 SB\_CK[9] AT2 DDR\_B\_D9  
 SB\_CK[10] AV4 DDR\_B\_D10  
 SB\_CK[11] BA1 DDR\_B\_D11  
 SB\_CK[12] AR3 DDR\_B\_D12  
 SB\_CK[13] AY2 DDR\_B\_D13  
 SB\_CK[14] BA3 DDR\_B\_D14  
 SB\_CK[15] BE9 DDR\_B\_D15  
 SB\_CK[16] BD9 DDR\_B\_D16  
 SB\_CK[17] BD10 DDR\_B\_D17  
 SB\_CK[18] BD13 DDR\_B\_D18  
 SB\_CK[19] BF8 DDR\_B\_D19  
 SB\_CK[20] BD10 DDR\_B\_D20  
 SB\_CK[21] BF18 DDR\_B\_D21  
 SB\_CK[22] BE13 DDR\_B\_D22  
 SB\_CK[23] BF16 DDR\_B\_D23  
 SB\_CK[24] BE18 DDR\_B\_D24  
 SB\_CK[25] BE17 DDR\_B\_D25  
 SB\_CK[26] BF18 DDR\_B\_D26  
 SB\_CK[27] BE21 DDR\_B\_D27  
 SB\_CK[28] BE14 DDR\_B\_D28  
 SB\_CK[29] BG14 DDR\_B\_D29  
 SB\_CK[30] BG18 DDR\_B\_D30  
 SB\_CK[31] BF19 DDR\_B\_D31  
 SB\_CK[32] BD50 DDR\_B\_D32  
 SB\_CK[33] BF48 DDR\_B\_D33  
 SB\_CK[34] BC33 DDR\_B\_D34  
 SB\_CK[35] BF52 DDR\_B\_D35  
 SB\_CK[36] BD49 DDR\_B\_D36  
 SB\_CK[37] BE49 DDR\_B\_D37  
 SB\_CK[38] BD54 DDR\_B\_D38  
 SB\_CK[39] BE53 DDR\_B\_D39  
 SB\_CK[40] BE57 DDR\_B\_D40  
 SB\_CK[41] BC59 DDR\_B\_D42  
 SB\_CK[42] AY60 DDR\_B\_D43  
 SB\_CK[43] BE54 DDR\_B\_D44  
 SB\_CK[44] BG54 DDR\_B\_D45  
 SB\_CK[45] BA58 DDR\_B\_D46  
 SB\_CK[46] AW59 DDR\_B\_D47  
 SB\_CK[47] AU58 DDR\_B\_D48  
 SB\_CK[48] AN61 DDR\_B\_D49  
 SB\_CK[49] AN59 DDR\_B\_D50  
 SB\_CK[50] AU59 DDR\_B\_D51  
 SB\_CK[51] AU61 DDR\_B\_D52  
 SB\_CK[52] AN58 DDR\_B\_D53  
 SB\_CK[53] AR58 DDR\_B\_D54  
 SB\_CK[54] AK58 DDR\_B\_D55  
 SB\_CK[55] AL58 DDR\_B\_D56  
 SB\_CK[56] AG58 DDR\_B\_D57  
 SB\_CK[57] AG59 DDR\_B\_D58  
 SB\_CK[58] AM60 DDR\_B\_D59  
 SB\_CK[59] AL59 DDR\_B\_D60  
 SB\_CK[60] AF61 DDR\_B\_D61  
 SB\_CK[61] AH60 DDR\_B\_D62  
 SB\_CK[62] AH60 DDR\_B\_D63

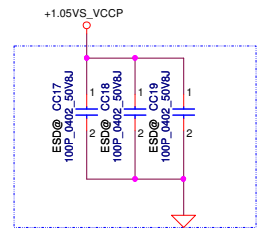
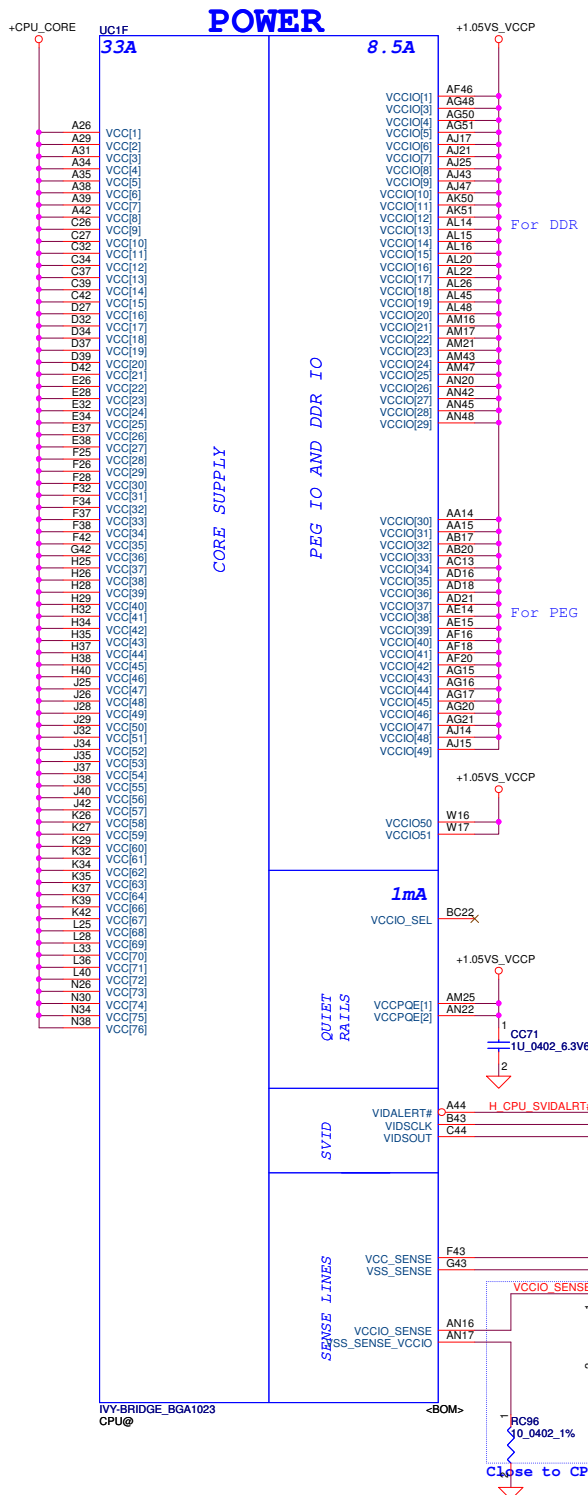
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 SB\_CS#0 BE41 DDRB\_SCS0#  
 SB\_CS#1 BE47 DDRB\_SCS1#  
 SB\_ODT[0] AT43 DDRB\_ODT0  
 SB\_ODT[1] BG47 DDRB\_ODT1  
 SB\_DQS#0 AL3 DDR\_B\_DQS#0  
 SB\_DQS#1 AV3 DDR\_B\_DQS#1  
 SB\_DQS#2 BG11 DDR\_B\_DQS#2  
 SB\_DQS#3 BD17 DDR\_B\_DQS#3  
 SB\_DQS#4 BG51 DDR\_B\_DQS#4  
 SB\_DQS#5 BA59 DDR\_B\_DQS#5  
 SB\_DQS#6 AT60 DDR\_B\_DQS#6  
 SB\_DQS#7 AK59 DDR\_B\_DQS#7  
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 SB\_DQS#1 AV1 DDR\_B\_DQS#1  
 SB\_DQS#2 BE11 DDR\_B\_DQS#2  
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 SB\_DQS#4 BE51 DDR\_B\_DQS#4  
 SB\_DQS#5 BA61 DDR\_B\_DQS#5  
 SB\_DQS#6 AR59 DDR\_B\_DQS#6  
 SB\_DQS#7 AK61 DDR\_B\_DQS#7  
 SB\_MA[0] BF32 DDR\_B\_MA0  
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 SB\_MA[3] AU30 DDR\_B\_MA3  
 SB\_MA[4] BD30 DDR\_B\_MA4  
 SB\_MA[5] AV30 DDR\_B\_MA5  
 SB\_MA[6] BC30 DDR\_B\_MA6  
 SB\_MA[7] BD29 DDR\_B\_MA7  
 SB\_MA[8] BE30 DDR\_B\_MA8  
 SB\_MA[9] BE28 DDR\_B\_MA9  
 SB\_MA[10] BD43 DDR\_B\_MA10  
 SB\_MA[11] AT28 DDR\_B\_MA11  
 SB\_MA[12] AV28 DDR\_B\_MA12  
 SB\_MA[13] BD46 DDR\_B\_MA13  
 SB\_MA[14] AT26 DDR\_B\_MA14  
 SB\_MA[15] AU22 DDR\_B\_MA15

DDR\_A\_BS0 DDR A BS0 BD37 SA\_BS[0]  
 DDR\_A\_BS1 DDR A BS1 BF36 SA\_BS[1]  
 DDR\_A\_BS2 DDR A BS2 BA28 SA\_BS[2]  
 DDR\_A\_CAS# DDR A CAS# BE39 SA\_CAS#  
 DDR\_A\_RAS# DDR A RAS# BD39 SA\_RAS#  
 DDR\_A\_WE# DDR A WE# AT41 SA\_WE#

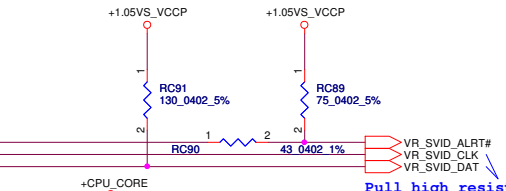
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 DDR\_B\_BS2 DDR B BS2 AT22 SB\_BS[2]  
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 DDR\_B\_RAS# DDR B RAS# BF40 SB\_RAS#  
 DDR\_B\_WE# DDR B WE# BD45 SB\_WE#



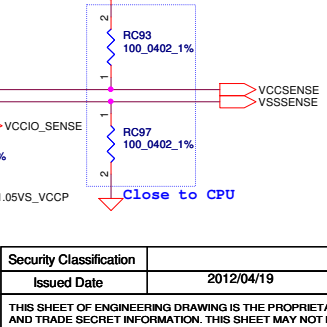
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Rev 1.0 Sheet 7 of 56				



by ESD requestion and place near CPU



Pull high resistor on VR side



Close to CPU

Security Classification	Compal Secret Data		Title	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Ivy Bridge_POWER-1
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Rev 1.0			Sheet 8 of 56	



# POWER

- UC1G**  
29A
- AA46 VAXG[1]
  - AB47 VAXG[2]
  - AB50 VAXG[3]
  - AB51 VAXG[4]
  - AB52 VAXG[5]
  - AB53 VAXG[6]
  - AB55 VAXG[7]
  - AB56 VAXG[8]
  - AB58 VAXG[9]
  - AB59 VAXG[10]
  - AC81 VAXG[11]
  - AD47 VAXG[12]
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  - AD56 VAXG[19]
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  - AE46 VAXG[22]
  - M45 VAXG[23]
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  - P53 VAXG[29]
  - P56 VAXG[30]
  - P61 VAXG[31]
  - T48 VAXG[32]
  - T58 VAXG[33]
  - T59 VAXG[34]
  - T61 VAXG[35]
  - U46 VAXG[36]
  - V47 VAXG[37]
  - V48 VAXG[38]
  - V50 VAXG[39]
  - V51 VAXG[40]
  - V52 VAXG[41]
  - V53 VAXG[42]
  - V55 VAXG[43]
  - V56 VAXG[44]
  - V58 VAXG[45]
  - V59 VAXG[46]
  - W50 VAXG[47]
  - W51 VAXG[48]
  - W52 VAXG[49]
  - W53 VAXG[50]
  - W55 VAXG[51]
  - W56 VAXG[52]
  - W61 VAXG[53]
  - Y48 VAXG[54]
  - Y61 VAXG[55]
  - Y61 VAXG[56]

## GRAPHICS

### DDR3 - 1.5V RAILS

### 1mA

### QUIET RAILS

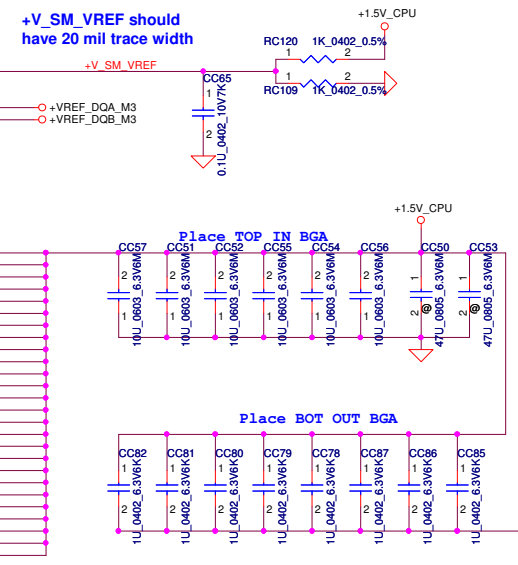
### 1.8V RAIL

### SA RAIL

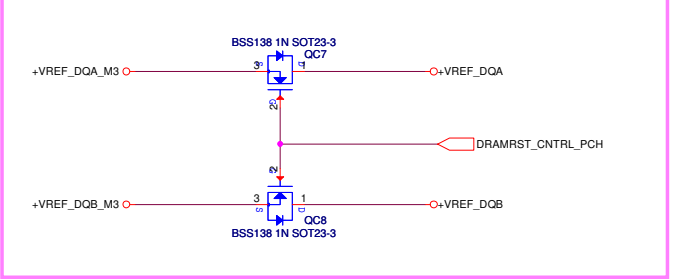
### SENSE LINES

### VCCSA VID Lines

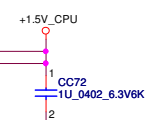
IVY-BRIDGE\_BGA1023  
CPU@



### Intel DDR Vref M3

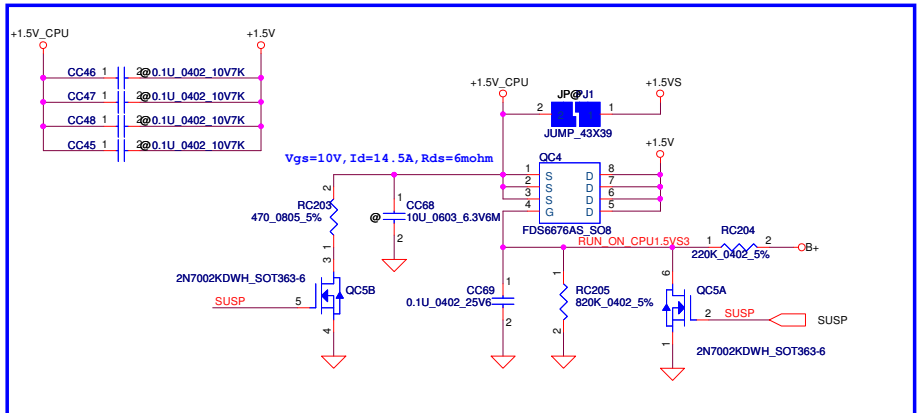
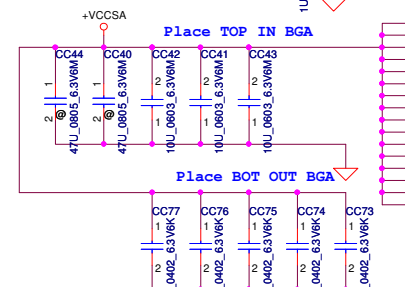
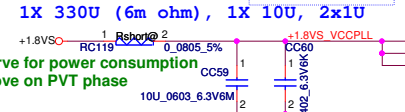
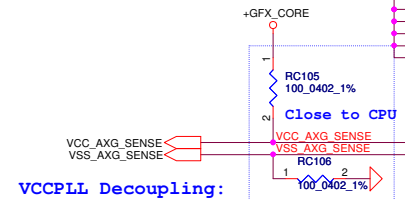
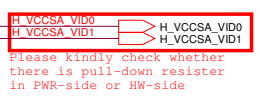


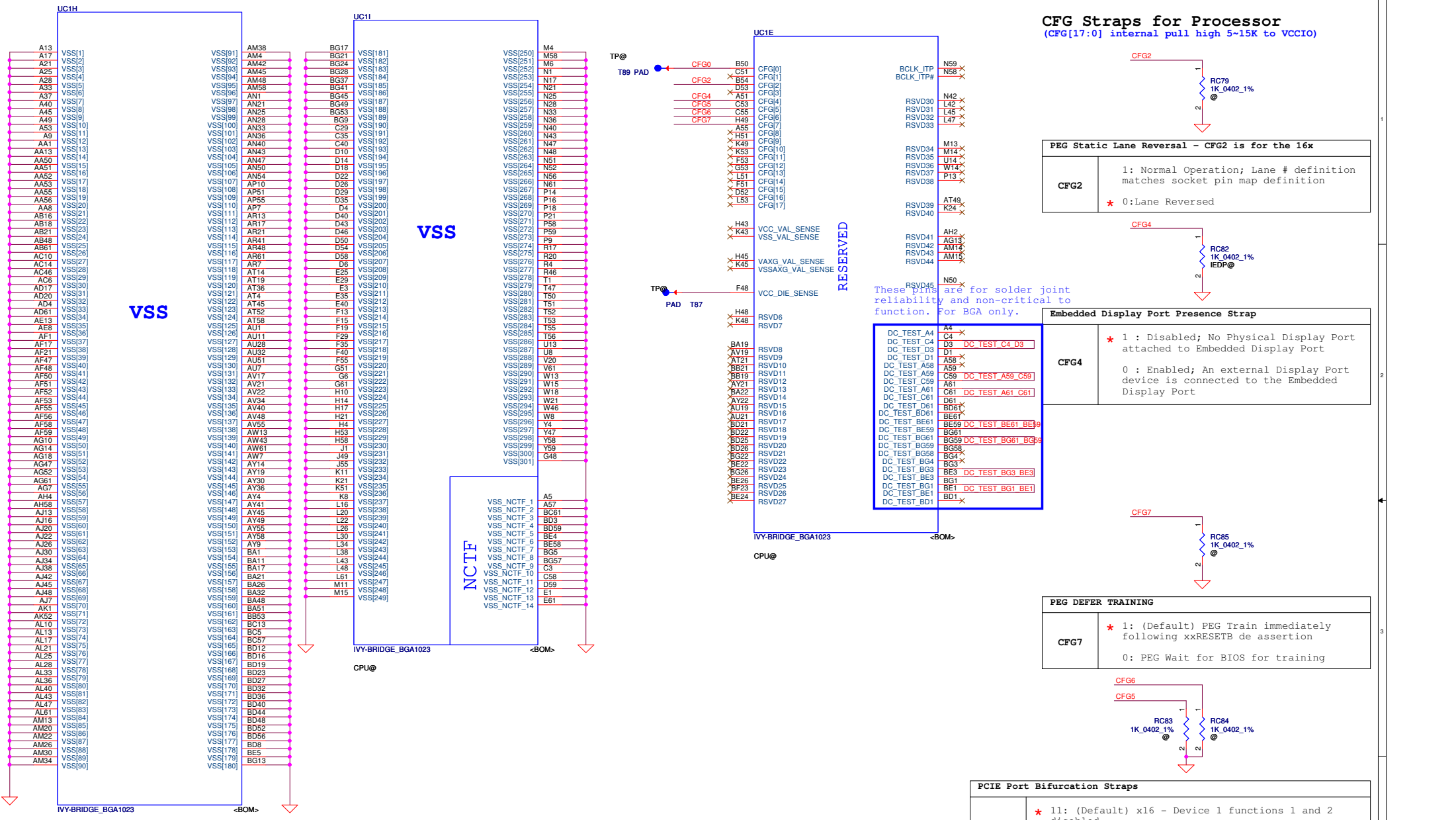
+1.5V\_CPU Decoupling:  
2X 47U (MLCC), 6X 10U, 8X 1U



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge





### CFG Straps for Processor (CFG[17:0] internal pull high 5-15K to VCCIO)

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
* 0: Lane Reversed	

Embedded Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port
0 : Enabled; An external Display Port device is connected to the Embedded Display Port	

PEG DEFER TRAINING

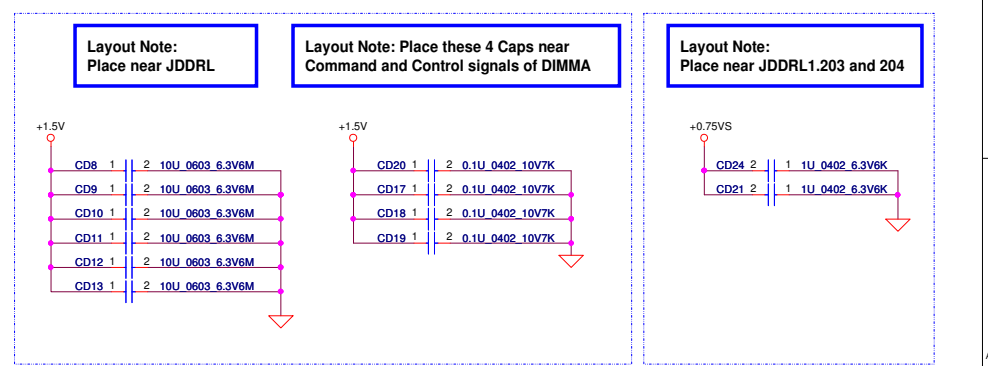
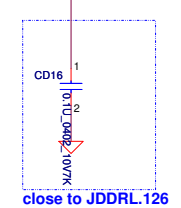
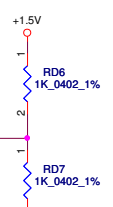
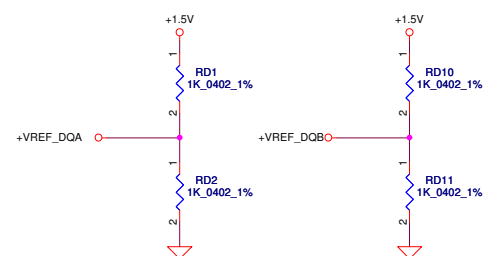
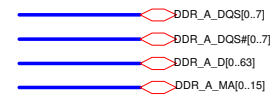
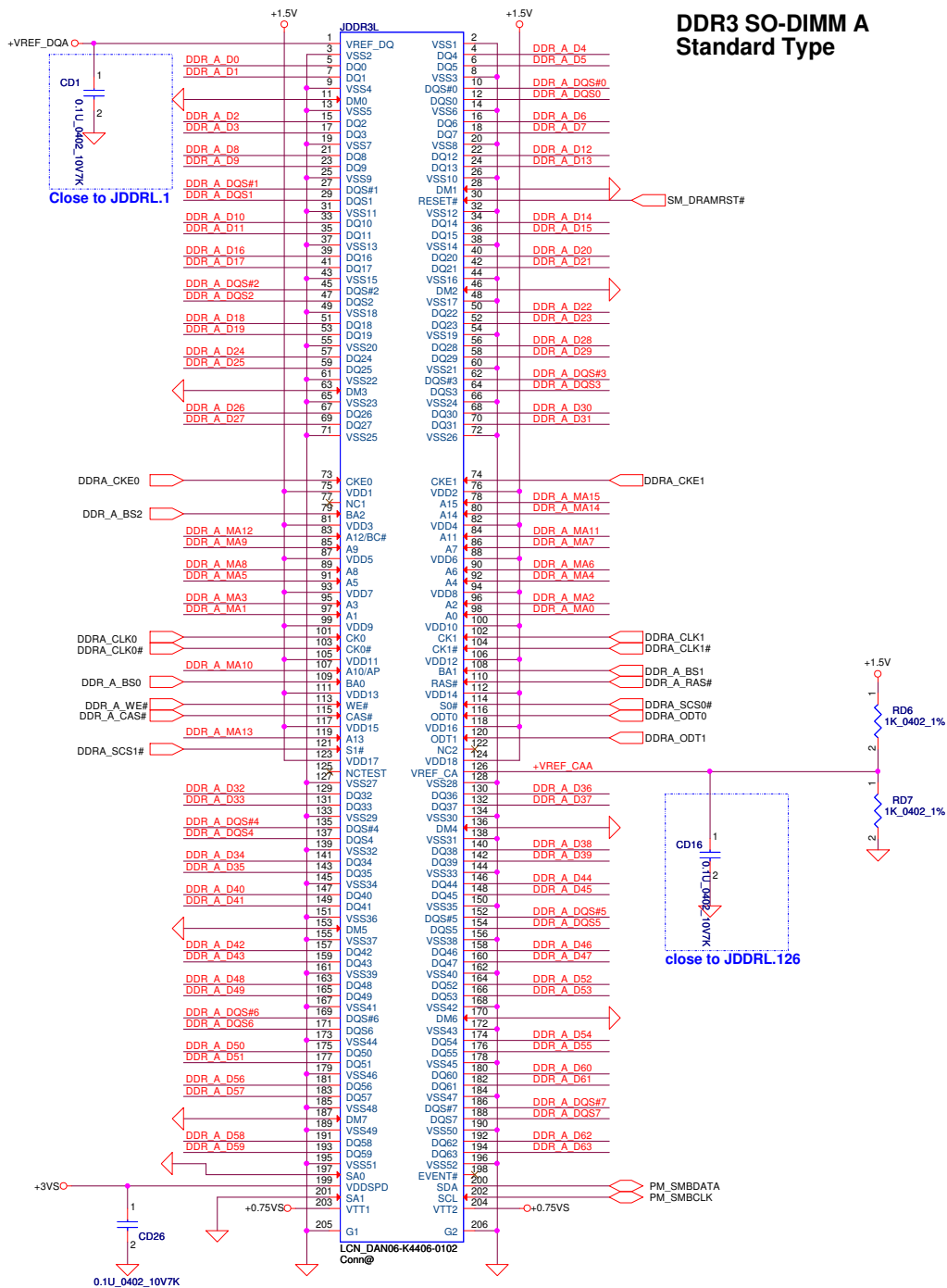
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion
0: PEG Wait for BIOS for training	

PCIe Port Bifurcation Straps

CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled	
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)	
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled	

These pins are for solder joint reliability and non-critical to function. For BGA only.

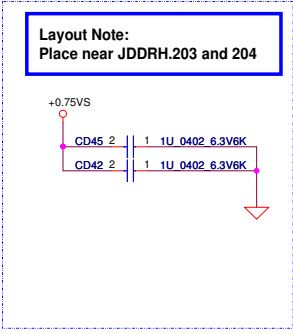
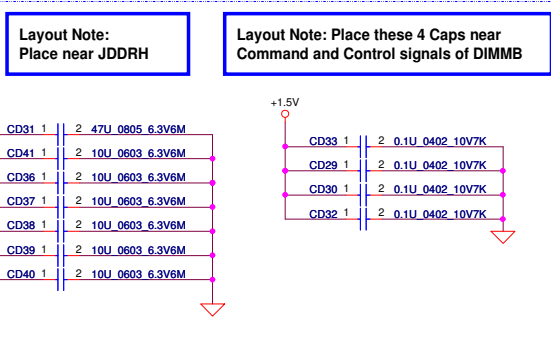
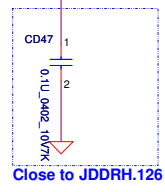
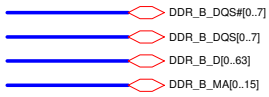
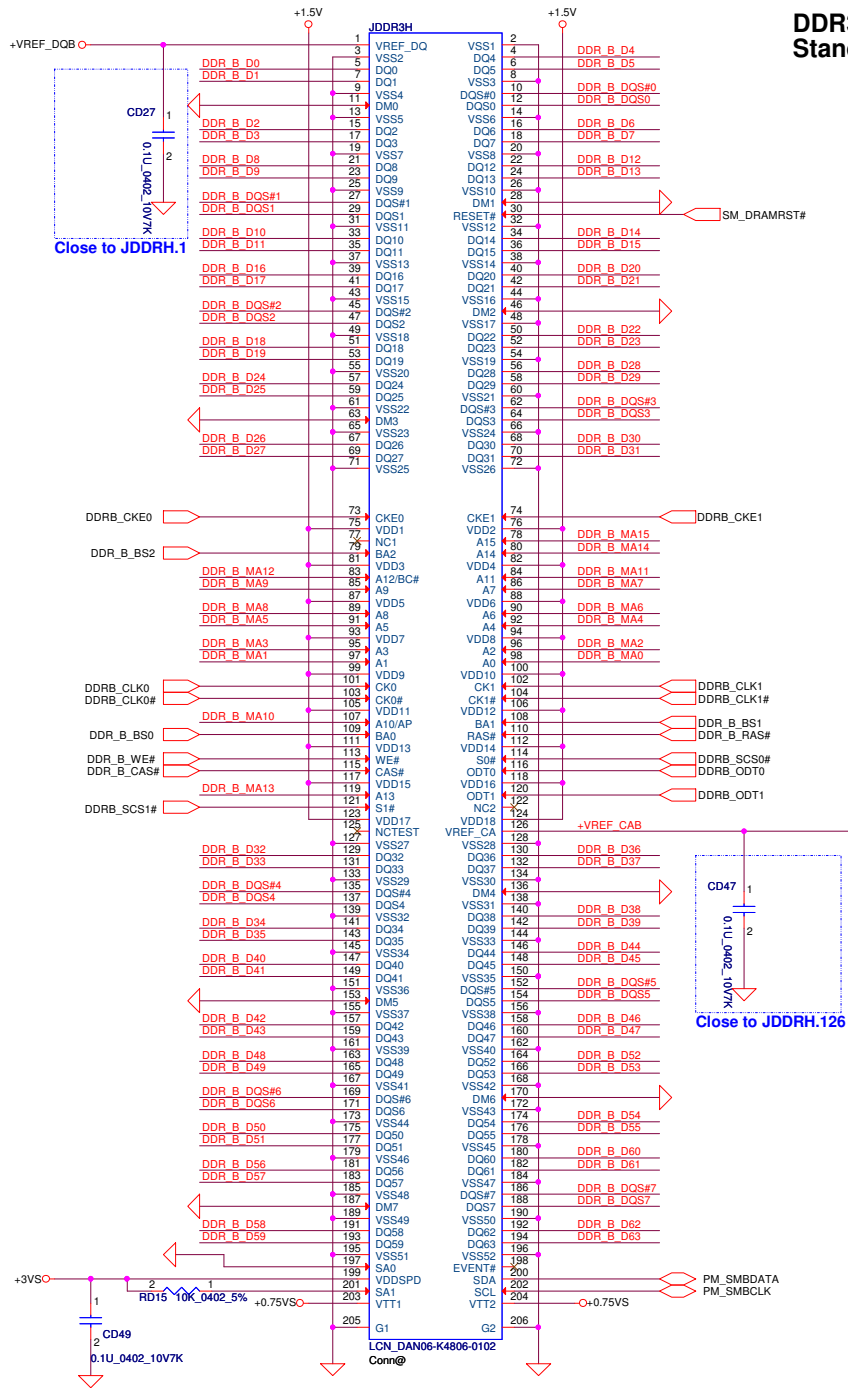
# DDR3 SO-DIMM A Standard Type



SPD setting (SA0, SA1)  
 PU/PD by Channel A/B  
 ->Channel A 00  
 ->Channel B 01

Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	DDRIII-SODIMMO
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Page 11 of 56				Rev 1.0

# DDR3 SO-DIMM B Standard Type



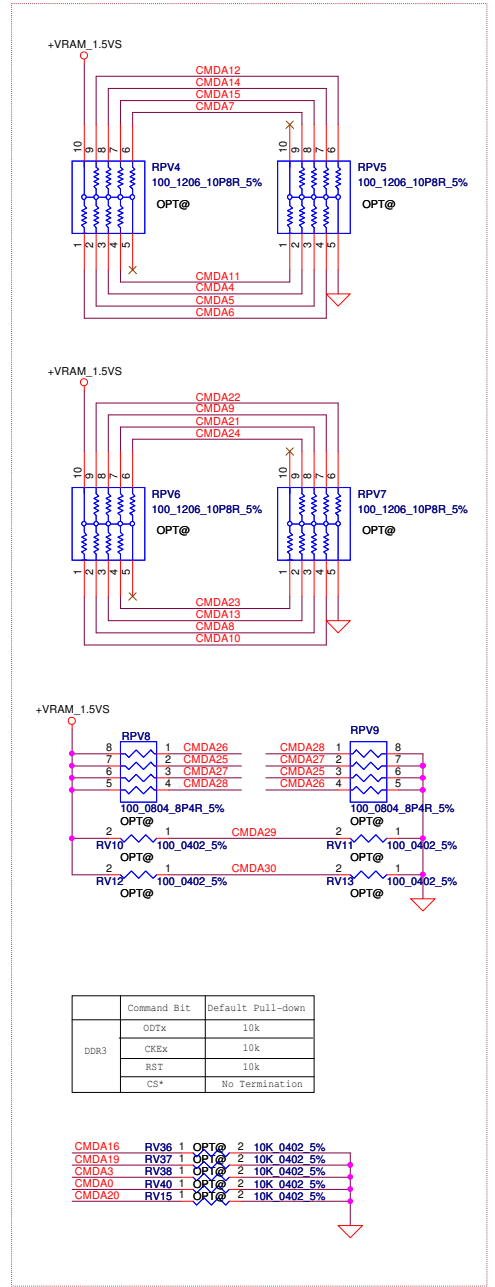
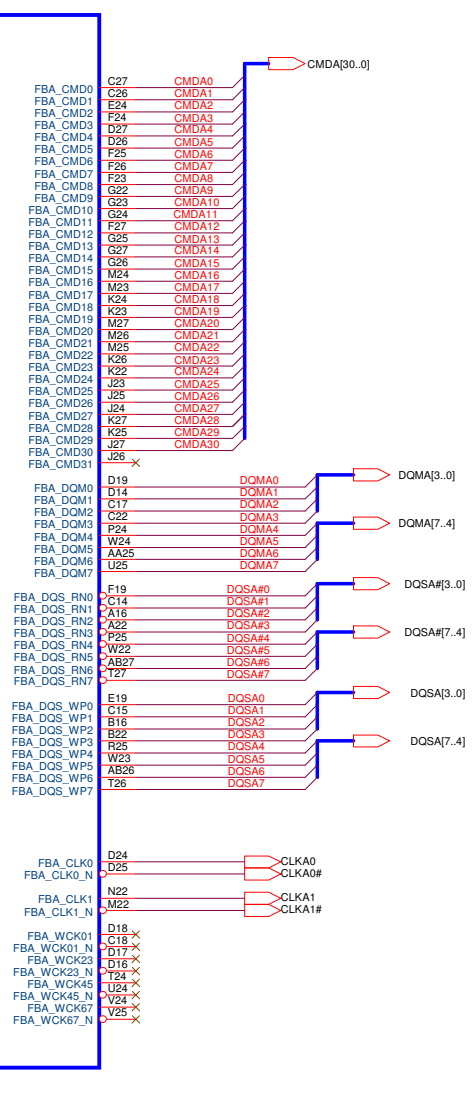
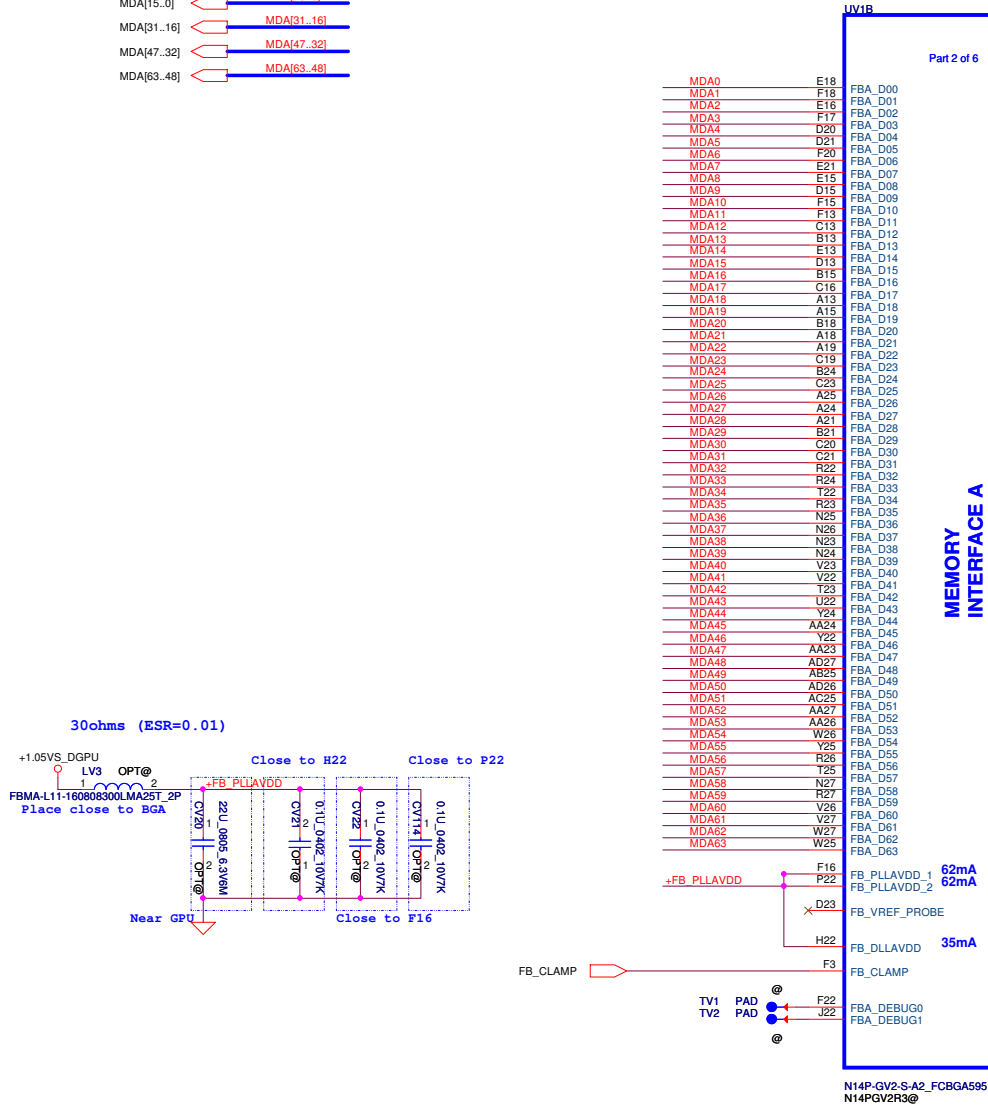
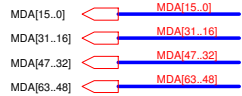
SPD setting (SA0, SA1)  
PU/PD by Channel A/B  
->Channel A 00  
->Channel B 01

Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	DDRIII-SODIMM1
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				Rev 1.0 Sheet 12 of 56



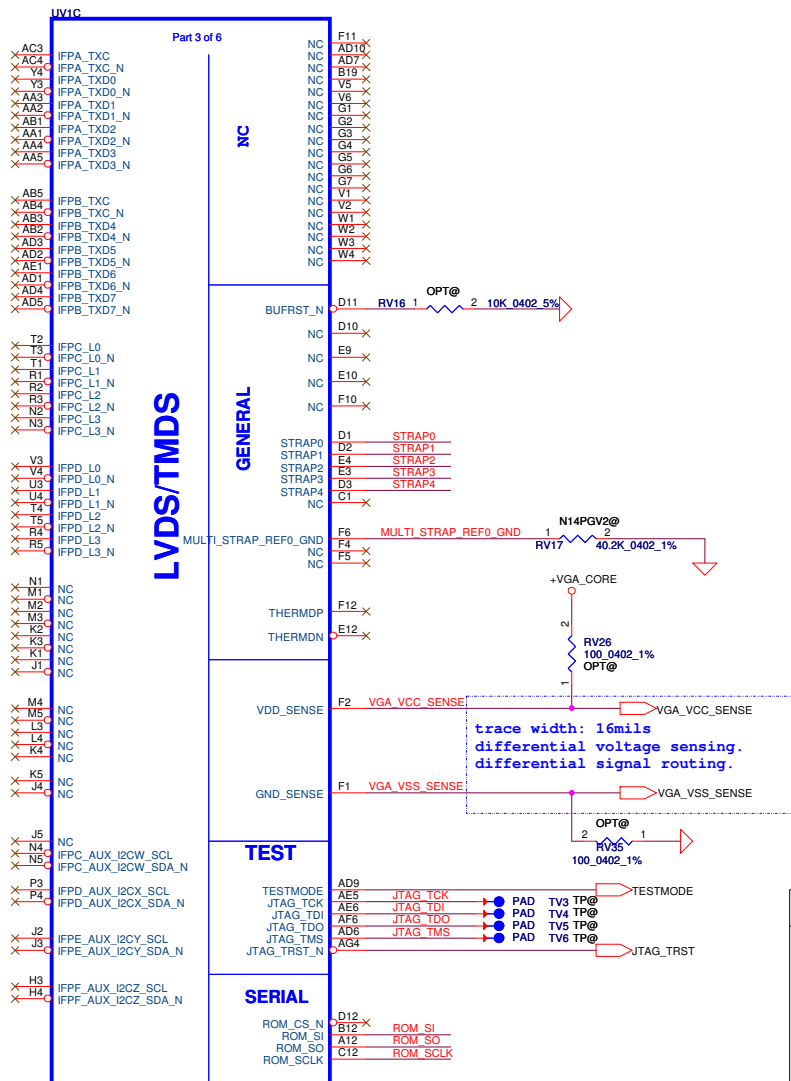
# VRAM Interface

Place close to the first T point



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CkEx	10k
	RSt	10k
	CS*	No Termination



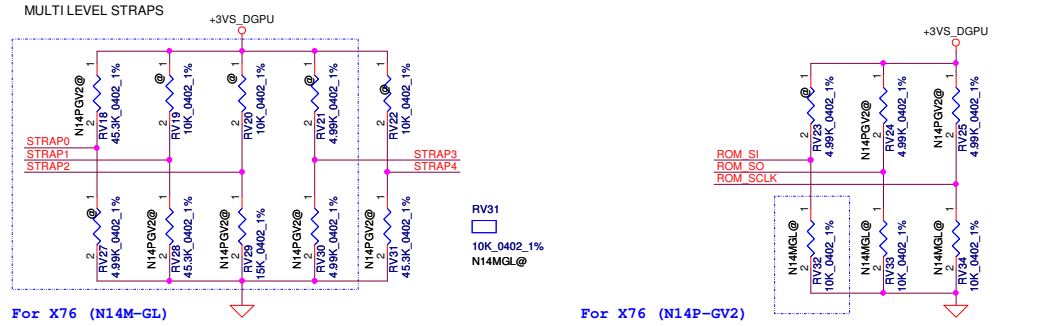


N14P-GV2-S-A2\_FCBGA595  
N14PGV2R3@

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR3_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN#	PCIE_MAX_SPEED	DP_PLL_VDD33V

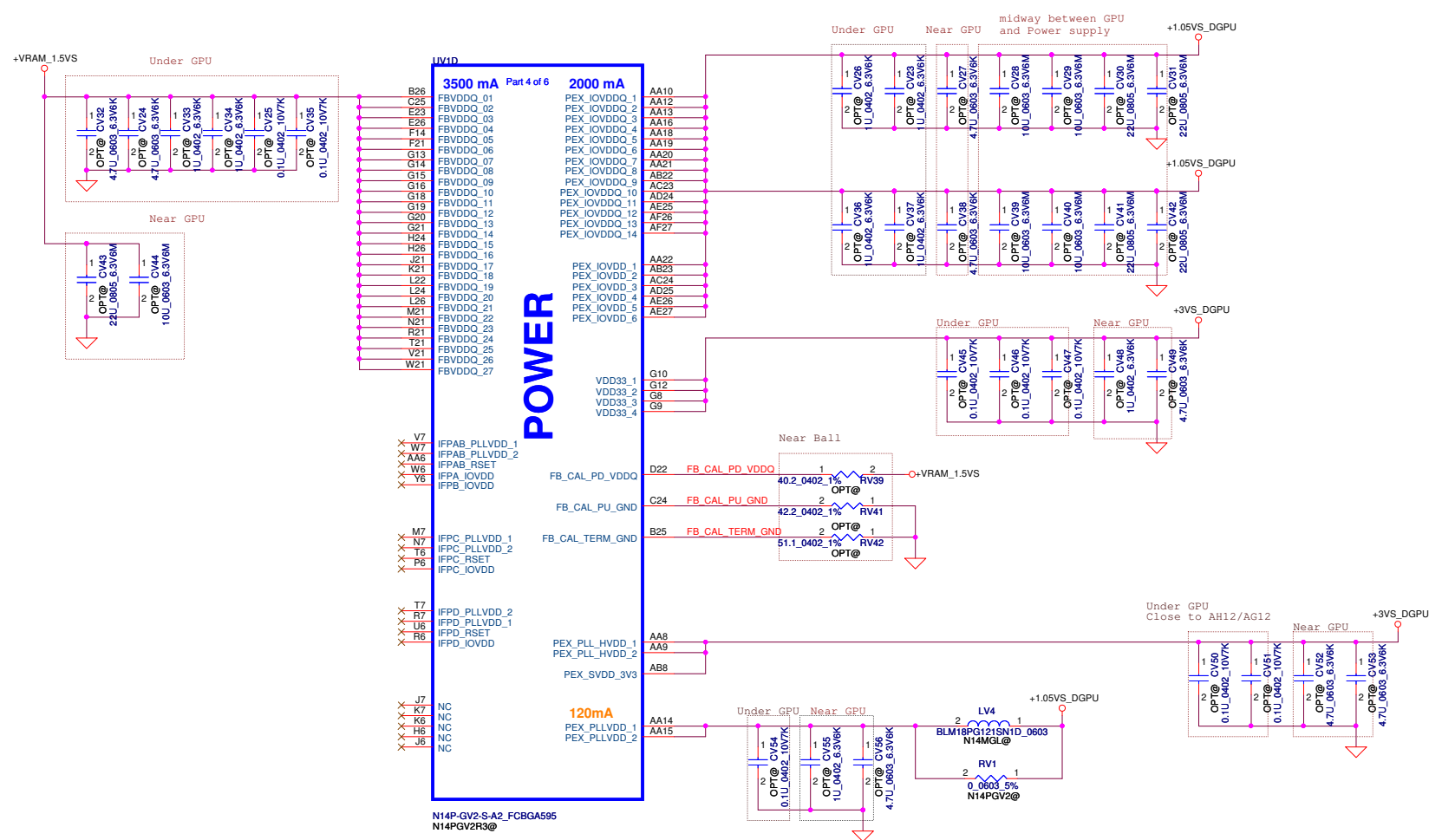
SKU	Device ID	bit5 to bit0
N14P-GV2	TBD	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS_DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



GPU	FB Memory gDDR3	ROM_SI
N14P-GV2	Samsung 900MHz K4W2G1646E-BC11	PD 45K
		1GHz K4W2G1646E-BC1A
	Hynix 900MHz H5TQ2G63DFR-11C	PD 34.8K
		1GHz H5TQ2G63DFR-N0C
	Micron 900MHz MT41K128M16JT-107G	PD 30K
		Samsung 900MHz K4W4G1646B-HC11
Micron 900MHz MT41K256M16HA-107G	PD 10K	

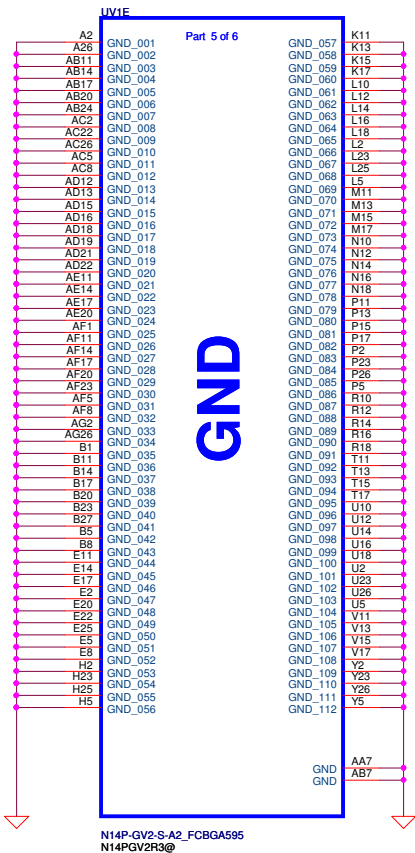
GPU	FB Memory gDDR3	STRAP [3:0]
N14M-GL	Samsung 900MHz K4W2G1646E-BC11	0101
		1GHz K4W2G1646E-BC1A
	Hynix 900MHz H5TQ2G63DFR-11C	0110
		1GHz H5TQ2G63DFR-N0C
	Micron 900MHz MT41K128M16JT-107G	0001
		Samsung 900MHz K4W4G1646B-HC11
Micron 900MHz MT41K256M16HA-107G	Hynix 900MHz H5TC4G63AFR-11C	0100
	Micron 900MHz MT41K256M16HA-107G	1101



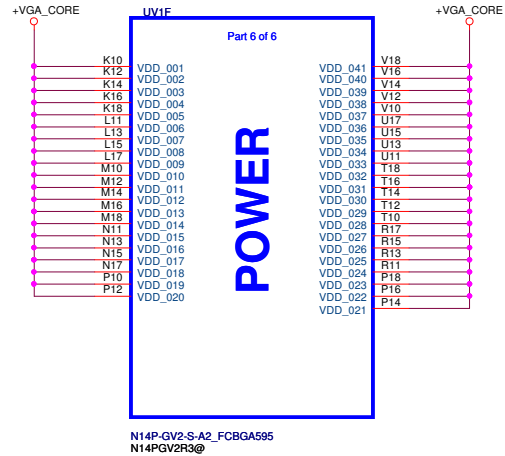
N14P-GV2-S-A2\_FCBGA595  
N14PGV2R3@

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Issued Date	2012/09/28	Deciphered Date	2013/09/28	Title
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Date:	Monday, March 11, 2013	Sheet	16	of 56

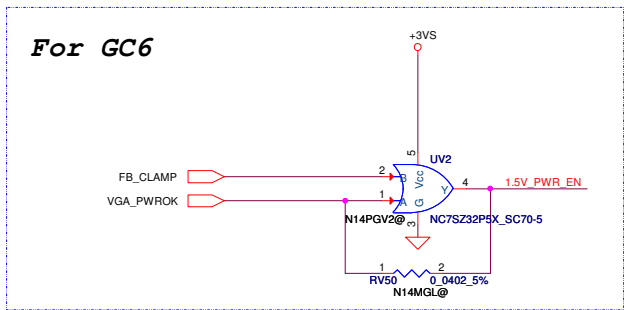




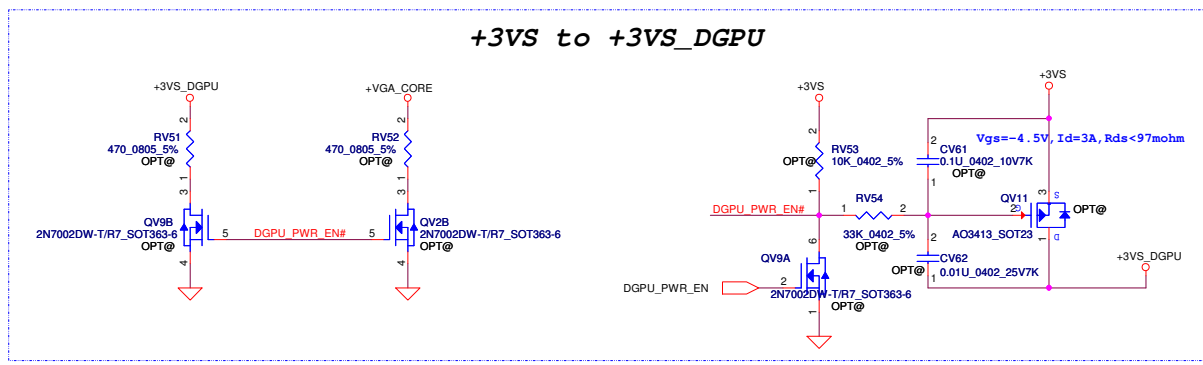
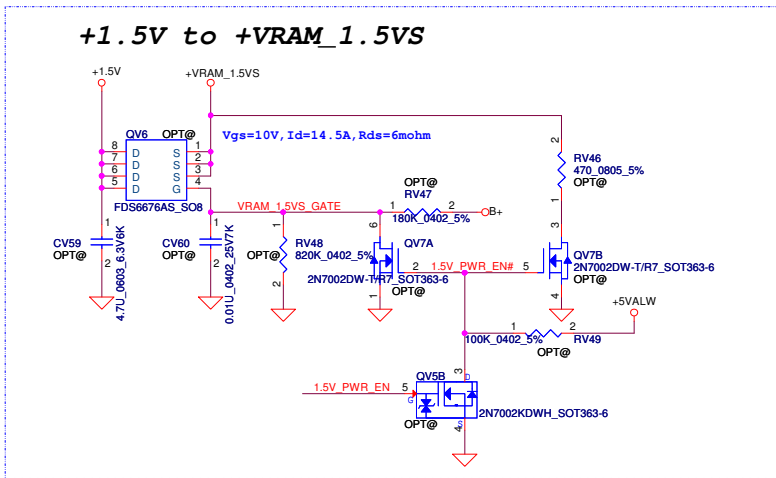
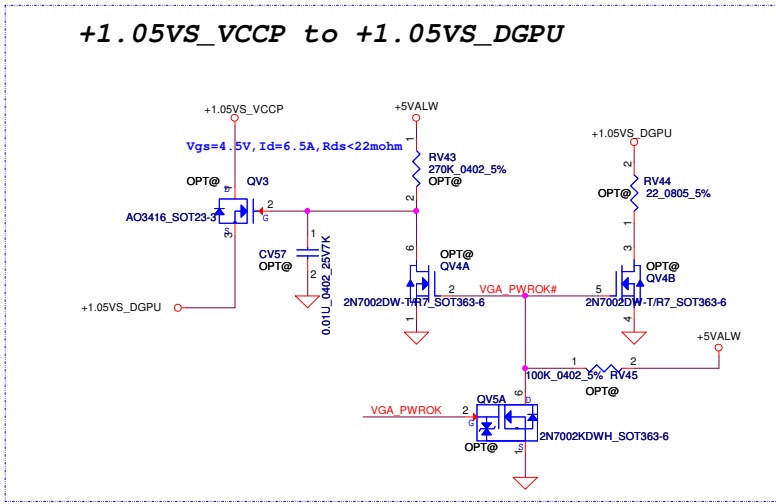
N14P-GV2-S-A2\_FCBGA595  
N14PGV2R3@



N14P-GV2-S-A2\_FCBGA595  
N14PGV2R3@



For GC6

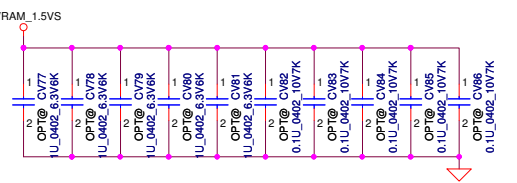
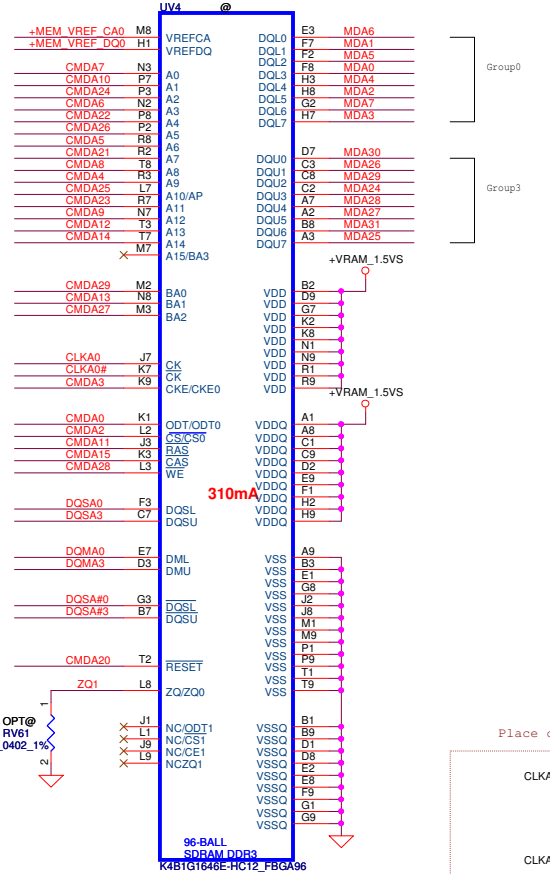
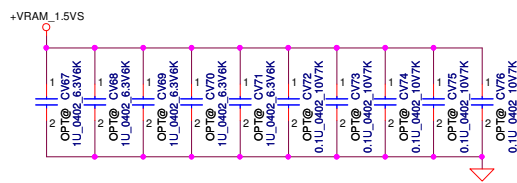
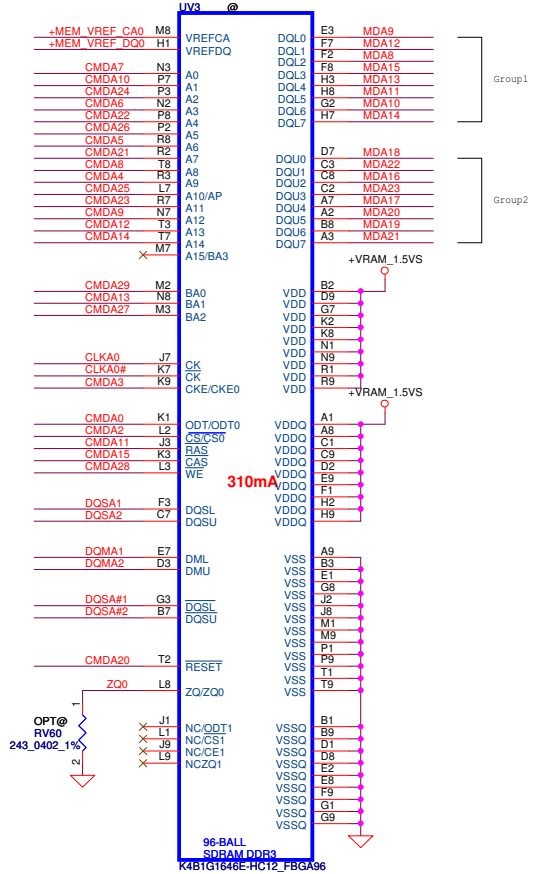
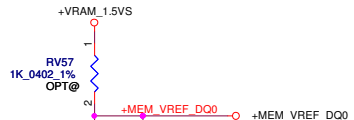
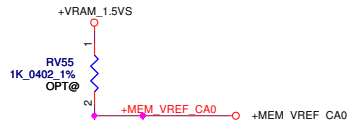
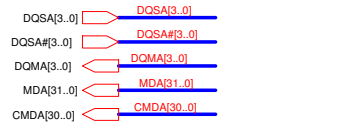


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Date: Monday, March 11, 2013				Sheet 17 of 56

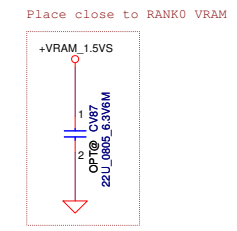
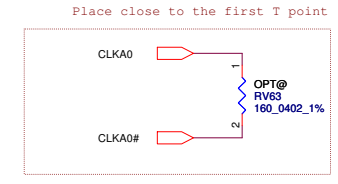
**Compal N14x POWER & GND**

Rev 1.0

# RANK 0 [31...0] VRAM DDR3 Chips



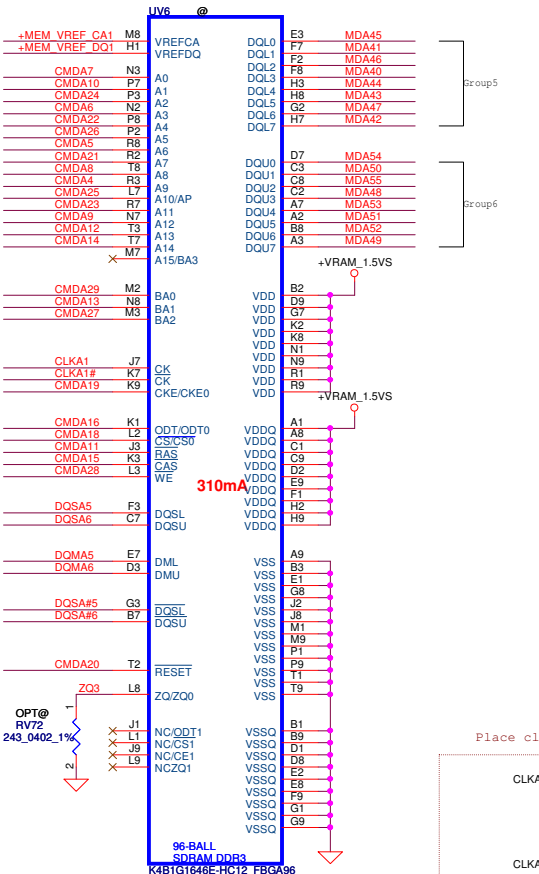
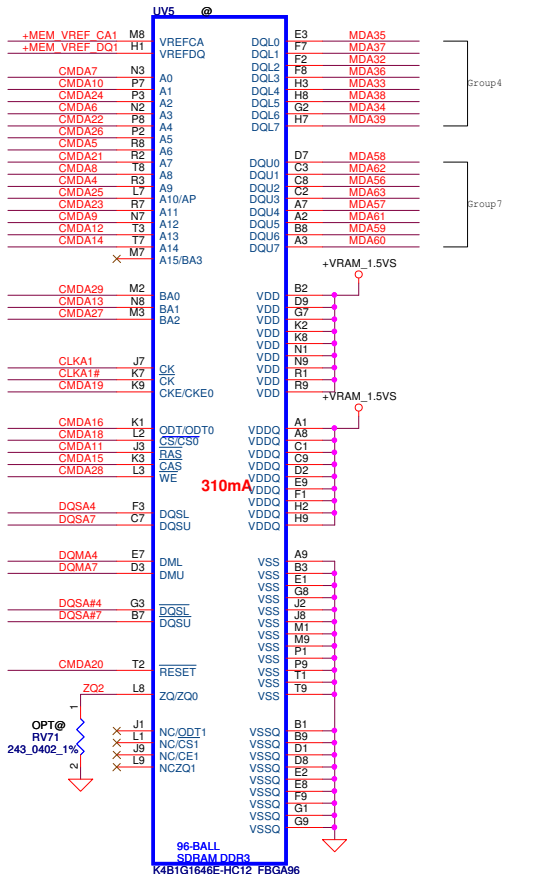
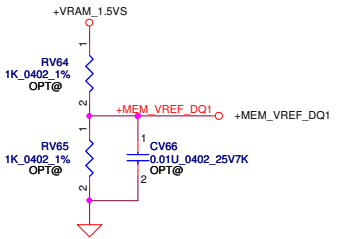
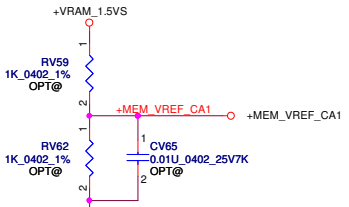
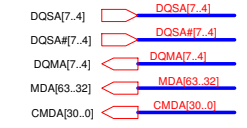
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	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



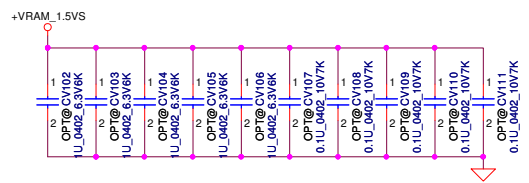
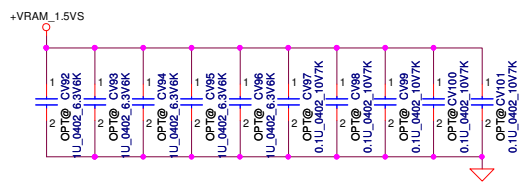
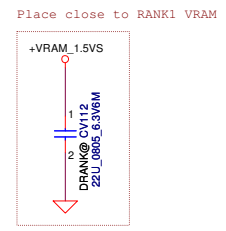
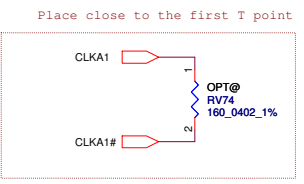
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					1.0	
				Date:	Monday, March 11, 2013	Sheet 18 of 56

## Compal N14x VRAM RANK 0L

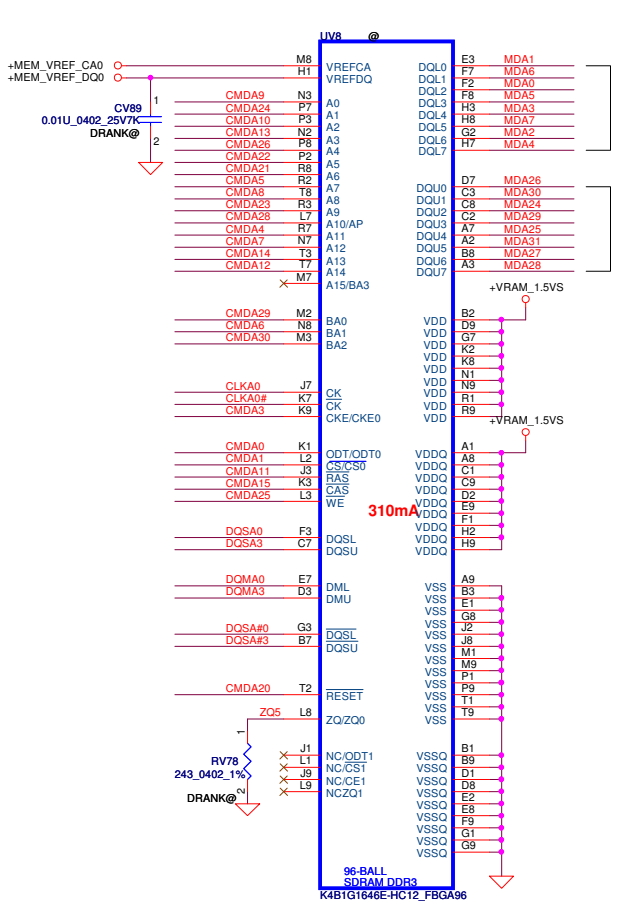
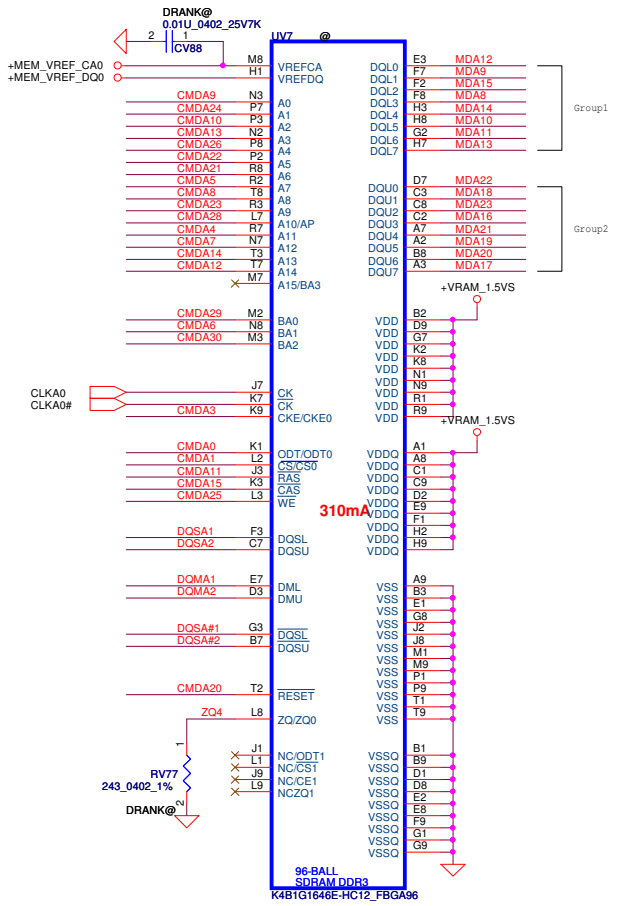
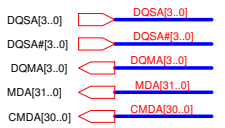
# RANK 0 [63...32] VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



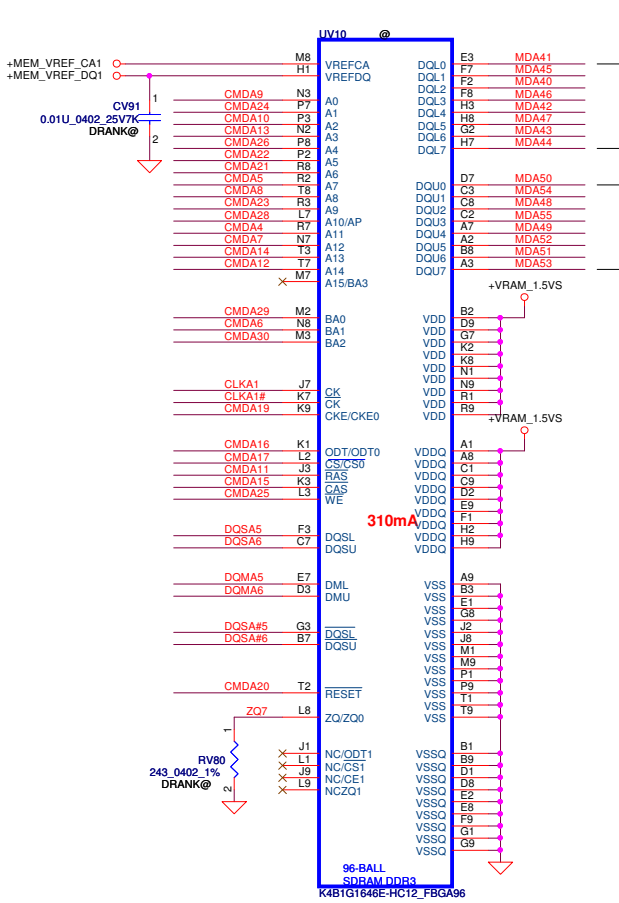
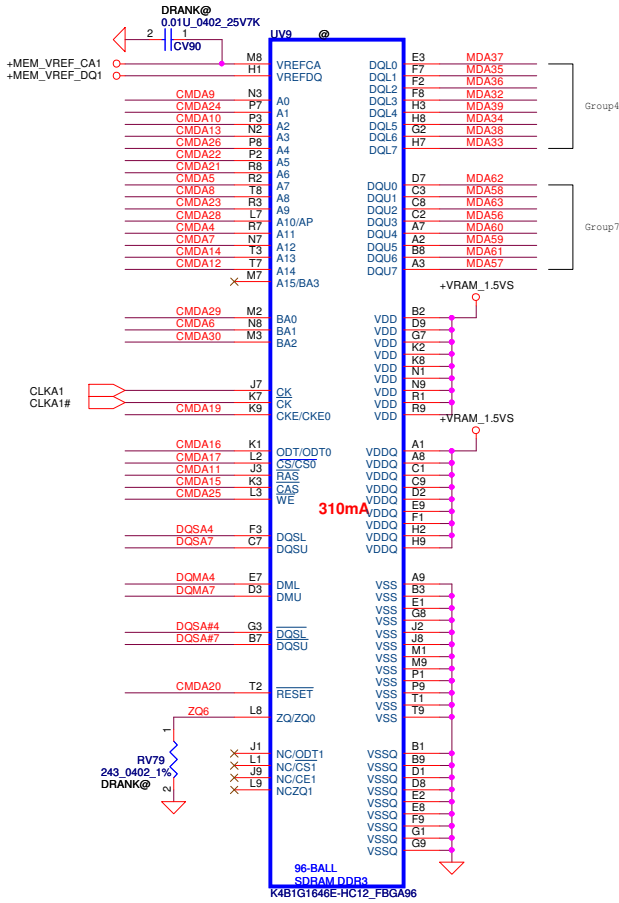
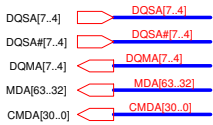
# RANK 1 [31...0] VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

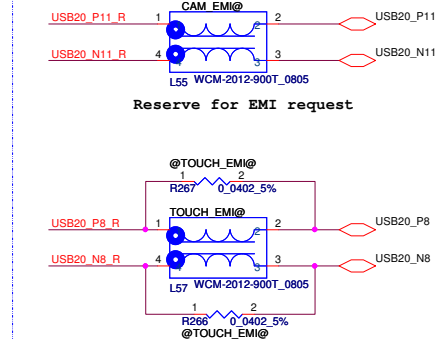
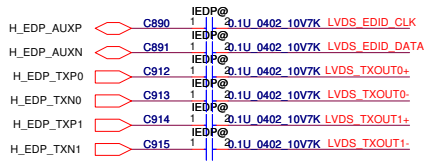
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/28	Deciphered Date	2013/09/28	Title
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Date:	Monday, March 11, 2013	Sheet	20	of 56

# RANK 1 [63...32] VRAM DDR3 Chips



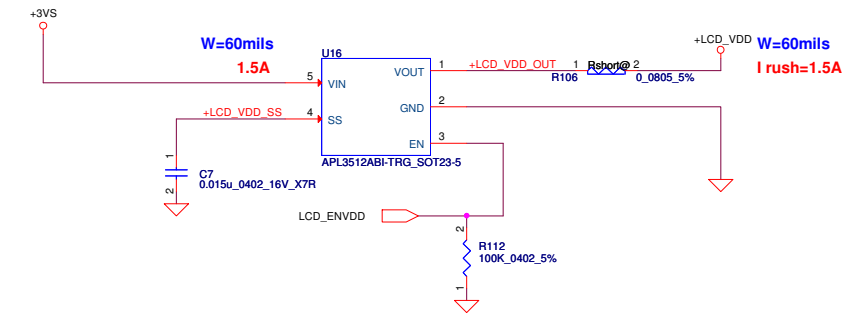
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

### For eDP Panel

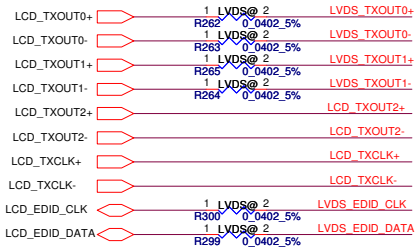


### LCD POWER CIRCUIT

Need check eDP&LVDS both 3V power rail.



### For LVDS 1ch Panel



Reserve for EMI request

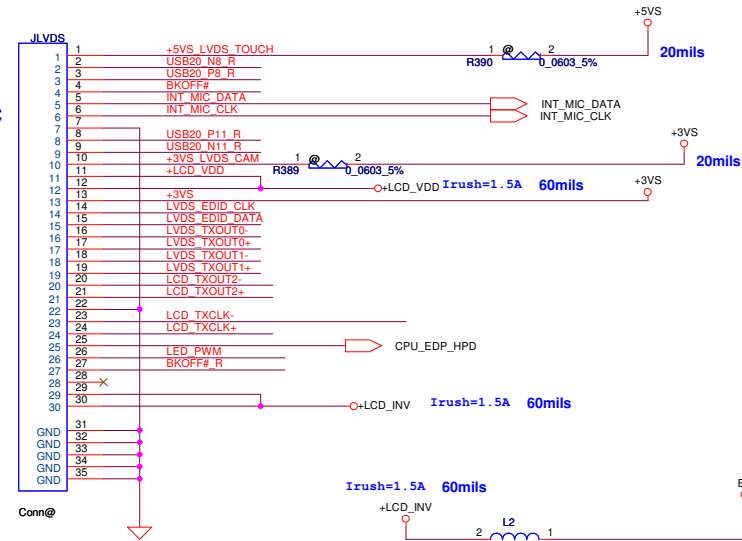
### LVDS coloy eDP cable

Pin define will be change after ME ready

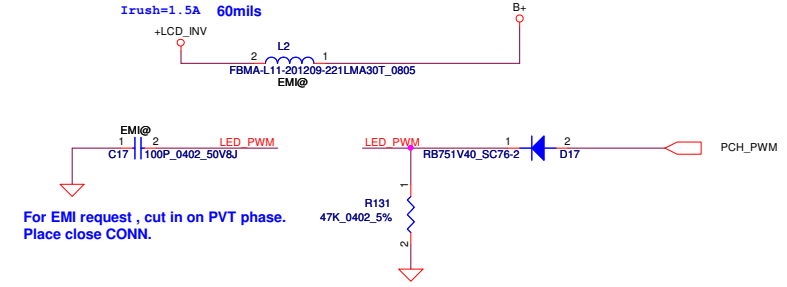
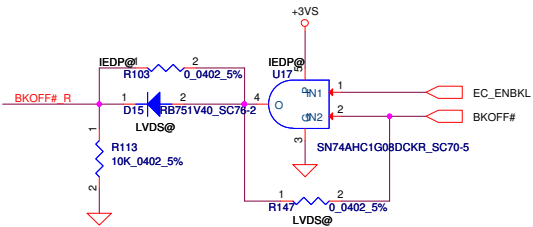
pin1-4 Touch function for panel

pin5-10 For Webcam with single or dual MIC

pin11-30 For LVDS or EDP panel

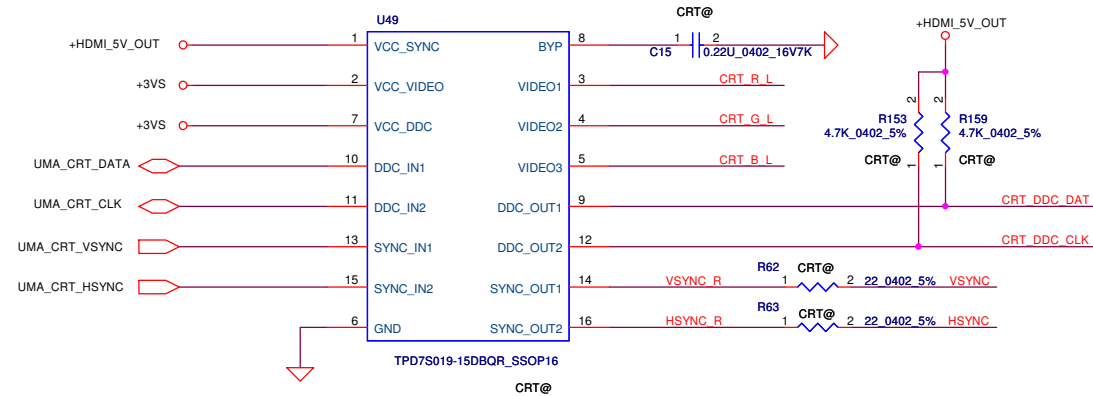
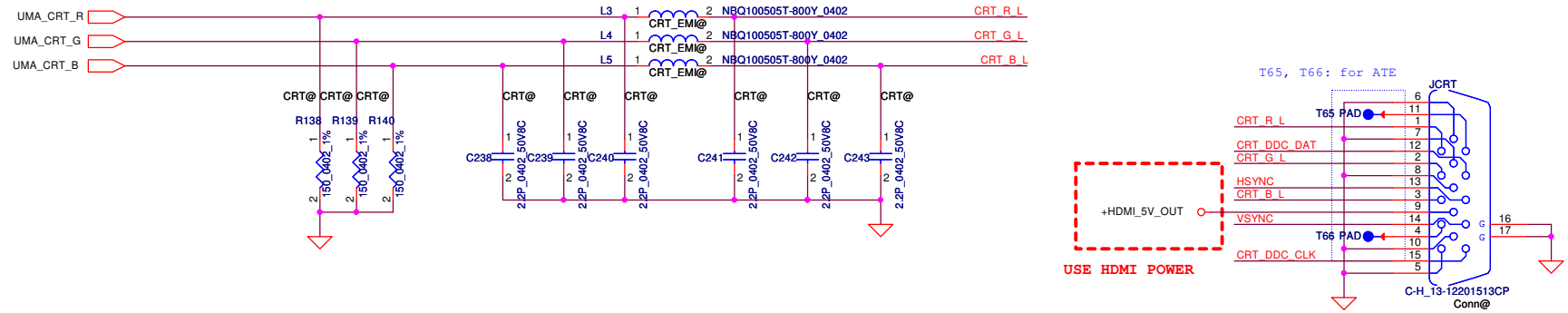


### Reserve for eDP panel potential issue

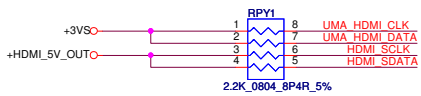


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Issued Date	2012/09/24	Deciphered Date	2013/09/24	LVDS
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				Rev 1.0
				Sheet 22 of 56

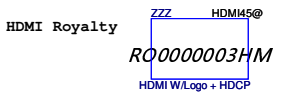
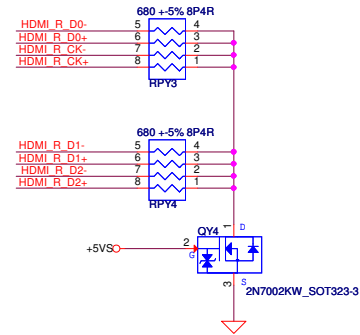
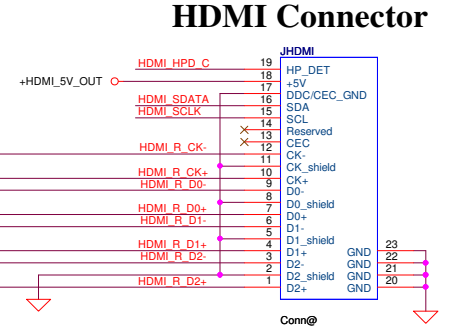
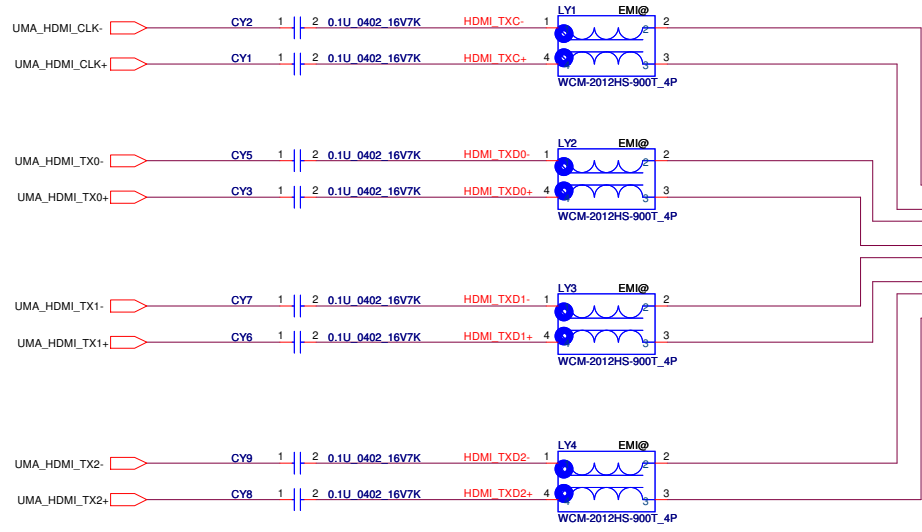
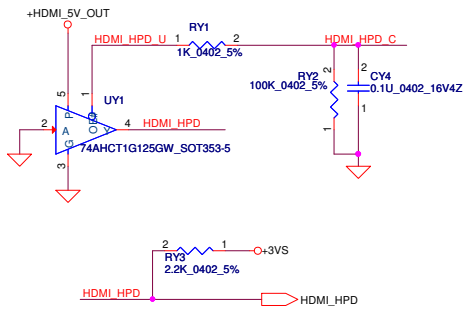
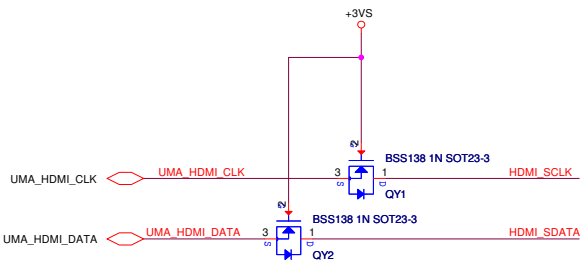
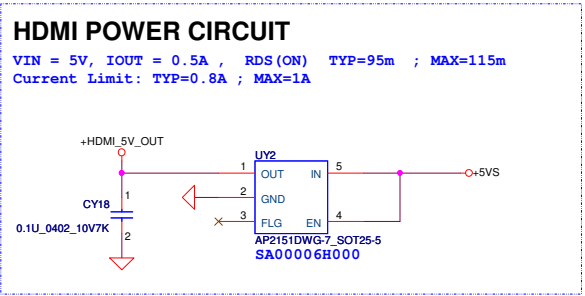
# CRT CONNECTOR



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title <b>CRT</b>	
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				Date	Monday, March 11, 2013
				Sheet	23 of 56
				Rev	1.0



OE#	A	Y
L	L	L
L	H	H
H	X	Z

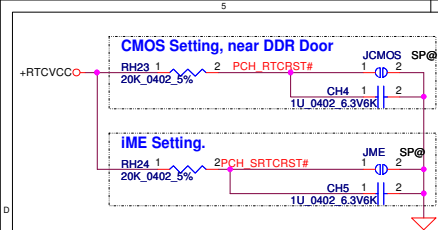


HDMI W/O Logo: RO0000001HM  
HDMI W/Logo: RO0000002HM  
HDMI W/Logo + HDCP: RO0000003HM

please manually load  
this virtual material to 45@ BOM

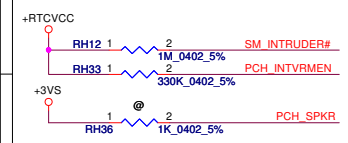
Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Compal Electronics, Inc.	
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				VFKTA	1.0
Date: Monday, March 11, 2013				Sheet	24 of 56



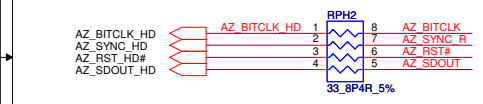
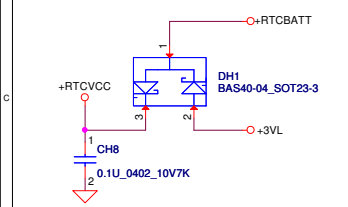


**Integrated SUS 1.05V VRM Enable**

PCH\_INTVRMEN High - Enable Internal VRs (must be always pulled high)

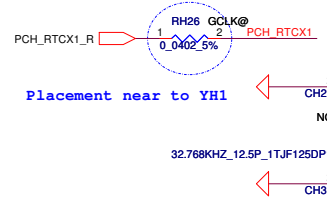
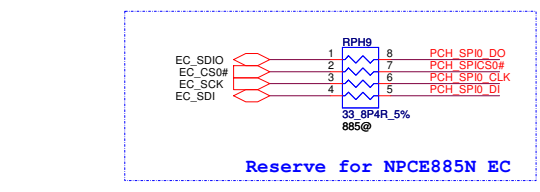
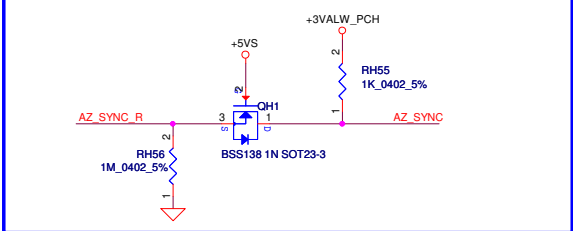


**PCH\_SPKR**  
 High = Enabled "No Reboot Mode"  
 Low = Disabled (Default)

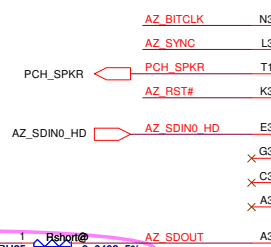


**HDA\_SDO**  
 ME debug mode,  
 this signal has a weak internal pull down  
 \*Low = Disable (default)  
 High = Enable (flash descriptor security override)

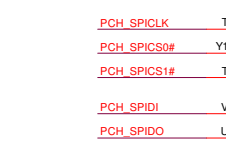
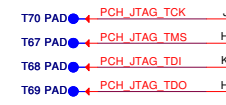
**HDA\_SYNC**  
 \*This signal has a weak internal pull down  
 H=>On Die PLL is supplied by 1.5V  
 L=>On Die PLL is supplied by 1.8V  
 Need to pull high for Chief River Mobile platform



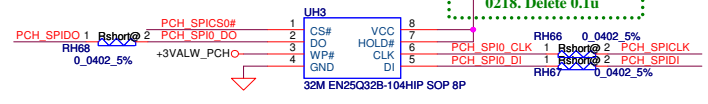
Placement near to YH1



Change Net name due to this function is high active



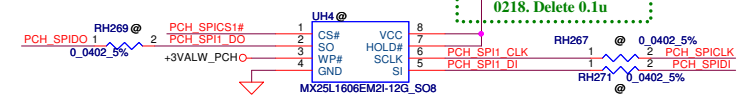
**SPI ROM for BIOS & ME (4MByte)**



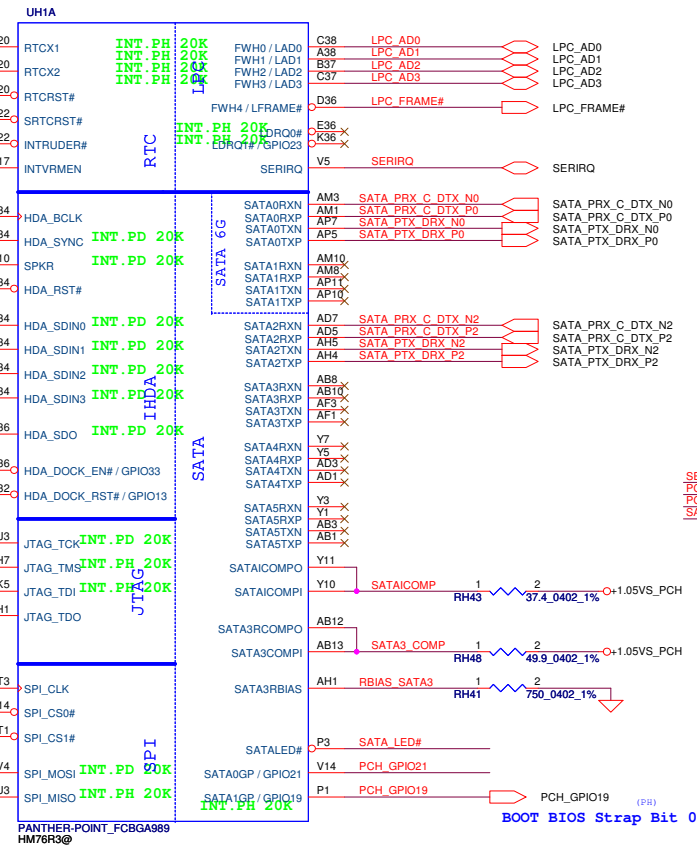
**4MB ROM P/N:**  
 SA00003K800  
 SA00004L100

Please place UH3 & UH4 close to UH1 PCH,  
 please place RH66, RH67, RH68 near UH3  
 Please place RH267 near RH66, Please place RH271 near RH67,  
 Please place RH269 near RH68.

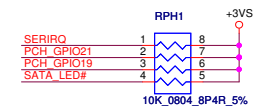
**SPI ROM (2MByte)**



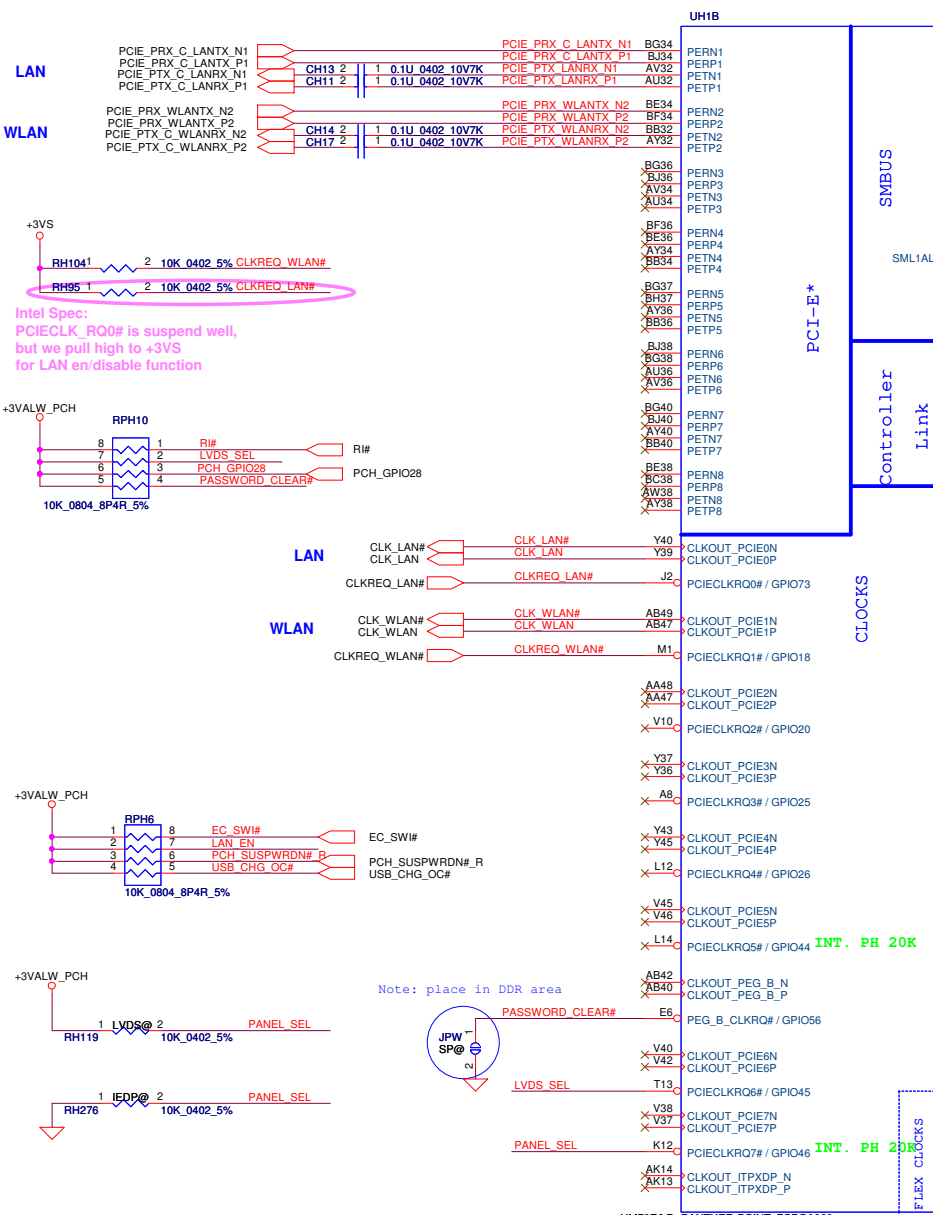
**2MB ROM P/N:**  
 SA000041N00  
 SA00003F010



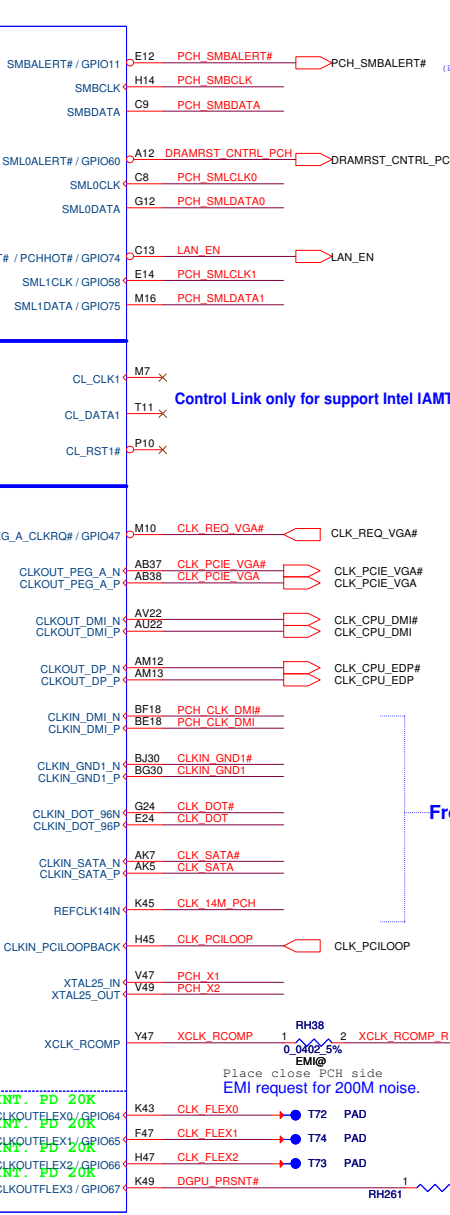
**HDD**  
**ODD**



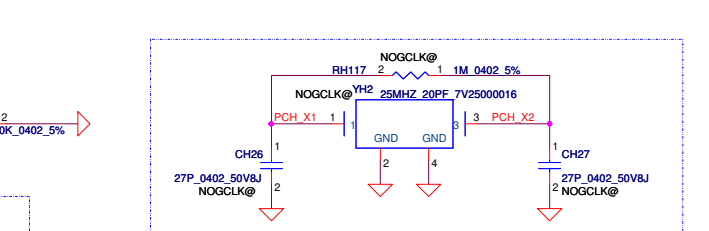
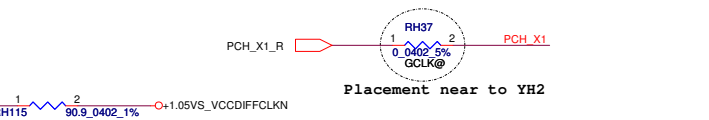
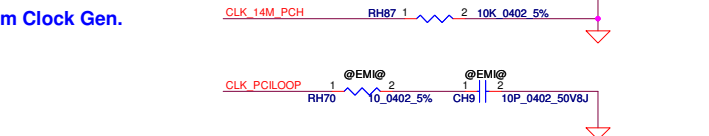
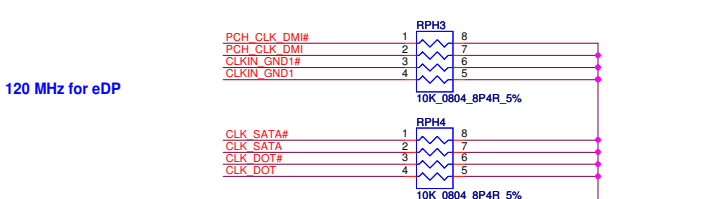
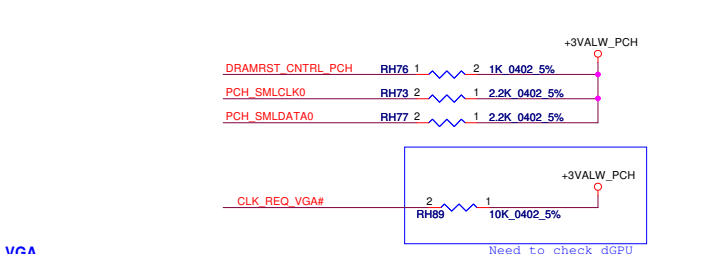
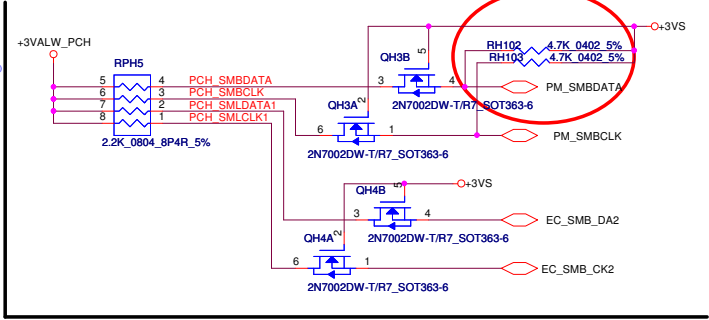
Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	PCH HDA/JTAG/SATA/SPI/LPC	
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Date	Monday, March 11, 2013	Sheet	25	of 56	

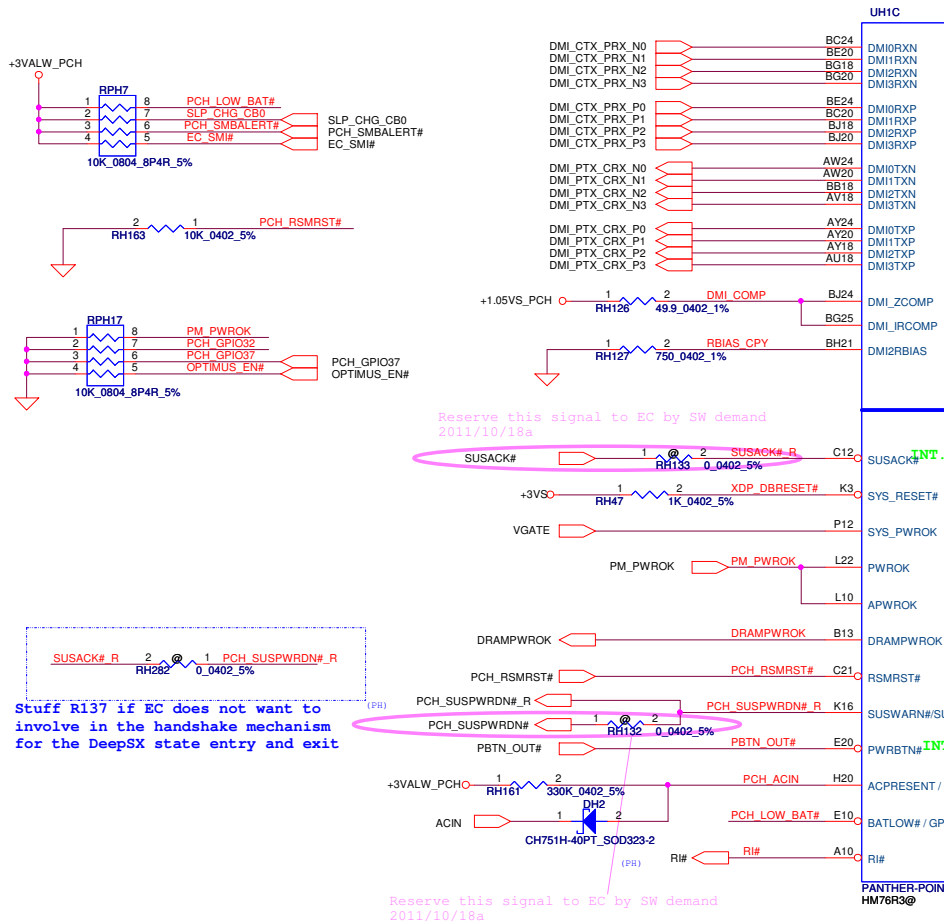


LVDS_SEL			PANEL_SEL		
LVDS_SEL	H	L	PANEL_SEL	H	L
Channel	Single (Default)	Dual	Channel	LVDS	EDP



DGPU_PRSENT#		
DGPU_PRSENT#	H	L
M/B SKU	UMA	DIS/OPT

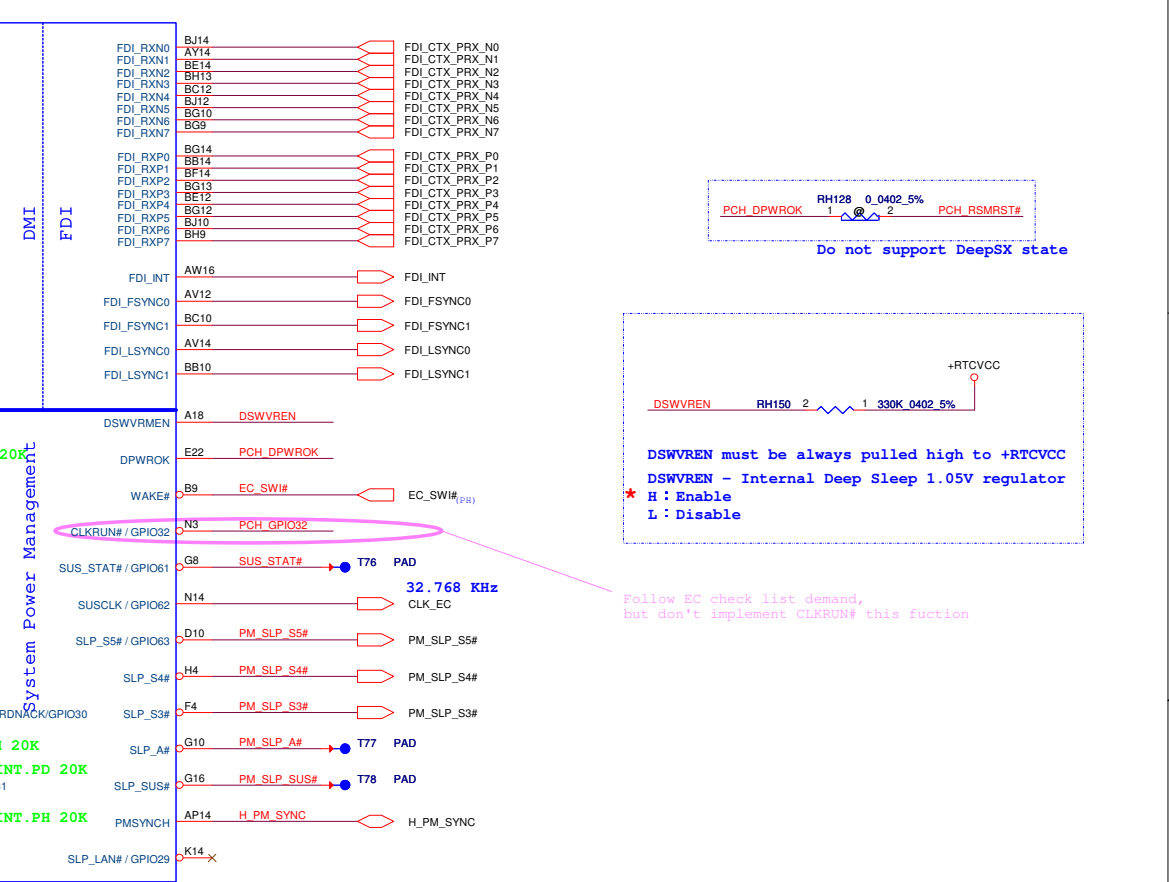
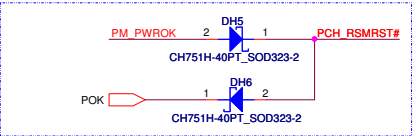




Stuff R137 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

Reserve this signal to EC by SW demand 2011/10/18a

Reserve this signal to EC by SW demand 2011/10/18a

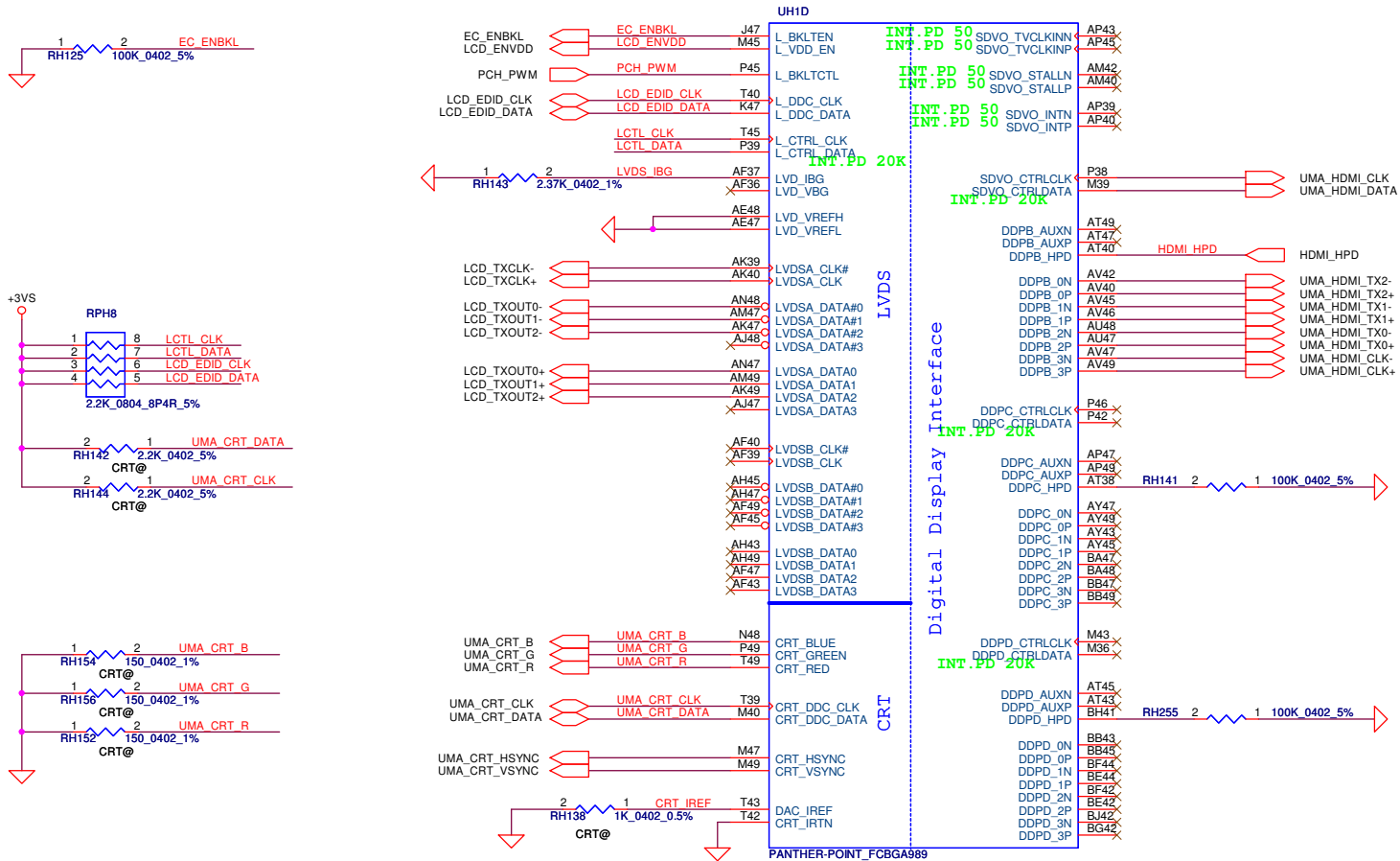


PCH\_DPWROK RH128 0\_0402\_5% PCH\_RSMRST#  
Do not support DeepSX state

DSWVREN RH150 2 330K 0402 5% +RTCVCC  
DSWVREN must be always pulled high to +RTCVCC  
DSWVREN - Internal Deep Sleep 1.05V regulator  
\* H : Enable  
L : Disable

Follow EC check list demand, but don't implement CLKRUN# this function

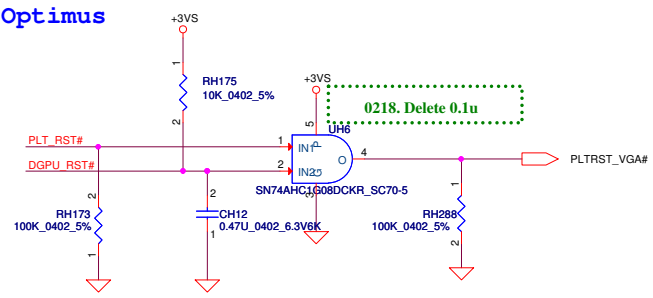
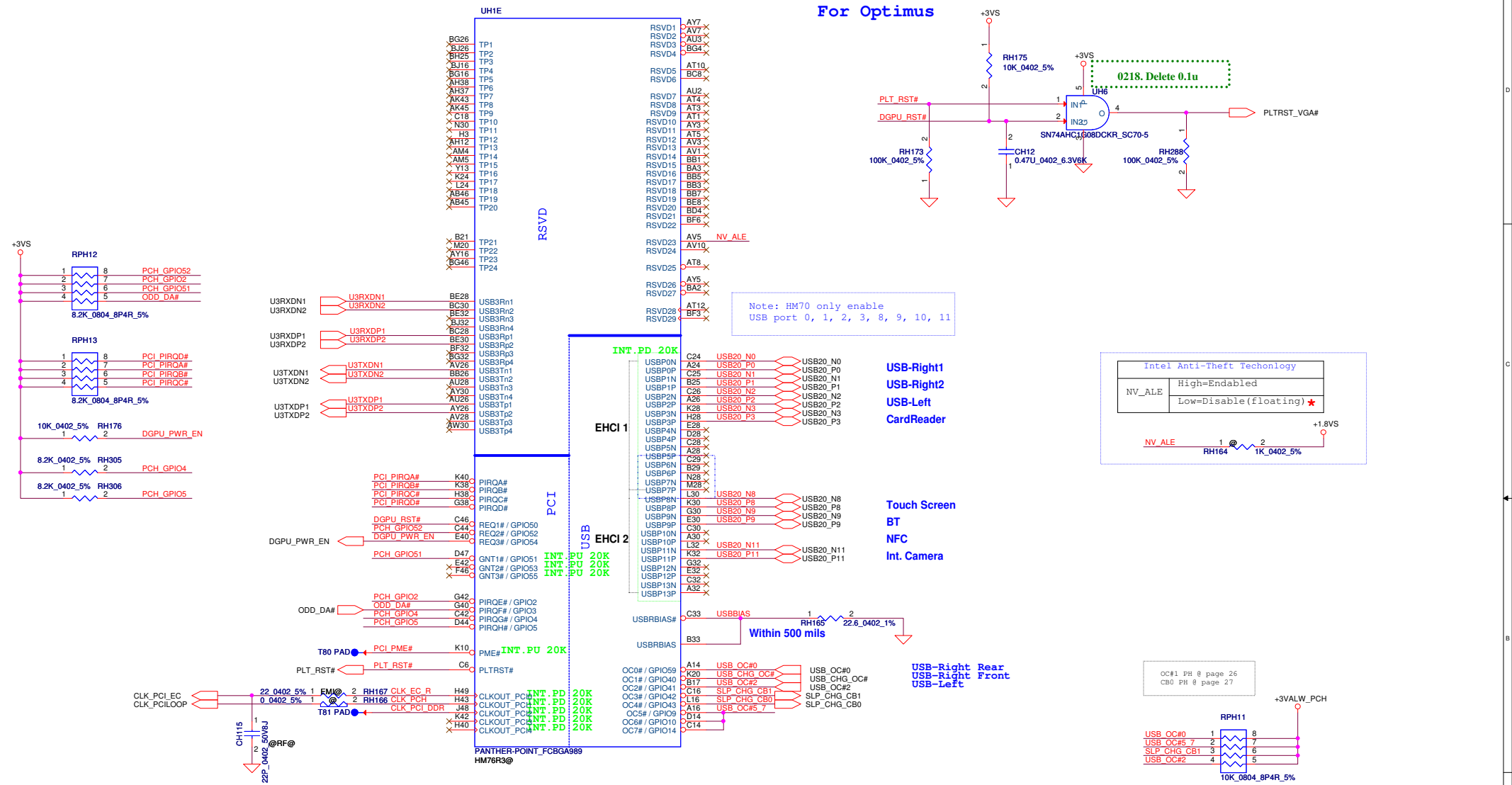
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title
				PCH_DMI/FDI/PM
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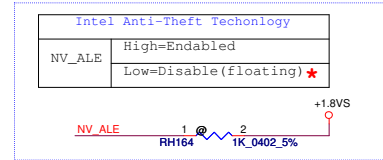
RH138  
1K\_0402\_5%  
NOCRT@

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Size	Document Number	Rev		1.0	
Custom	VFKTA	Date:		Monday, March 11, 2013	
				Sheet	28 of 56

For Optimus



Note: HM70 only enable  
USB port 0, 1, 2, 3, 8, 9, 10, 11

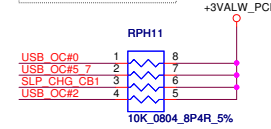


USB-Right1  
USB-Right2  
USB-Left  
CardReader

Touch Screen  
BT  
NFC  
Int. Camera

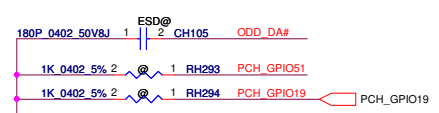
USB-Right Rear  
USB-Right Front  
USB-Left

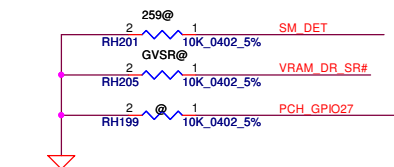
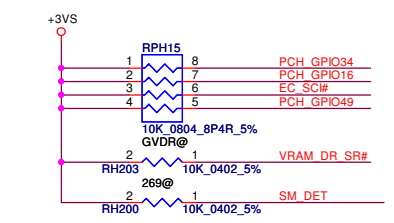
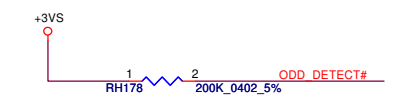
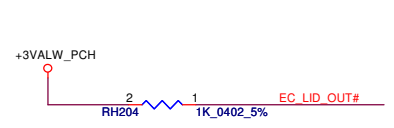
OC1 PH @ page 26  
CB0 PH @ page 27



Boot BIOS Strap		
PCH_GPIO19	PCH_GPIO51	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
*	High= A16 swap override Disable





**GPIO28**  
 On-Die PLL Voltage Regulator  
 H: Enable  
 L: Disable

**GPIO8**  
 Integrated Clock Chip Enable (Removed)  
 H: Disable  
 L: Enable

Integrated clock enable functionality is achieved by soft-strap  
 The current default is clock enable

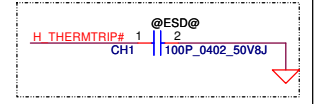
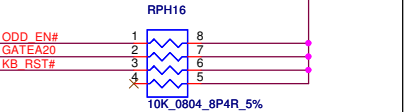
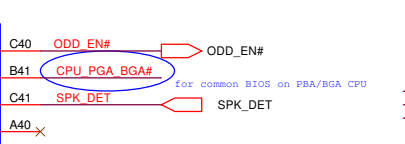
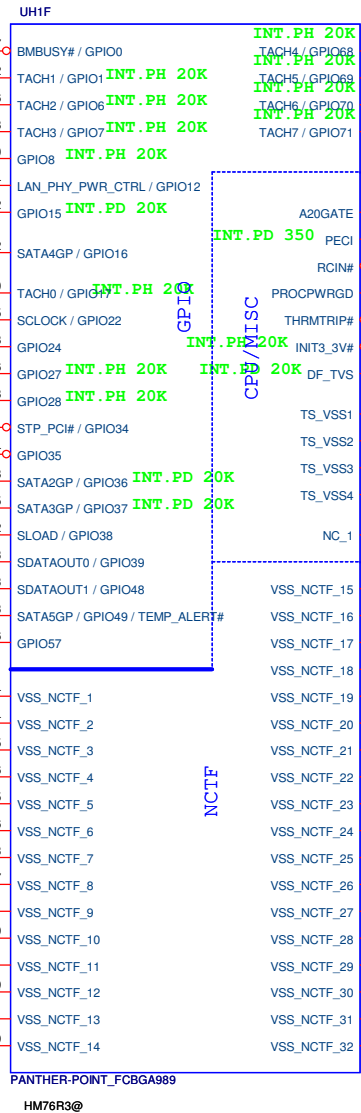
VRAM_DR_SR#	0	Single Rank
	1	Dual Rank

Follow Compal ORB and Intel Check list 460603 V1.5

**OPTIMUS\_EN#**

OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

For Optimus



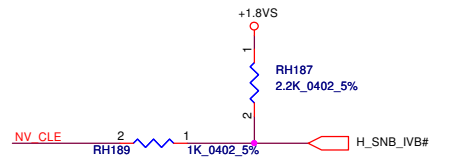
SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

**Non-Harman detection**

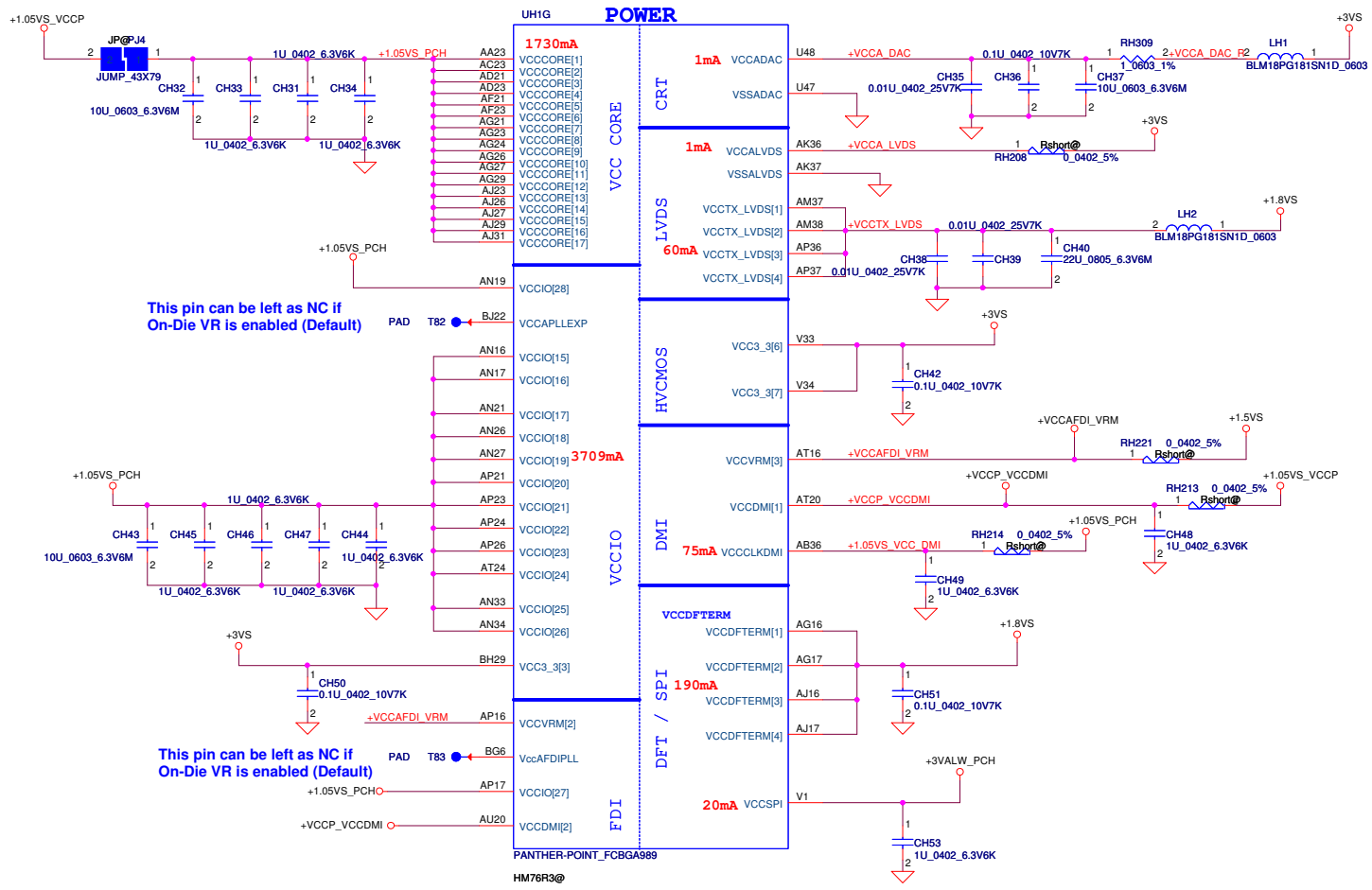
SPK_DET	0	ONKYO
	1	Non-Brand

**DMI & FDI Termination Voltage**

NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW



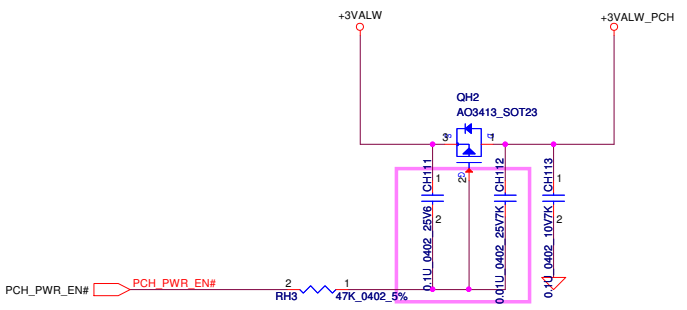
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	
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				VFKTA	
				Date:	Monday, March 11, 2013
				Sheet	30 of 56
				Rev	1.0



This pin can be left as NC if On-Die VR is enabled (Default)

This pin can be left as NC if On-Die VR is enabled (Default)

**+3VALW to +3VALW\_PCH**

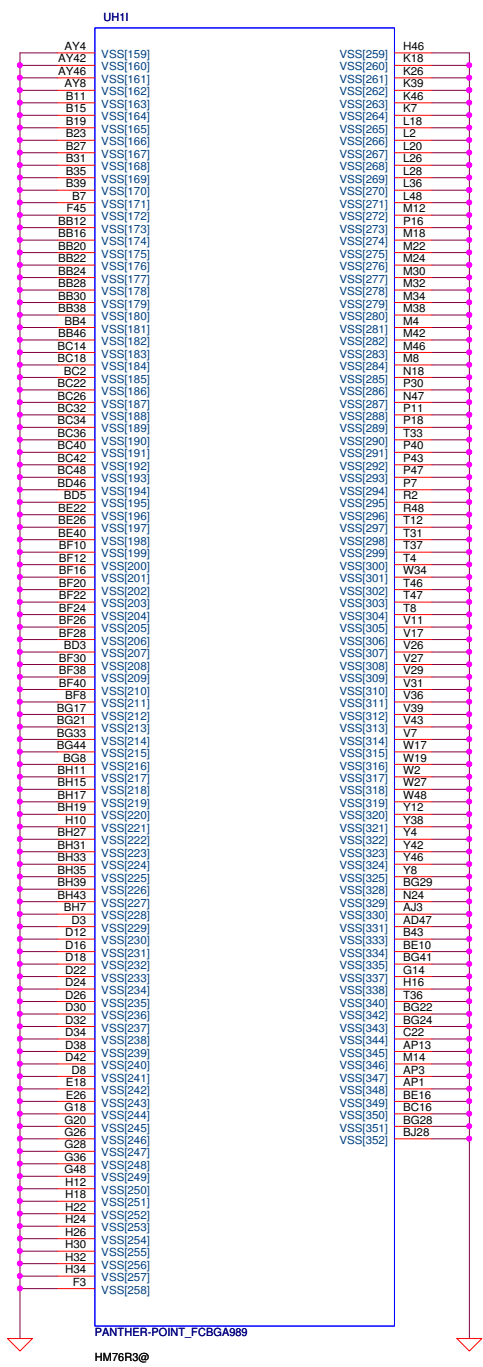
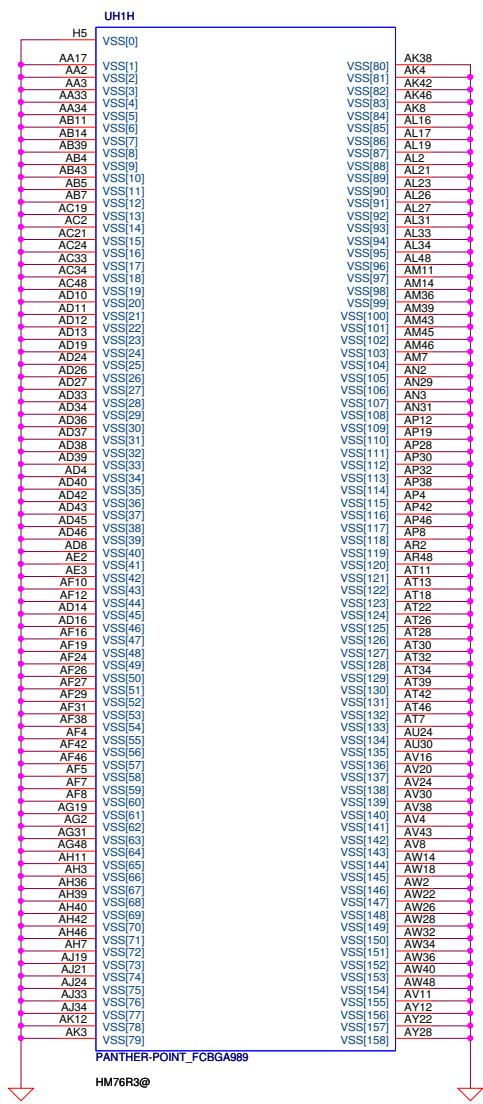


PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



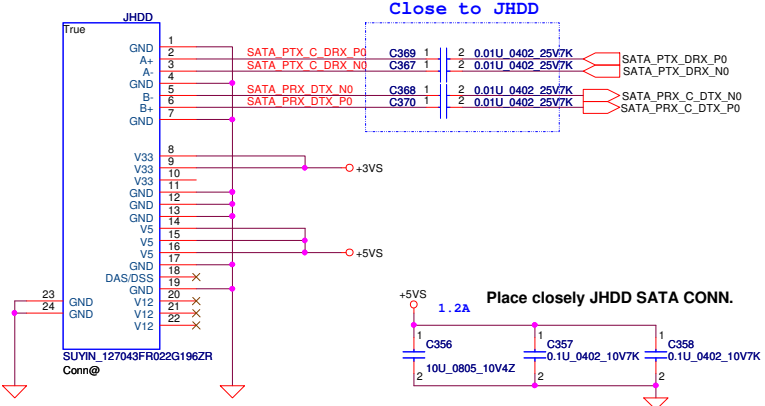




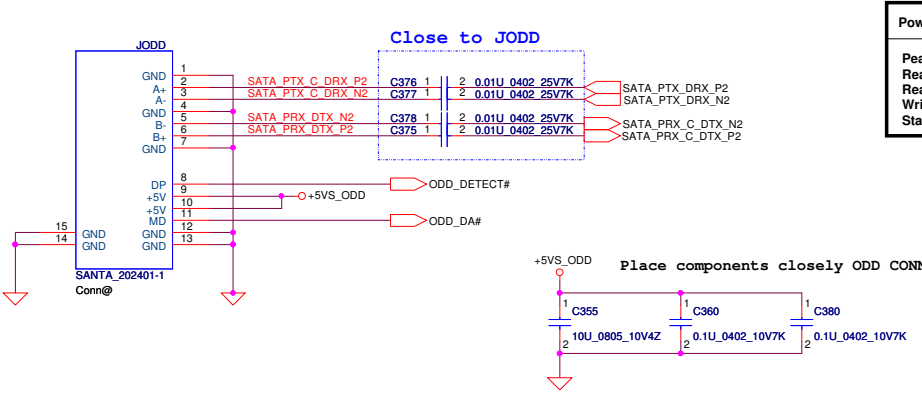


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Date:	Monday, March 11, 2013	Sheet	33	of 56

# SATA HDD Conn.

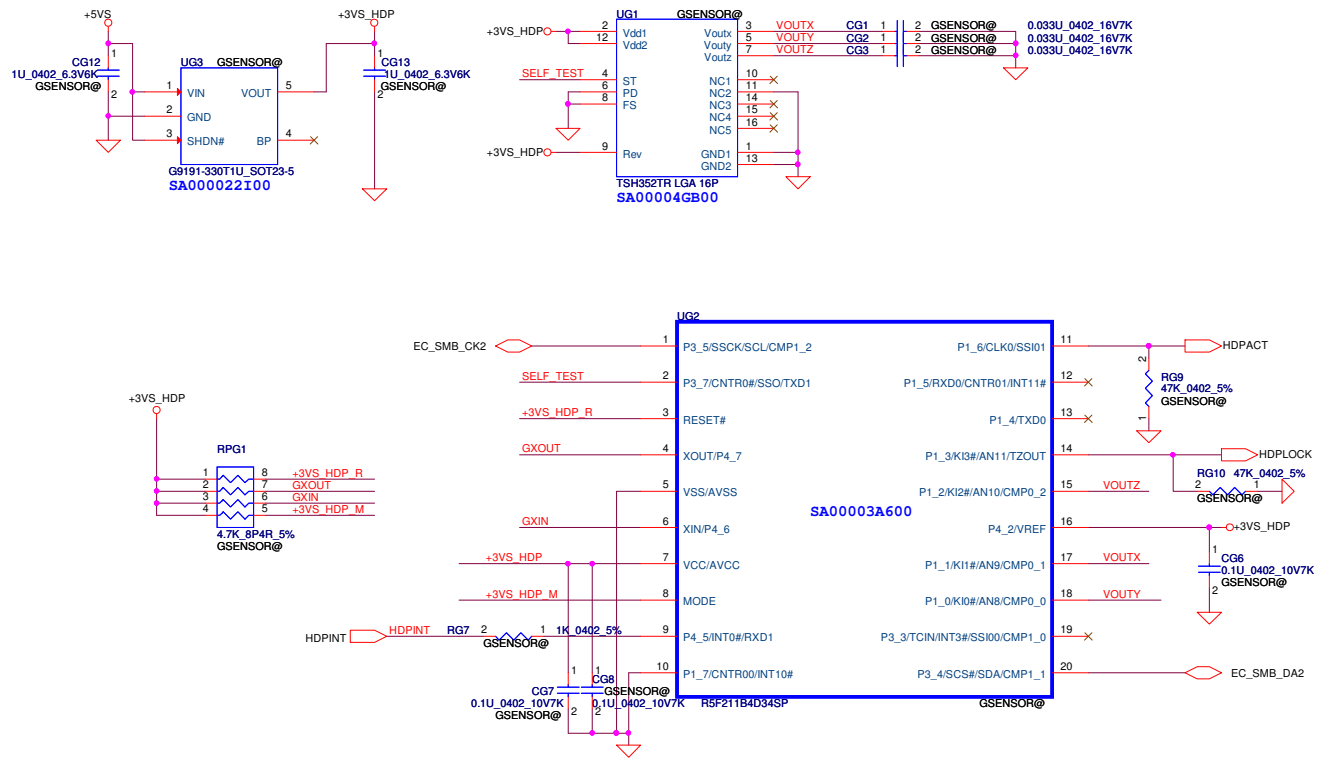


# SATA ODD Conn



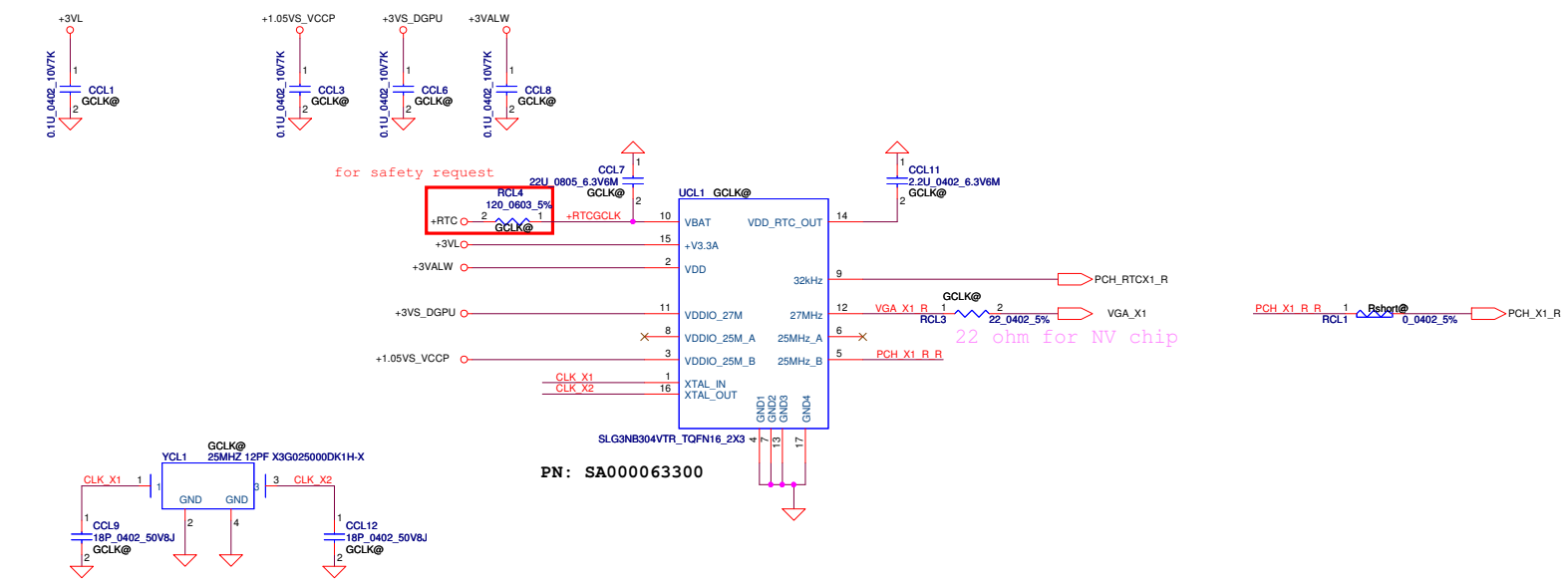
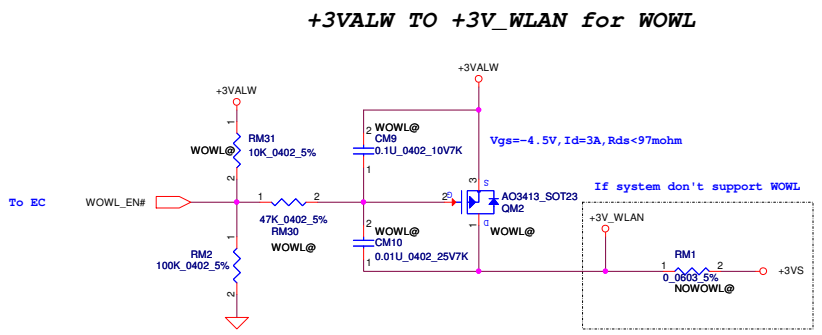
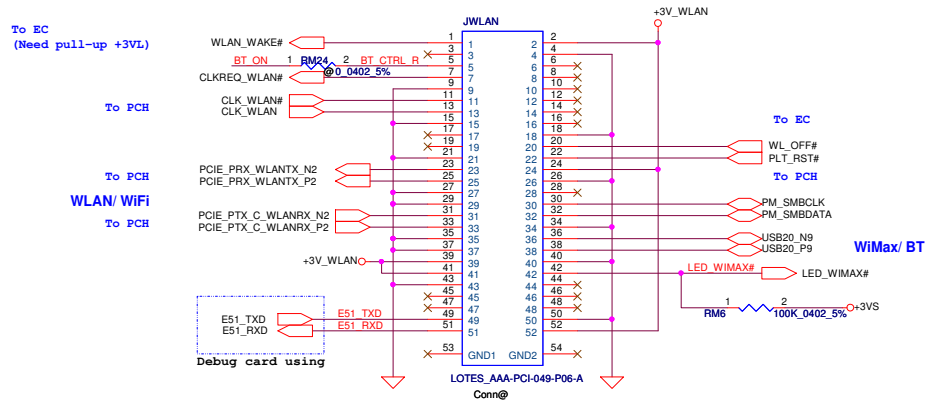
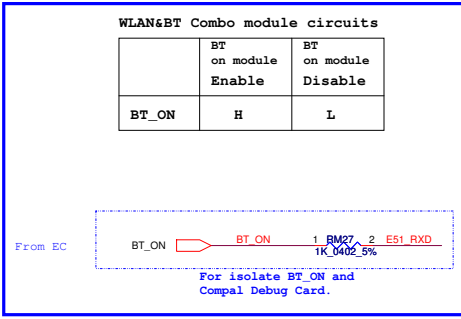
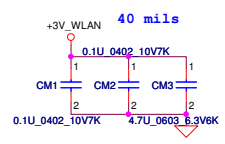
Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

# G-Sensor



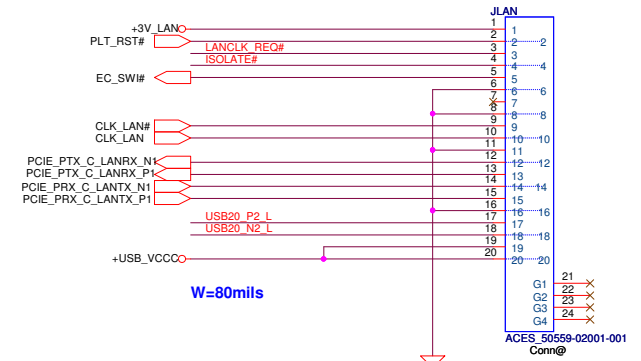
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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Document Number
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Date: Monday, March 11, 2013				Sheet 34 of 56

**Slot 1 Half PCIe Mini Card-WLAN**

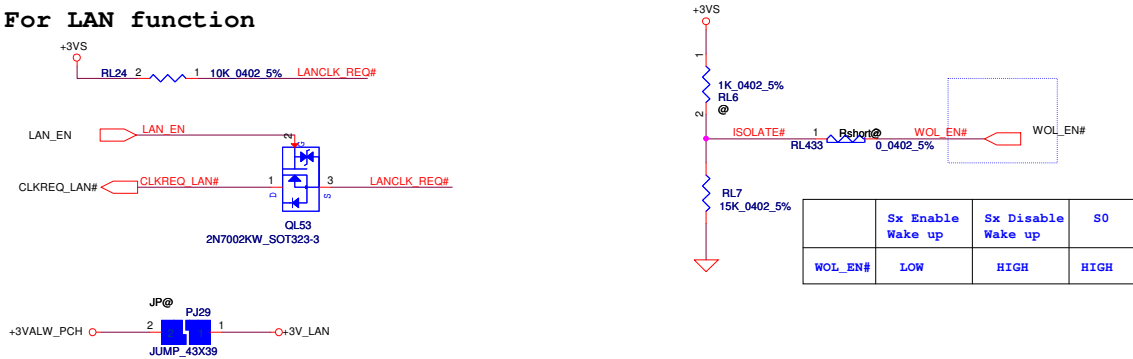


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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Date: Monday, March 11, 2013			Sheet: 35 of 56	Rev: 1.0

Left USB 2.0 x 1



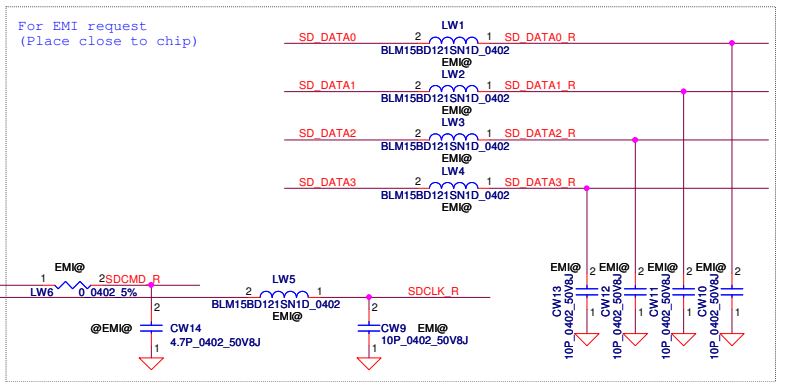
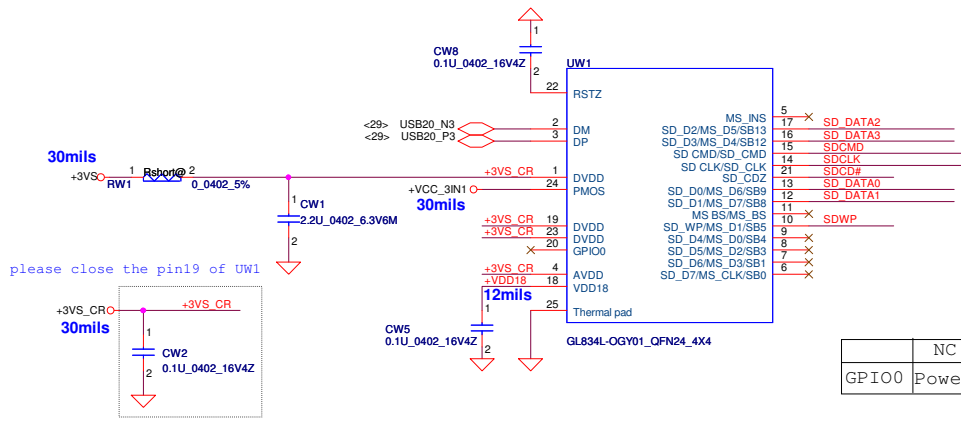
For LAN function



+3V\_LAN rising time (10%~90%) need > 1ms and <100ms.

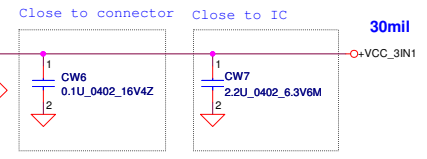
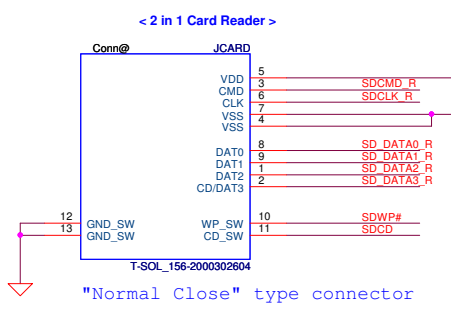
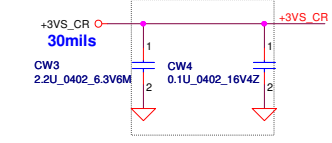
LAN	WOL	LAN_EN		ISOLATE#	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

\*  
S3: after SUSP# assert low over 100ms  
S4/S5: after SYSON assert low over 100ms

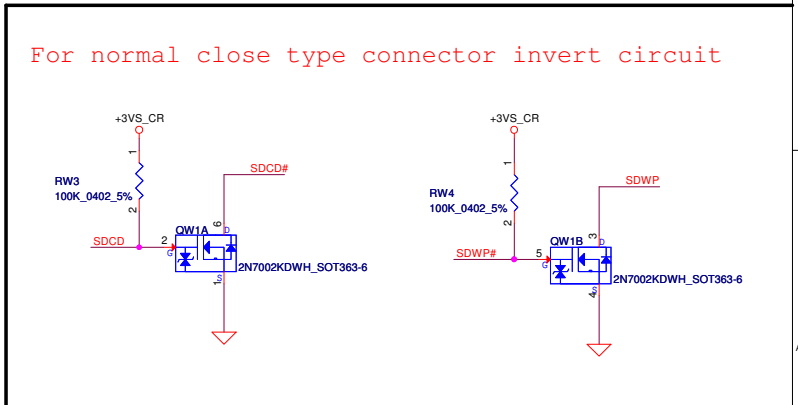


	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

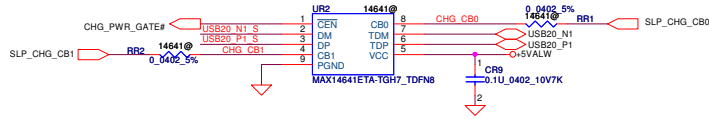
De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

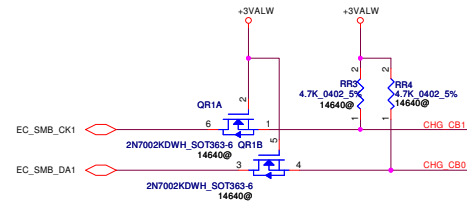


UR2  
Address  
0x35  
MAX1464ETA+TGH7  
14640@

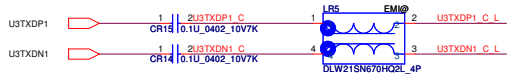
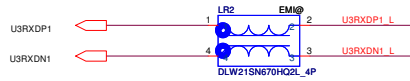
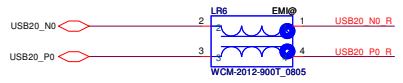


### USB Sleep & Charge

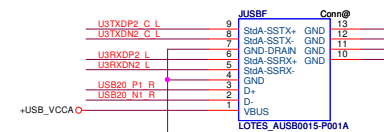
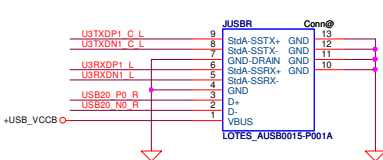
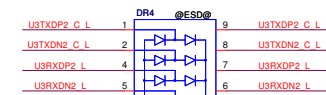
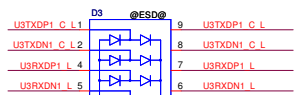
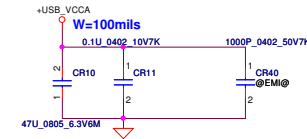
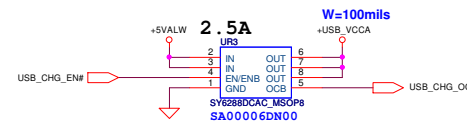
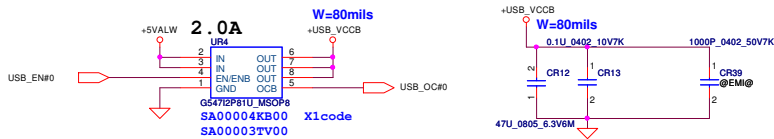
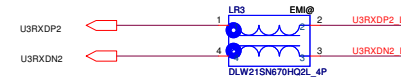
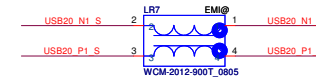
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode. DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



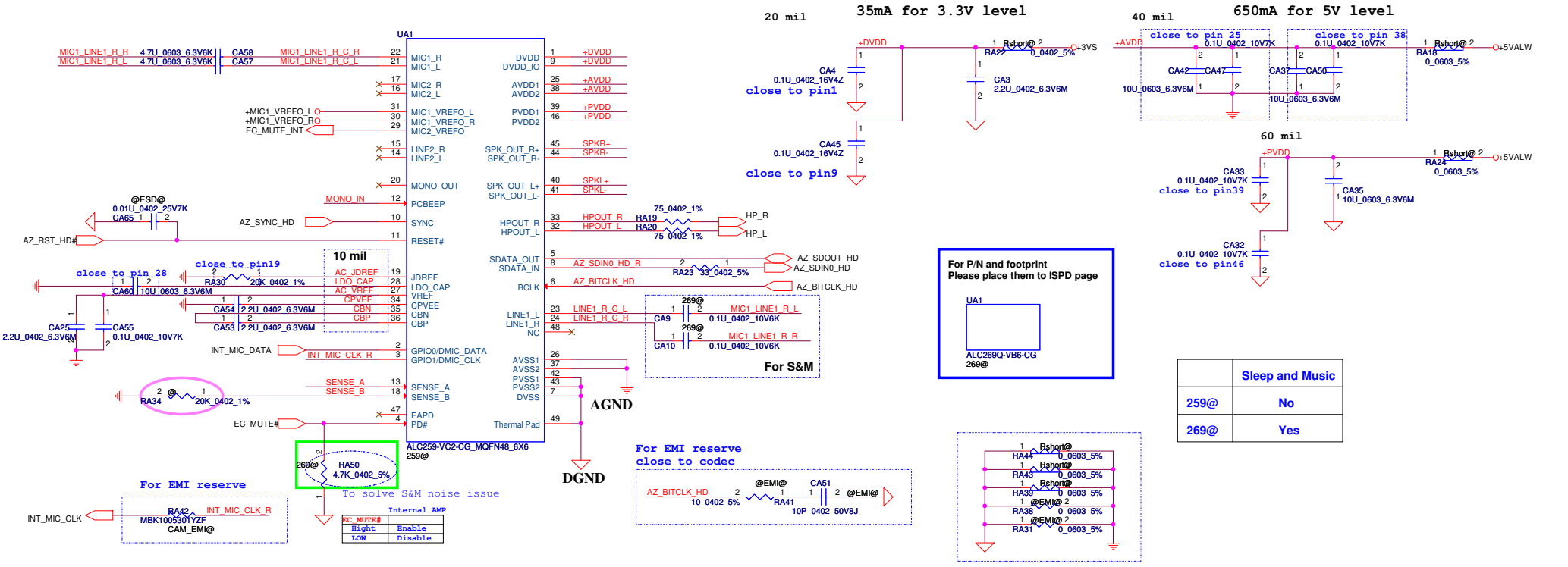
### Right rear USB3.0 Conn.



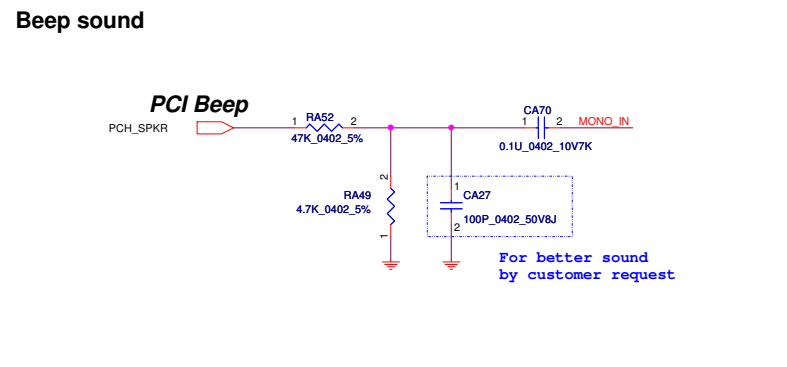
### Right front USB3.0 Conn. (Support S&C function)



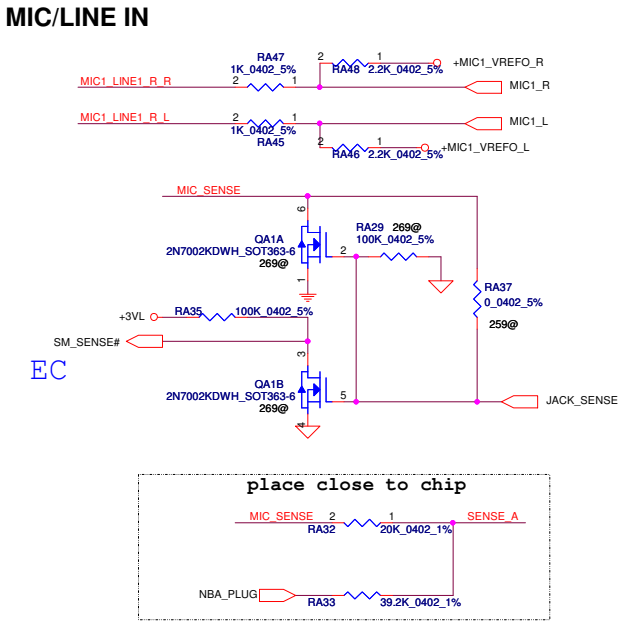
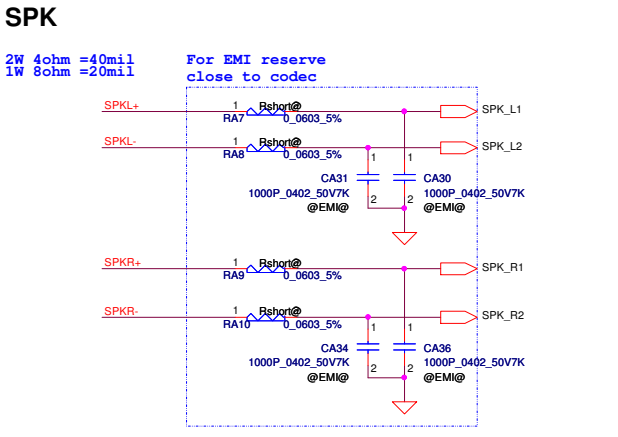
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	<b>RUSB30/S&amp;C</b>	
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			Date:	Monday, March 11, 2013	Sheet 38 of 56



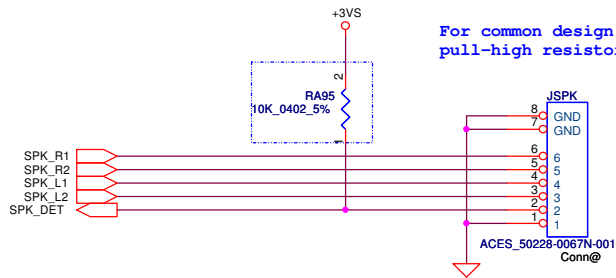
	Sleep and Music
259@	No
269@	Yes



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



# SPK Conn.



For common design, pull-high resistor should be placed at connector side.

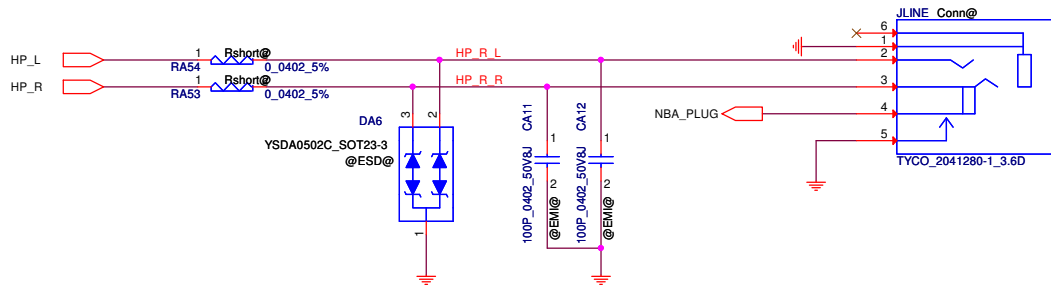
<SM\_DET>  
 Intel : GPIO48  
 AMD Richland : GPIO173  
 AMD Kabini : GPIO70

<SPK\_DET>  
 Intel : GPIO70  
 AMD Richland : GPIO74  
 AMD Kabini : GPIO62

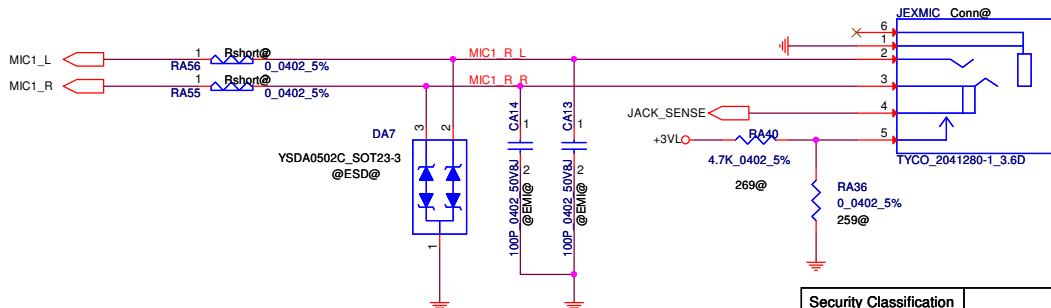
SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

# HeadPhone/LINE Out JACK

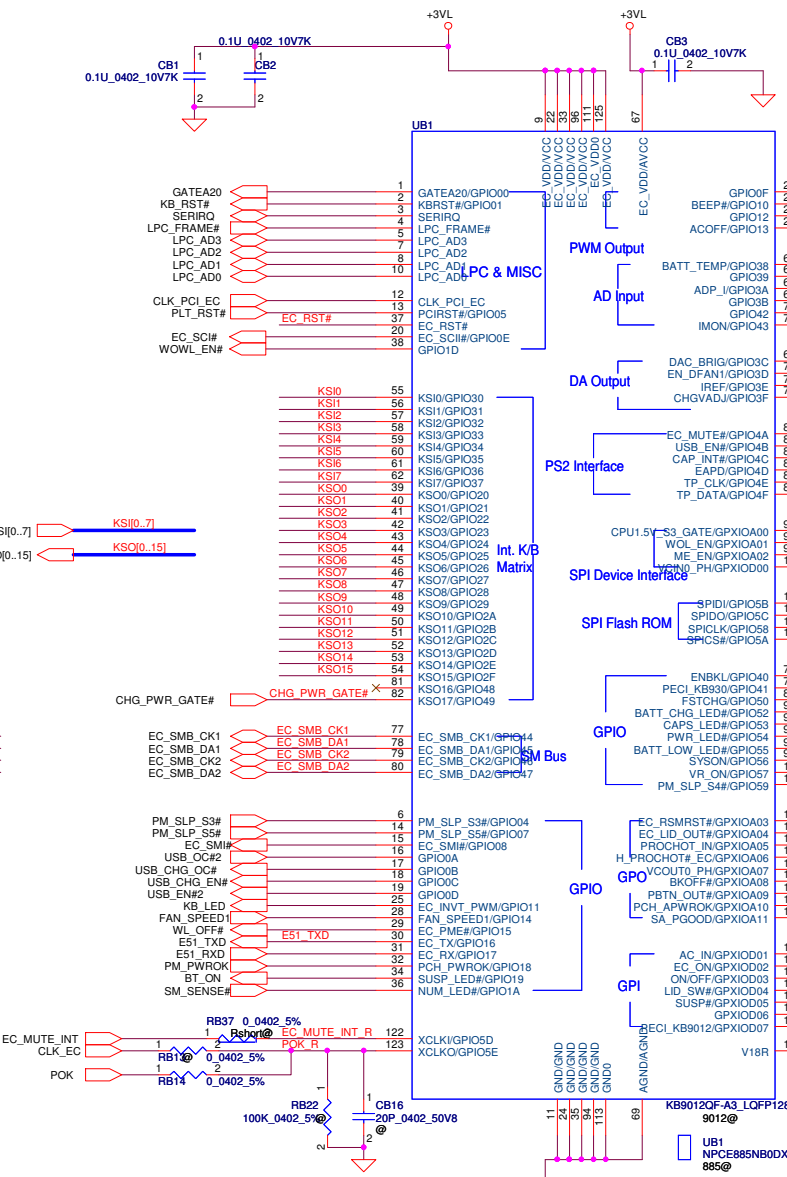
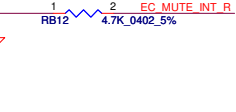
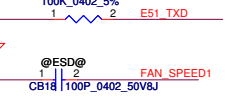
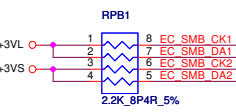
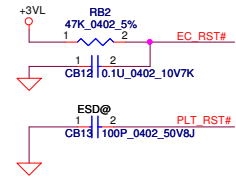
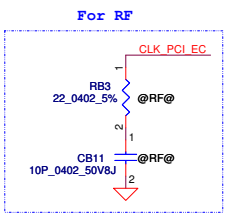


# MIC/LINE IN JACK



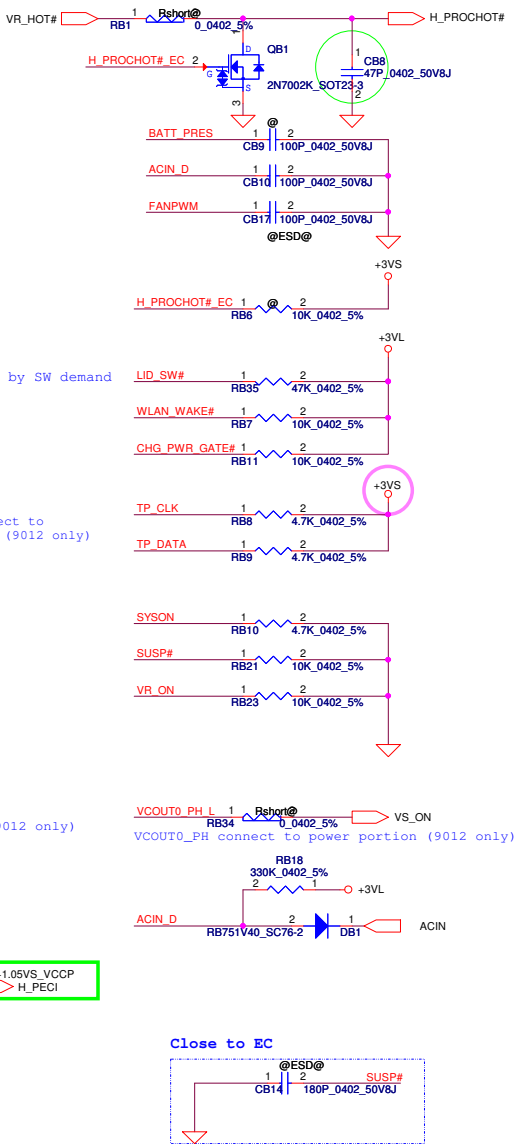
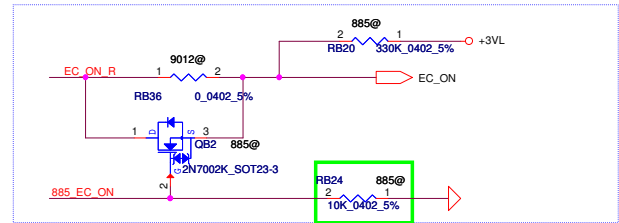
Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	AUDIO CONN
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Date:	Monday, March 11, 2013	Sheet	40 of 56	



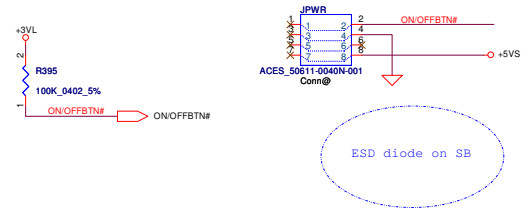


**Voltage Comparator Pins FOR 9012 A3**

VCIN0 pin109	>1.2V	<1.2V
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)

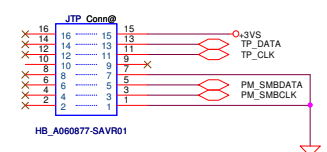


### Power Button



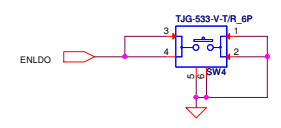
### Conn.

### Touchpad Connector

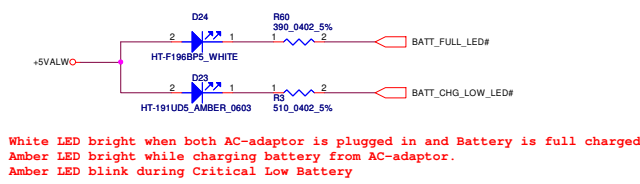


### NFC

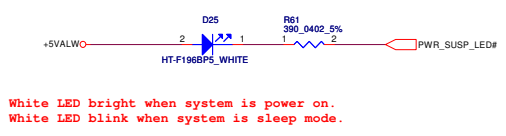
### Battery Reset



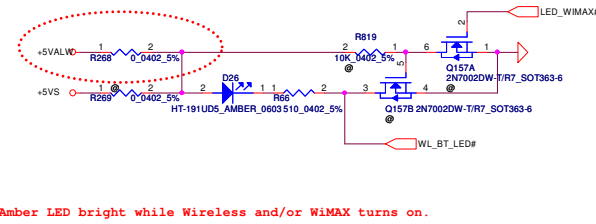
### BATT CHARGE / FULL LED



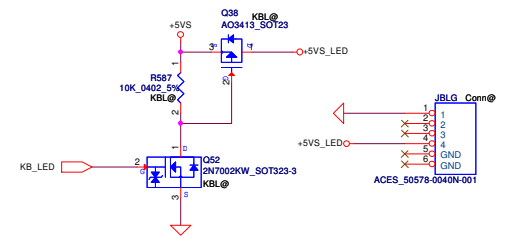
### POWER LED



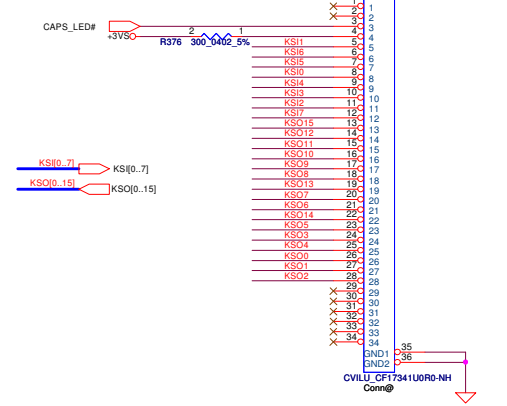
### WLAN/WiMAX LED



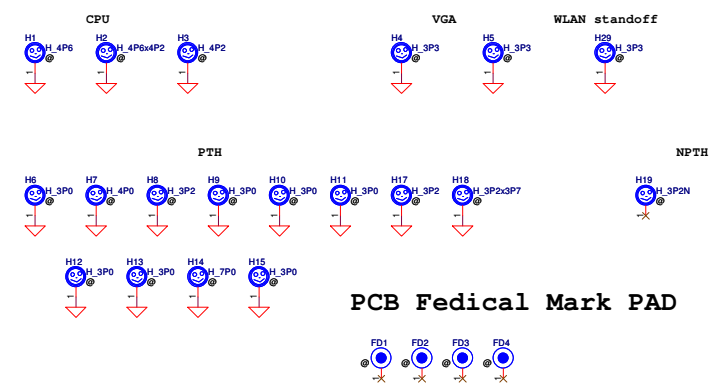
### Keyboard LED



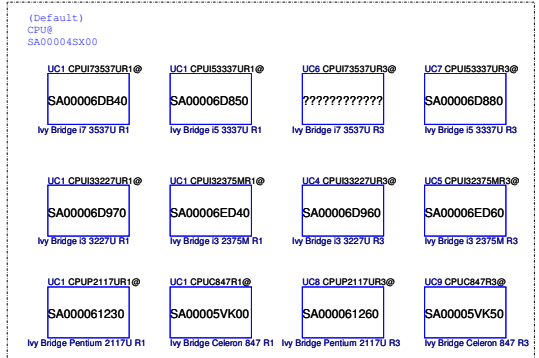
### KEYBOARD CONN.



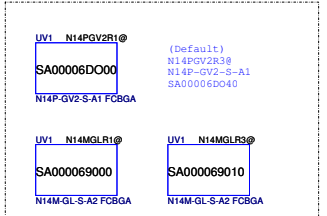
### Screw Hole



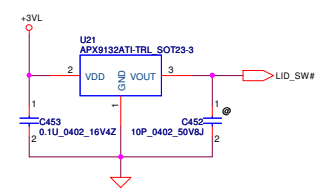
### CPU



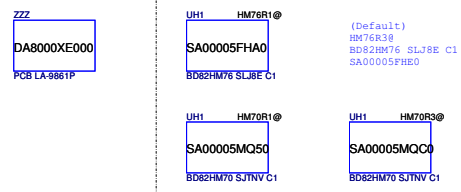
### GPU



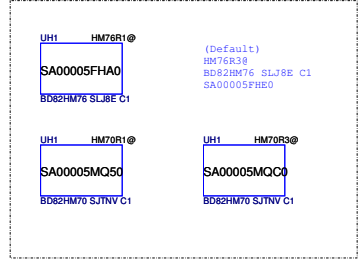
### Lid SW



### ISPD

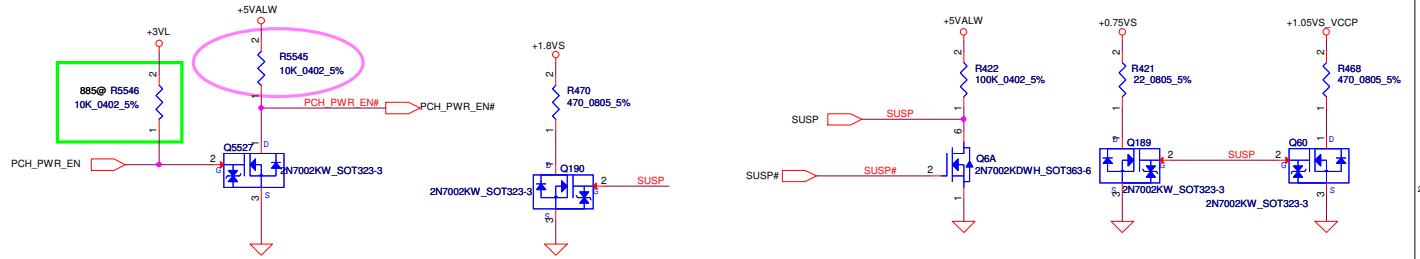
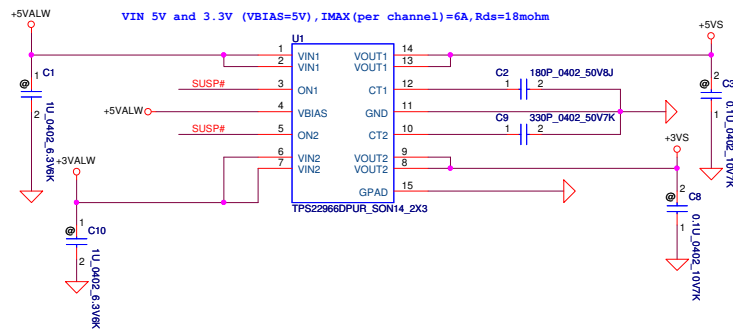


### PCH

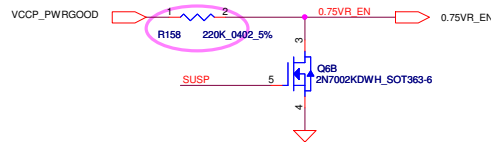


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Size	Document Number	Rev		1.0
Date:	Monday, March 11, 2013	Sheet	42	of 56

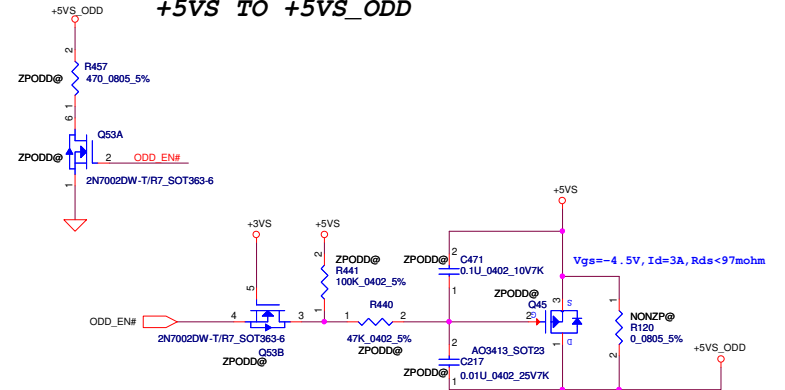
**+5VALW TO +5VS**  
**+3VALW TO +3VS**  
**Load switch**



**For S3 CPU Power Saving**

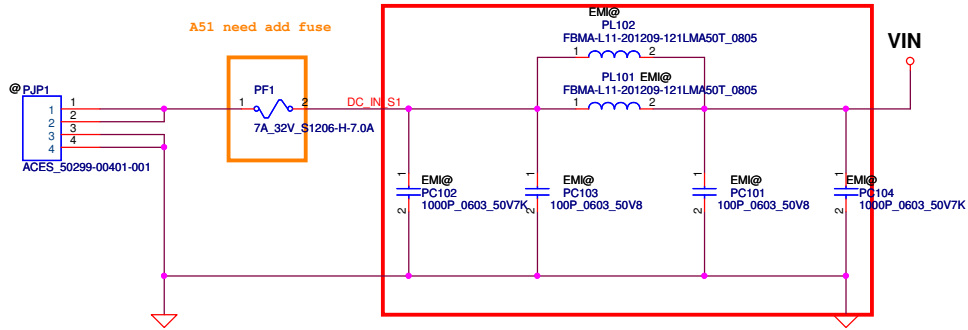


**+5VS TO +5VS\_ODD**



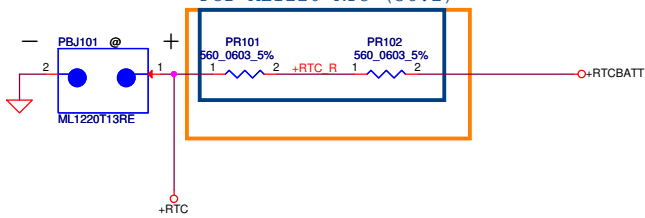
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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title
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				VFKAA
				Rev 1.0
				Date: Monday, March 11, 2013 Sheet 43 of 56

EMI Part (47.1)

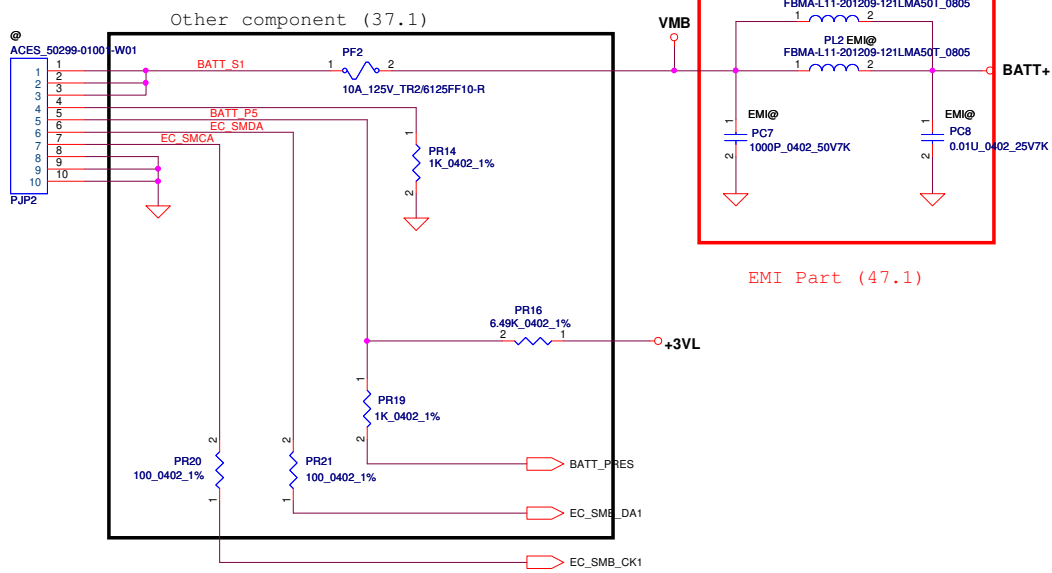


A51 need add fuse

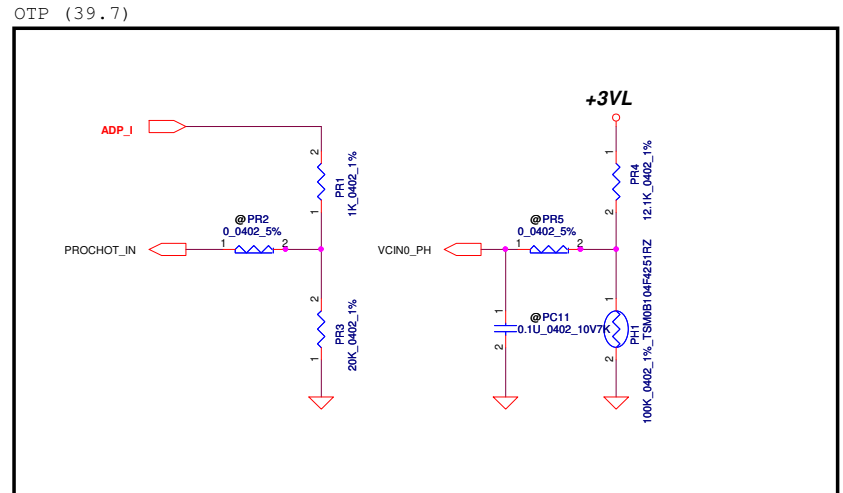
For ML1220 RTC (38.2)



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				Author	VFKTA
				Date:	Sheet 44 of 56



EMI Part (47.1)



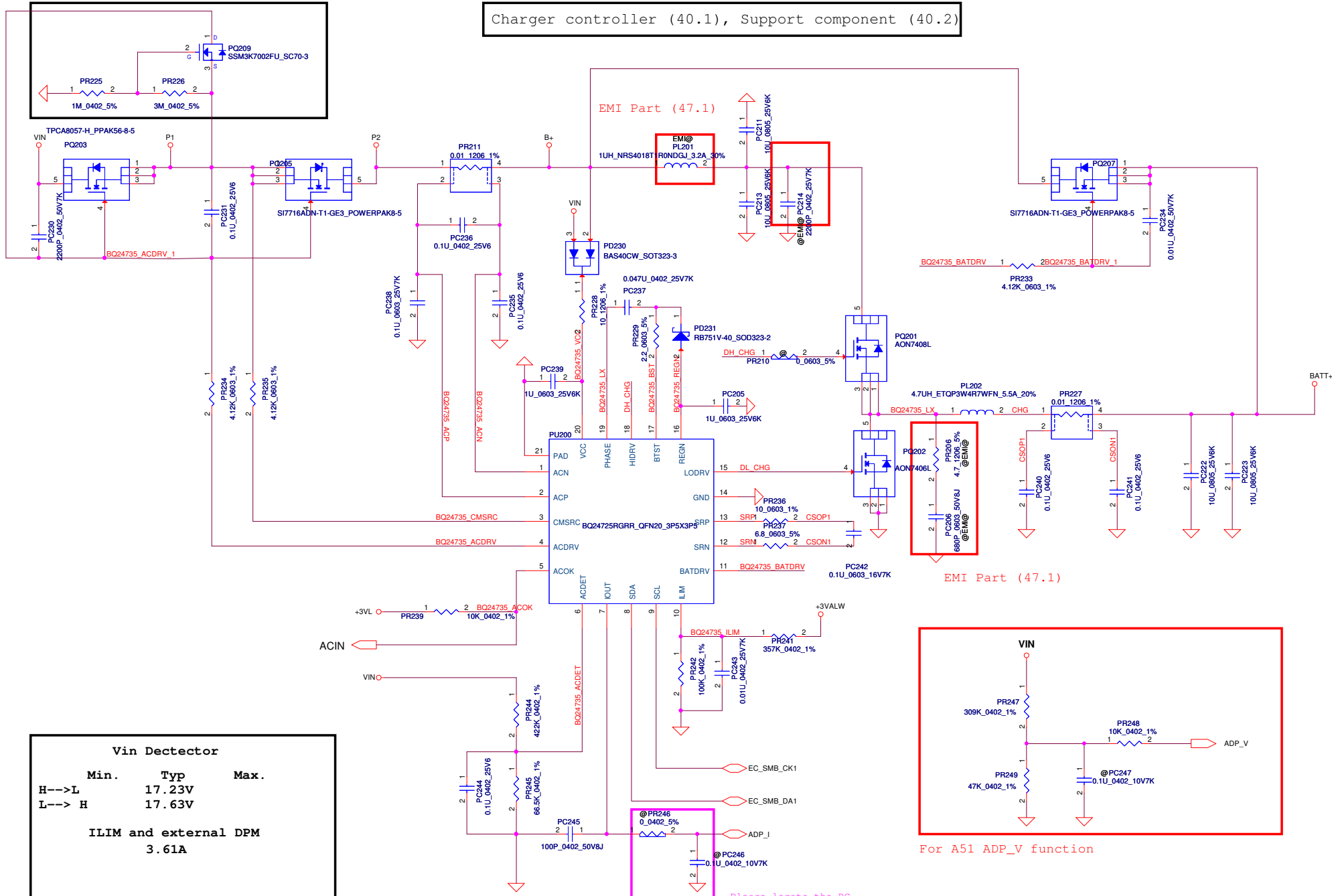
**PH1 under CPU bottom side :**  
**CPU thermal protection at 93 +/-3 degree C**  
**Recovery at 56 +/-3 degree C**

	Protect	Recovery
65W	0.752V	0.626V
75W	0.902V	0.722V

	Initial	Protect	Recovery
CPU OTP	65W	93 C	56 C

for reverse input protection

Charger controller (40.1), Support component (40.2)



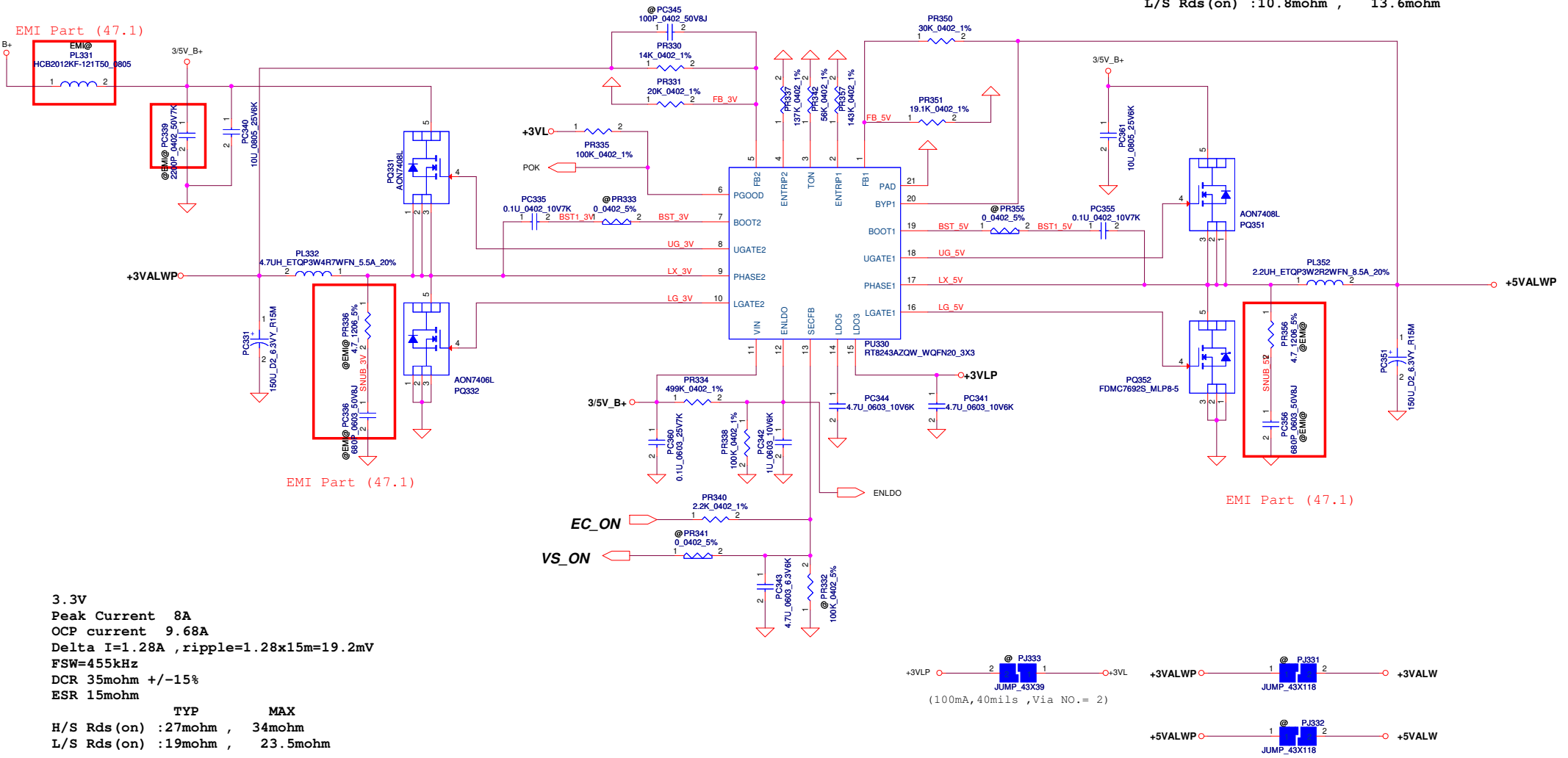
Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
		3.61A	

Please locate the RC  
Near EC chip  
2011-02-22

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				Custom	VFKTA
				Date:	Rev 1.0
				Sheet	46 of 56

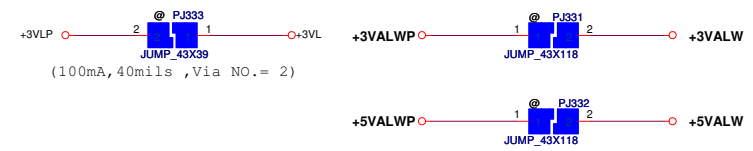
5V  
 Peak Current 8.5A  
 OCP current 10.2A  
 FSW=390kHz  
 Delta I=4.29A, ripple=4.29\*17m=72.93mV  
 DCR 15.5mohm+/-15%  
 ESR 17mohm

	TYP	MAX
H/S Rds (on)	:27mohm	34mohm
L/S Rds (on)	:10.8mohm	13.6mohm



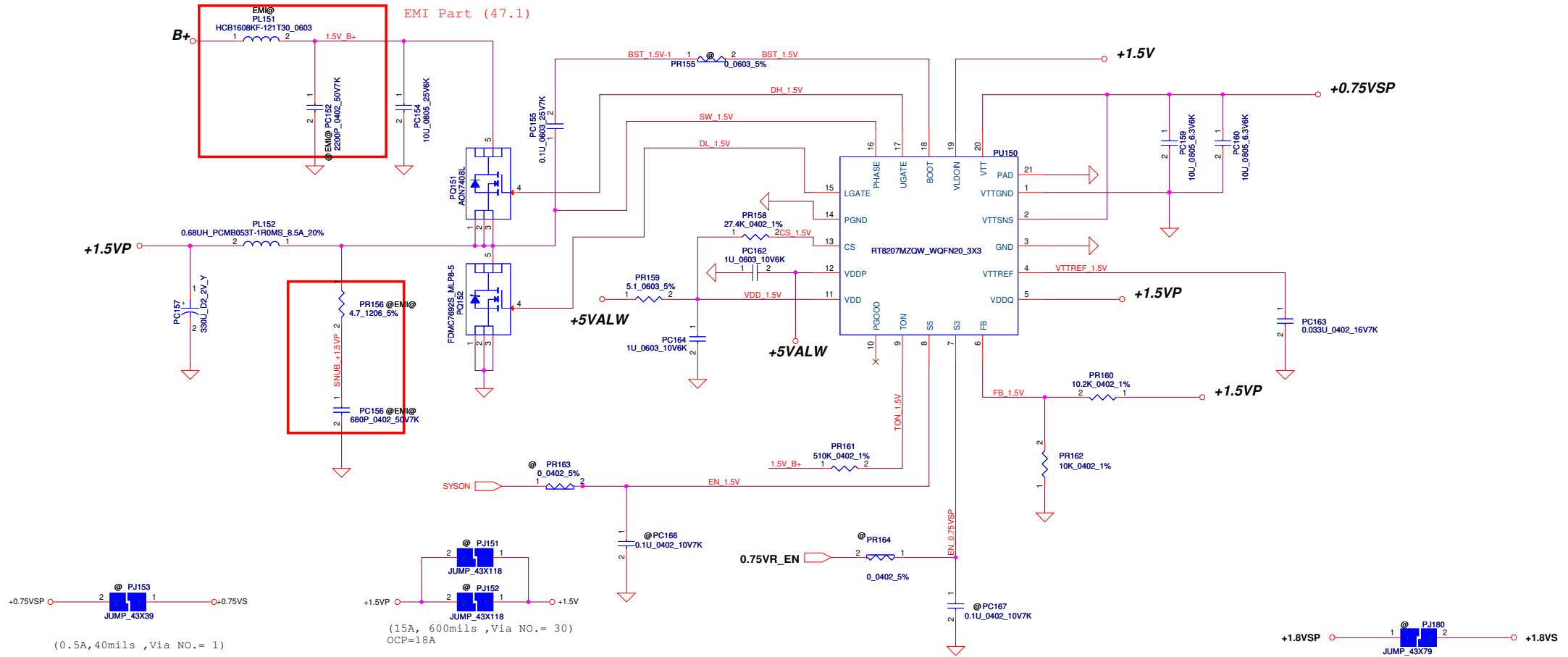
3.3V  
 Peak Current 8A  
 OCP current 9.68A  
 Delta I=1.28A, ripple=1.28\*15m=19.2mV  
 FSW=455kHz  
 DCR 35mohm +/-15%  
 ESR 15mohm

	TYP	MAX
H/S Rds (on)	:27mohm	34mohm
L/S Rds (on)	:19mohm	23.5mohm



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Date:	Sheet	47	of	56

DDR controller (35.3), Support component (35.4)



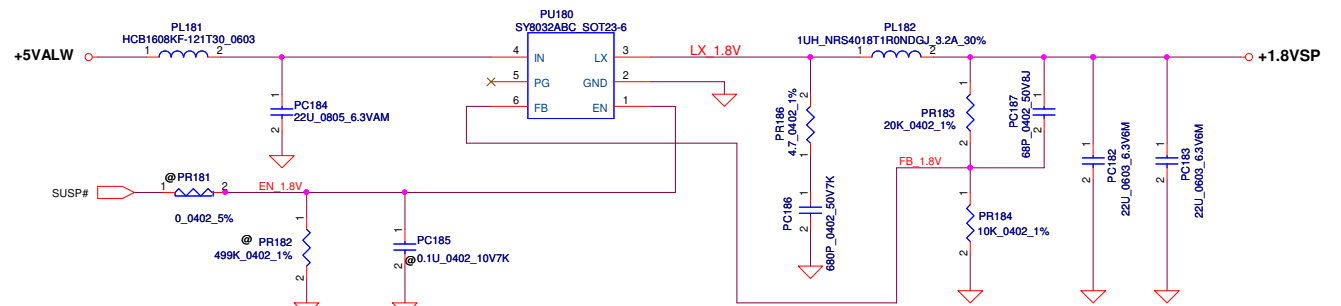
1.5V  
 Peak Current 16.66A  
 OCP current 20 A  
 FSW=495kHz  
 DCR 12mohm  
 ESR 10mohm

TYP      MAX  
 H/S Rds (on) :27mohm , 34mohm  
 L/S Rds (on) :10.8mohm , 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

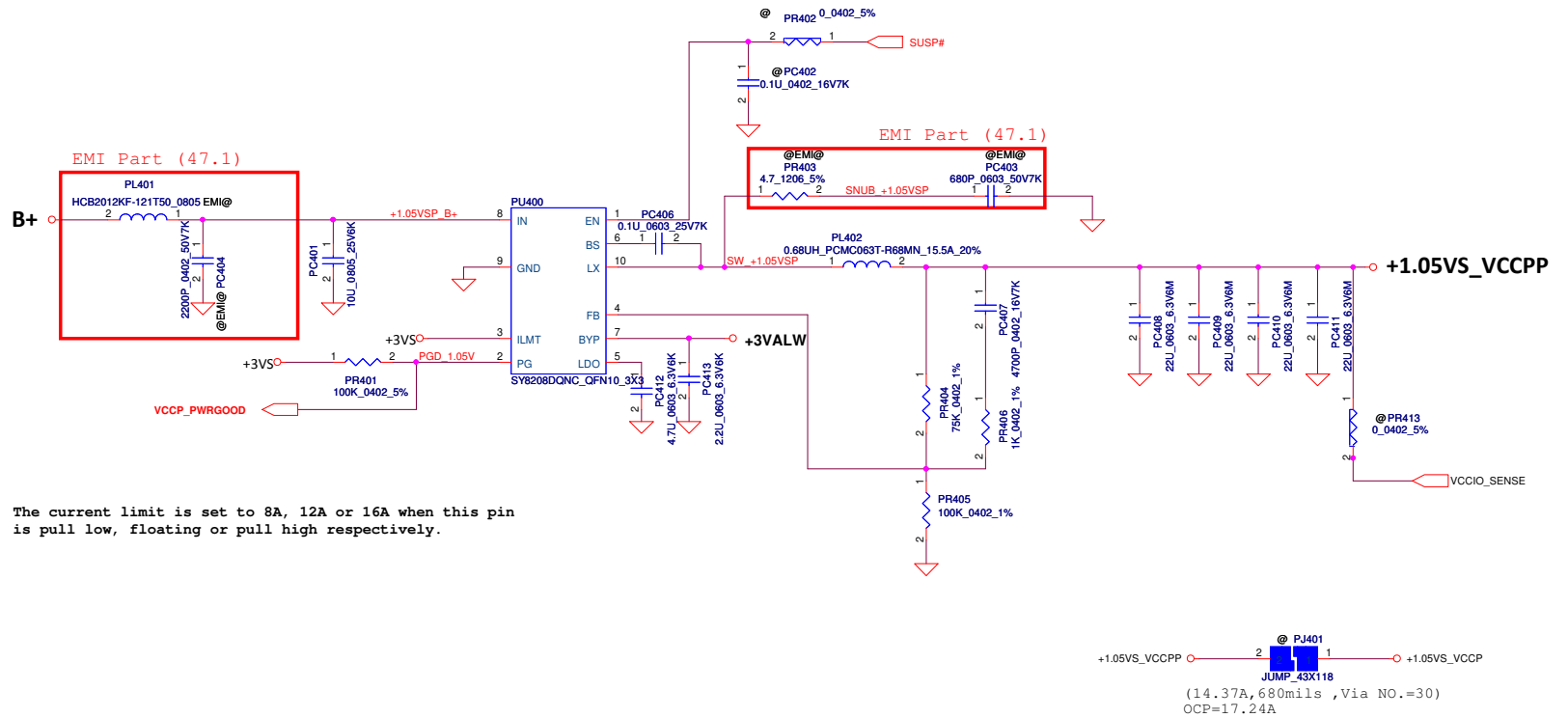
1.8VS controller (35.15), Support component (35.16)



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				Custom	VFKTA
				Date:	Sheet 48 of 56



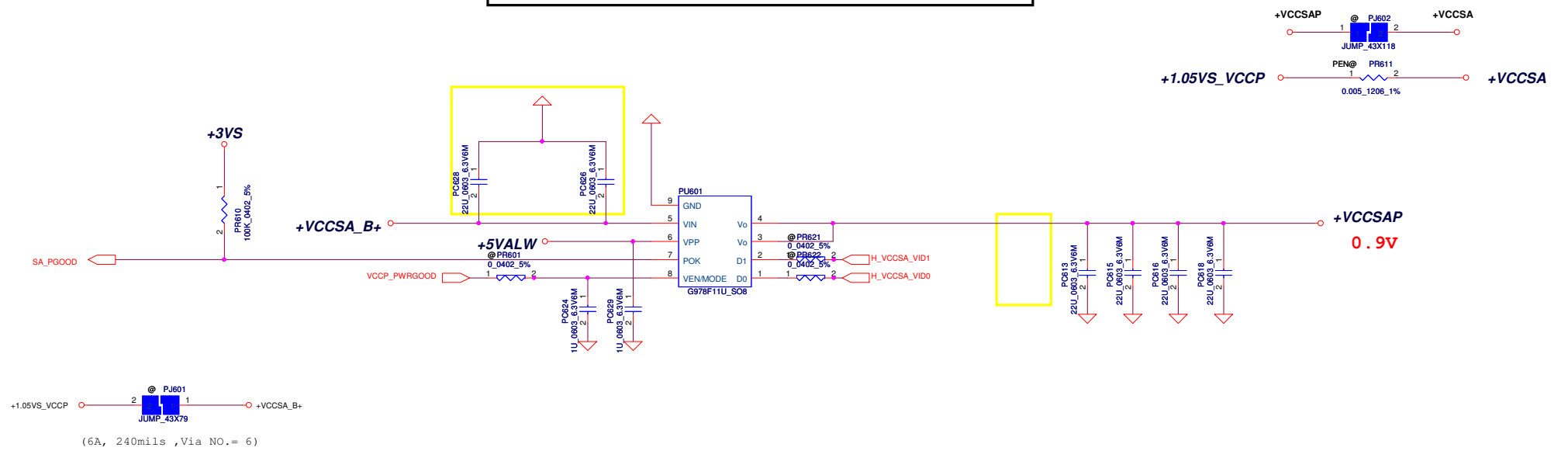
1.05VCCP controller (35.5), Support component (35.6)



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					VFKTA	1.0
				Date:	Monday, March 11, 2013	Sheet 49 of 56

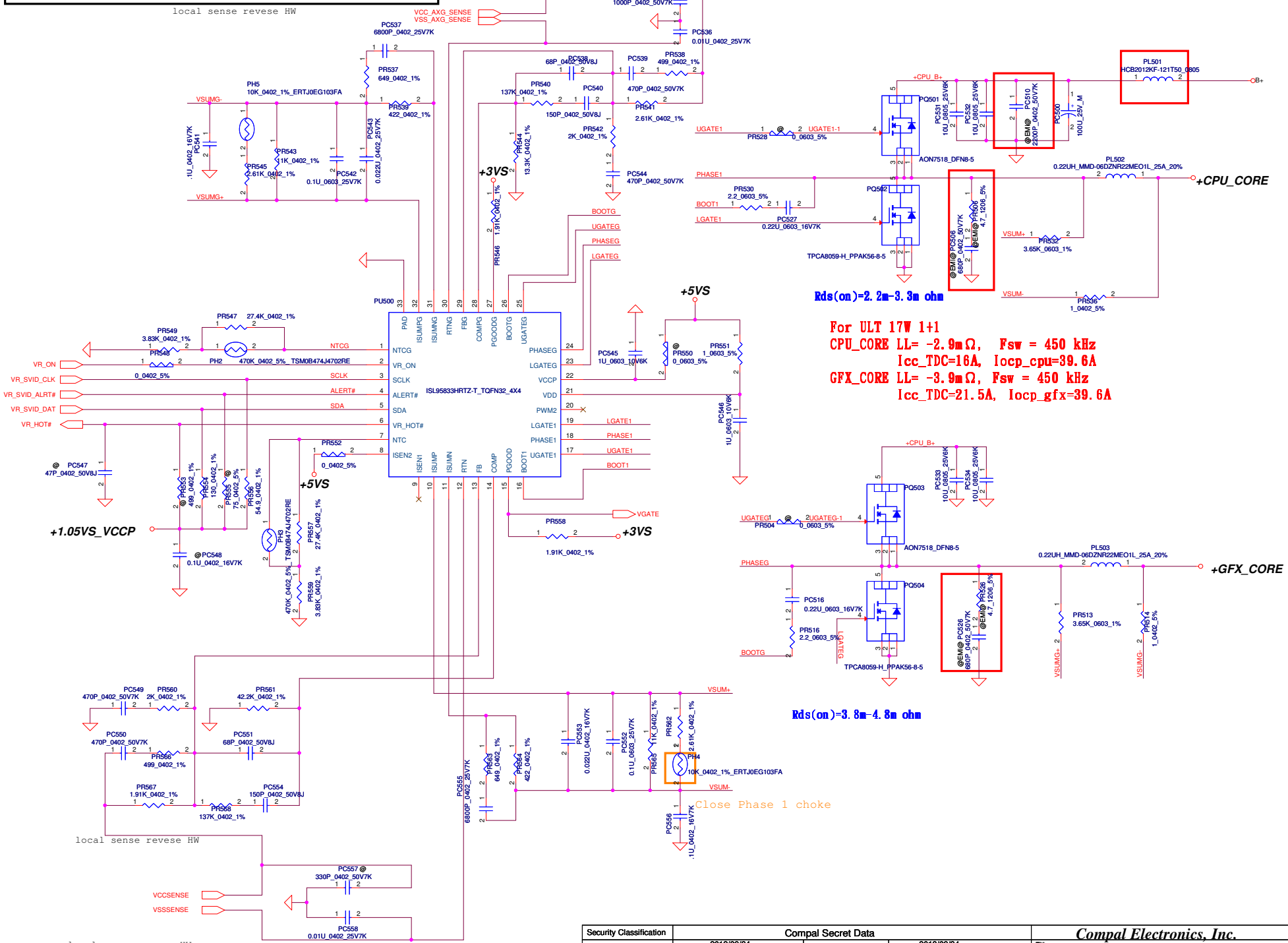
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA controller (35.17), Support component (35.18)



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				Document Number <b>VFKTA</b>
				Rev 1.0
				Date: _____ Sheet 50 of 56

CPU\_Core controller (36.1), Support component (36.3)



For ULT 17W 1+1  
 CPU\_CORE LL= -2.9mΩ, Fsw = 450 kHz  
 Icc\_TDC=18A, Iocp\_cpu=39.6A  
 GFX\_CORE LL= -3.9mΩ, Fsw = 450 kHz  
 Icc\_TDC=21.5A, Iocp\_gfx=39.6A

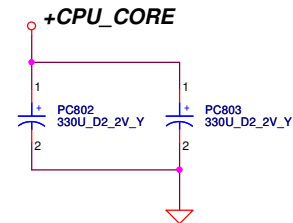
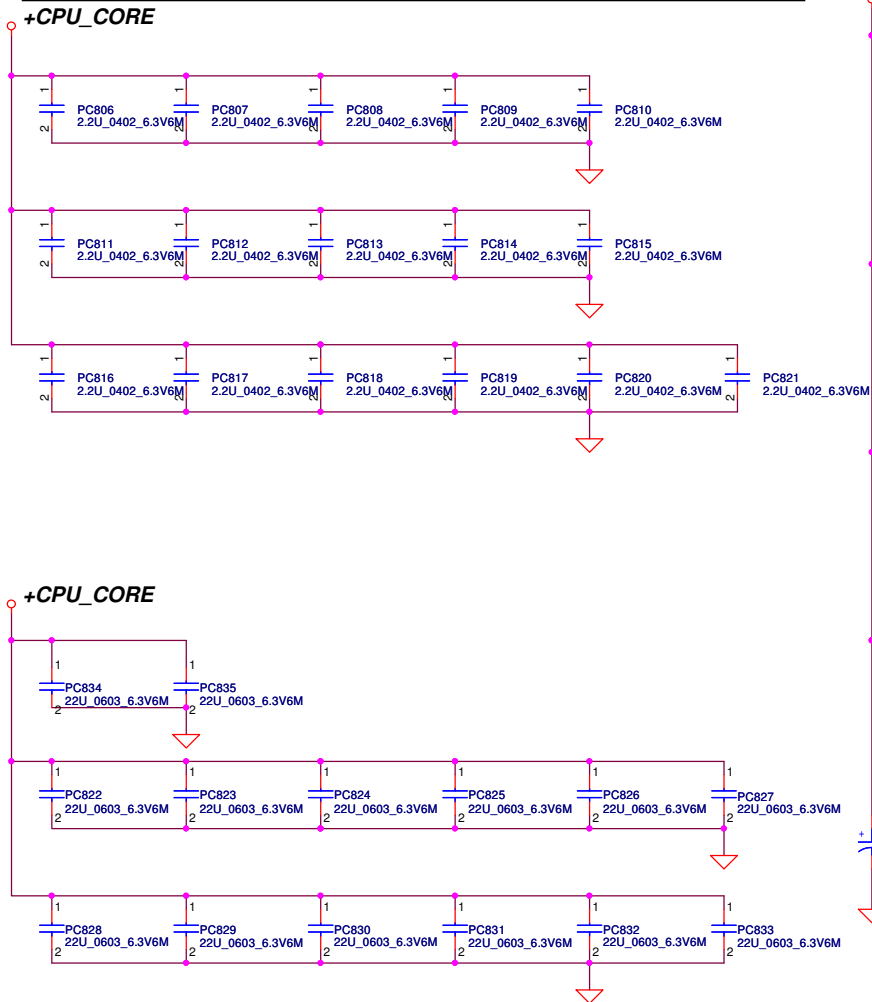
Rds(on)=2.2m-3.3m ohm

Rds(on)=3.8m-4.8m ohm

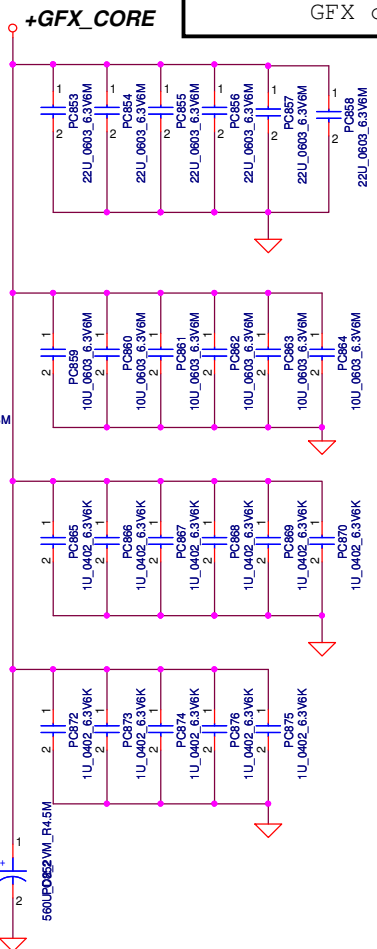
Close Phase 1 choke

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				VFKTA
				Rev 1.0
				Date: Monday, March 11, 2013   Sheet 51 of 56

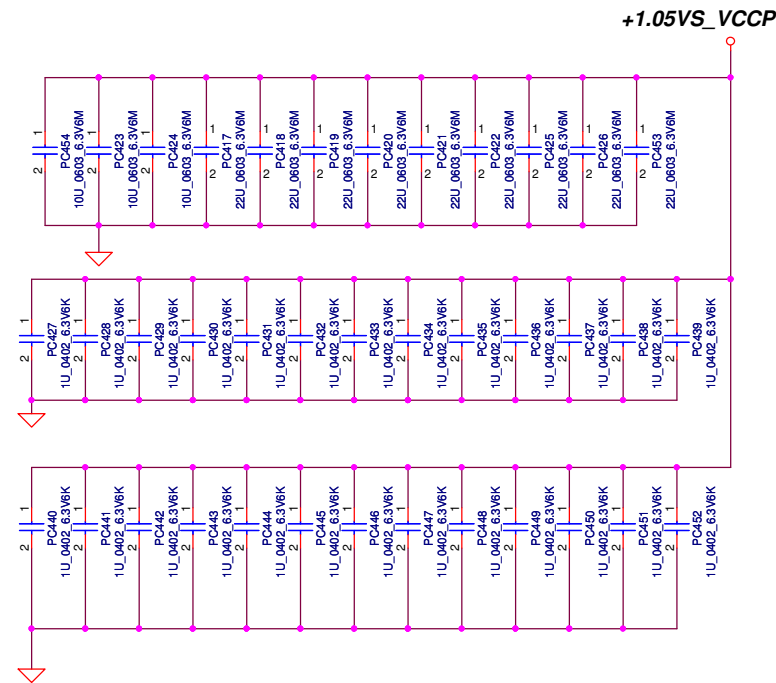
CPU\_Core output CAP (Including MLCC) 36.4



GFX output CAP (Including MLCC) 36.5

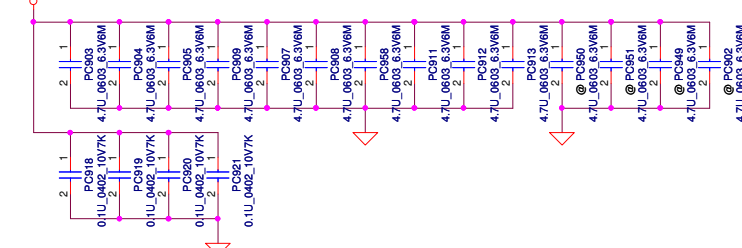


VCCP output Cap (Including MLCC) 36.6

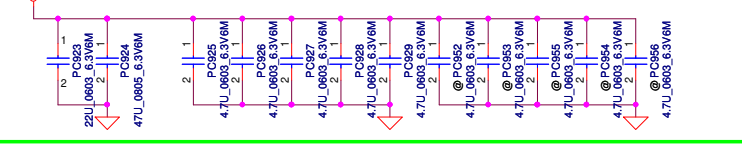


Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF	470uF	560uF
CPU	2	14		16			
GFX_CORE		6	6		11		1
1.05V_VCCP		9	3		26		1

**+VGA\_CORE Under VGA Core GB4-128 package**

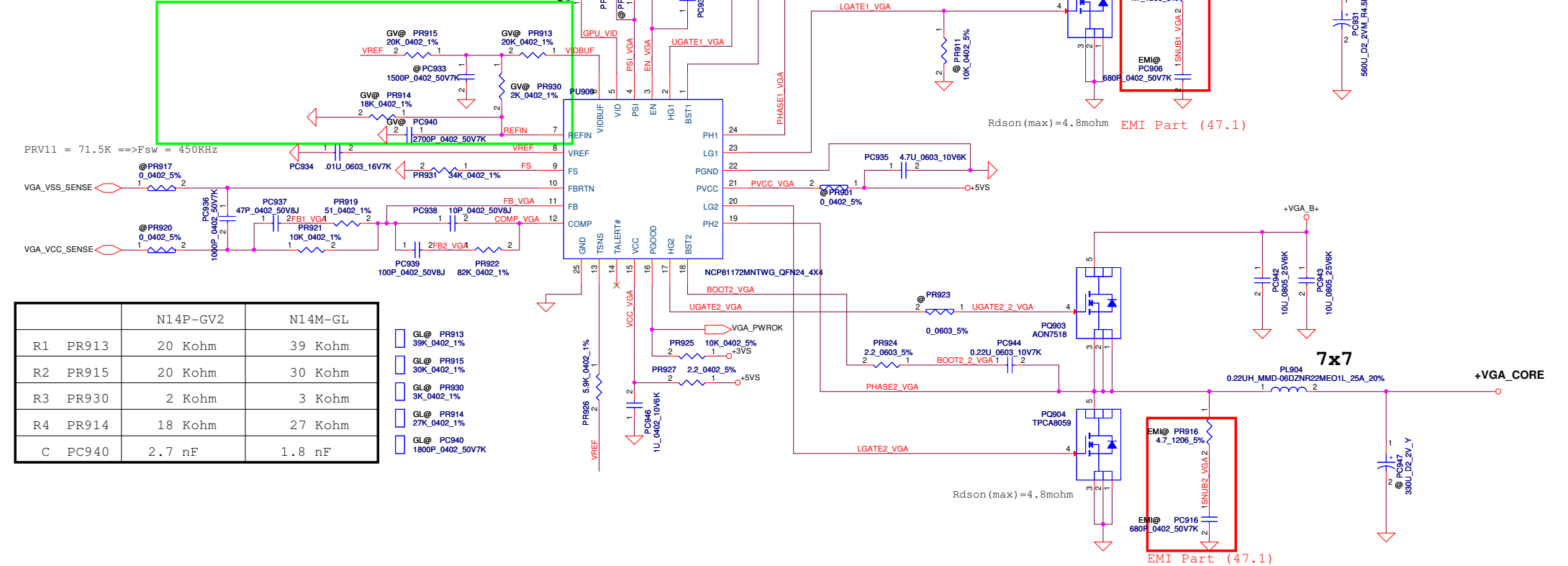


**+VGA\_CORE Near VGA Core**



VGA\_CORE controller (43.1), Support component (43.2)

EMI Part (47.1)



$PRV11 = 71.5K \Rightarrow F_{sw} = 450KHz$

	N14P-GV2	N14M-GL	
R1	PR913	20 Kohm	39 Kohm
R2	PR915	20 Kohm	30 Kohm
R3	PR930	2 Kohm	3 Kohm
R4	PR914	18 Kohm	27 Kohm
C	PC940	2.7 nF	1.8 nF

- GL@ PR913 39K\_0402\_1%
- GL@ PR915 30K\_0402\_1%
- GL@ PR930 3K\_0402\_1%
- GL@ PR914 27K\_0402\_1%
- GL@ PC940 1800P\_0402\_50V7K

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								Custom	VFKTA	1.0	
Date:								Sheet	53	of	56

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)
1	EVT-2012/10/24	P45-PWR-BATTERY CONN / OTP	@PD5 / Remove ESD diode	company	For part count reduction
2	EVT-2012/10/24	P45-PWR-BATTERY CONN / OTP	@PD6 / Remove ESD diode	company	For part count reduction
3	EVT-2012/10/24	P46-PWR-CHARGER	@PC221 /Remove 10uF capacitor	company	For part count reduction
4	EVT-2012/10/24	P47-PWR-3VALW/5VALW	PC331 /Reserve	PWR	ME limitation
5	EVT-2012/10/24	P47-PWR-3VALW/5VALW	@PC354/mount	PWR	ME limitation
6	EVT-2012/10/24	P47-PWR-3VALW/5VALW	PR337/235K change to 137K	PWR	for RT8243 3V OCP setting
7	EVT-2012/10/24	P47-PWR-3VALW/5VALW	PR357/156K change to 143K	PWR	for RT8243 5V OCP setting
8	EVT-2012/10/24	P48-1.5VP/0.75VSP/1.8VSP	PR158/16.2K change to 27.4K	PWR	for RT8207 OCP setting
9	EVT-2012/10/24	P52-PWR +CPU_CORE DECOUPLING	PC416 / change 560uF	PWR	Based on height and space limitation
10	EVT-2012/10/24	P52-PWR +CPU_CORE DECOUPLING	PC415/ Remove	PWR	Based on height and space limitation
11	EVT-2012/10/24	P53-PWR-VGA_COREP	PR929 / Add 10K ohm	HW	Pull high PSI port
12	EVT-2012/10/24	P53-PWR-VGA_COREP	PR913 / 39k change to 20K(GV)	PWR	For N14 PWM VID setting
13	EVT-2012/10/24	P53-PWR-VGA_COREP	PR915 / 39k change to 20K(GV) 30K(GL)	PWR	For N14 PWM VID setting
14	EVT-2012/10/24	P53-PWR-VGA_COREP	PR930 / 1.5k change to 2K(GV) 3K(GL)	PWR	For N14 PWM VID setting
15	EVT-2012/10/24	P53-PWR-VGA_COREP	PR914 / 30k change to 18K(GV) 24K(GL)	PWR	For N14 PWM VID setting
16	EVT-2012/10/24	P53-PWR-VGA_COREP	PR904 / 1.5k change to 0K(GV) 3K(GL)	PWR	For N14 PWM VID setting
17	EVT-2012/10/24	P53-PWR-VGA_COREP	PC940 / Add 2700pF(GV) 1800pF(GL)	PWR	For N14 PWM VID setting
18	EVT-2012/10/24	P53-PWR-VGA_COREP	PC933 /Reserve	PWR	For N14 PWM VID setting
19	EVT-2012/10/24	P53-PWR-VGA_COREP	@PC914 /Remove 0.1uF capacitor	company	For part count reduction
20	EVT-2012/10/24	P53-PWR-VGA_COREP	PR931/71.5K change to 34K	PWR	For NCP81172 Fsw setting
21	EVT-2012/10/24	P53-PWR-VGA_COREP	PR927/PN change to SD028220B80	PWR	for PN setting error
22	EVT-2012/10/25	P46-PWR-CHARGER	PQ203/change to TPCA8507	PWR	for design change
23	DVT-2012/12/06	P46-PWR-CHARGER	PU200/change to BQ24725RGR	PWR	for design change
24	DVT-2012/12/06	P46-PWR-CHARGER	PQ203 / change to TPCA8507	PWR	AON6504 has burnt out issue
25	DVT-2012/12/06	P47-PWR-3VALW/5VALW	PC534,PC351/Delete	PWR	Based on height and space limitation
26	DVT-2012/12/06	P47-PWR-3VALW/5VALW	PR335/add 100K ohm	PWR	Pull high +3VL
27	DVT-2012/12/06	P47-PWR-3VALW/5VALW	PC344/add 4.7U	PWR	for design request
28	DVT-2012/12/06	P47-PWR-3VALW/5VALW	PC341/change to 4.7U	PWR	for design request
29	DVT-2012/12/06	P47-PWR-3VALW/5VALW	PC352,PC353/add 150U_D2	PWR	Based on height and space limitation
30	DVT-2012/12/06	P48-1.5VP/0.75VSP/1.8VSP	PL152/change to 0.68UH	PWR	for design change
31	DVT-2012/12/06	P49-PWR-1.05VS_VCCP	PL401/change PN	PWR	to integrate PN
32	DVT-2012/12/06	P49-PWR-1.05VS_VCCP	PR403 PC403/Reserve	EMI	EMI Command
33	DVT-2012/12/06	P51-CPU_CORE	CPU_CORE(PR5XX,PC5XX)/change solution	PWR	change solution
34	DVT-2012/12/06	P52-PWR +CPU_CORE DECOUPLING	PC802 PC803/change to 470U	PWR	change solution
35	DVT-2012/12/06	P54-PWR-VGA_COREP	PR912/add 10K ohm	PWR	pull high +3VS_DGPU
36	DVT-2012/12/06	P54-PWR-VGA_COREP	PC934/change 0.01U	PWR	For N14 PWM VID setting
37	DVT-2012/12/06	P54-PWR-VGA_COREP	PL903 PL904/change PN	PWR	have higher loss
38	DVT-2012/12/06	P45-PWR-BATTERY CONN / OTP	PF2/change PN	company	For cost down
39	PVT-2013/01/18	P47-PWR-3VALW/5VALW	PC352,PC353/change location to PC331,PC351	PWR	change location
40	PVT-2013/01/18	P48-1.5VP/0.75VSP/1.8VSP	PC157/change 390U	PWR	for design change
41	PVT-2013/01/18	P49-PWR-1.05VS_VCCP	PC414 / change 0ohm	PWR	change solution(change to location sense)
42	PVT-2013/01/18	P52-PWR +CPU_CORE DECOUPLING	PC417,PC418,PC419,PC420,PC421,PC422,PC425/change to 22U	PWR	for 1.05VCCP test
43	PVT-2013/01/18	P52-PWR +CPU_CORE DECOUPLING	PC426,PC453/add 22U	PWR	for 1.05VCCP test
44	PVT-2013/01/18	P49-PWR-1.05VS_VCCP	PC407/change 4700P	PWR	for design change
45	PVT-2013/01/18	P52-PWR +CPU_CORE DECOUPLING	PC416/Delete	PWR	for 1.05VCCP test(change to location sense)
46	PVT-2013/01/18	P49-PWR-1.05VS_VCCP	PL402/change to 0.68U	PWR	for 1.05VCCP test
47	PVT-2013/01/18	P51-CPU_CORE	PQ501,PQ503 / change AON7518	PWR	AON7514 EOL
48	PVT-2013/01/18	P51-CPU_CORE	PR553/Reserve	PWR	change solution
49	PVT-2013/01/18	P54-PWR-VGA_COREP	PC906 ,PC915,PC916,PR906,PR916/add	EMI	EMI Command
50	PVT-2013/01/18	P54-PWR-VGA_COREP	PC934/change PN	PWR	change PN
51	PVT-2013/01/21	P52-PWR +CPU_CORE DECOUPLING	PC802,PC852/change to 560U	PWR	for CPU,GFX Transient
52	PVT-2013/01/21	P51-CPU_CORE	PQ502,PQ504 /change TPCA8059	PWR	for design change
53	PVT-2013/01/21	P54-PWR-VGA_COREP	PC947/Reserve	PWR	for VGA Transient(for cost down)
54	PVT-2013/01/22	P52-PWR +CPU_CORE DECOUPLING	PC802,PC803/change to 330U	PWR	for CPU Transient
55	Pre-MP-2013/03/04	P49-PWR-1.05VS_VCCP	PR406/add 1k ohm	PWR	for 1.05VCCP test(change to location sense)
56	Pre-MP-2013/03/04	P53-PWR-VGA_COREP	PR904 PR918 PR928 PC945 remove PR914 change from 24K to 27K	PWR	Remove and change for Richtek solution setting

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				Document Number VFKTA
				Rev 1.0
Date: Monday, March 11, 2013				Sheet 54 of 56

# HW PIR (Product Improve Record)

VFKTA LA-9861P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/13	39	Add CA39 (SE102104K00)	BOM structure change
2.	11/13	39	Reserve RA31,RA38	EMI request
3.	11/13	41	Change RB36 from 2.2k to 0 ohm and CB50 to @	Design change
4.	11/13	15	Update VGA strap pin all page	Design change
5.	11/21	42	Remove NFC function	Design change
6.	11/21	42	Update CPU config&PN	Design change
7.	11/26	23	change BOM structure C238,C239,C240,C241,C242,C243 to CRT@EMI@	EMI request
8.	11/26	22	Add D92 for LID_SW#_D to isolate the +3VL power rail from LID_SW#	Design change
9.	11/26	24	Add @ to JHDMI	Design change
10.	11/26	37	Change JCARD.10 to SDWP# and JCARD.11 to SDCD.	Design change
		37	Add QW1, RW3, RW4 for normal close type connector.	
11.	11/26	40	Update HDMI power circuit	Design change
12.	11/26	40	Change JSPK from 8 pin to 6 pin (SP02000WS00)	Design change
13.	11/26	40	Remove SPK_DET1 and change SPK_DET0 net name to SPK_DET	Design change
14.	11/26	39	Change RA50 to 269@	Design change
15.	11/26	40	Reverse JSPK to keep same layout routing on MB	Design change
16.	11/27	30	Remove GPIO71 and change SPK_DET1 to SPK_DET	Design change
17.	11/29	30	Add GPIO22 as VRAM_DR_SR# and add RH203, RH205 for BOM control <DIS>	For dual&single rank common bios
18.	11/30	30	Change RH202, RH203 BOM structure to GVDR@ and GVSR@	For dual&single rank common bios
19.	11/30	42	Change H7 to 4P0, Add H19 (3P2N), Change H17, H18 to PTH	ME request
20.	11/30	25	Change UH3 from socket to IC	Design change
21.	11/30	09	Change CC53 to 47U 0805 (SE00000PL00)& add CC50 (SE00000PL00)	For 1206 MLCC Crack issue
		09	Change CC44 to 47U 0805 (SE00000PL00)& add CC40 (SE00000PL00)	
		12	Change CD31 to 47U 0805 (SE00000PL00)	
		38	Change CR10&CR12 to 47U 0805 (SE00000PL00)	
22.	11/30	07	Change RC73 to 0 ohm (do not use short pad on this location)	For debug
23.	11/30	17	Change RV53 pull high to +3VS	Design change
24.	11/30	15	Change RV24 to 4.99K	Strap pin change
25.	11/30	22	Delete D92 and change the netname to BKOFF#	Avoid LCD_INV leak to Touch/B
26.	11/30	23	Add R62 & R63 for CRT undershoot issue	For CRT undershoot issue
27.	11/30	25	Chane UH4, RH269, RH271 to @, change RH267 from shortpad to 0-ohm @.	Design change
28.	11/30	08	Add CC17~CC19 for ESD request	ESD request
29.	11/30	29,41	Move PLT_RST# ESD capacitor (CH104) to EC side (CB13) and mount 0.1uF	ESD request
30.	11/30	05	Change CC63 from @ESD@ to ESD@	ESD request
31.	11/30	41	Change PM_SLP_S4# from pin127 to pin84.	For ENE common code
32.	11/30	41	Change USB_EN#0 from pin84 to pin23.	For ENE common code
33.	11/30	41	Change FB_CLAMP from pin23 to pin127.	For ENE common code
34.	11/30	17	CV57 and CV60 change to 0.01U.	For sequence
35.	11/30	17	RV47 change to 180K.	For sequence
36.	12/03	38	Update USB circuit	For S&C MAX4640 and MAX4641 co-layer circuit
37.	12/04	42	Change H19 to NPPTH	Design change
38.	12/04	17	Change QV2 footprint to NC7ST32P5X_SC70-5	For non-A51 part change
39.	12/04	04	Add S&C SMBus address in the table	Design change

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				Title <b>HW-PIR</b> Rev 1.0

# HW PIR (Product Improve Record)

## QCLA4 LA-8861P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO DATE PAGE MODIFICATION LIST PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
40.	12/04	41	Add short-pad (RB5) on pin127.	Design change
41.	12/04	13	Reverse DV1, Change DV1, QV8 to OPT@, 13 Change FB_CLAMP_MON from pull down to pull high +3VS_DGPU	
42.	12/04	17	Change UV2 PN to SA007320300	Design change
		17	Change UV2, CV58 to OPT@ and change RV50 to @	
43.	12/04	43	Add R5546 put high PCH_PWR_EN to +3VL	Design change
45.	12/05	41	Add CHG_PWR_GATE# pull high 3VL and add RB11 10K.	Design change
46.	12/05	38	S&C IC Pin1 was connected to the EC(GPIO49) Pin82.	Design change

## VFKTA LA-9861P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2 TO 0.3

NO DATE PAGE MODIFICATION LIST PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/24	17	Change RV43 to 270K	For GC6 timing requirements
2.	12/24	17	Change RV53 to 10K	For GC6 timing requirements
3.	12/24	17	Change RV54 to 33K	For GC6 timing requirements
4.	12/24	17	Change RV50to N14MGL@	N14M-GL doesn't support GC6
5.	12/24	17	Change UV2to N14PGV2@	N14M-GL doesn't support GC6
6.	12/24	17	Change CV58 to @	Cost reduction
7.	12/24	13	Change QV8to N14PGV2@	N14M-GL doesn't support GC6
8.	12/24	13	Change DV1 P/N to SCS00002G00	BOM reduction
9.	01/09	41	Change CB31 to 100P P/NSE071101J80	Design Change
10.	01/09	7,9,25	Change QC3,QC7,QC8,QH1 to SB00000PF00	SB501380020 X1 code
11.	01/15	22	Reserve R267&R266 0 ohm	For EMI cost down
12.	01/15	41	Reserve CB50 1U	Common design
13.	01/15	13	GPIO12 be connected to EC_GPXIOA01(remove EC_DRAMRST_CNTRL_PCH&RC3)	For GPS
14.	01/16	42	Modify JTP pin define	For DFB highlight
15.	01/16	22	Add C17 100P on LED_PWM	For EMI request
16.	01/17	39/42	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	For boot bobo issue
17.	01/17	5/30/42	Reserve CCL1,CH1,CB17,CB18,CC35 100P	For ESD
18.	01/17	26	Add RH38 0 ohm on XCLK_RCOMP	For EMI 200M noise

## VFKTA LA-9861P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

NO DATE PAGE MODIFICATION LIST PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	02/18	06	Swap H_EDP_TXN[0\1] to H_EDP_TXP[0\1]	Design mistake
2.	02/18	22	Change C7 to SE076153K80 (15nF)	for LCD sequence tuning
3.	02/19	05	Delete CC33, CC36, C4; change R1 to short pad	for part count reduce
4.	02/19	07	Change RC73 to short pad	for part count reduce
5.	02/19	09	Delete CC61, CC83; change RC119 to short pad	for part count reduce
6.	02/19	11	Delete CD2, CD15	for part count reduce
7.	02/19	12	Delete CD28, CD46	for part count reduce
8.	02/19	17	Delete CV58	for part count reduce
9.	02/19	22	Change R106 to shortpad	for part count reduce
10.	02/19	23	Delete C250	for part count reduce
11.	02/19	25	Delete CH6, CH100; change RH67, RH68 to short pad	for part count reduce
12.	02/19	26	Delete RH275	for part count reduce
13.	02/19	28	Delete RH254	for part count reduce
14.	02/19	29	Delete CH30, RH287	for part count reduce
15.	02/19	35	Delete CCL2, RCL5, RCL2, net: LAN_X1_R_R, LAN_X1_R	for part count reduce
16.	02/19	36	Delete net: LAN_X1_R	for part count reduce
17.	02/19	37	Change RW1 to shortpad	for part count reduce
18.	02/19	38	Delete CR7, CR8	for part count reduce
19.	02/19	39	Change RA22, RA18, RA24 to short pad	for part count reduce
20.	02/19	41	Delete CB4, CB5, CB50	for part count reduce
21.	02/19	42	Delete SW2, SW3	for part count reduce
22.	02/23	37	Change RW2 to 330ohm and mount CW9 10PF	for EMI request
23.	03/04	41	Connect RB14 form POK_R to POK and reserve RB13, RB22, CB16	for abnormal shut down power request
24.	03/04	37	Add RW5-RW8 for EMI request and change netname SD_DATAx to SD_DATAx_R on conn side	for EMI request

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Date:	Monday, March 11, 2013	Sheet	56 of 56		