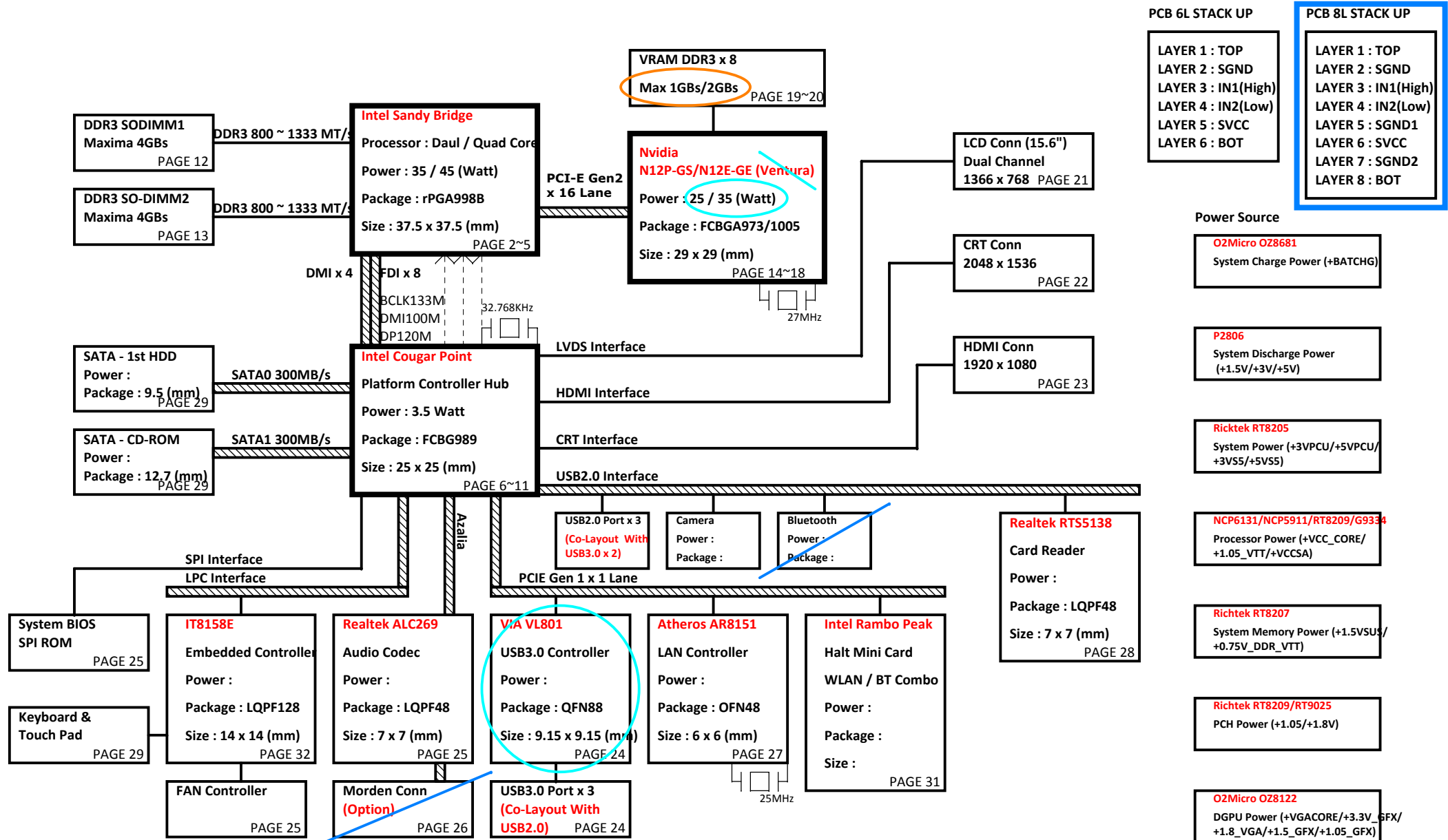
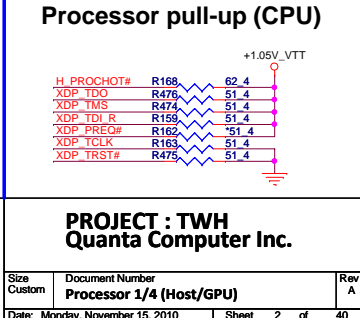
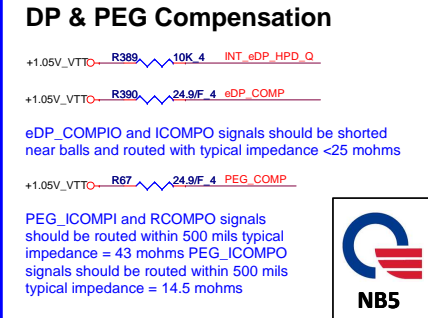
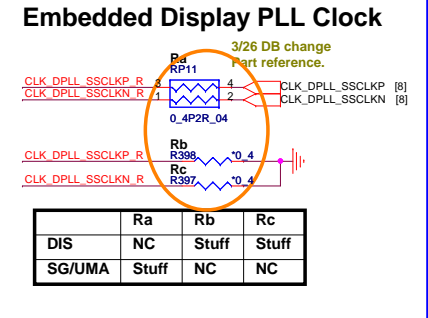
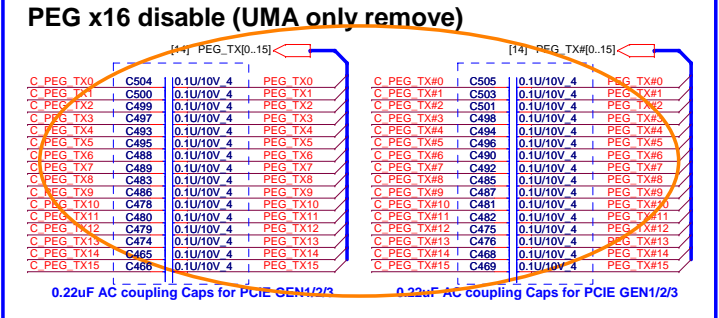
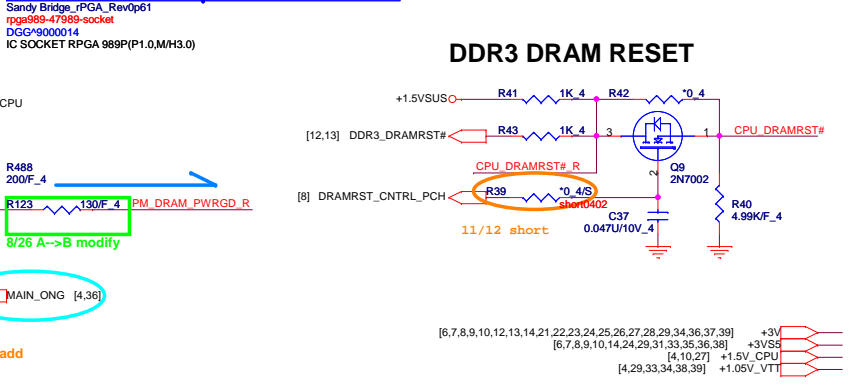
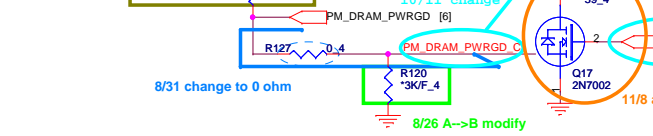
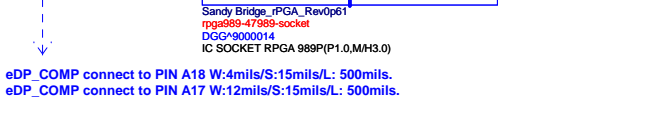
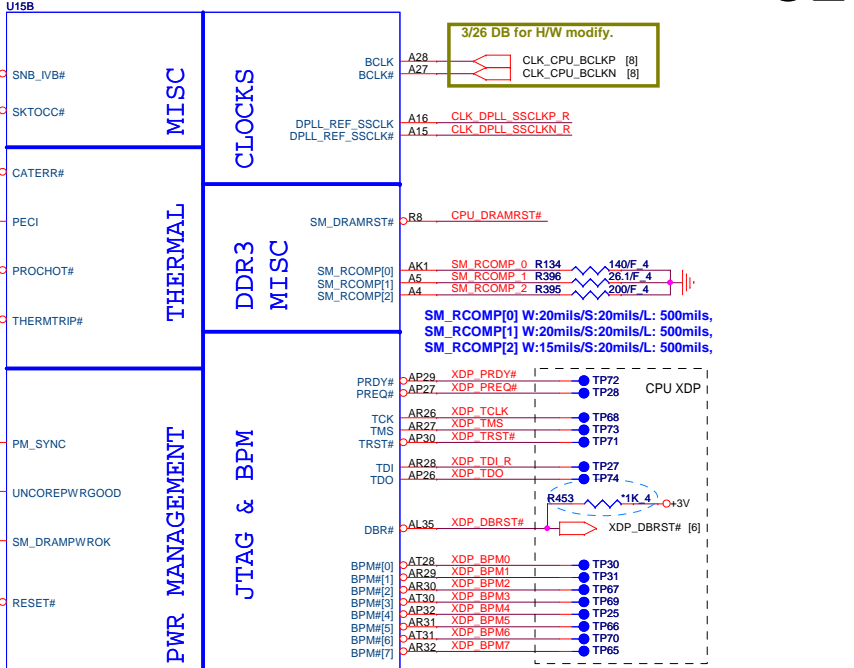
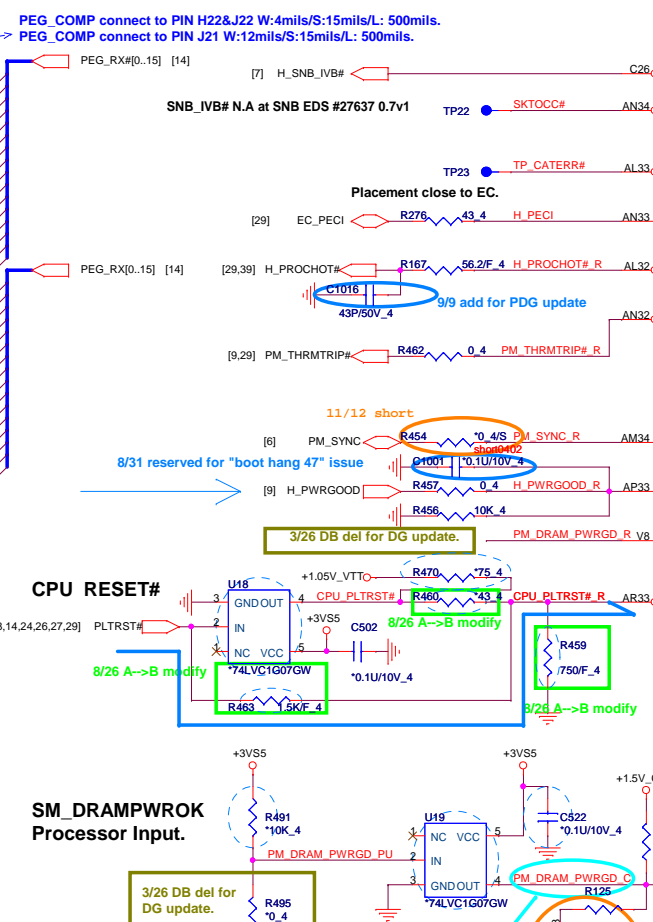
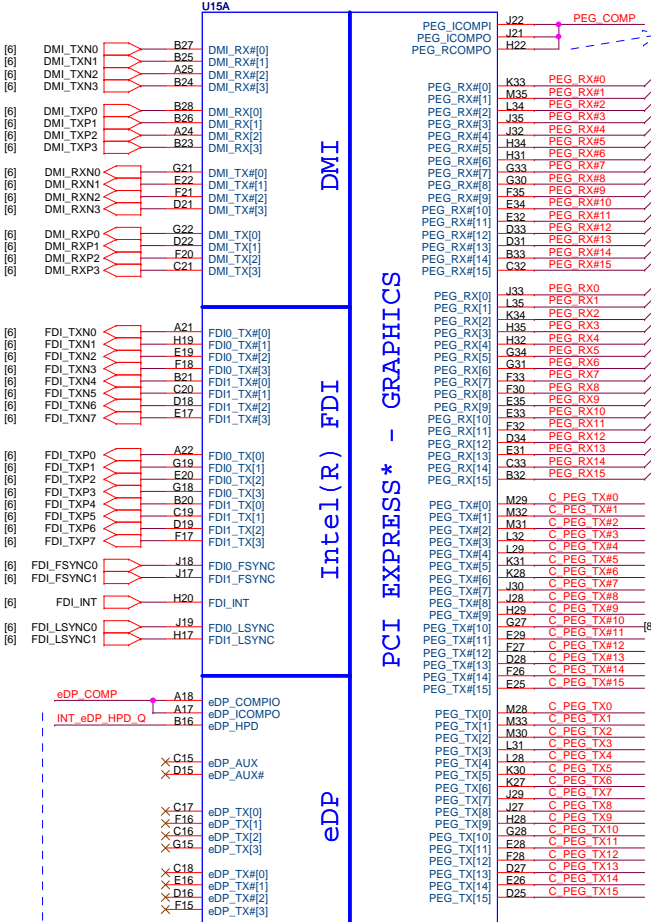


TWH (15.6") Intel Huron River Platform Block Diagram



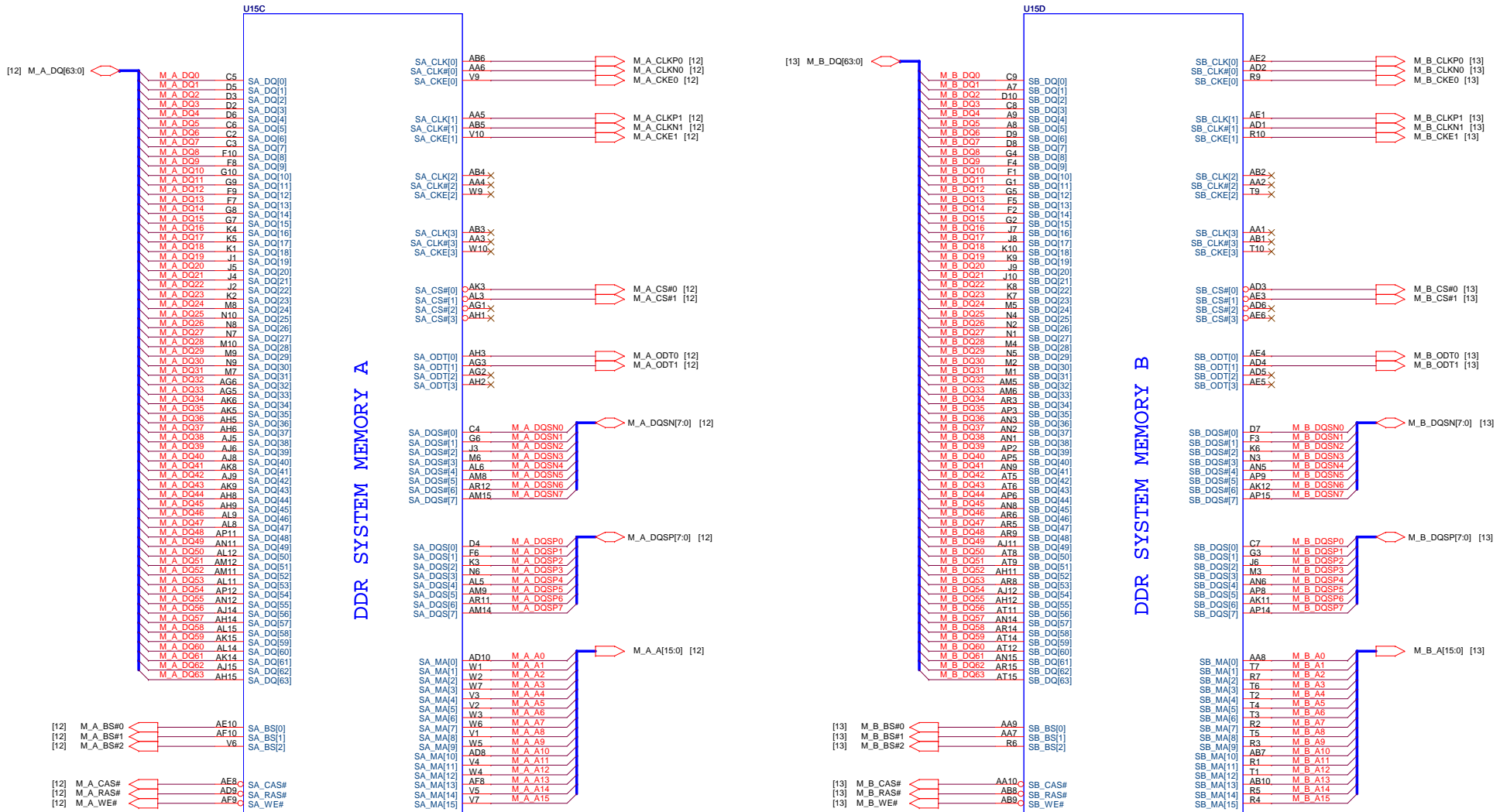


PROJECT : TWH
Quanta Computer Inc.

NBS

Size Custom	Document Number Processor 1/4 (Host/GPU)	Rev A
Date: Monday, November 15, 2010	Sheet 2 of 40	

Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG#9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG#9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

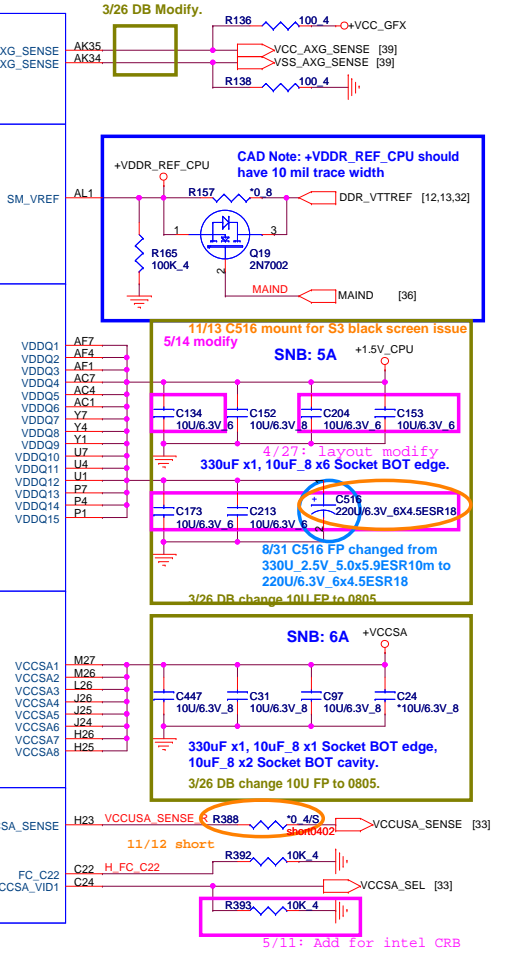
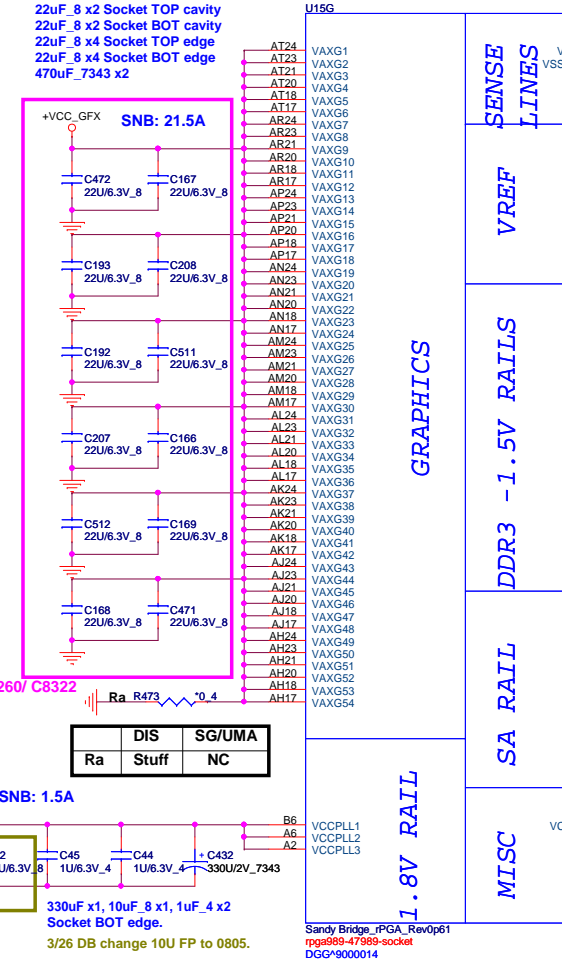
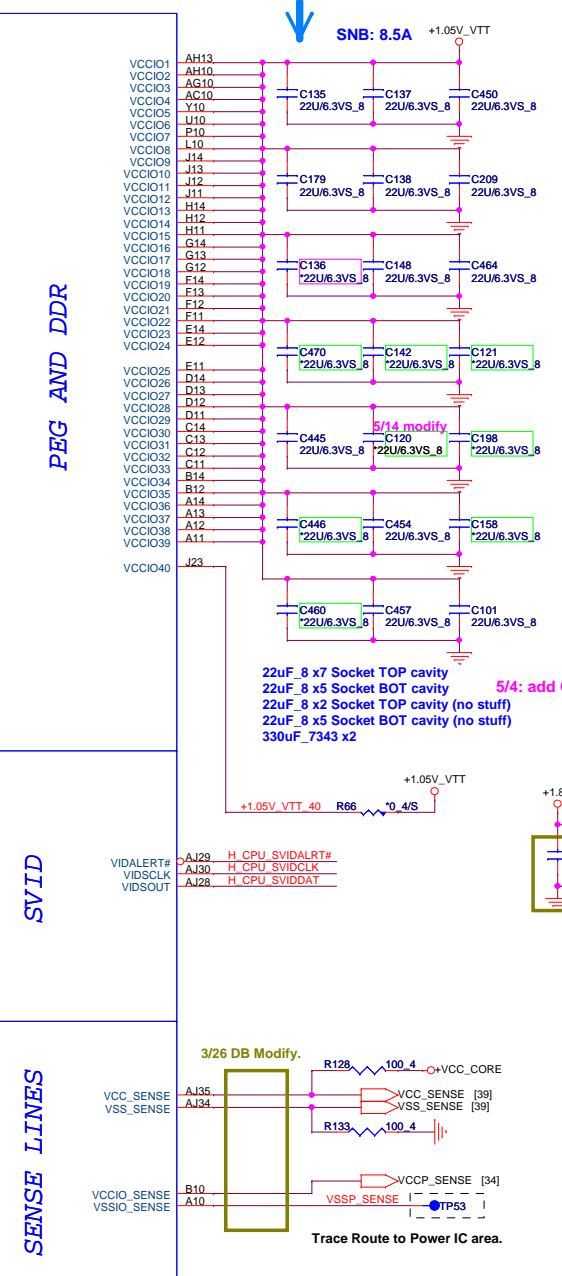
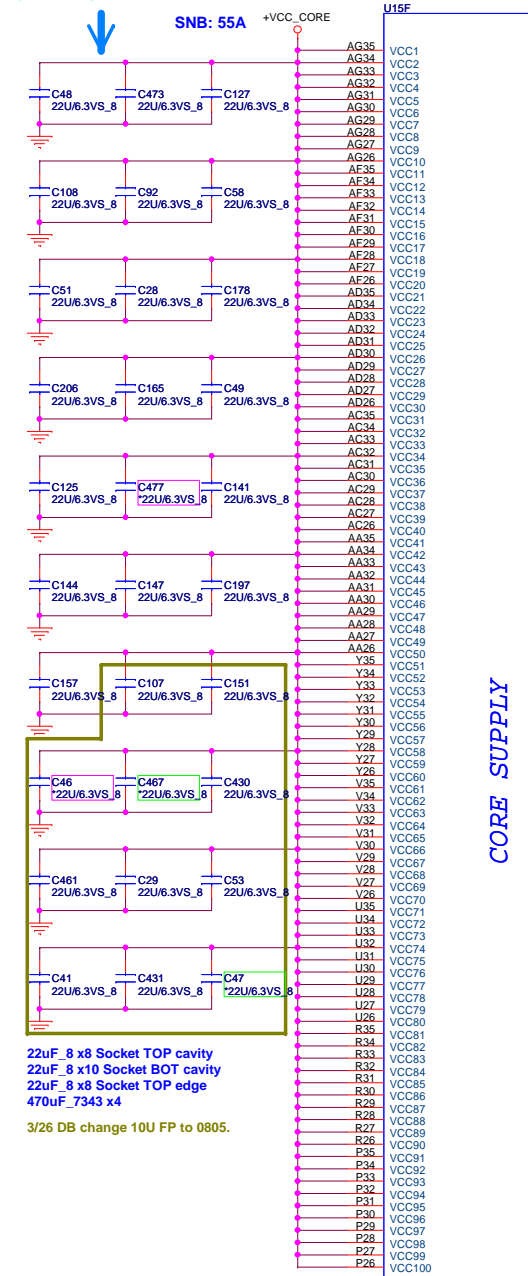
	PROJECT : TWH		Rev A
	Quanta Computer Inc.		
	Size Custom	Document Number Processor 2/4 (Memory)	
Date: Monday, November 15, 2010		Sheet 3 of 40	

Sandy Bridge Processor (POWER)

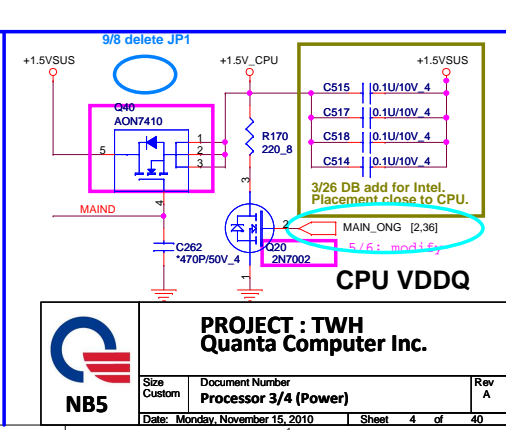
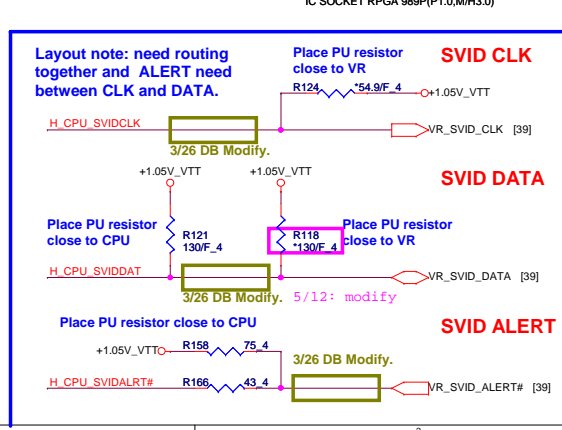
Sandy Bridge Processor (GRAPHIC POWER)

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM



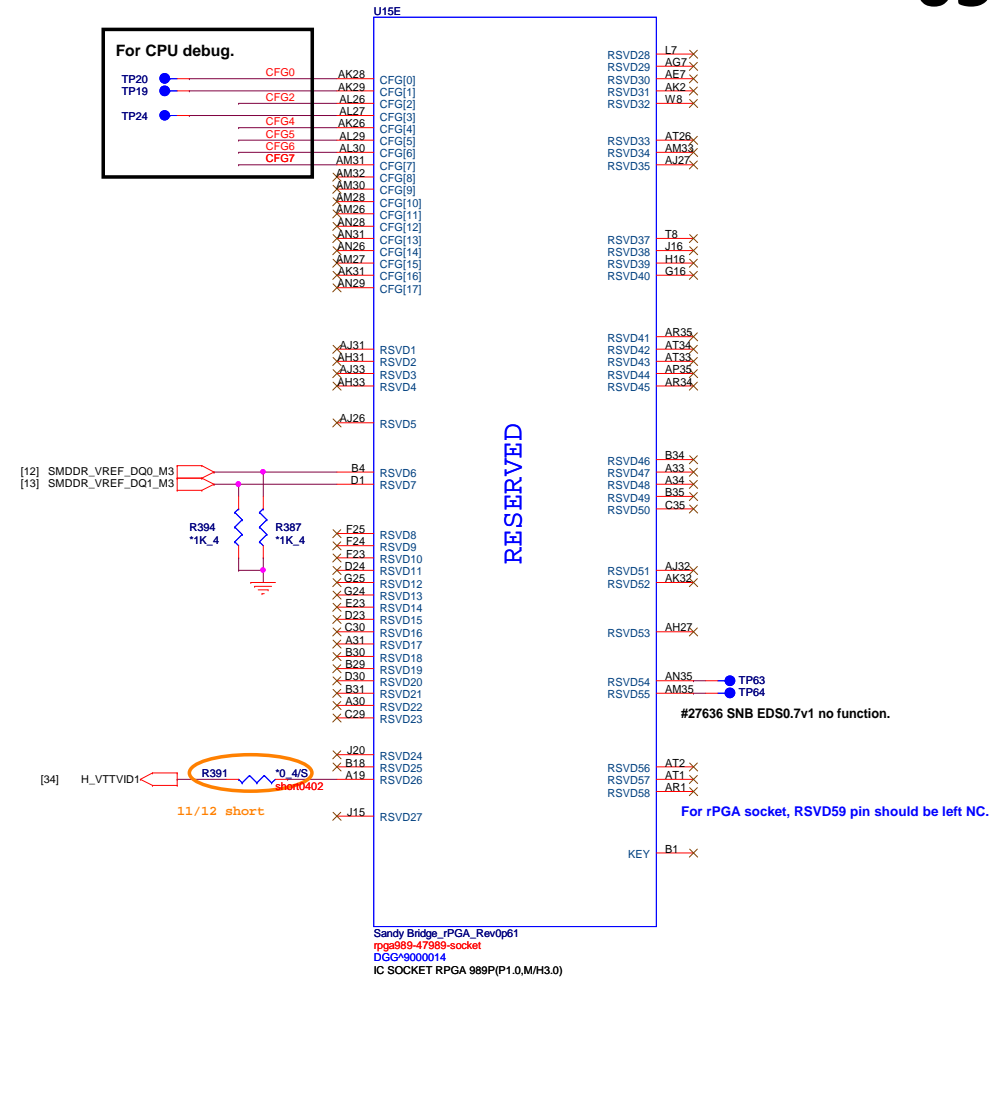
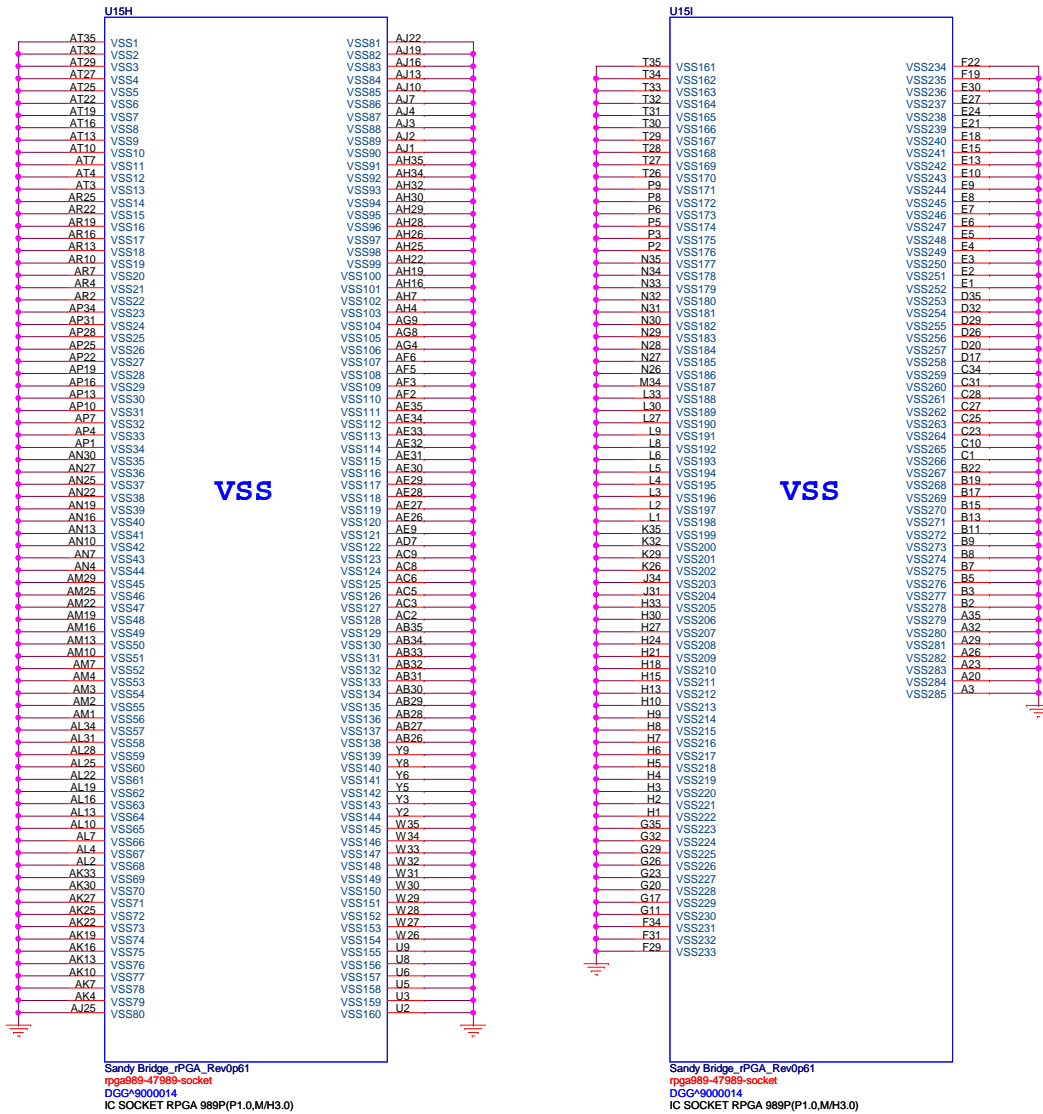
Sandy_Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MMH3.0)



PROJECT : TWH
Quanta Computer Inc.

NBS

Size	Document Number	Rev
Custom	Processor 3/4 (Power)	A
Date: Monday, November 15, 2010	Sheet 4 of 40	

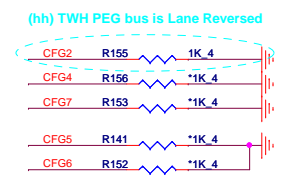


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



**PROJECT : TWH
Quanta Computer Inc.**

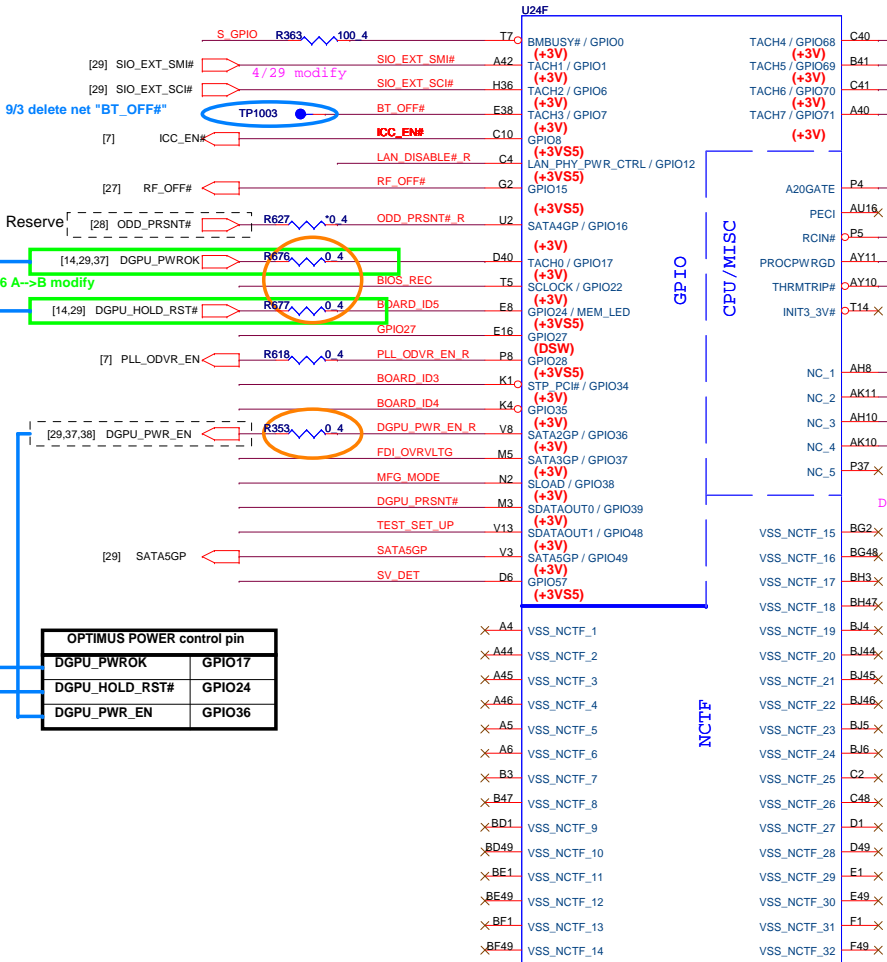
Size Custom	Document Number Processor 4/4 (Ground)	Rev A
Date: Monday, November 15, 2010		Sheet 5 of 40

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG*9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG*9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG*9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Cougar Point (GPIO,VSS_NCTF,RSVD)

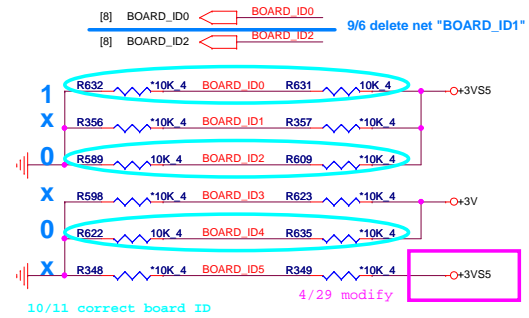


OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

CougarPoint_Rev_0p7 IC CTRL(989P)COUGARPOINT QMYYTOP B/S
 fcbgs99-intel-cougarpoint
 AJQ0MIV0T01

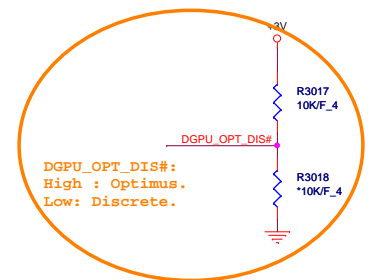
BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LG	0=LG 1=CB					
UMA/Dis.						0=UMA 1=Dis.
15.6"/14"			0=QLH/TWH 1=QLC/SWH			
MDC						0=YES 1=NO
Dobly					0=NO 1=YES	
Optiums						1=YES 0=NO



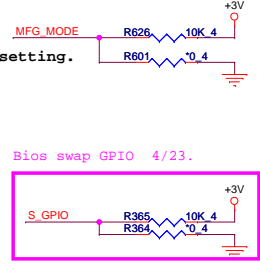
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

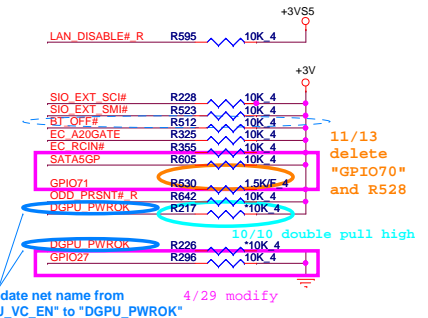


09

MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
 Low = Disable (Default)
 High = Enable

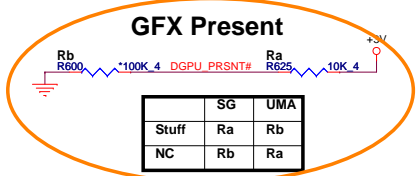
BIOS RECOVERY High = Disable (Default)
 Low = Enable

SV_SET_UP
 High = Strong (Default)

TEST DETECT
 Low = Default

DMI TERMINATION VOLTAGE OVERRIDE Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE LOW - Tx, Rx terminated to same voltage

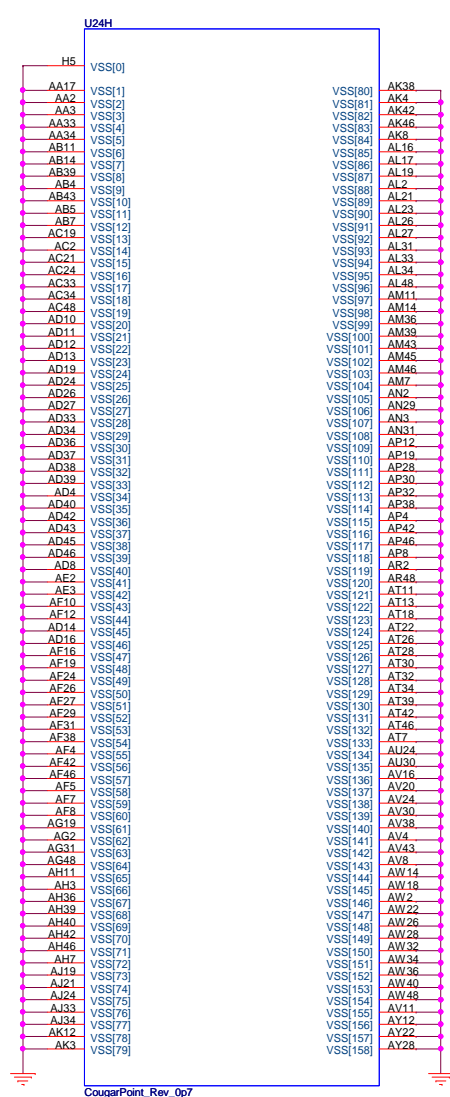
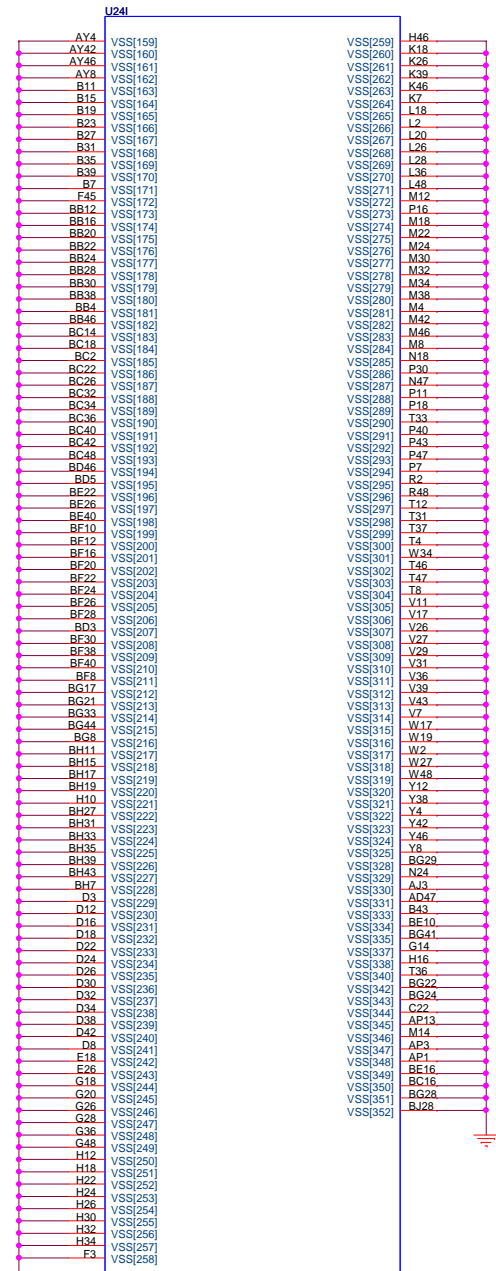


PROJECT : TWH
Quanta Computer Inc.

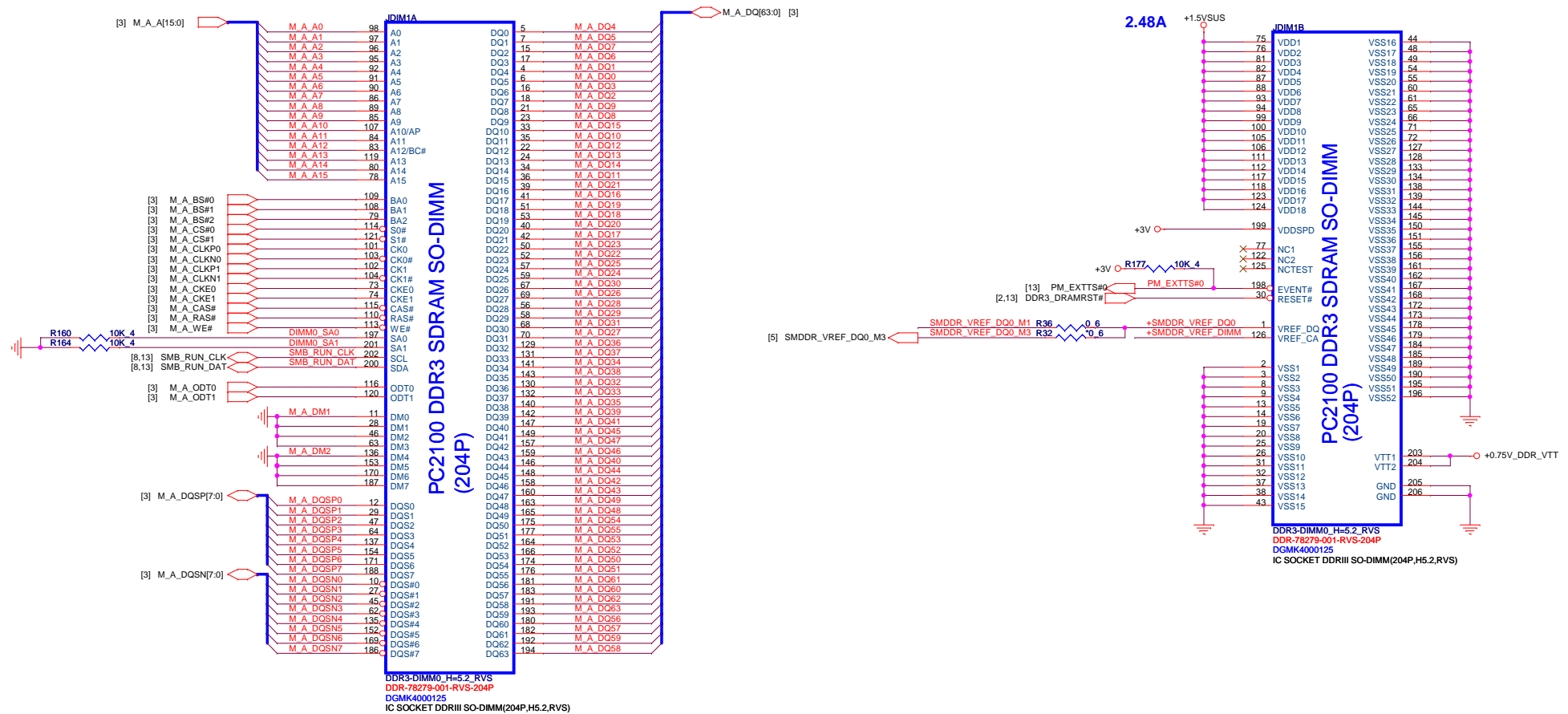
Size Custom Document Number PCH 4/6 (GPIO)
 Date: Monday, November 15, 2010 Sheet 9 of 40

IBEX PEAK-M (GND)

IBEX PEAK-M (GND)

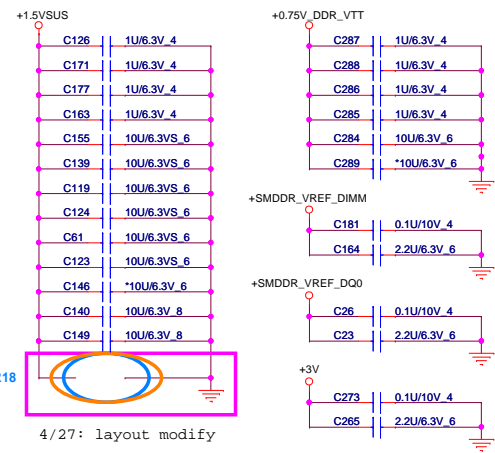


	PROJECT : TWH Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (Ground)	Rev A
	Date: Monday, November 15, 2010	Sheet 11 of 40	



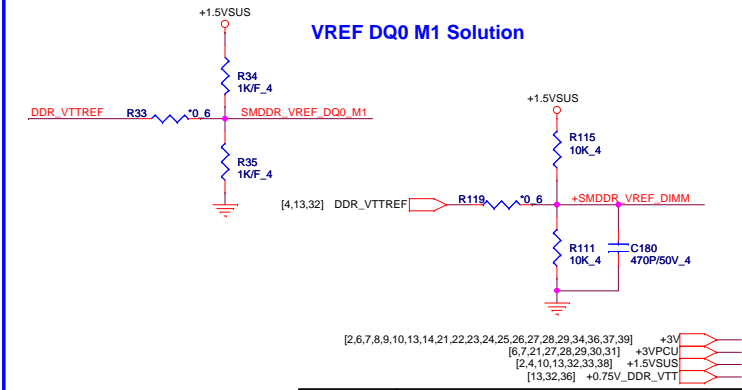
Remove M2 Solution (Intel 436996 Doc)

Place these Caps near So-Dimm0.



8/31 C513 FP changed from 330U_2.5V_5.0x5.9ESR10m to 220U/6.3V_6x4.5ESR18
11/13 delete C513

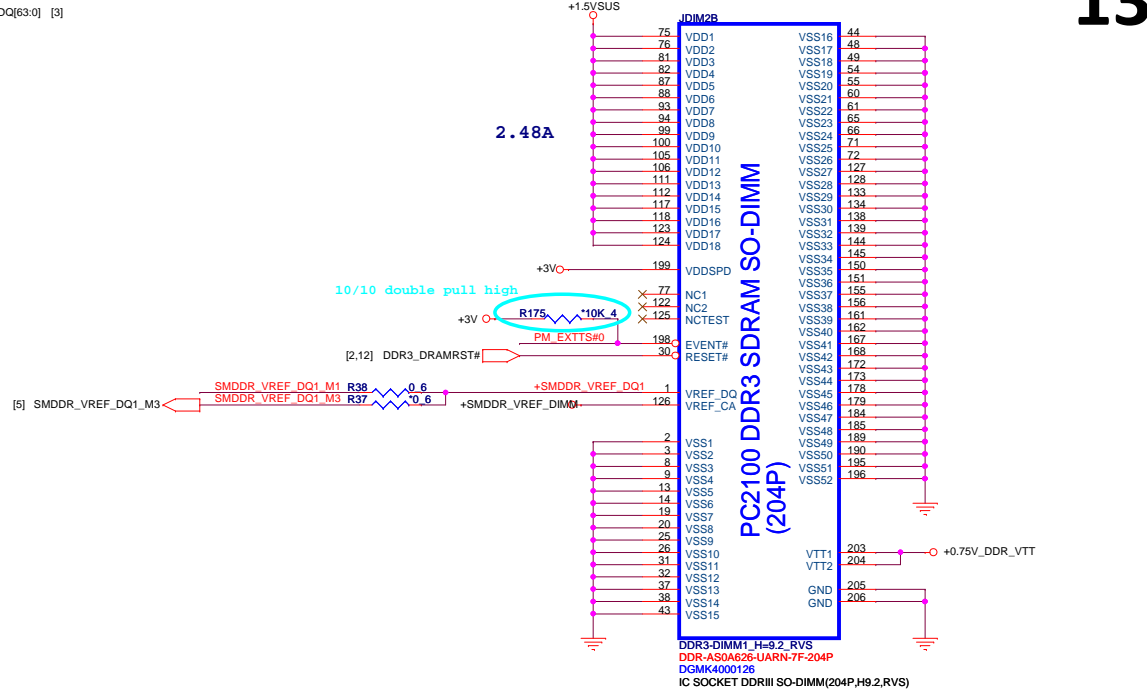
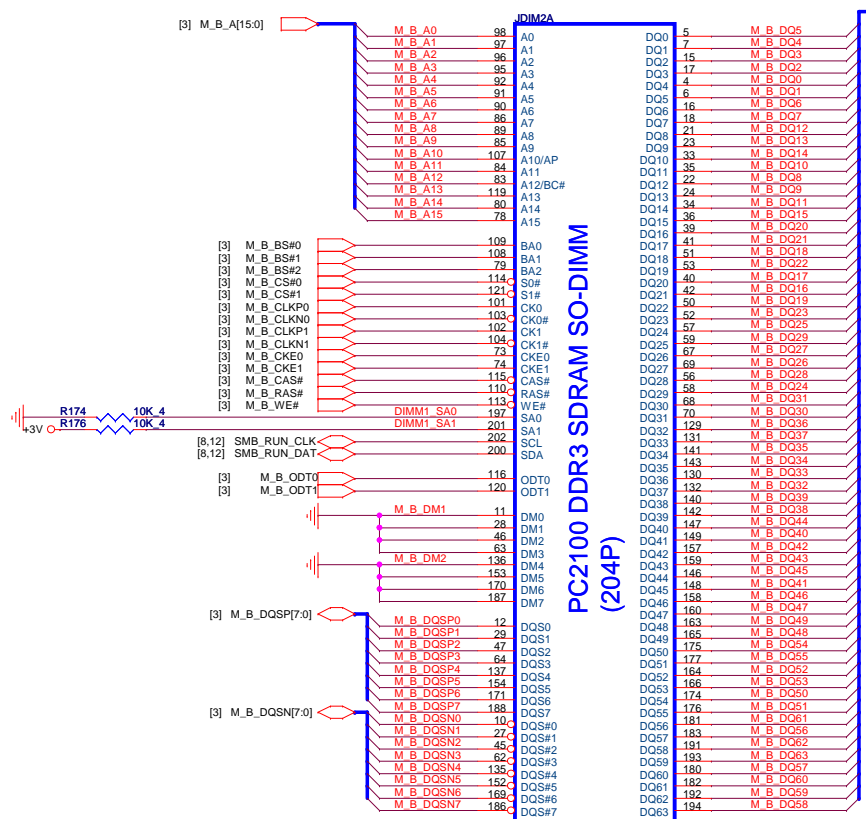
VREF DQ0 M1 Solution

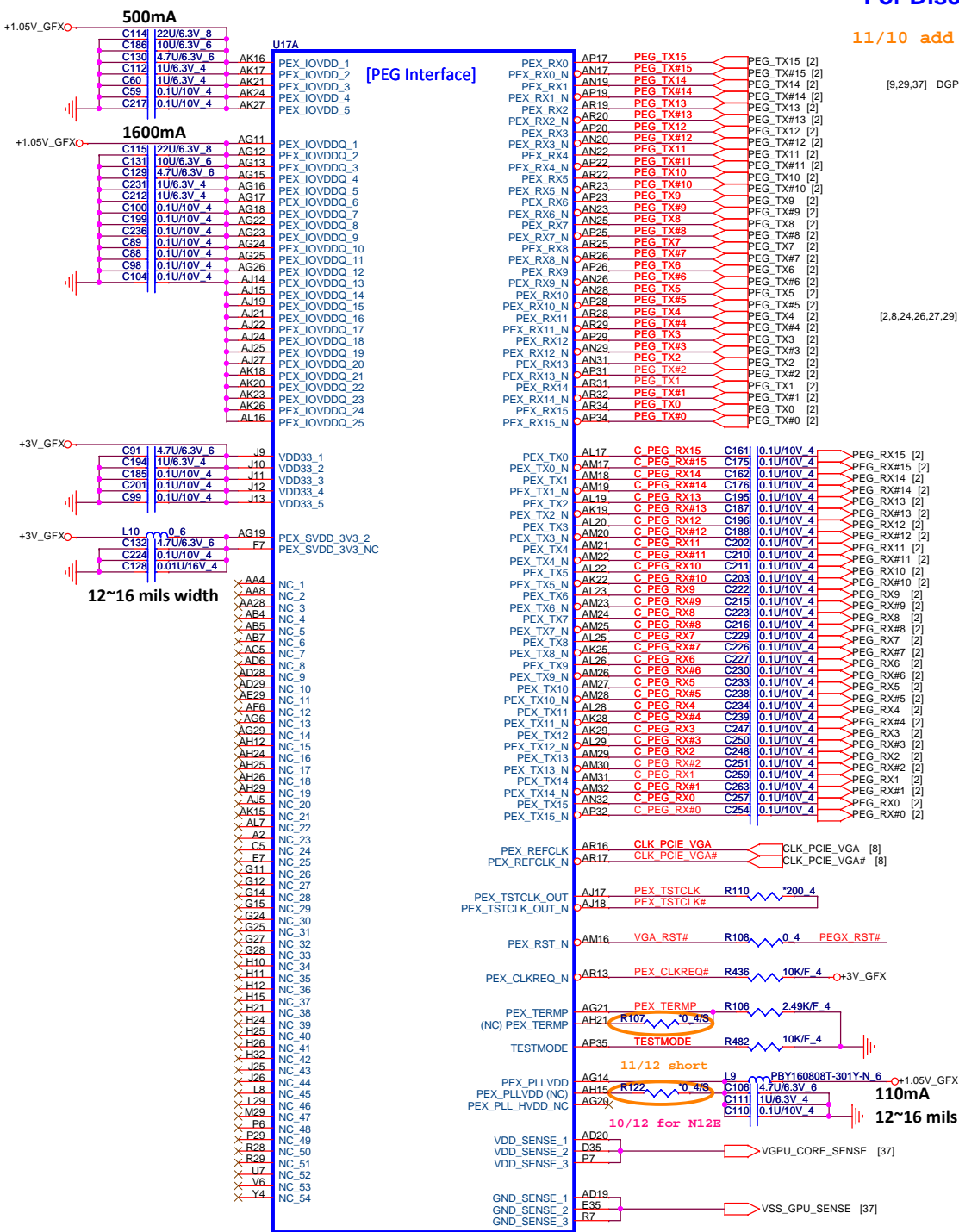


NBS

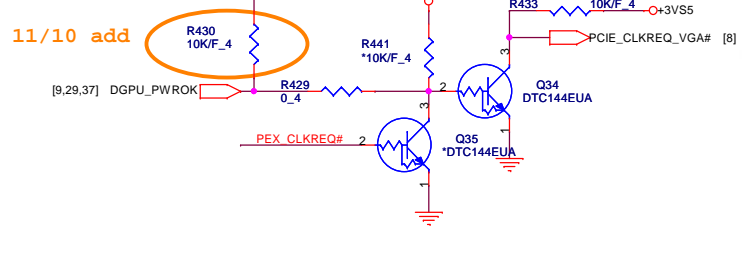
**PROJECT : TWH
Quanta Computer Inc.**

Size Custom	Document Number System Memory 1/2 (5.2H)	Rev A
Date: Monday, November 15, 2010	Sheet 12 of 40	





For Discrete



For Discrete

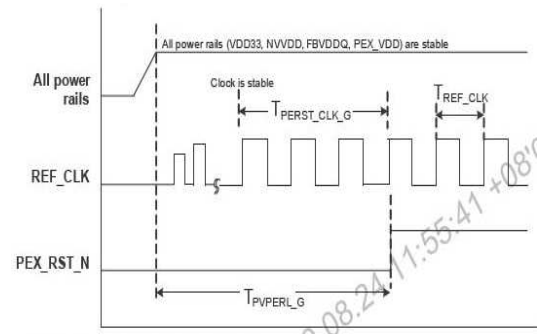
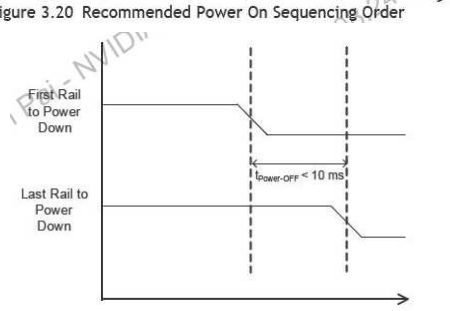
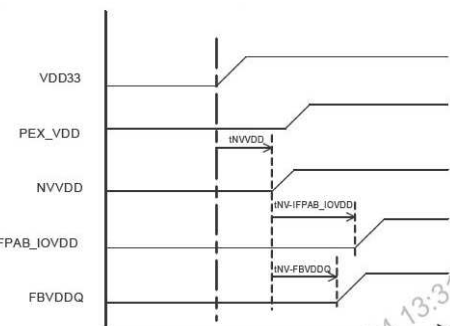
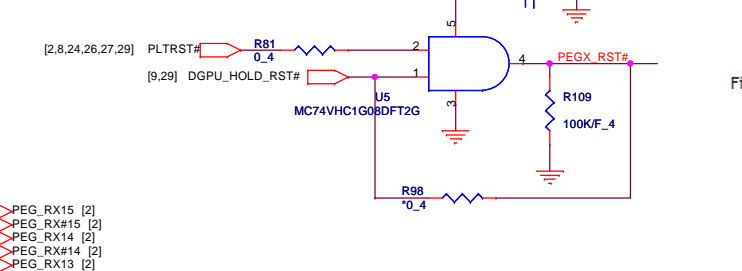


Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T _{PVPERL_G}	T _{PVPERL_G} ≥ 1μs	
T _{PERST_CLK_G}	T _{PERST_CLK_G} ≥ 11T _{REF_CLK}	

NVVDD Settling Time

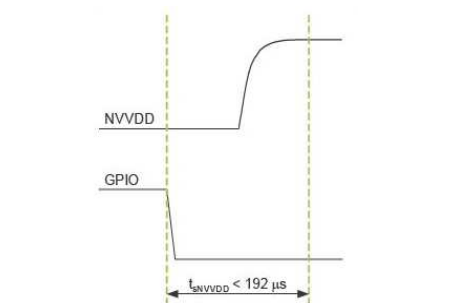
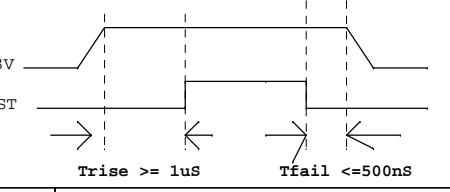


Figure 3.12 NVVDD Settling Time

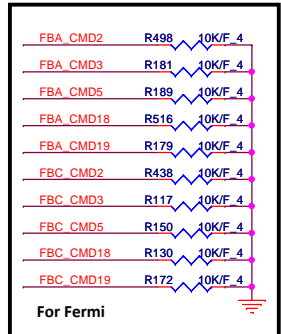
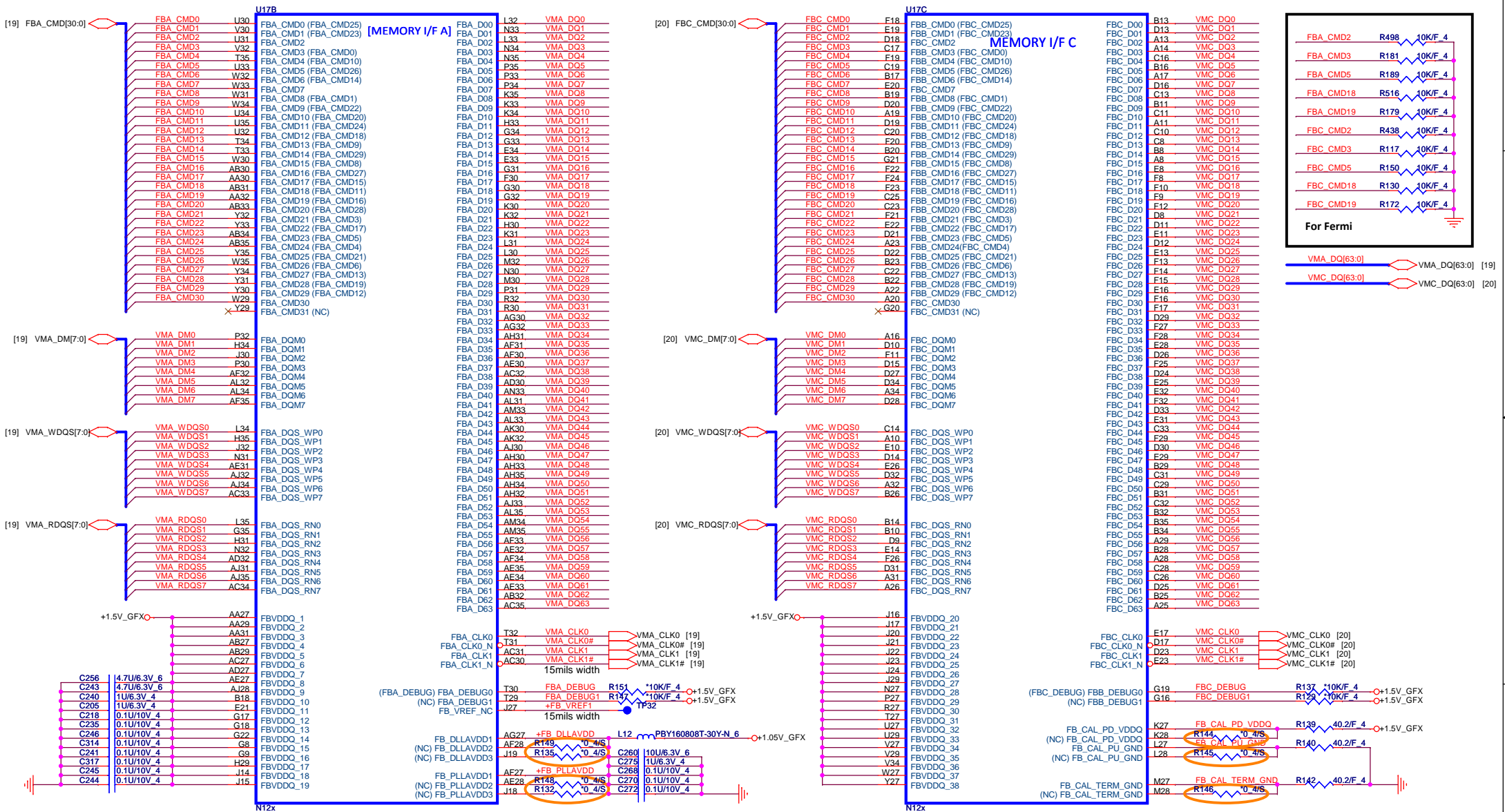
PEX_RST timing



PROJECT : TWH
Quanta Computer Inc.

Size A3	Document Number DGPU 1/5 (PEG)	Rev A
Date: Monday, November 15, 2010		Sheet 14 of 40

[15,16,37,38] +1.05V_GFX
[16,17,22,37,38] +3V_GFX



N12P AJ0N12P0T04

10/12 for N12E
11/12 short

N12P AJ0N12P0T04

10/12 for N12E
11/12 short

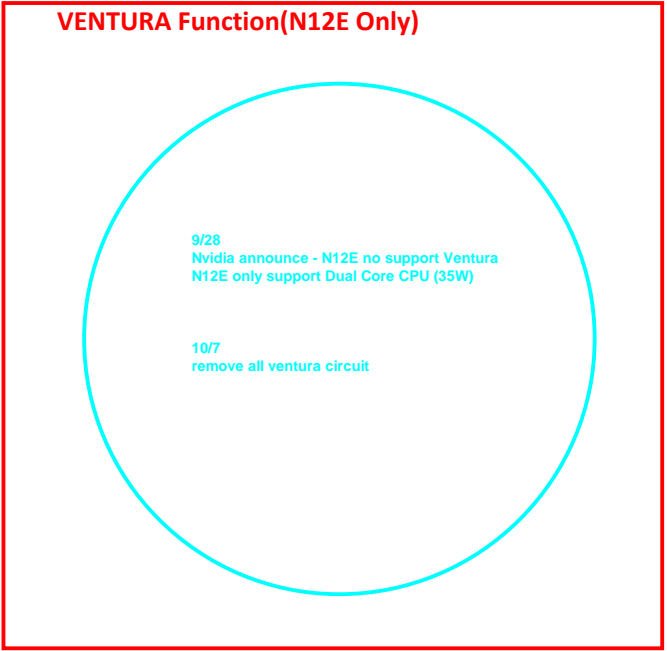
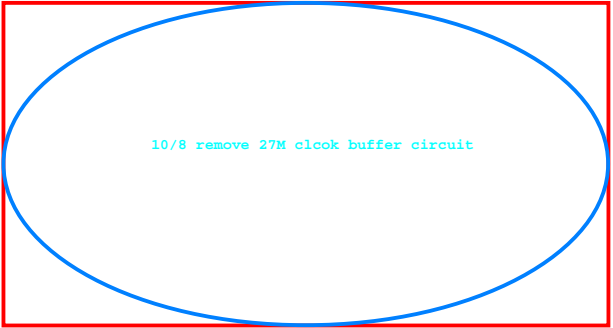
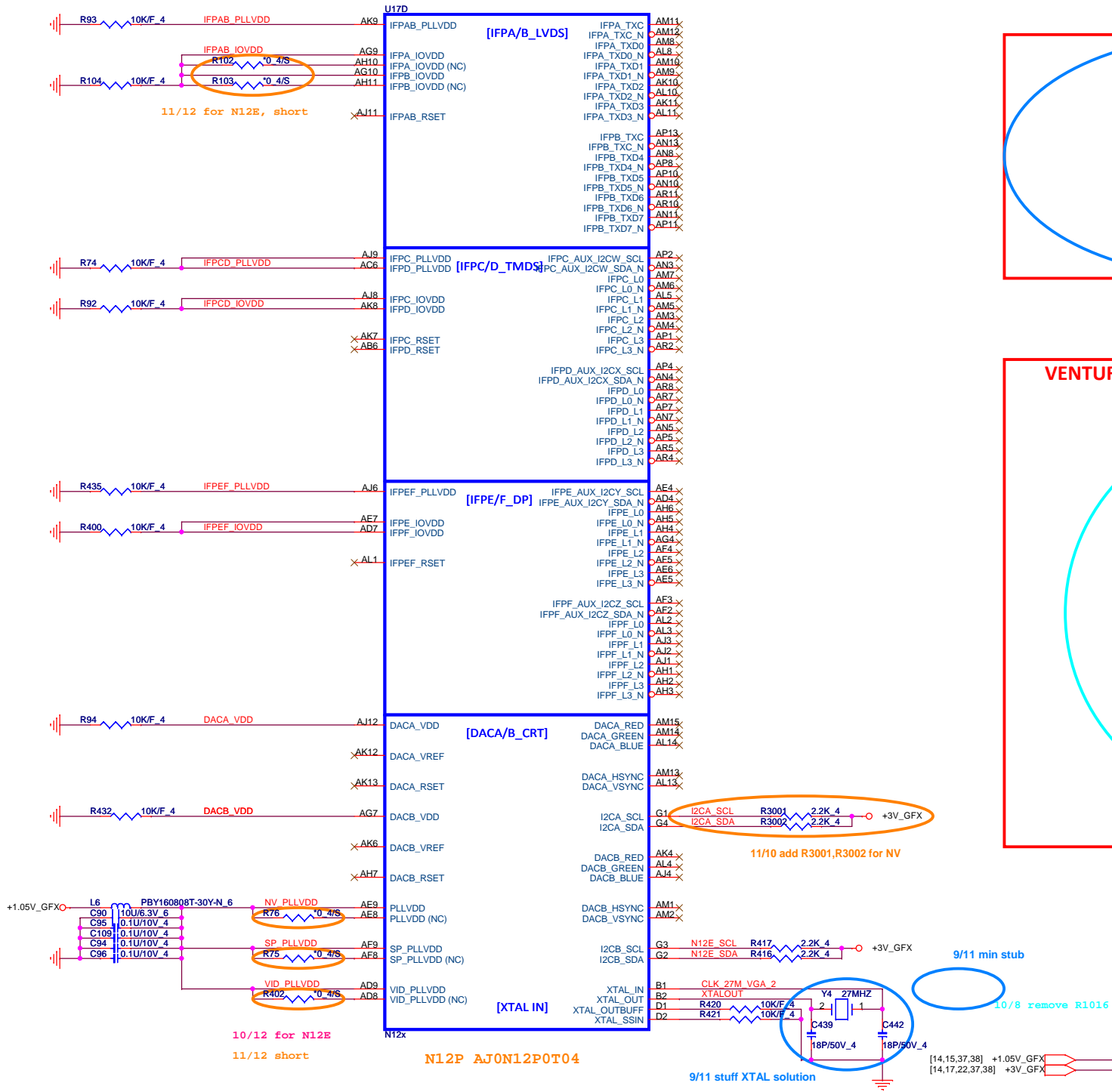
NBS

PROJECT : TWH
Quanta Computer Inc.

Size A3 Document Number **DGPU 2/5 (Memory)** Rev A

Date: Monday, November 15, 2010 Sheet 15 of 40

[14,16,37,38] +1.05V_GFX
[19,20,37,38] +1.5V_GFX

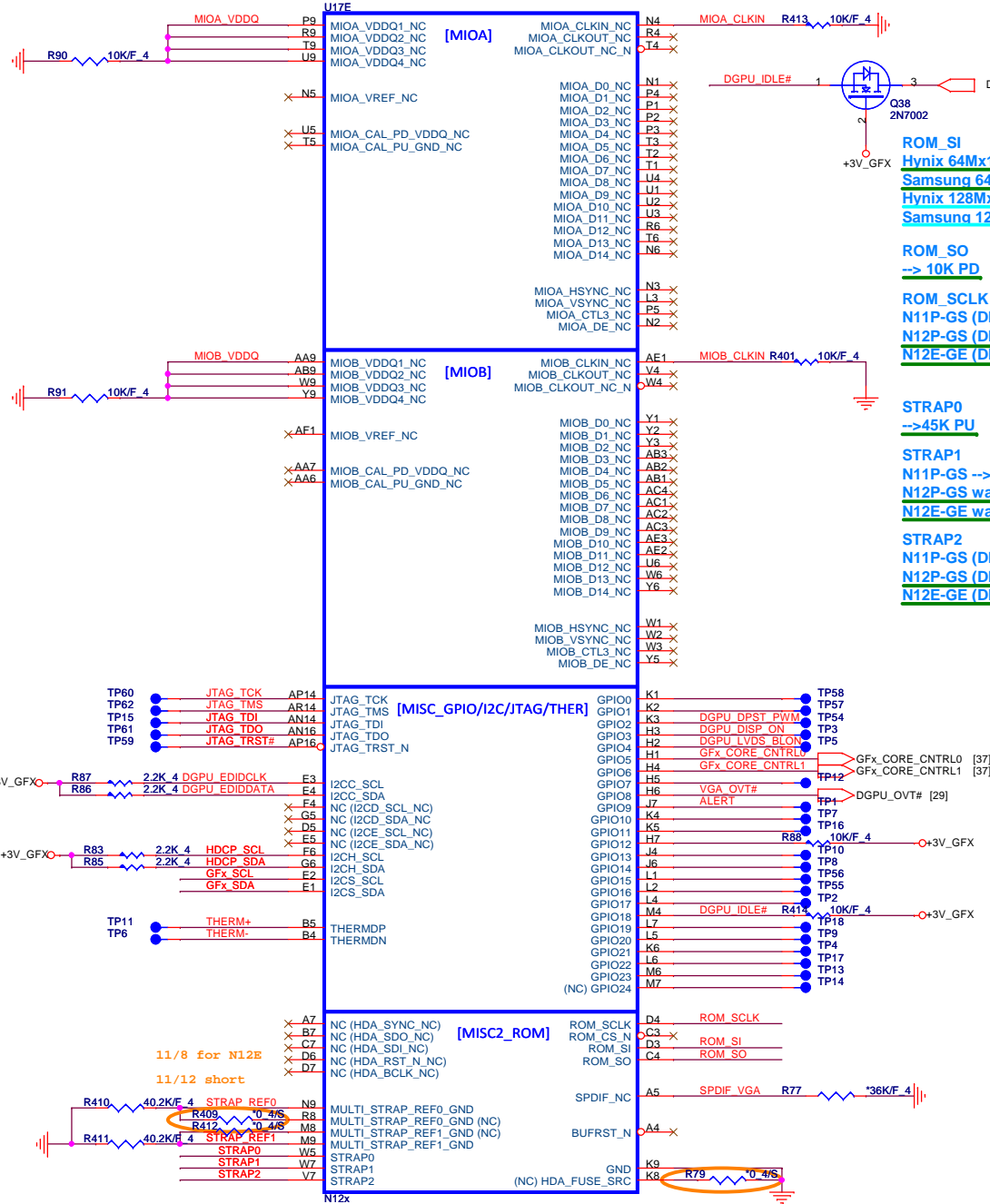


**PROJECT : TWH
Quanta Computer Inc.**

Size A3	Document Number DGPU 3/5 (Display)	Rev A
Date: Monday, November 15, 2010	Sheet 16 of 40	

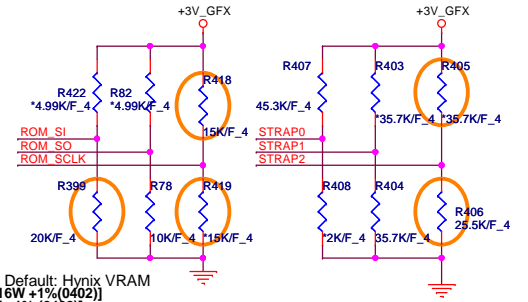
N11P-GS ES
Strap2 = 35K Pull High
ROM_CLK=15k Pull High

N11P-GS QS
Strap2 = 5K Pull High
ROM_CLK=15k Pull High



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



ROM_SI
Hynix 64Mx16 -->15K PD
Samsung 64Mx16 -->20K PD
Hynix 128Mx16 -->35K PD
Samsung 128Mx16 -->45K PD

ROM_SO
--> 10K PD

ROM_SCLK
N11P-GS (DID=0DF0) ----> 15k PU
N12P-GS (DID=0DF4) ---->15K PU
N12E-GE (DID=0DCE) ---->15K PU

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111

STRAP0
-->45K PU

STRAP1
N11P-GS -->35K PD
N12P-GS waiting PUN update
N12E-GE waiting PUN update

STRAP2
N11P-GS (DID=0DF0) ----> 5k PD
N12P-GS (DID=0DF4) ---->25K PD
N12E-GE (DID=0DCE)---->35K PU

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

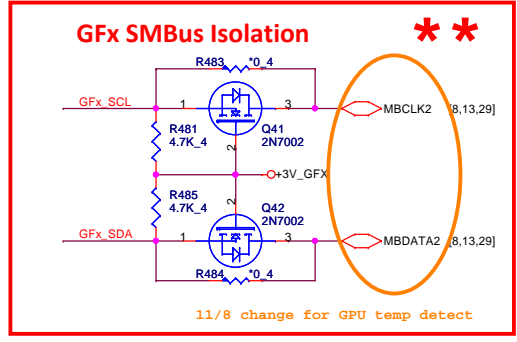
Default: Hynix VRAM
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



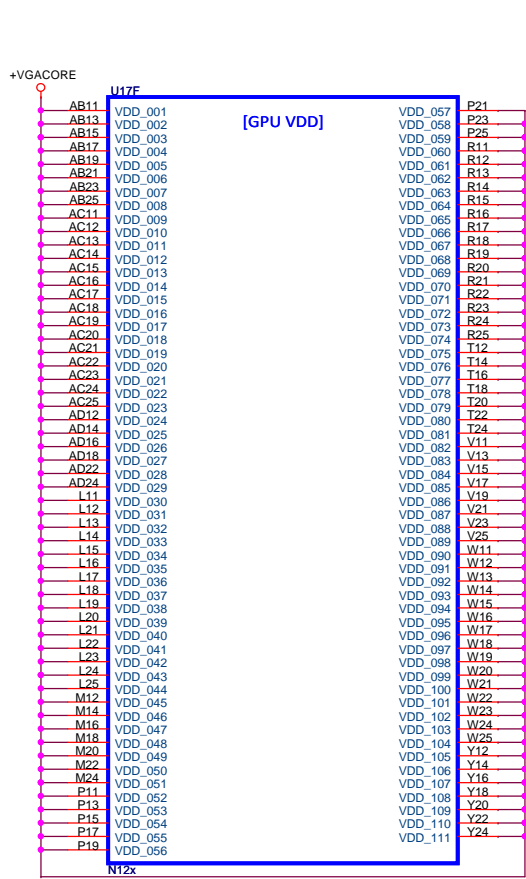
N12P AJ0N12P0T04

PROJECT : TWH Quanta Computer Inc.

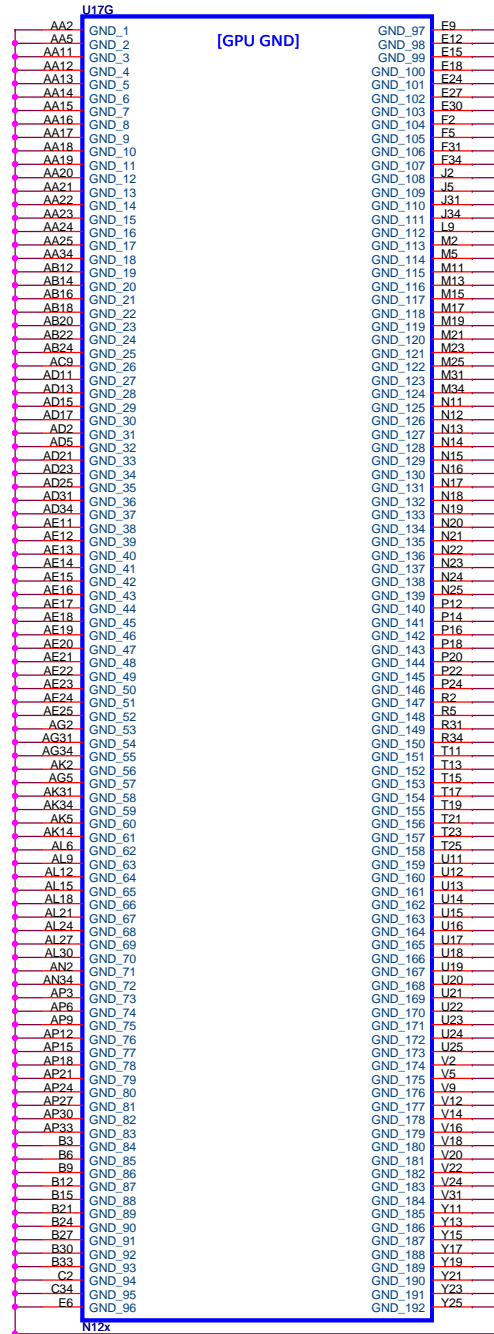
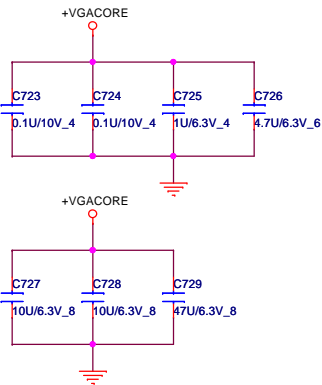
NBS

Size Custom Document Number **DGPU 4/5 (MIO/GPIO)** Rev A

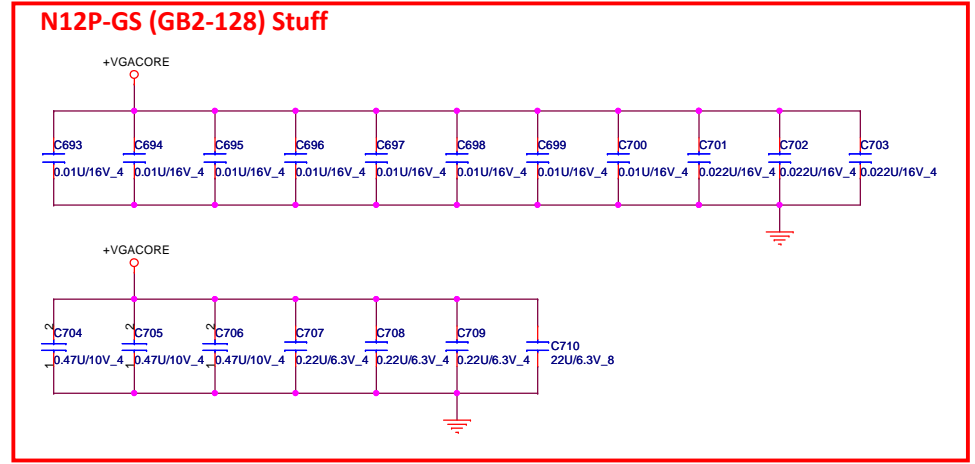
Date: Monday, November 15, 2010 Sheet 17 of 40



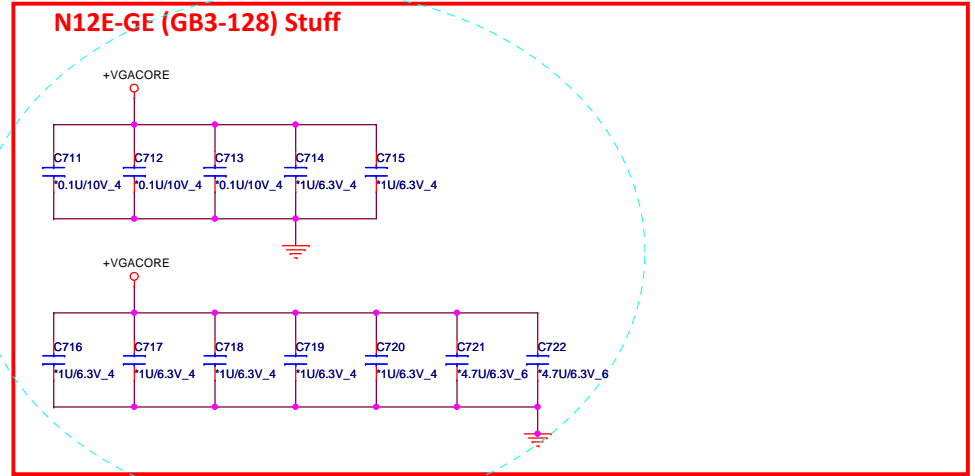
N12P AJON12P0T04



N12P AJON12P0T04



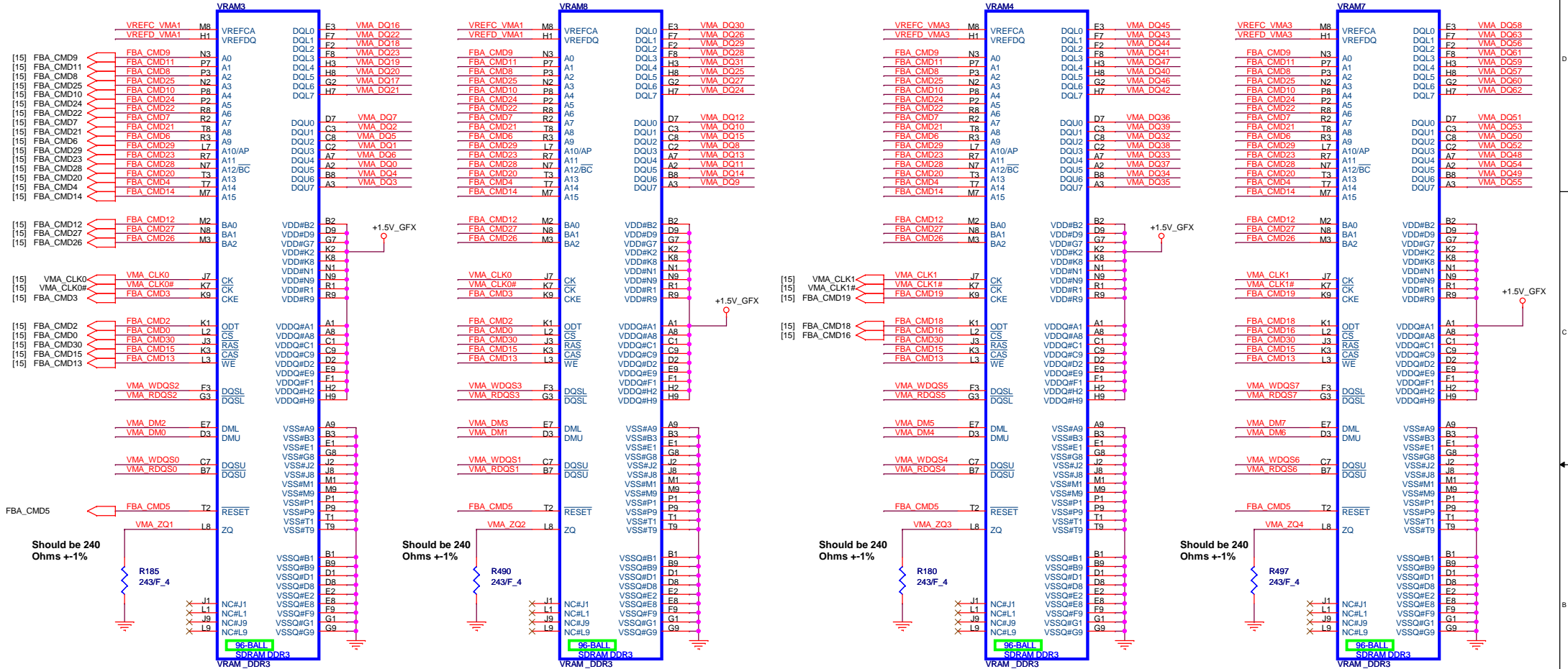
N12E-GE: C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411 stuff 0.1U/10V_4. N12E-GE: C412 Stuff 47U/6.3V_8



9/28 need check for N12E

	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size A3	Document Number DGPU 5/5 (Power/Ground)	Date: Monday, November 15, 2010

CHANNEL A: 256MB/512MB DDR3

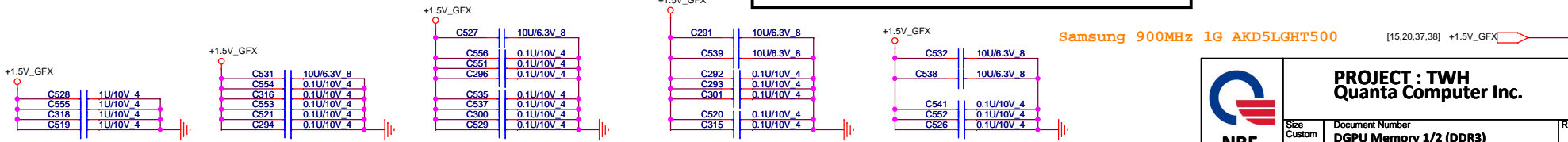


VMA_CLKO
R178
160/F_4
VMA_CLKO#

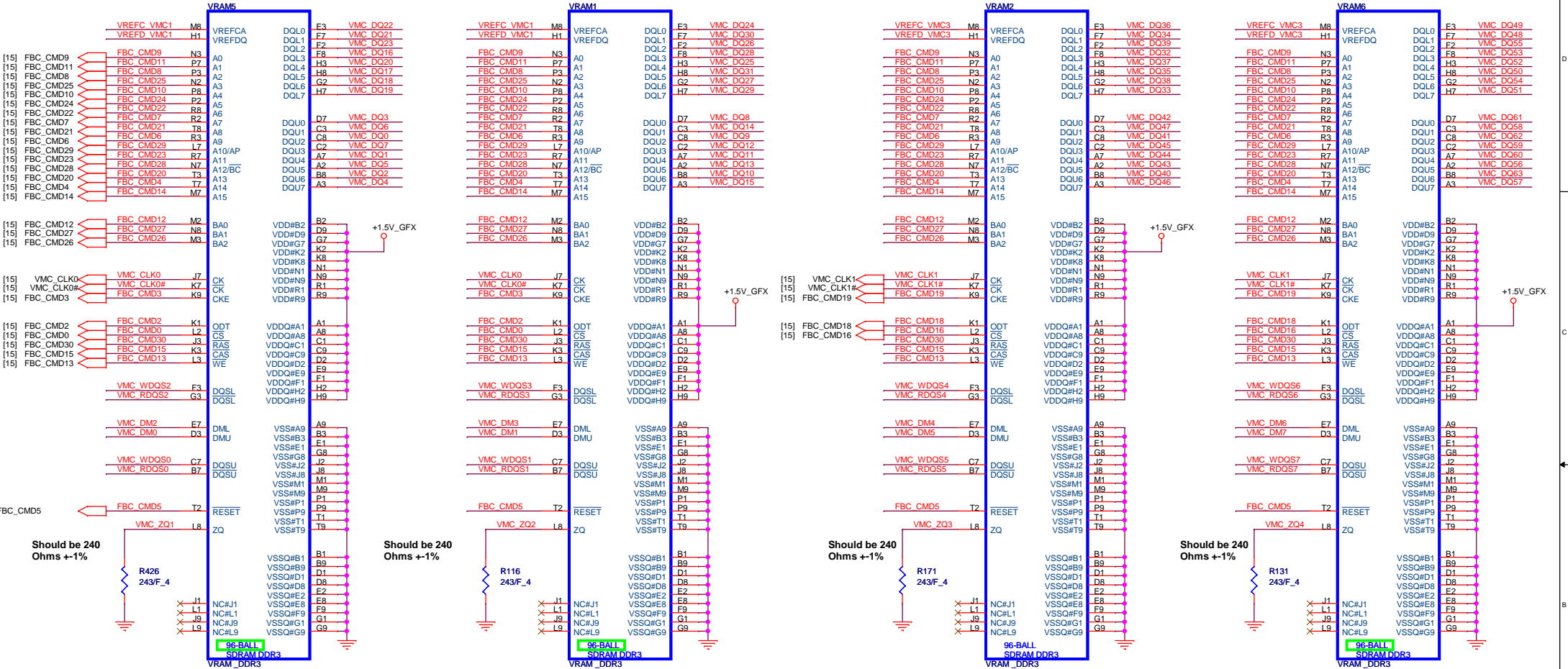
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1#
R183
160/F_4
VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)



CHANNEL B: 256MB/512MB DDR3

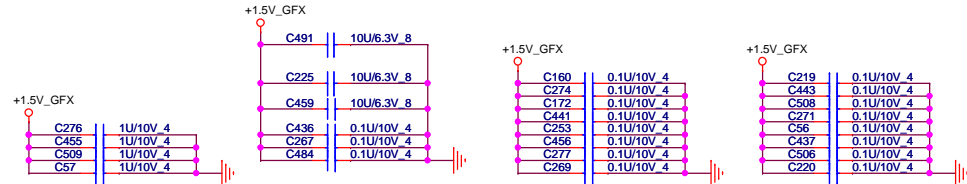


VMC CLK0
 R61 160F_4
 VREFC VMC1
 VREFD VMC1#

Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMC CLK1
 R173 160F_4
 VREFC VMC3
 VREFD VMC3#

Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)



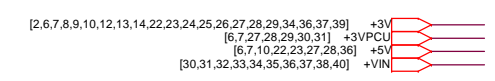
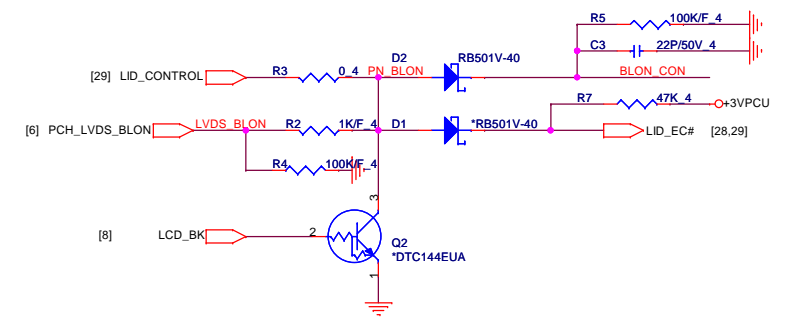
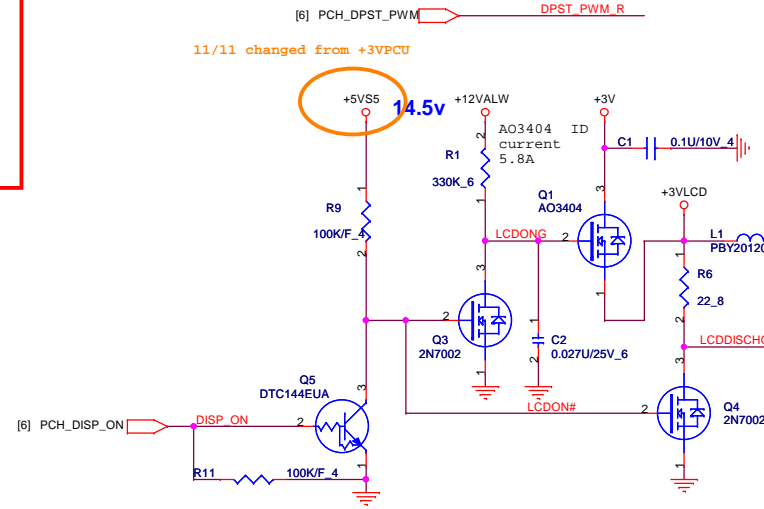
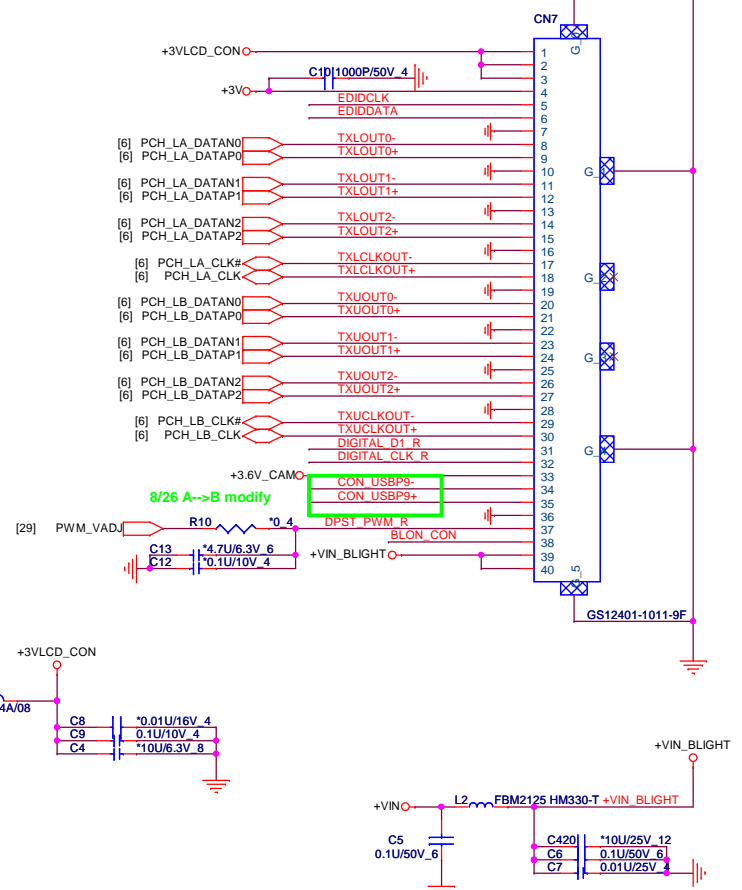
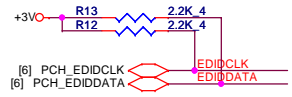
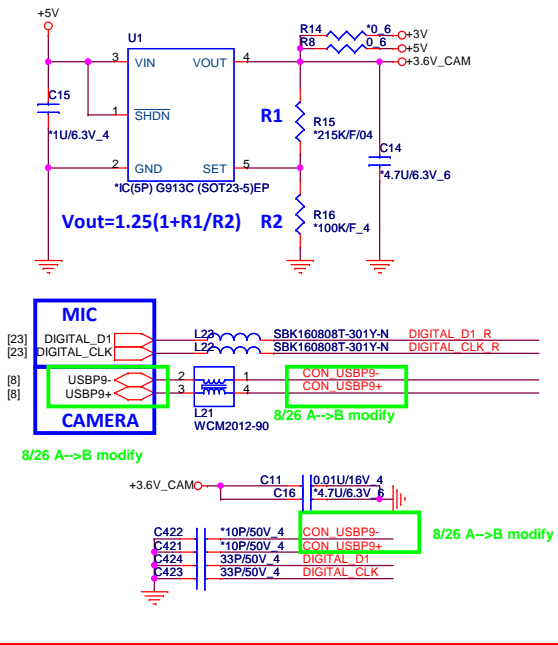
[15] FBC_CMD17 <-> FBC_CMD17 TP26
 [15] FBC_CMD1 <-> FBC_CMD1 TP21
 [15,19,37,38] <-> +1.5V_GFX

PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number DGPU Memory 2/2 (DDR3)	Rev A
Date: Monday, November 15, 2010	Sheet 20 of 40	

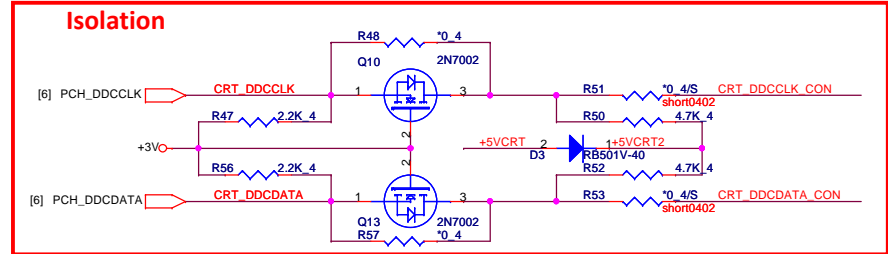
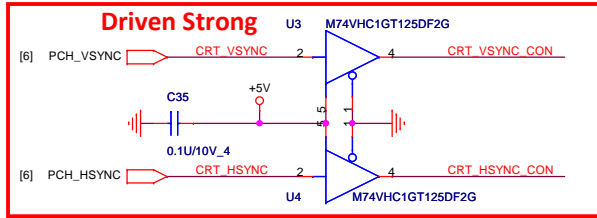
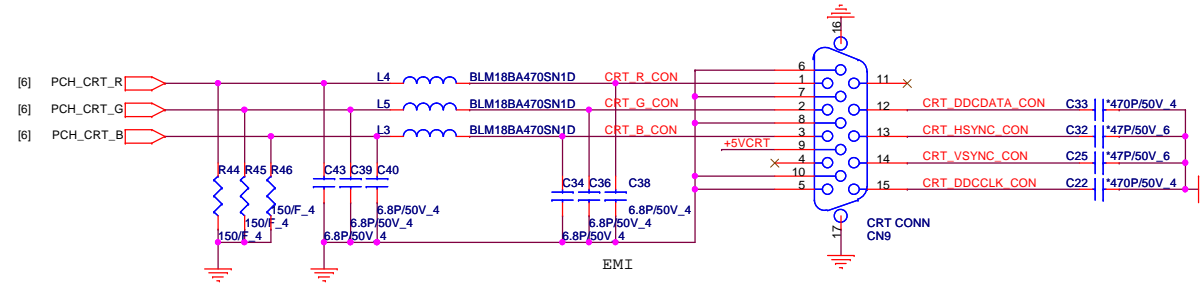
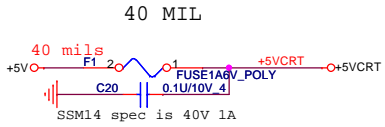
Samsung 900MHz 1G AKD5LGH500

USB Camera Connector

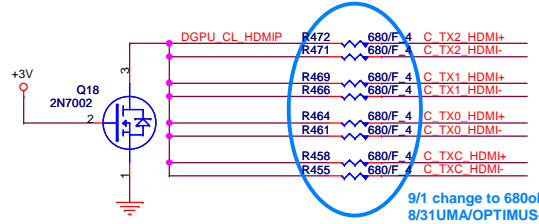
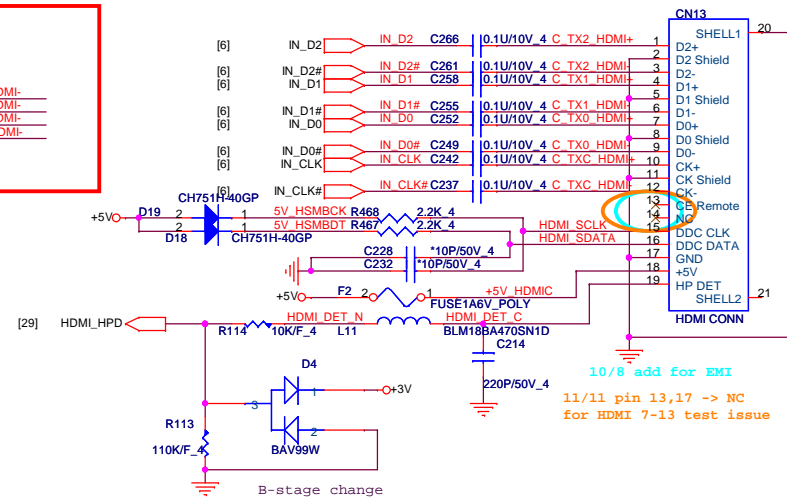
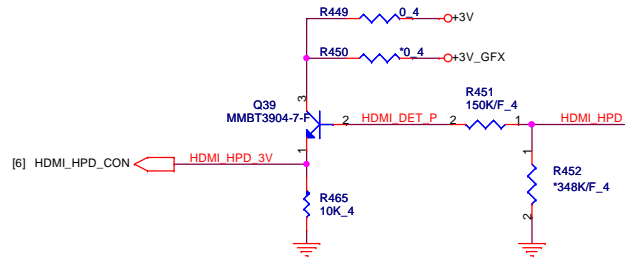
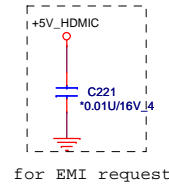
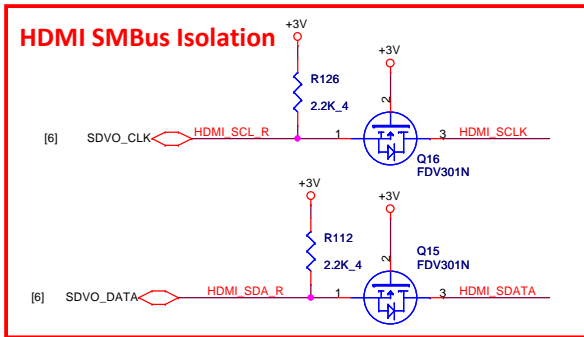


		PROJECT : TWH Quanta Computer Inc.	
		Size Custom Document Number LCD Connector (LVDS)	Rev A
Date: Monday, November 15, 2010		Sheet 21 of 40	

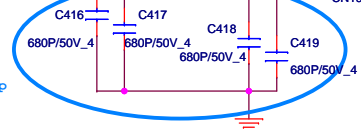
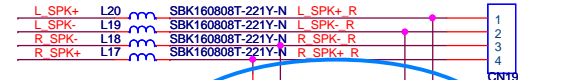
CRT PORT



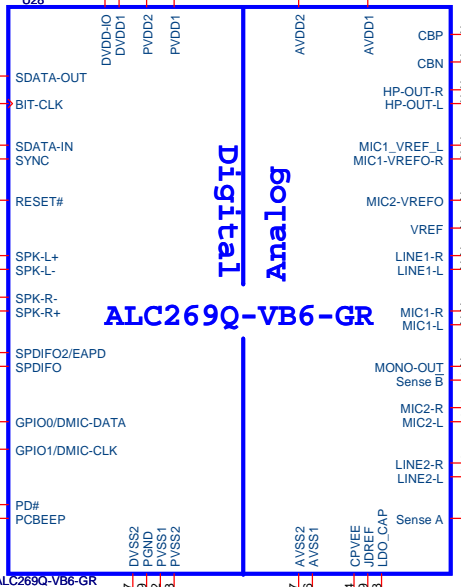
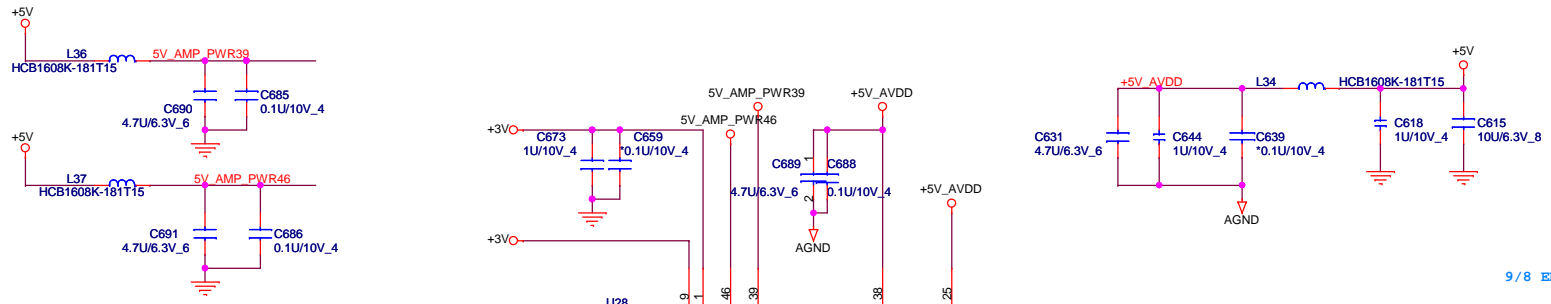
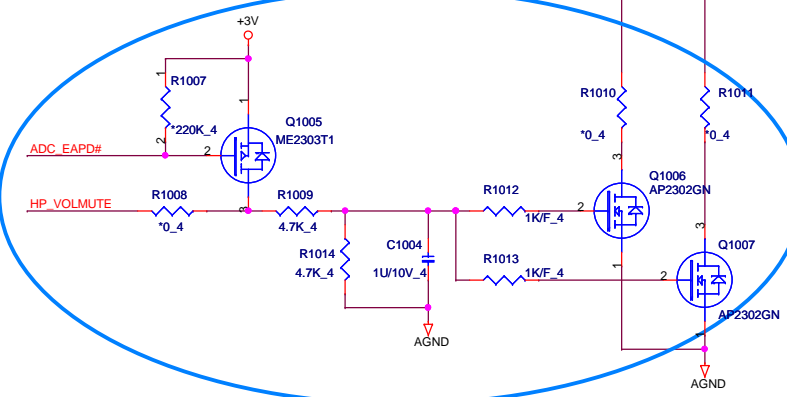
HDMI PORT



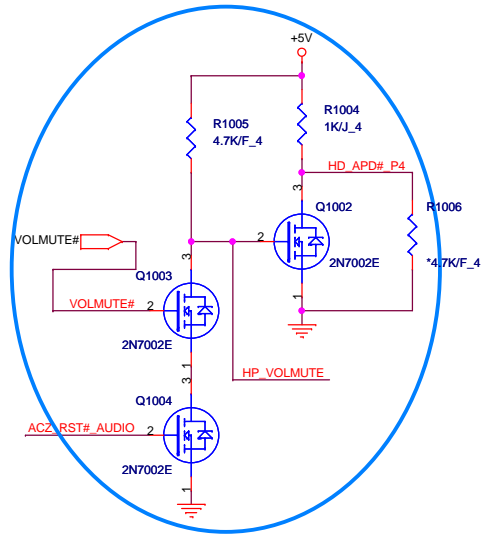
Internal Speaker



9/5 add de-pop circuit, add C1002, C1003, C1004 Q1005, Q1006, Q1007 R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014

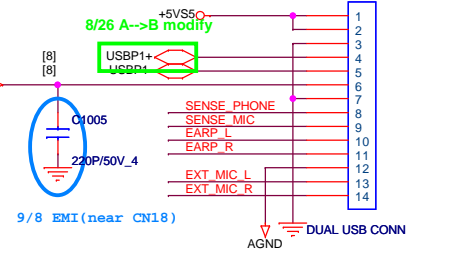
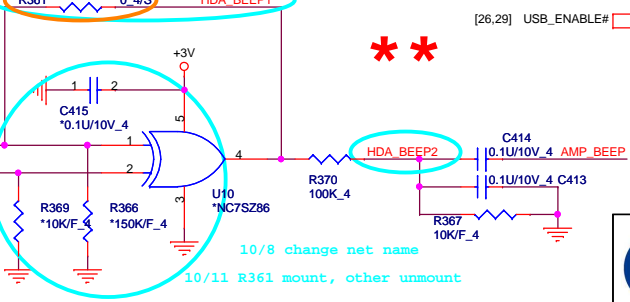


9/5 "PD#" circuit modify
 1.delete R650, R372, R373, Q27, Q28, D16, D17, D15
 2.add Q1002, Q1003, Q1004, R1004, R1005, R1006



10/5 change VB6

11/12 short



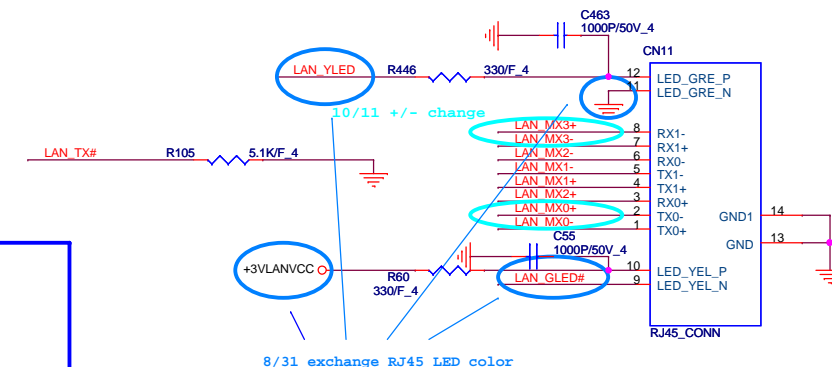
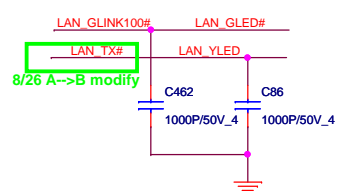
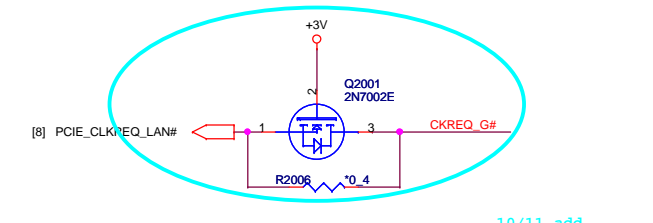
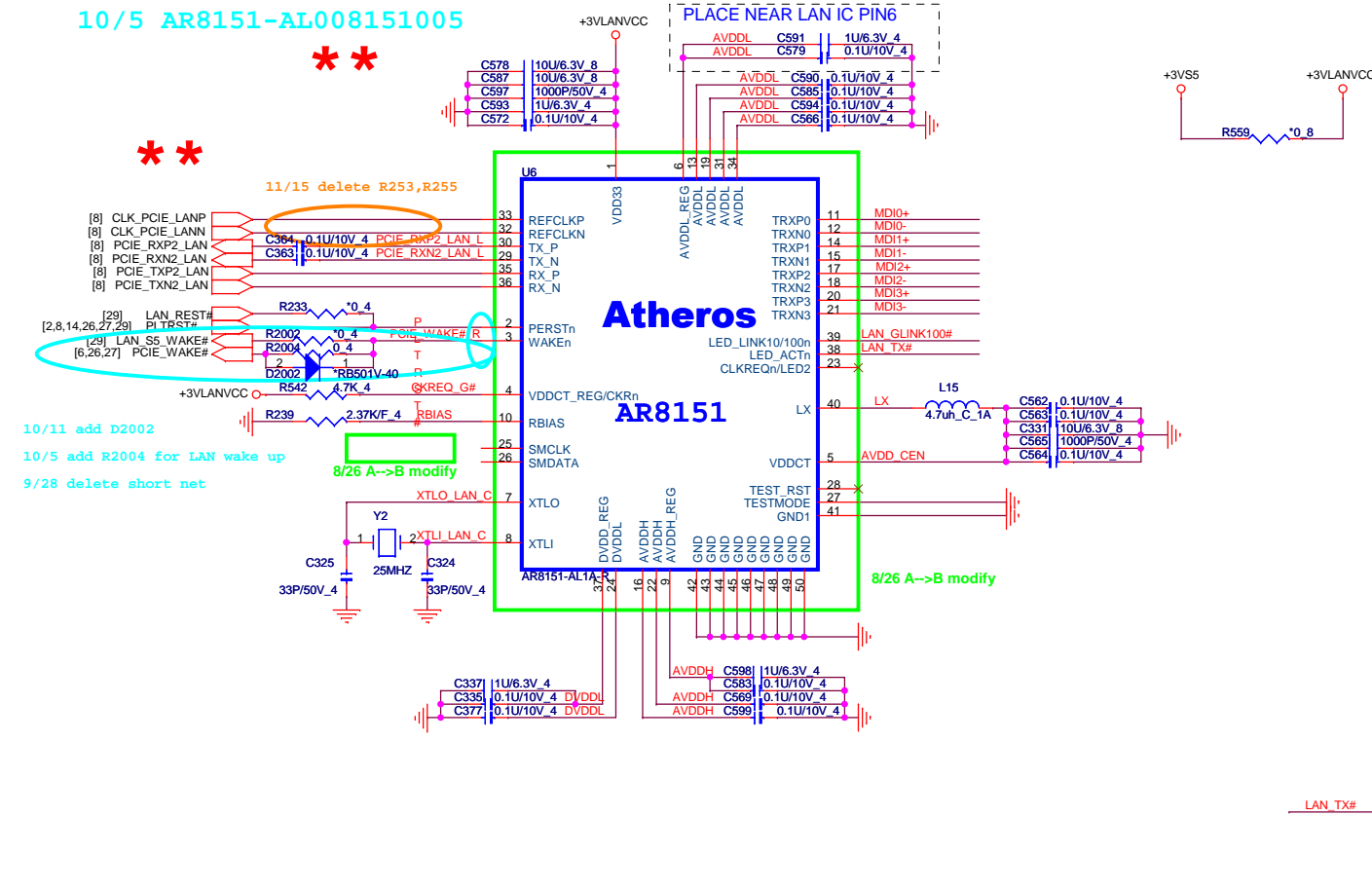
PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number **Audio Codec (Realtek_ALC269)** Rev A

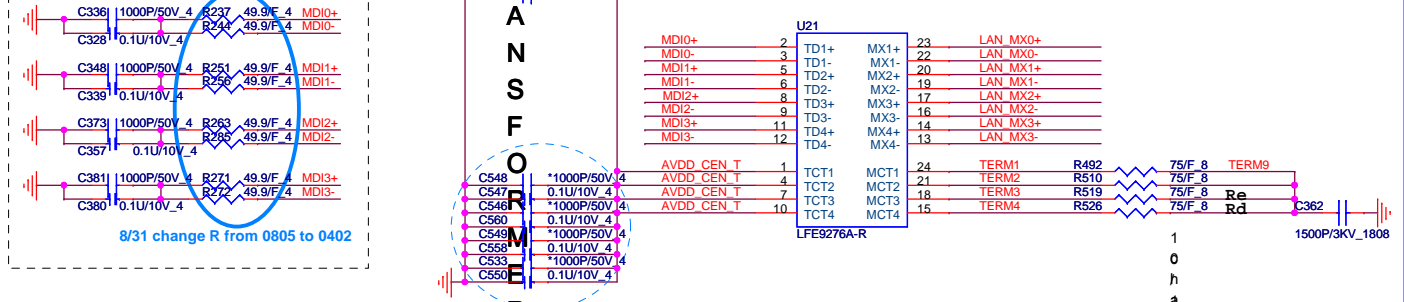
Date: Monday, November 15, 2010 Sheet 23 of 40

Atheros Lan

10/5 AR8151-AL008151005



PLACE NEAR LAN IC SIDE



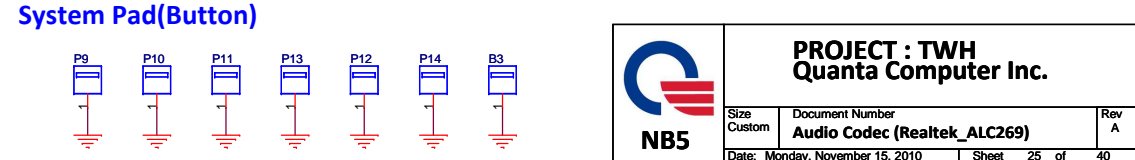
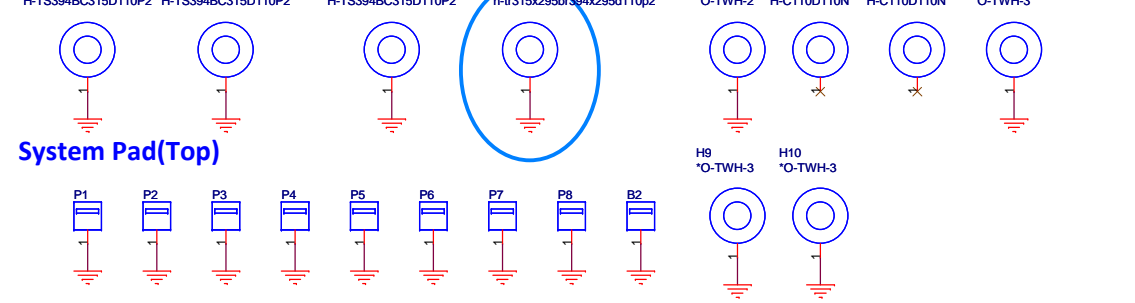
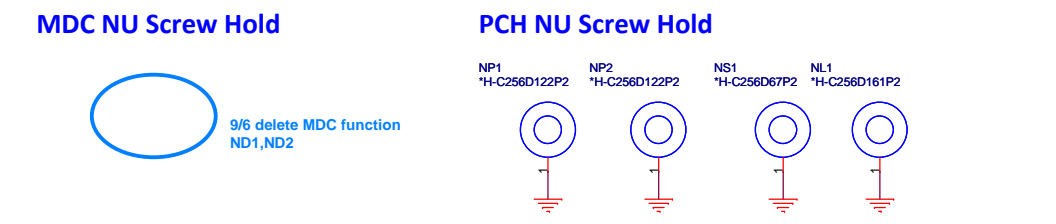
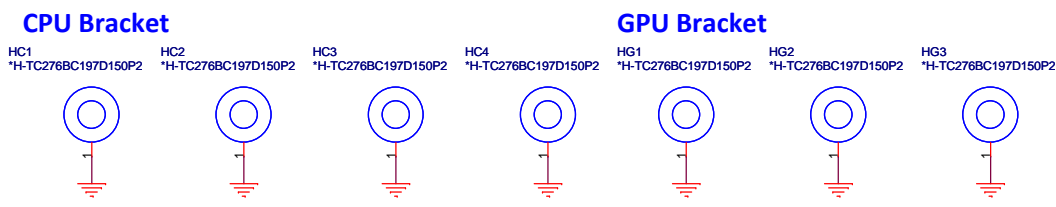
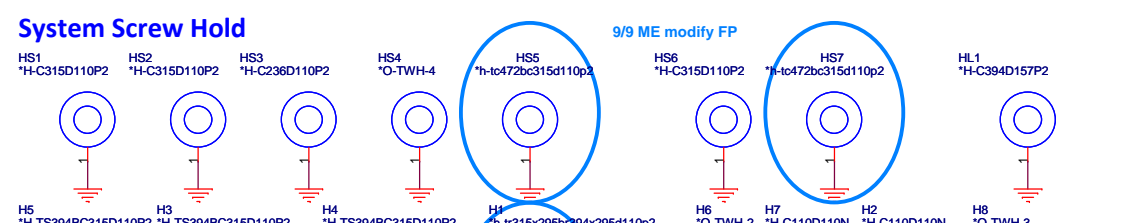
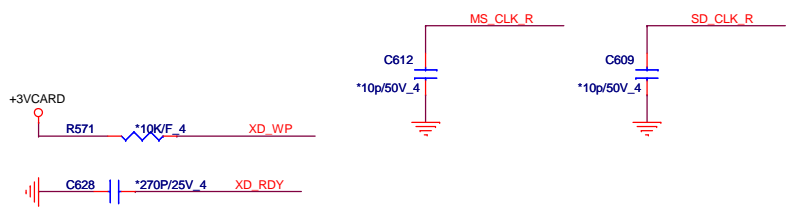
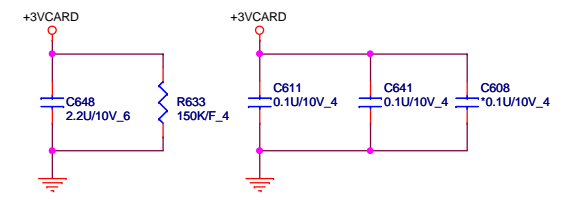
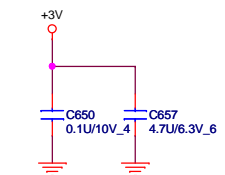
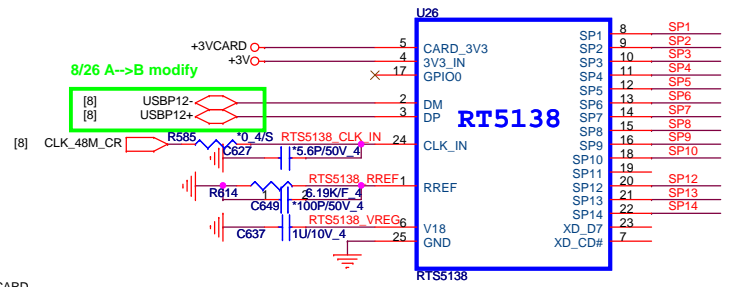
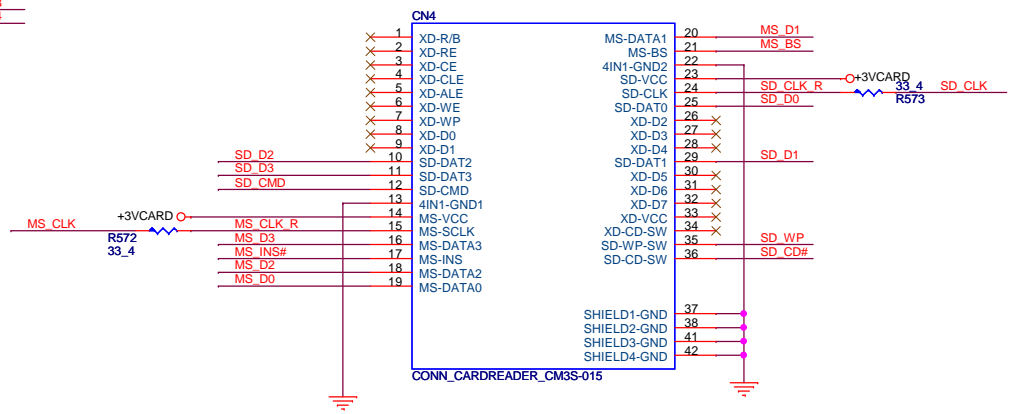
D3A: only UMA sku support 1G,If support 10/100 in UMA SKU, R55,R56 change to 0-ohm

PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number LAN Controller (Atheros_AR8151)	Rev A
Date: Monday, November 15, 2010		Sheet 24 of 40

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CMD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS

Share Pin

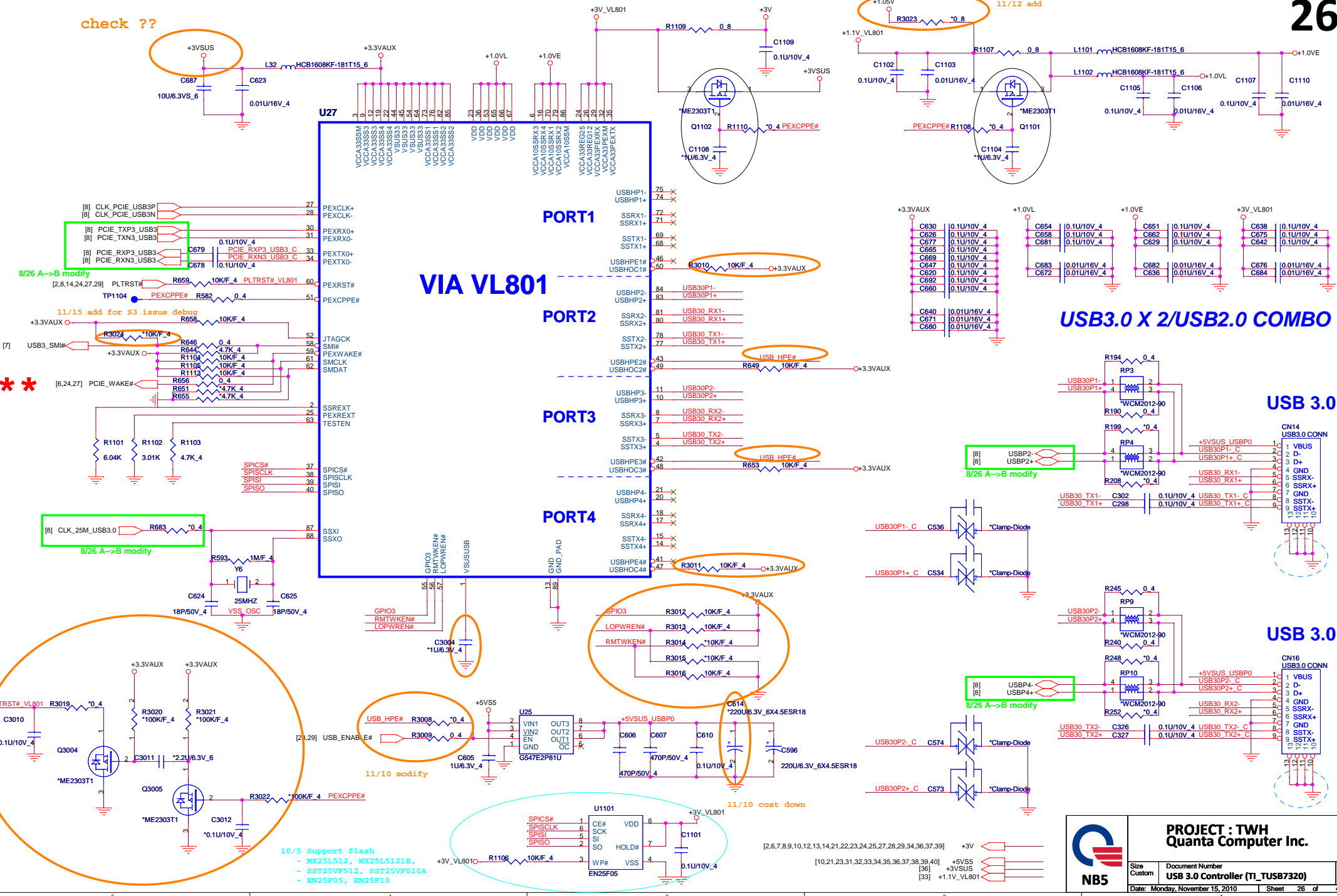


PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number **Audio Codec (Realtek_ALC269)** Rev A

Date: Monday, November 15, 2010 Sheet 25 of 40

check ??



VIA VL801

PORT1

PORT2

PORT3

PORT4

USB3.0 X 2/USB2.0 COMBO

USB 3.0

USB 3.0

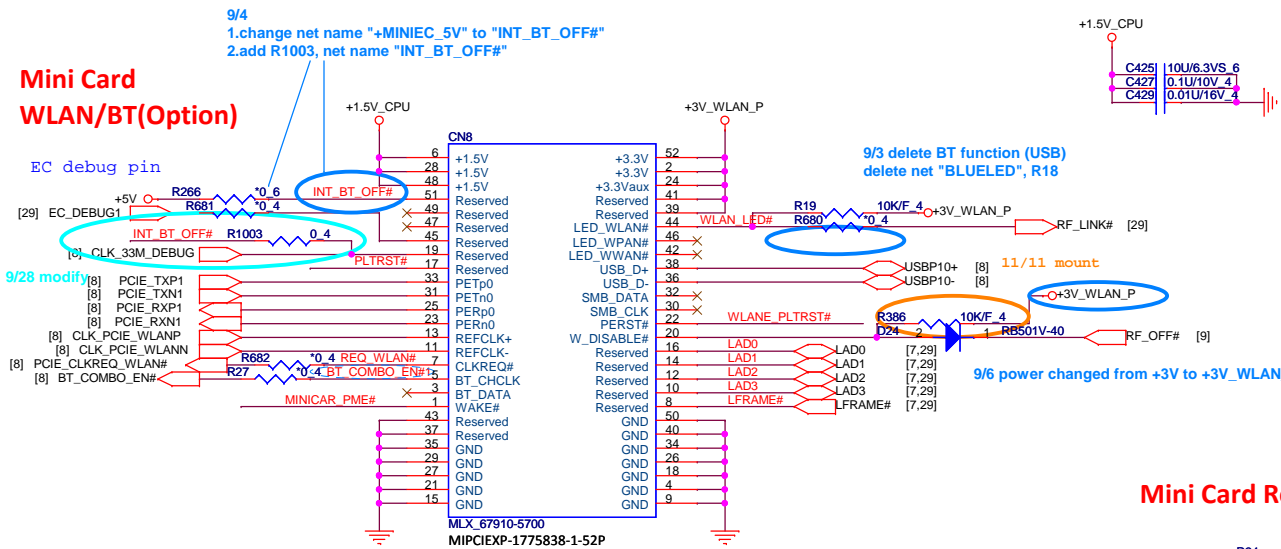
- 10/5 Support flash
- MX25L512, MX25L512E,
- SST25VF512, SST25VF010A
- EN25F05, EN25F10

PROJECT : TWH
Quanta Computer Inc.

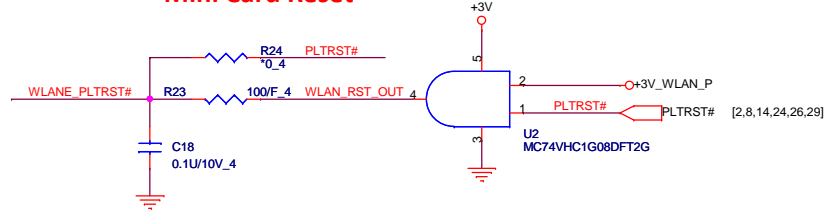
Size Custom	Document Number USB 3.0 Controller (TI_TUSB7320)	Rev A
Date: Monday, November 15, 2010	Sheet 26 of 40	

- [6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,34,36,37,39]
- [10,21,23,31,32,33,34,35,36,37,38,39,40]
- [36]
- [33]

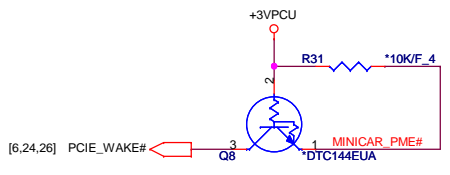
Mini Card WLAN/BT(Optional)



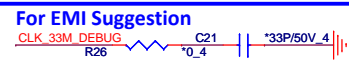
Mini Card Reset



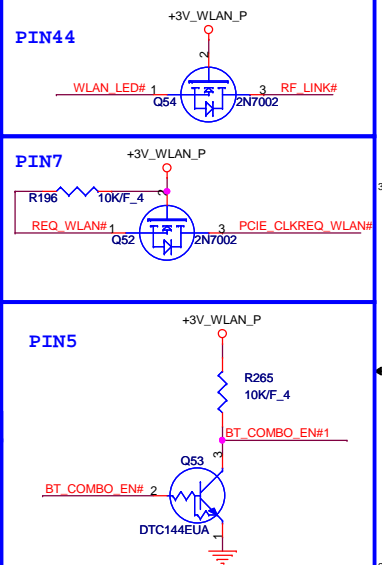
Support Wake Function(Reserve)



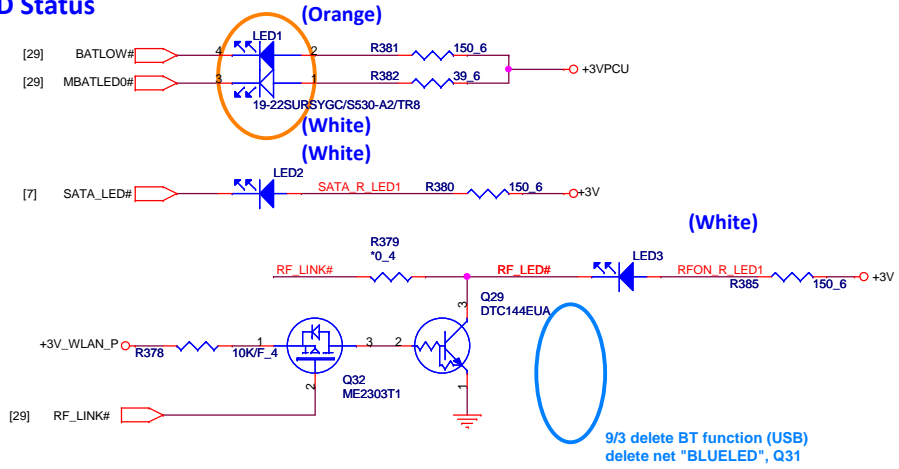
LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF



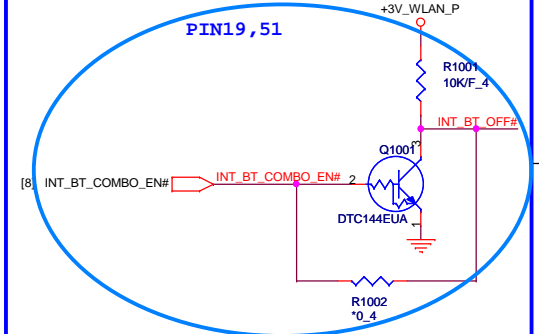
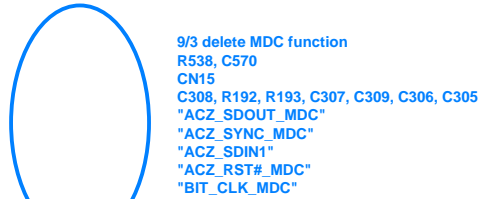
Avoid leakage issue



LED Status



MDC Connector(Optional)

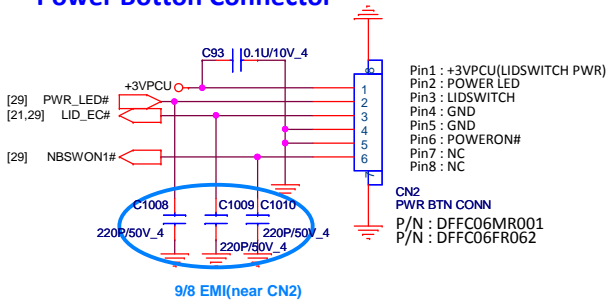


9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name "INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

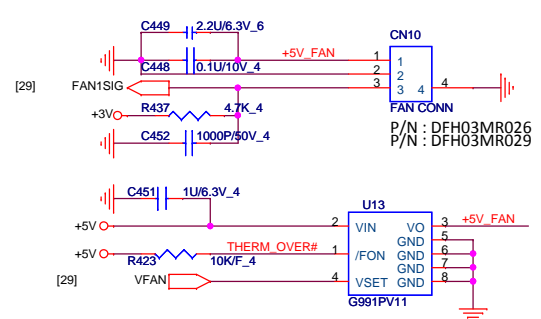
PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number Audio Codec (Realtek_ALC269)	Rev A
Date: Monday, November 15, 2010	Sheet 27 of 40	

Power Button Connector

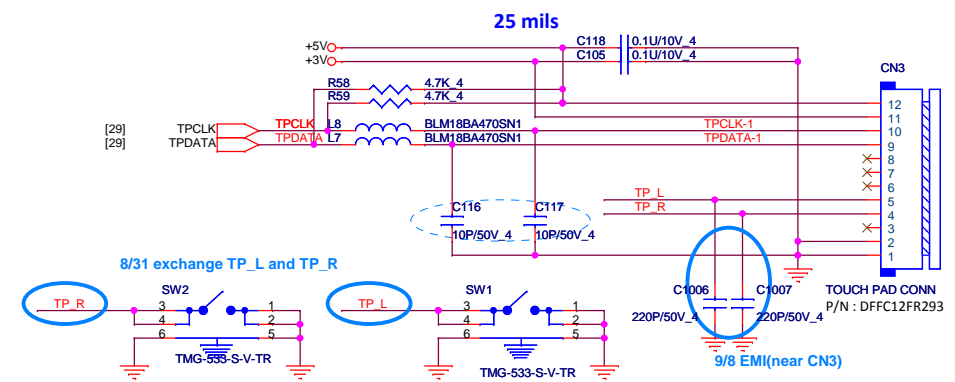


CPU FAN

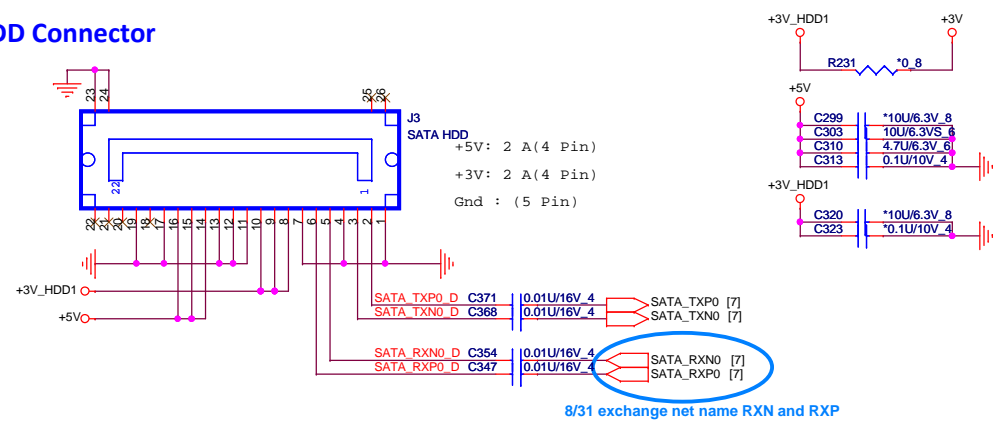


Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L



SATA HDD Connector

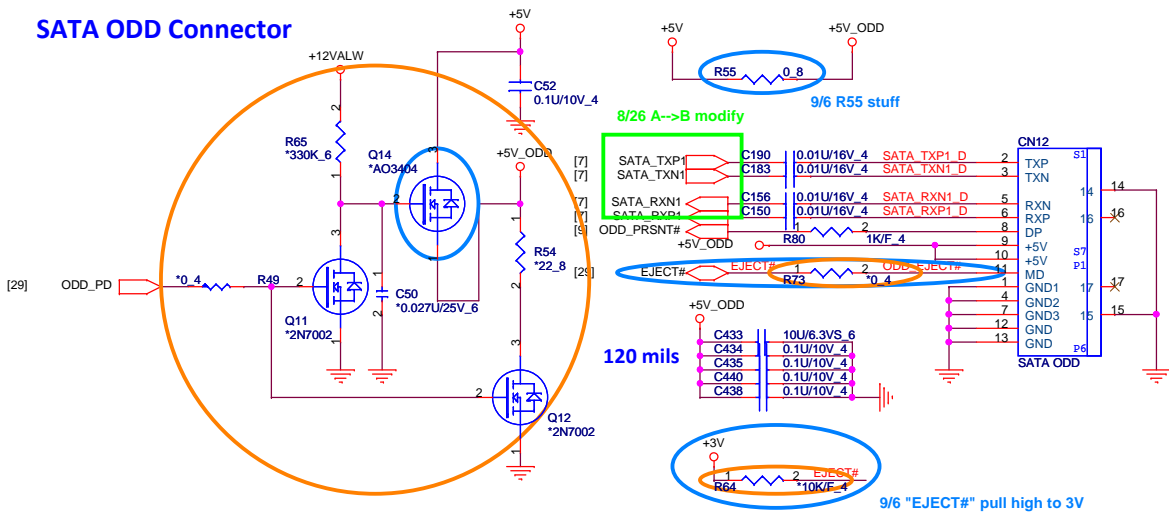


BT Connector

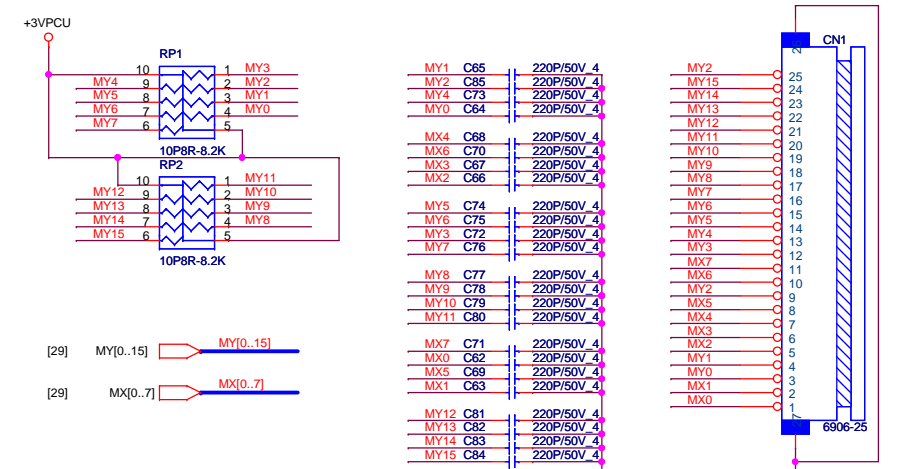


8/31 delete BT function (USB)
 delete CN20, net "BT_OFF#", "BLUELED", "USB8+", "USB8-"

SATA ODD Connector



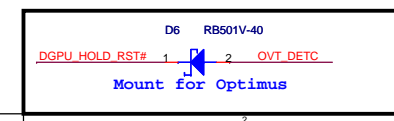
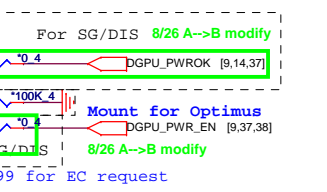
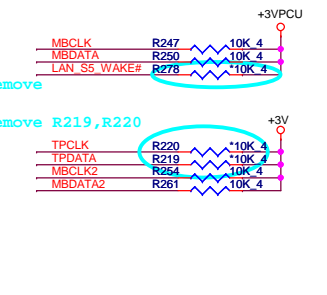
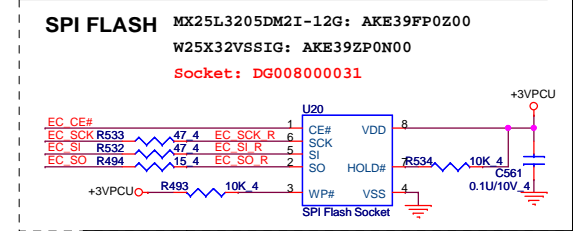
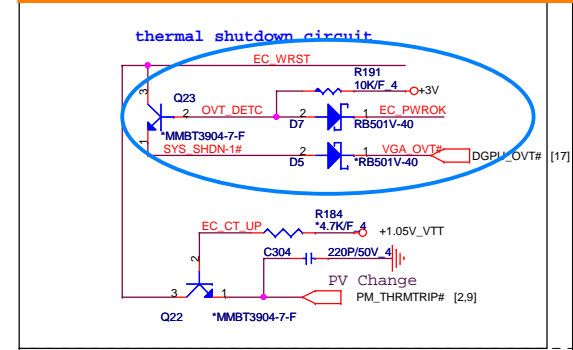
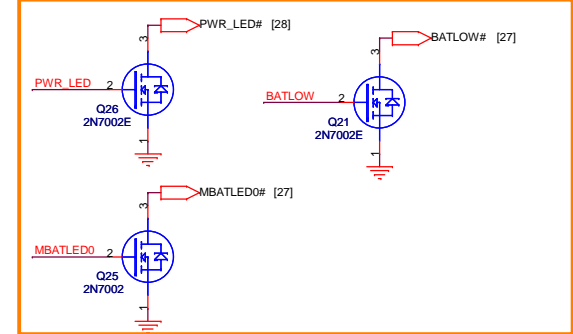
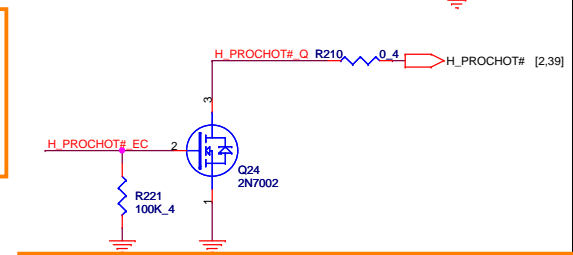
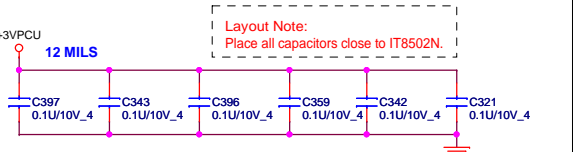
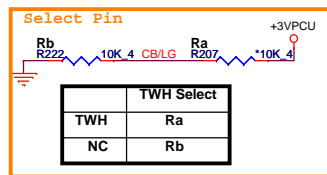
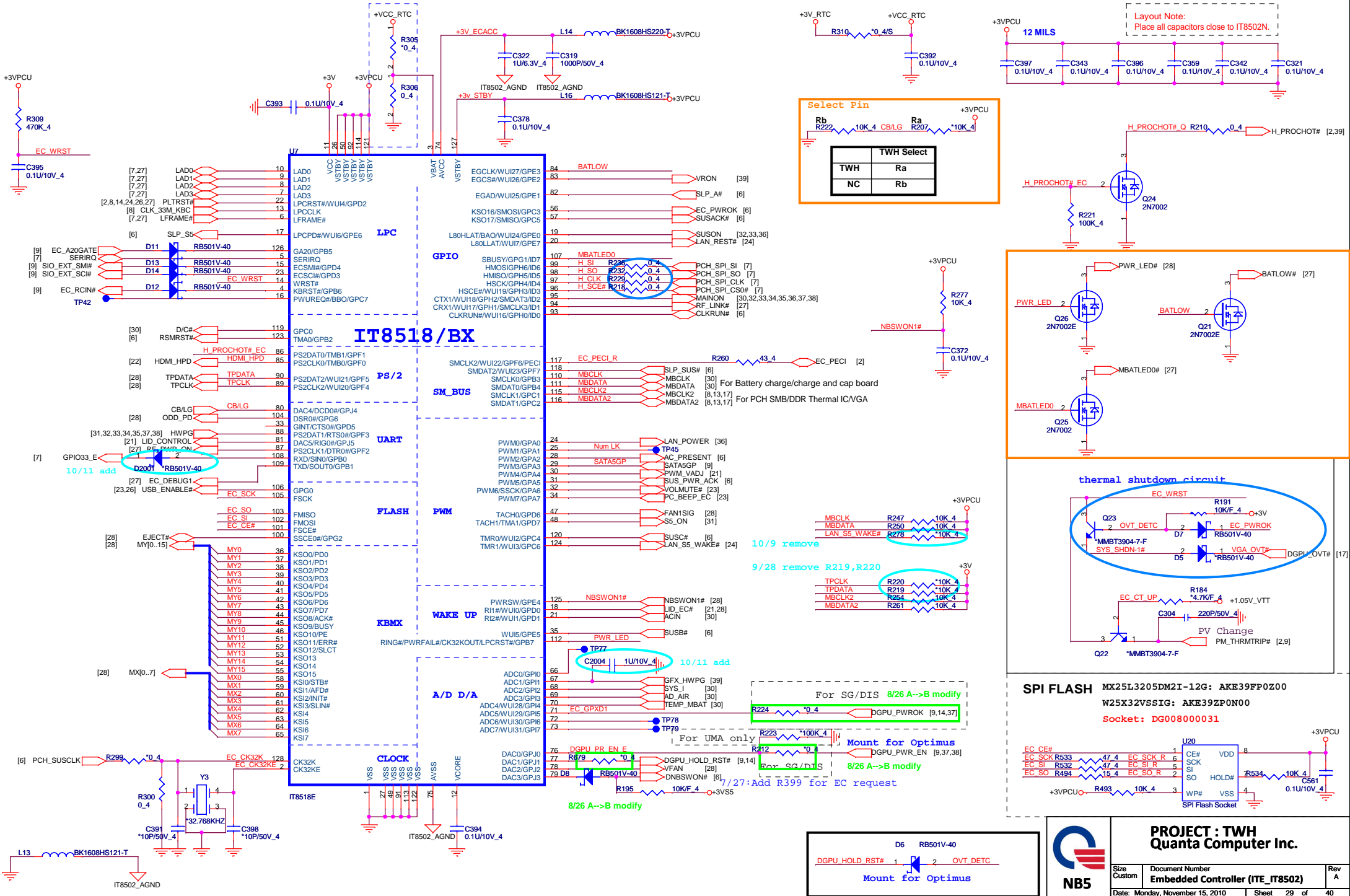
Keyboard Connector



PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number Audio Codec (Realtek_ALC269)	Rev A
Date: Monday, November 15, 2010		Sheet 28 of 40

[2,4,10,27] +1.5V_CPU
 [6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,29,34,36,37,39] +3V
 [6,7,10,21,22,23,27,36] +5V

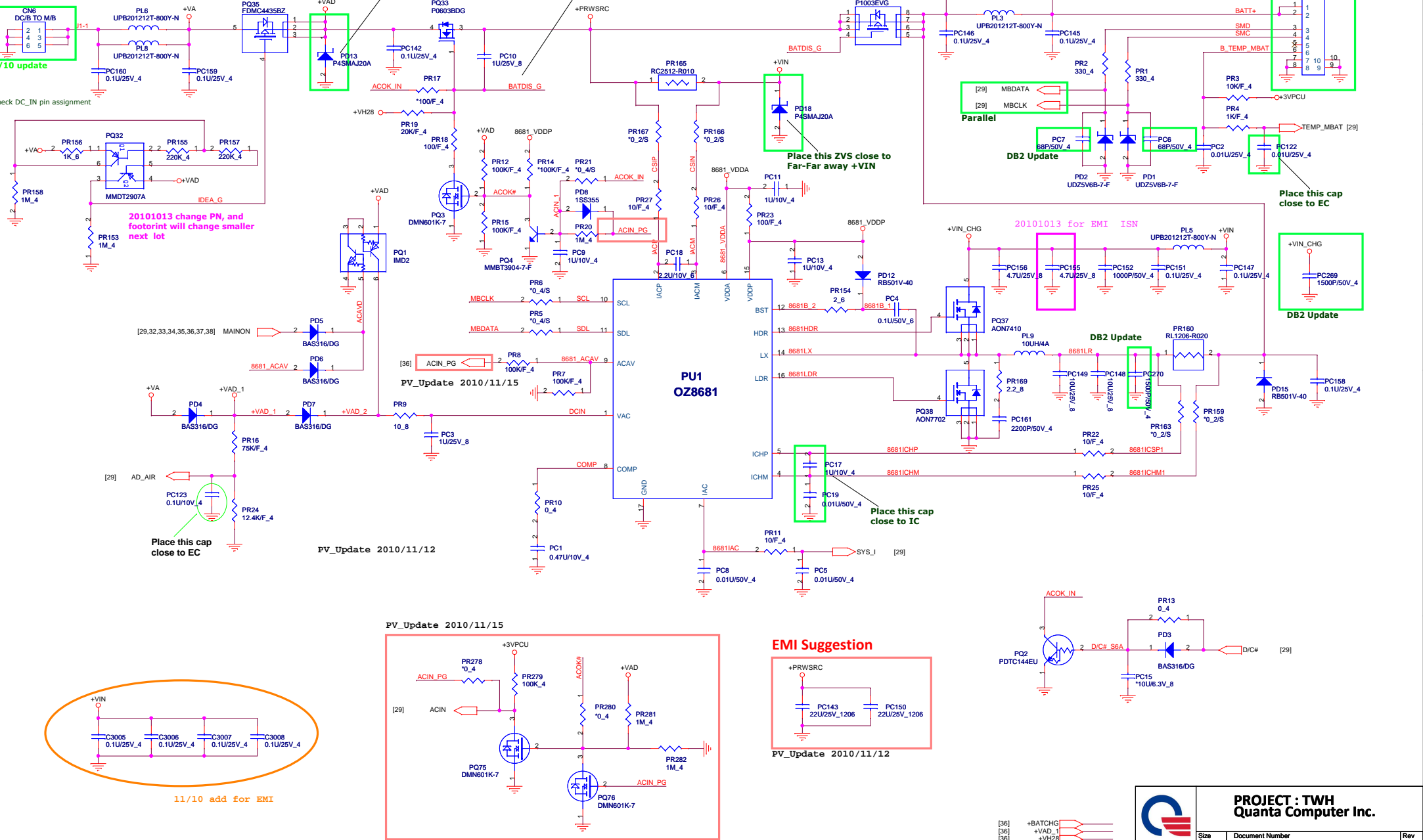


PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number **Embedded Controller (ITE_IT8502)** Rev A

Date: Monday, November 15, 2010 Sheet 29 of 40

**TOP DC_JACK
65W/90W**



CN6
DC/B TO MB
9/10 update

Check DC_IN pin assignment

20101013 change PN, and footprint will change smaller next lot

Place this ZVS close to idea diode

Do Not add test point on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to IC

Place this cap close to EC

PV_Update 2010/11/15

PV_Update 2010/11/15

EMI Suggestion

PV_Update 2010/11/12

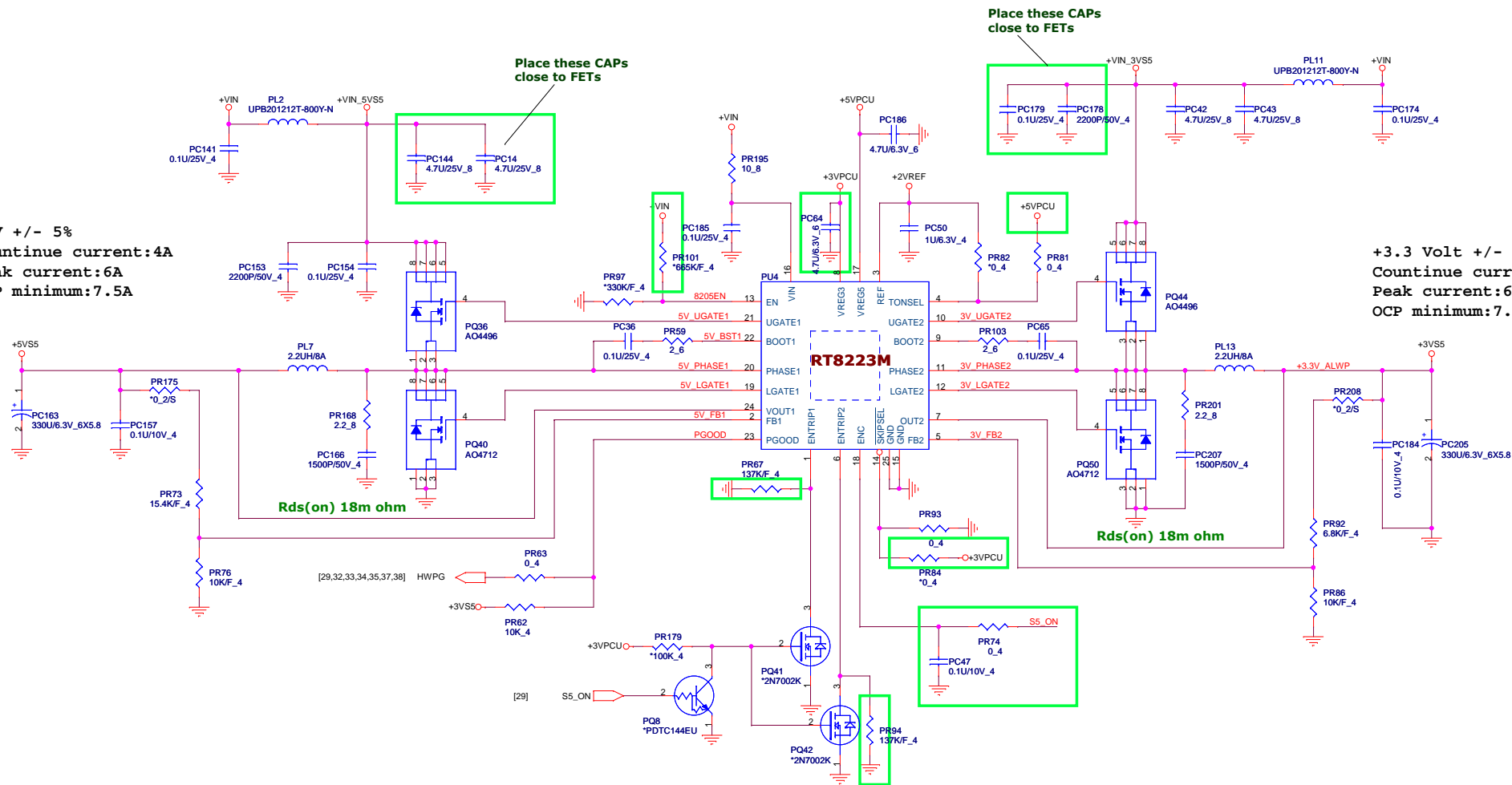
11/10 add for EMI

- [36] +BATCHG
- [36] +VAD_1
- [36] +VH28
- [36] +VA

	PROJECT : TWH Quanta Computer Inc.	
	Size Custom	Document Number <Doc>
Date: Monday, November 15, 2010		Sheet 30 of 40

+5V +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

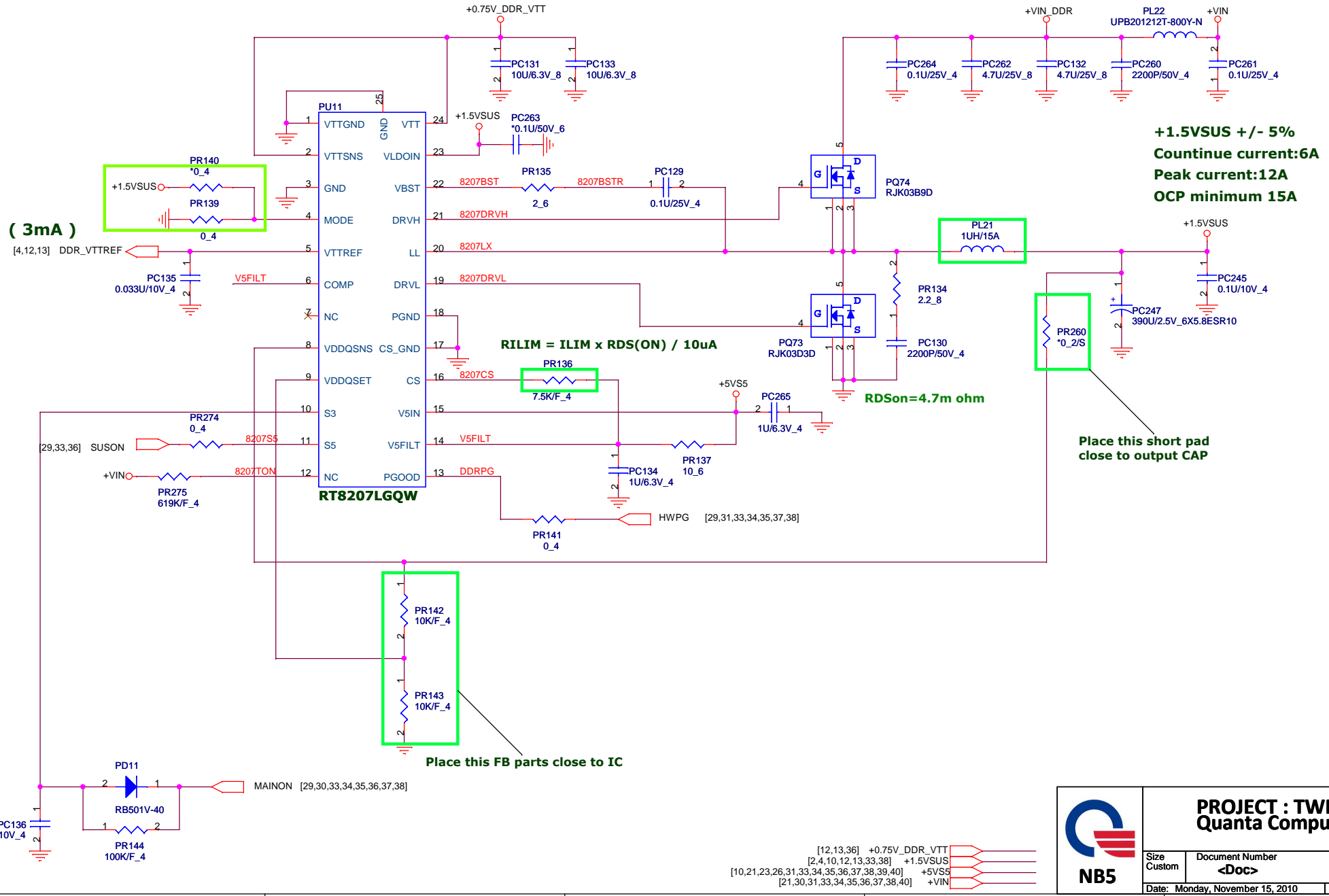
+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A



+5VPCU

<p>NBS</p>	<p>PROJECT : TWH Quanta Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number <Doc></p>	<p>Rev A</p>
	<p>Date: Monday, November 15, 2010</p>		<p>Sheet 31 of 40</p>

(VTT/2A)

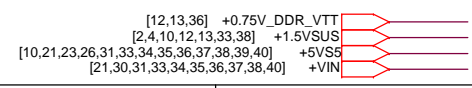


+1.5VSUS +/- 5%
Continue current:6A
Peak current:12A
OCp minimum 15A

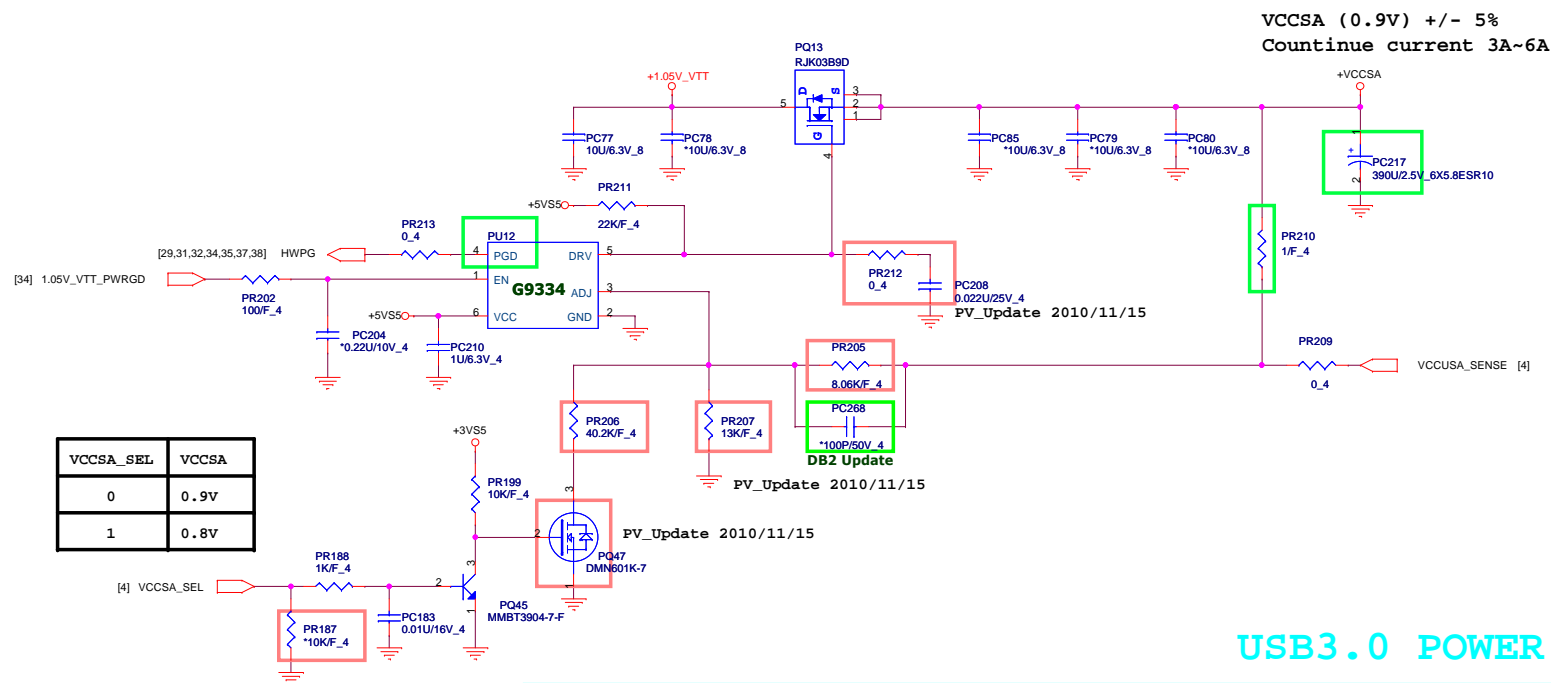
(3mA)

Place this short pad close to output CAP

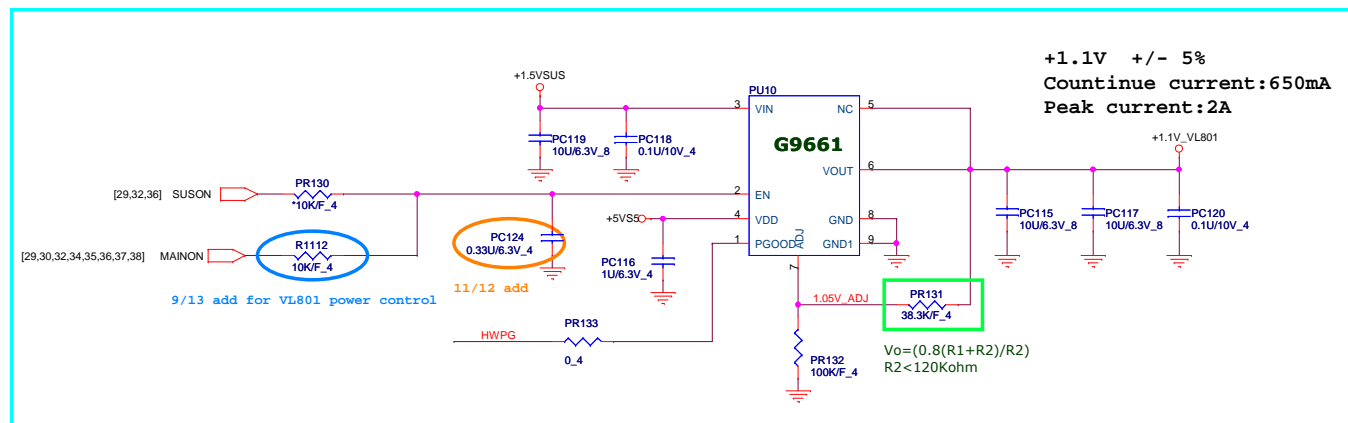
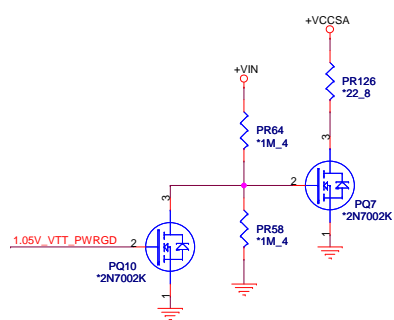
Place this FB parts close to IC

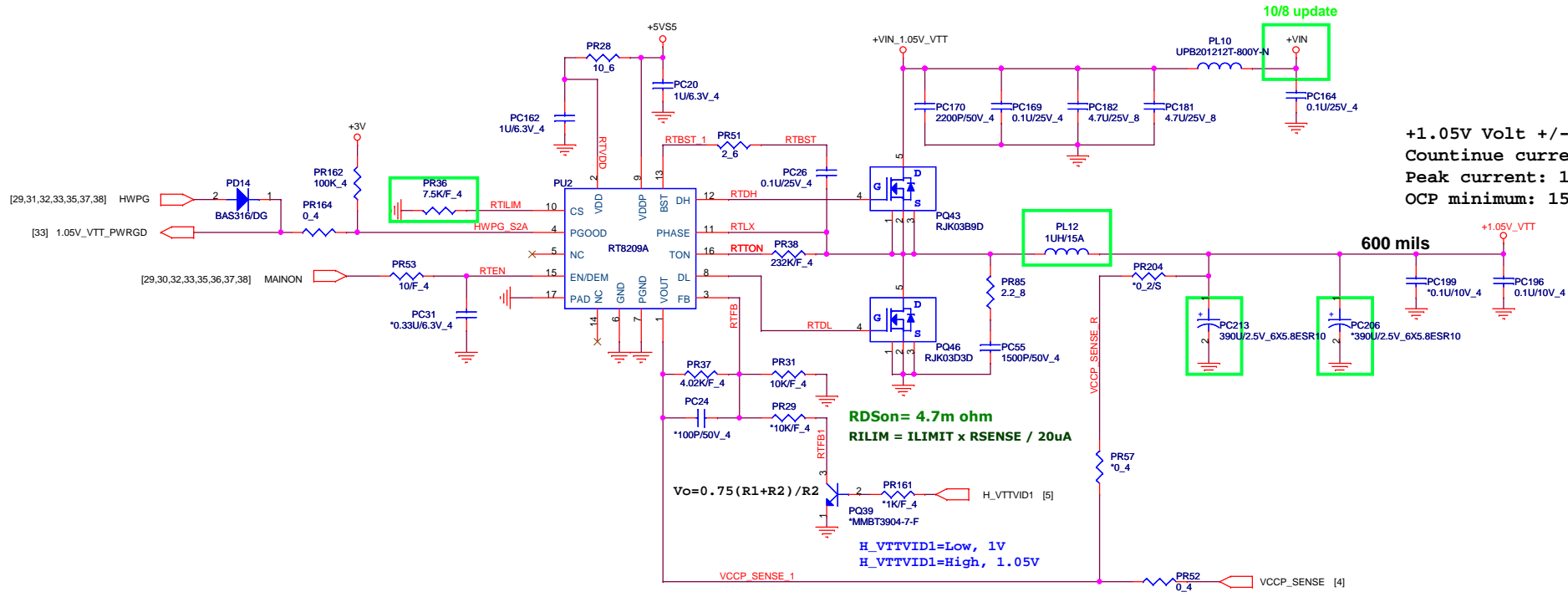


		PROJECT : TWH Quanta Computer Inc.	
Date: Monday, November 15, 2010		Sheet 32 of 40	Rev A



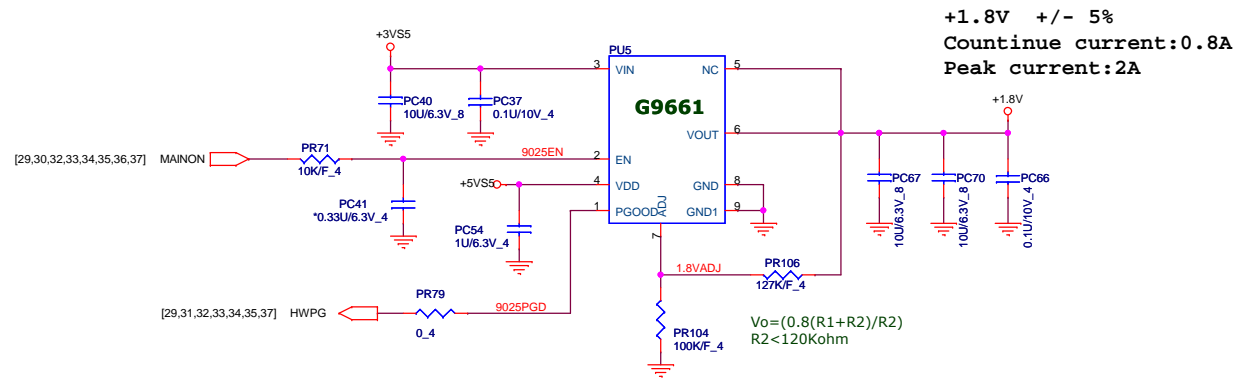
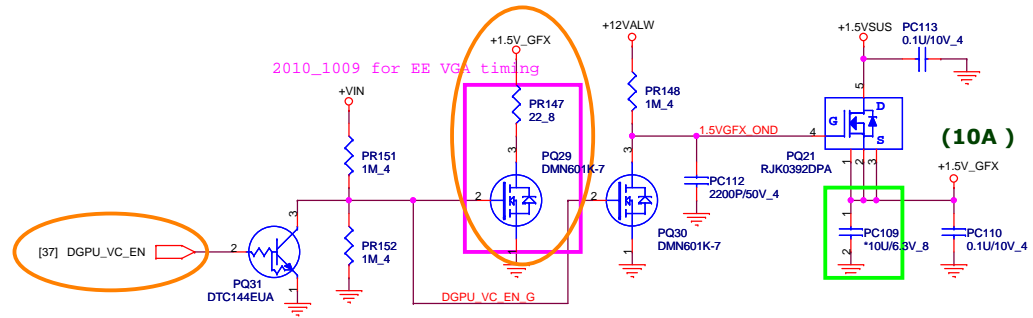
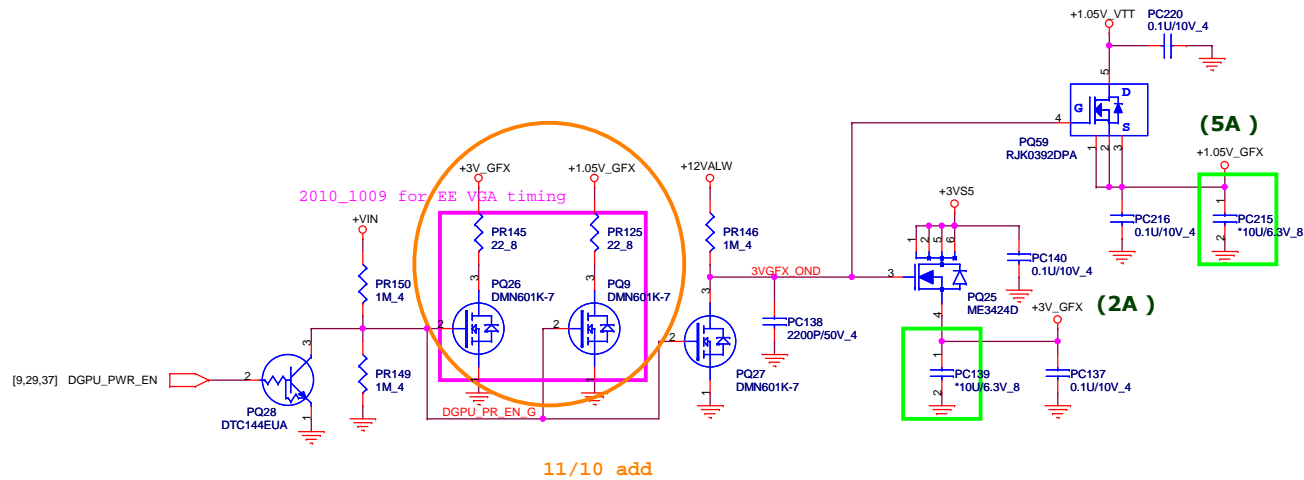
USB3.0 POWER



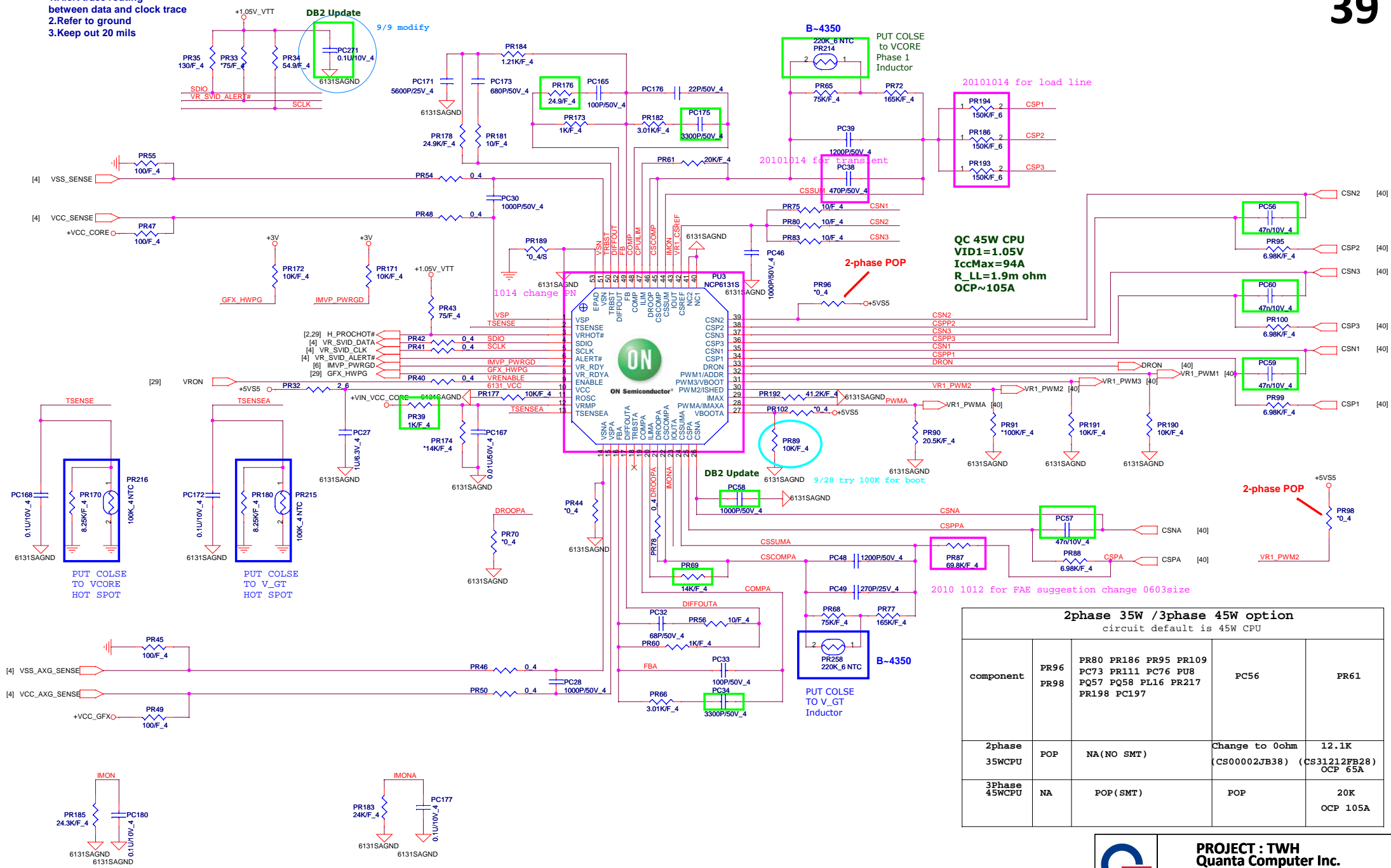


PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev A
Date: Monday, November 15, 2010	Sheet 34 of 40	



- Alert trace routing between data and clock trace
- Refer to ground
- Keep out 20 mils



2phase 35W /3phase 45W option
circuit default is 45W CPU

component	PR96 PR98	PR80 PR186 PR95 PR109 PC73 PR111 PC76 PU8 PQ57 PQ58 PL16 PR217 PR198 PC197	PC56	PR61
2phase 35W CPU	POP	NA (NO SMT)	Change to 0ohm (CS00002JB38)	12.1K (CS31212FB28) OCP 65A
3Phase 45W CPU	NA	POP (SMT)	POP	20K OCP 105A

PROJECT : TWH
Quanta Computer Inc.

NBS

Size: Custom
Document Number: <Doc>
Date: Monday, November 15, 2010
Sheet: 39 of 40
Rev: A

