Zynq MicroZed	
Avnet Engineering Services	
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Function	**Sheet Number**
Cover Sheet	1
Block Diagram	2
DDR3	3
QSPI FLASH, Micro SD	4
ETHERNET, USB	5
BANK 34, BANK 35	6
BANK 0, BANK 13, JTAG	7
MICROHEADERS JX1, JX2	8
FPGA POWER	9
POWER, RESET	10
Back Page	11

MicroZed Production

29 OCT 2013

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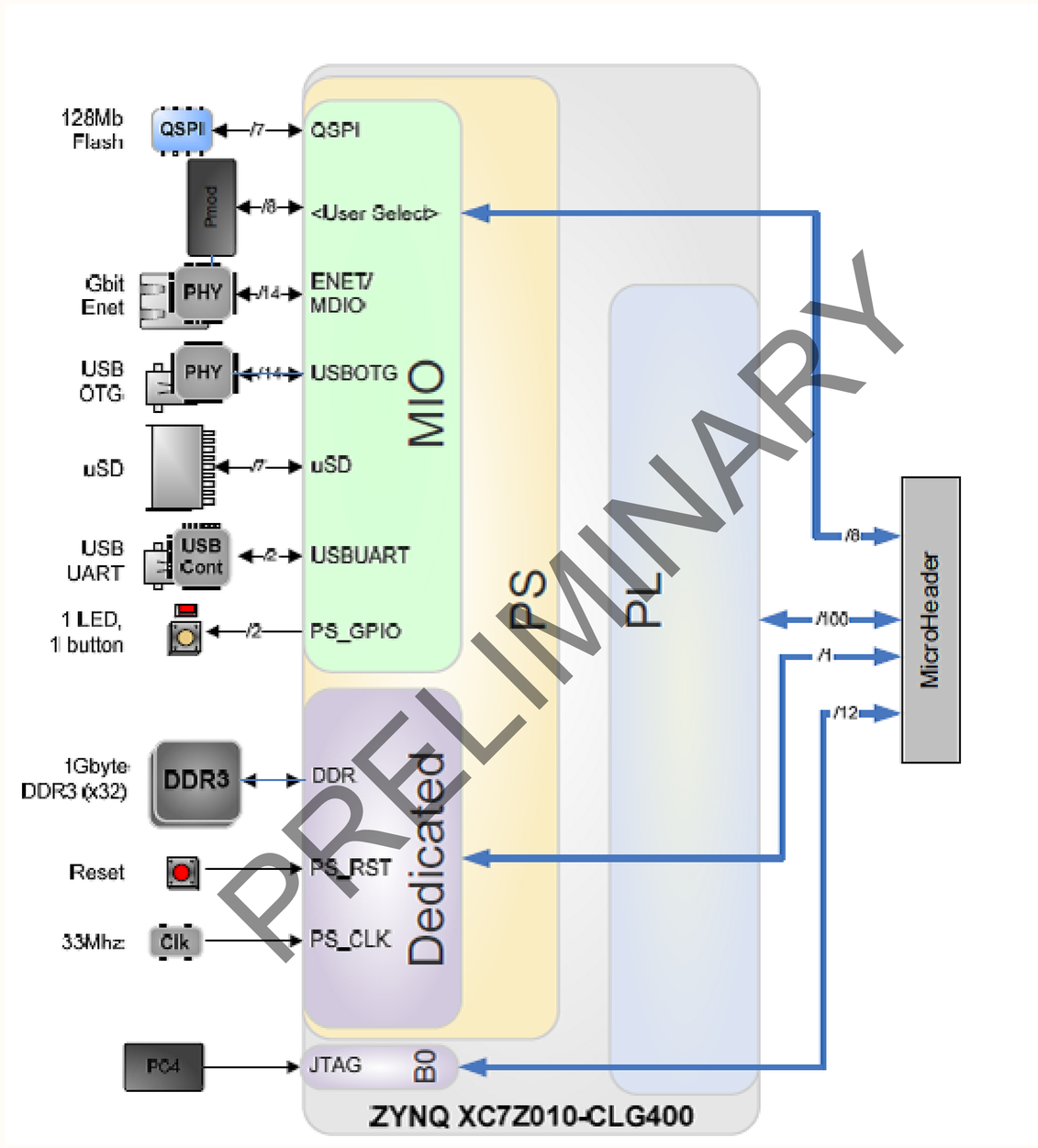
Title:	01 - Avnet Lead Sheet_B.SchDoc	
Size: B	Document Number: MicroZed 7010	Rev: F
Date: 10/29/2013	Sheet 1 of 11	



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Title:	02 - Block Diagram.SchDoc	
Size: B	Document Number: MicroZed 7010	Rev: F
Date: 10/29/2013	Sheet 2 of 11	

U9G
Zynq 7010/7020 SOC CLG400

BANK 502

PS_DDR_DQ0_502 C3 DDR3_DQ0
PS_DDR_DQ1_502 B3 DDR3_DQ1
PS_DDR_DQ2_502 A2 DDR3_DQ2
PS_DDR_DQ3_502 A4 DDR3_DQ3
PS_DDR_DQ4_502 D3 DDR3_DQ4
PS_DDR_DQ5_502 D1 DDR3_DQ5
PS_DDR_DQ6_502 C1 DDR3_DQ6
PS_DDR_DQ7_502 E1 DDR3_DQ7
PS_DDR_DQ8_502 E2 DDR3_DQ8
PS_DDR_DQ9_502 E3 DDR3_DQ9
PS_DDR_DQ10_502 G3 DDR3_DQ10
PS_DDR_DQ11_502 H3 DDR3_DQ11
PS_DDR_DQ12_502 J3 DDR3_DQ12
PS_DDR_DQ13_502 H2 DDR3_DQ13
PS_DDR_DQ14_502 H1 DDR3_DQ14
PS_DDR_DQ15_502 J1 DDR3_DQ15
PS_DDR_DQ16_502 P1 DDR3_DQ16
PS_DDR_DQ17_502 P3 DDR3_DQ17
PS_DDR_DQ18_502 R3 DDR3_DQ18
PS_DDR_DQ19_502 R1 DDR3_DQ19
PS_DDR_DQ20_502 T4 DDR3_DQ20
PS_DDR_DQ21_502 U4 DDR3_DQ21
PS_DDR_DQ22_502 U2 DDR3_DQ22
PS_DDR_DQ23_502 U3 DDR3_DQ23
PS_DDR_DQ24_502 Y1 DDR3_DQ24
PS_DDR_DQ25_502 Y3 DDR3_DQ25
PS_DDR_DQ26_502 W1 DDR3_DQ26
PS_DDR_DQ27_502 Y4 DDR3_DQ27
PS_DDR_DQ28_502 Y2 DDR3_DQ28
PS_DDR_DQ29_502 W3 DDR3_DQ29
PS_DDR_DQ30_502 Y2 DDR3_DQ30
PS_DDR_DQ31_502 Y3 DDR3_DQ31

DDR_D

PS_DDR_A0_502 N2 DDR3_A0
PS_DDR_A1_502 K2 DDR3_A1
PS_DDR_A2_502 M3 DDR3_A2
PS_DDR_A3_502 K3 DDR3_A3
PS_DDR_A4_502 M4 DDR3_A4
PS_DDR_A5_502 L1 DDR3_A5
PS_DDR_A6_502 L4 DDR3_A6
PS_DDR_A7_502 K4 DDR3_A7
PS_DDR_A8_502 K1 DDR3_A8
PS_DDR_A9_502 J4 DDR3_A9
PS_DDR_A10_502 F5 DDR3_A10
PS_DDR_A11_502 G4 DDR3_A11
PS_DDR_A12_502 E4 DDR3_A12
PS_DDR_A13_502 D4 DDR3_A13
PS_DDR_A14_502 F4 DDR3_A14

DDR_AC

PS_DDR_DQS_P0_502 C2 DDR3_DQS0_P
PS_DDR_DQS_N0_502 B2 DDR3_DQS0_N
PS_DDR_DQS_P1_502 G2 DDR3_DQS1_P
PS_DDR_DQS_N1_502 F2 DDR3_DQS1_N
PS_DDR_DQS_P2_502 R2 DDR3_DQS2_P
PS_DDR_DQS_N2_502 T2 DDR3_DQS2_N
PS_DDR_DQS_P3_502 W5 DDR3_DQS3_P
PS_DDR_DQS_N3_502 W4 DDR3_DQS3_N
PS_DDR_CKP_502 L2 DDR3_CK0_P
PS_DDR_CKN_502 M2 DDR3_CK0_N
PS_DDR_BA0_502 L5 DDR3_BA0
PS_DDR_BA1_502 R4 DDR3_BA1
PS_DDR_BA2_502 J5 DDR3_BA2
PS_DDR_DM0_502 A1 DDR3_DM0
PS_DDR_DM1_502 F1 DDR3_DM1
PS_DDR_DM2_502 T1 DDR3_DM2
PS_DDR_DM3_502 Y1 DDR3_DM3

DDR_DM

PS_DDR_CS_B_502 N1 DDR3_CS#
PS_DDR_WE_B_502 M5 DDR3_WE#
PS_DDR_CAS_B_502 P5 DDR3_CAS#
PS_DDR_RAS_B_502 P4 DDR3_RAS#
PS_DDR_CKE_502 N3 DDR3_CKE
PS_DDR_ODT_502 N5 DDR3_ODT
PS_DDR_DRST_B_502 B4 DDR3_RESET#
PS_DDR_VRP_502 H5 R74 80.6 GND
PS_DDR_VRN_502 G5 R75 80.6 1.5V

DDR_D_BL0 DDR3_DQ[7..0]
DDR_D_BL1 DDR3_DQ[15..8]
DDR_D_BL2 DDR3_DQ[23..16]
DDR_D_BL3 DDR3_DQ[31..24]

1.5V
DDR_PWR
C41 47uF, C170 0.1uF, C176 0.1uF, C181 0.1uF, C188 0.1uF
C193 0.01uF, C196 0.01uF, C200 0.01uF, C203 0.01uF
C43 47uF, C199 0.1uF, C194 0.1uF, C186 0.1uF, C184 0.1uF
C180 0.01uF, C178 0.01uF, C172 0.01uF, C174 0.01uF
GND
VTTREF
C187 0.01uF

U11
MT41K256M16HA-125:E

DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P7 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC#
DDR3_A13 T3 A13
DDR3_A14 T7 A14
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_CS# L2 CS#
DDR3_WE# L3 WE#
DDR3_CAS# K3 CAS#
DDR3_RAS# J3 RAS#
DDR3_CKE K9 CKE
DDR3_CK0_P J7 CK
DDR3_CK0_N K7 CK#
DDR3_RESET# T2 RESET#
L9 n/c
L1 n/c
J9 n/c
J1 n/c

DQ0 E3 DDR3_DQ0
DQ1 F7 DDR3_DQ1
DQ2 F2 DDR3_DQ2
DQ3 F8 DDR3_DQ3
DQ4 H3 DDR3_DQ4
DQ5 H8 DDR3_DQ5
DQ6 G2 DDR3_DQ6
DQ7 H7 DDR3_DQ7
DQ8 C3 DDR3_DQ8
DQ9 C8 DDR3_DQ9
DQ10 C2 DDR3_DQ10
DQ11 A7 DDR3_DQ11
DQ12 A2 DDR3_DQ12
DQ13 B8 DDR3_DQ13
DQ14 A3 DDR3_DQ14
DQ15 DDR3_DQ15
UDM D3 DDR3_DM1
LDM E7 DDR3_DM0
UDQS C7 DDR3_DQS1_P
UDQS# B7 DDR3_DQS1_N
LDQS F3 DDR3_DQS0_P
LDQS# G3 DDR3_DQS0_N
ODT K1 DDR3_ODT
ZQ L8 R79 240
M7 n/c

U12
MT41K256M16HA-125:E

DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P7 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC#
DDR3_A13 T3 A13
DDR3_A14 T7 A14
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_CS# L2 CS#
DDR3_WE# L3 WE#
DDR3_CAS# K3 CAS#
DDR3_RAS# J3 RAS#
DDR3_CKE K9 CKE
DDR3_CK0_P J7 CK
DDR3_CK0_N K7 CK#
DDR3_RESET# T2 RESET#
L9 n/c
L1 n/c
J9 n/c
J1 n/c

DQ0 E3 DDR3_DQ16
DQ1 F7 DDR3_DQ17
DQ2 F2 DDR3_DQ18
DQ3 F8 DDR3_DQ19
DQ4 H3 DDR3_DQ20
DQ5 H8 DDR3_DQ21
DQ6 G2 DDR3_DQ22
DQ7 H7 DDR3_DQ23
DQ8 C3 DDR3_DQ24
DQ9 C8 DDR3_DQ25
DQ10 C2 DDR3_DQ26
DQ11 A7 DDR3_DQ27
DQ12 A2 DDR3_DQ28
DQ13 B8 DDR3_DQ29
DQ14 A3 DDR3_DQ30
DQ15 DDR3_DQ31
UDM D3 DDR3_DM3
LDM E7 DDR3_DM2
UDQS C7 DDR3_DQS3_P
UDQS# B7 DDR3_DQS3_N
LDQS F3 DDR3_DQS2_P
LDQS# G3 DDR3_DQS2_N
ODT K1 DDR3_ODT
ZQ L8 R85 240
M7 n/c

Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 trace lengths must include Zynq package flight times. See UG933 and Layout Guidelines.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

DDR_T
DDR3_0V75

DDR3_A14 DDR3_T_A14 R29 40.2 R27 40.2
DDR3_A13 DDR3_T_A13
DDR3_A12 DDR3_T_A12 R80 40.2 R84 40.2
DDR3_A11 DDR3_T_A11
DDR3_A10 DDR3_T_A10 R78 40.2
DDR3_A9 DDR3_T_A9 R24 40.2
DDR3_A8 DDR3_T_A8 R31 40.2
DDR3_A7 DDR3_T_A7 R30 40.2 R86 40.2
DDR3_A6 DDR3_T_A6
DDR3_A5 DDR3_T_A5 R28 40.2 R83 40.2
DDR3_A4 DDR3_T_A4
DDR3_A3 DDR3_T_A3 R26 40.2 R23 40.2
DDR3_A2 DDR3_T_A2
DDR3_A1 DDR3_T_A1 R82 40.2 R21 40.2
DDR3_A0 DDR3_T_A0
DDR3_BA0 DDR3_T_BA0 R25 40.2 R81 40.2
DDR3_BA1 DDR3_T_BA1
DDR3_BA2 DDR3_T_BA2 R22 40.2 R18 40.2
DDR3_CS# DDR3_T_CS#
DDR3_WE# DDR3_T_WE# R20 40.2 R19 40.2
DDR3_CAS# DDR3_T_CAS#
DDR3_RAS# DDR3_T_RAS# R17 40.2 R16 40.2
DDR3_ODT DDR3_T_ODT
DDR3_RESET# DDR3_T_RESET#
DDR3_CK0_P DDR3_T_CK0_P R77 80.6
DDR3_CK0_N DDR3_T_CK0_N
DDR3_CKE DDR3_T_CKE R15 40.2

JT6
A 40.2 Com B
Jumper

Default: Pins 1 - 2, 40.2 ohm resistor.

NOTE:
RESET# requires 40.2 resistor for PD, to maintain logic high through FPGA Configuration. See UG933p62

DDR3 Termination Supply

3.3V C205 0.1uF GND
DDR3_0V75
U13
VDD 10, VDDQSNS 1, VLDOIN 2, PAD 9, S3 7, S5 9, PGND 4, VTT 3, VTTSNS 5, VTTREF 6, GND 8
TPS51206
3.3V R33 10K, 3.3V R32 10K
1.8V 1.5V C55 10uF
C48 10uF
C49 0.22uF
VTTREF
DDR_PWR
DDR3_0V75 C47 100uF, C46 100uF, C39 4.7uF, C45 4.7uF, C185 0.1uF, C204 0.1uF, C37 0.01uF, C38 0.01uF

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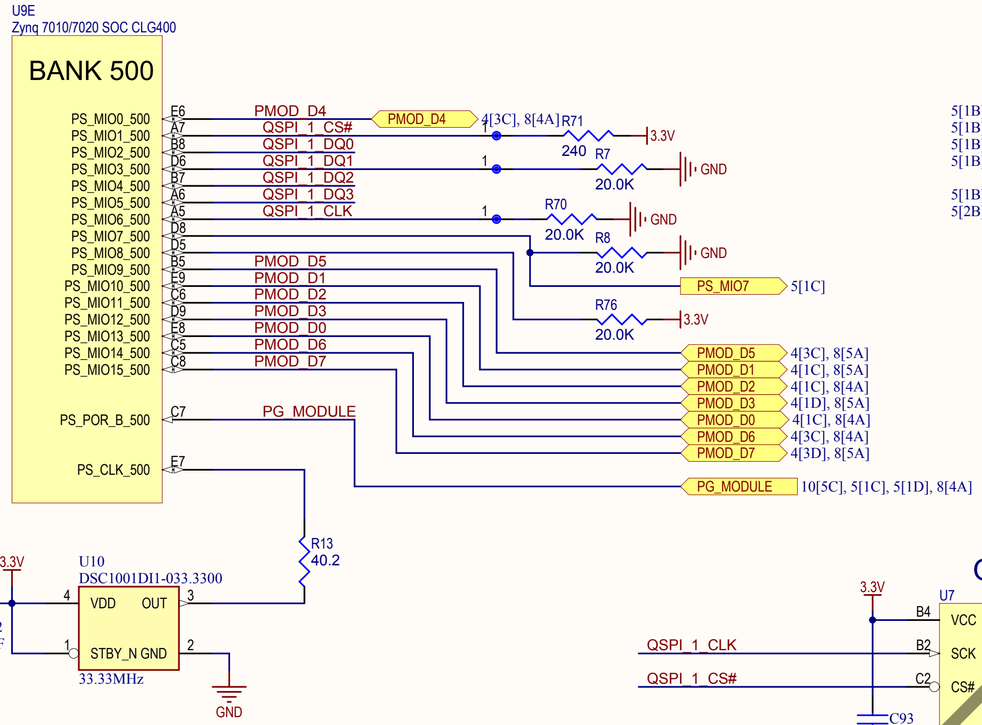
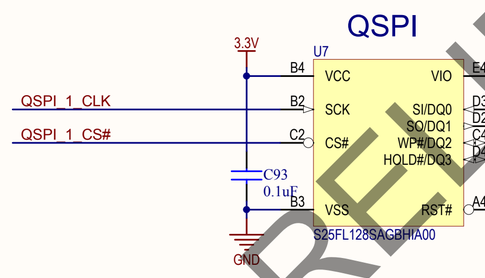
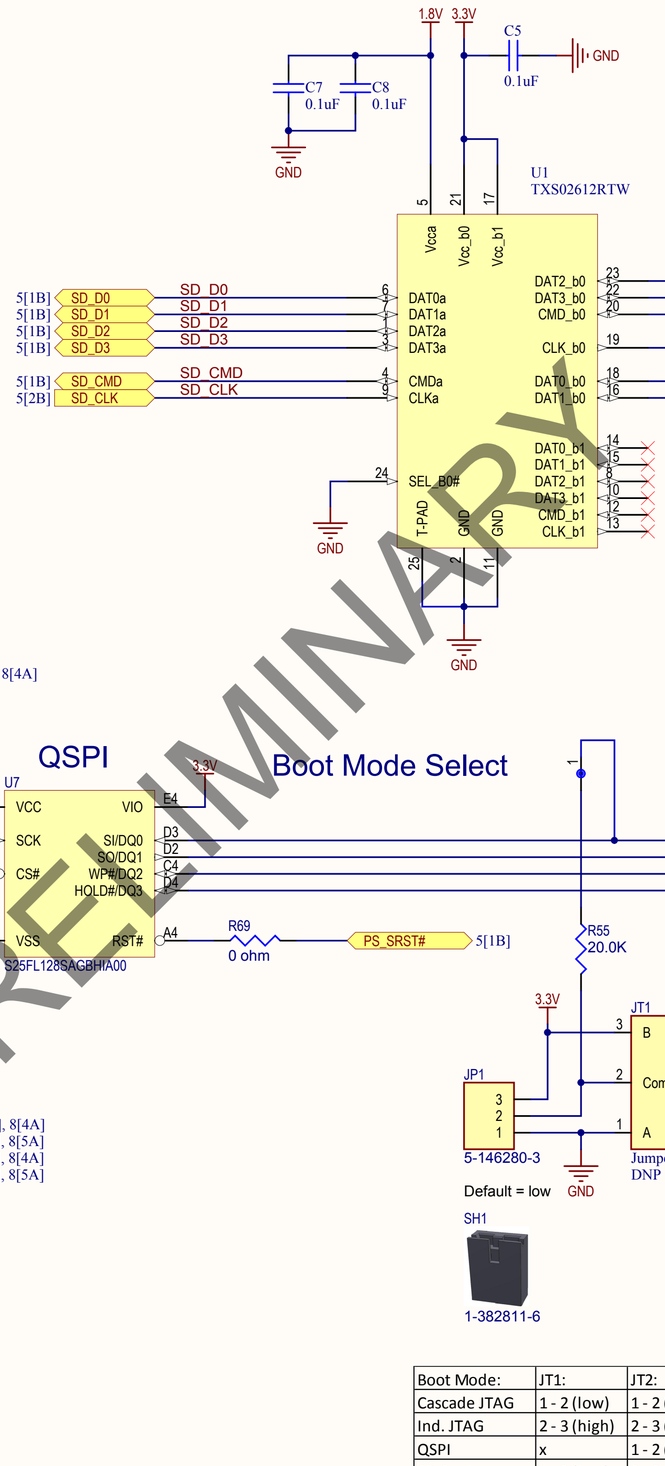
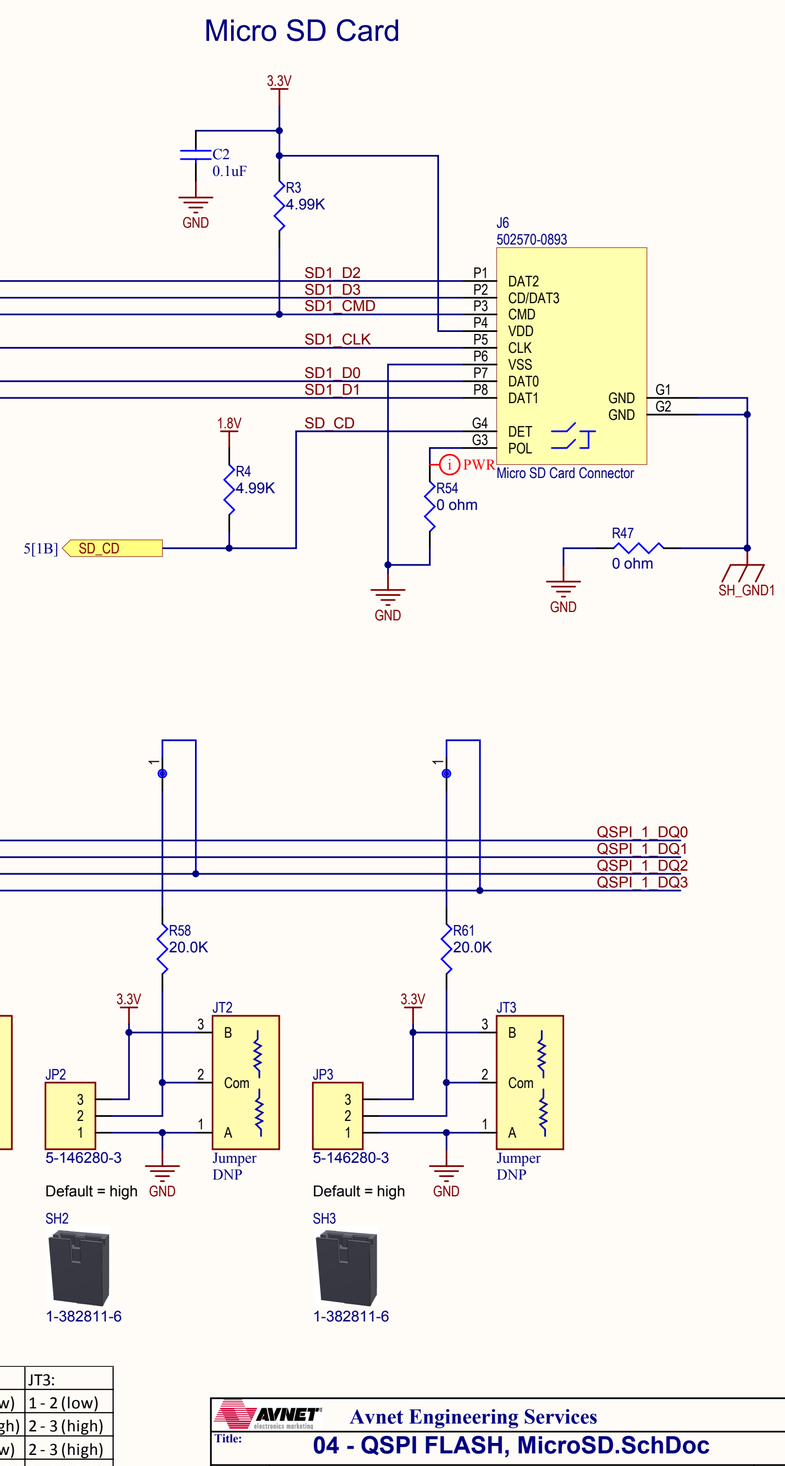
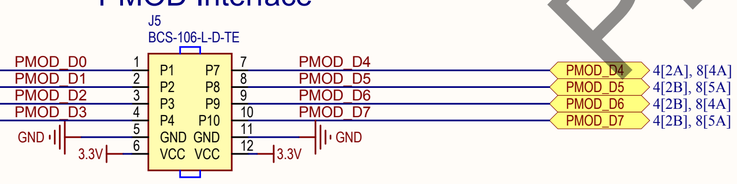
Rev: F	
Date: 10/29/2013	Sheet 3 of 11











Boot Mode:	JT1:	JT2:	JT3:
Cascade JTAG	1 - 2 (low)	1 - 2 (low)	1 - 2 (low)
Ind. JTAG	2 - 3 (high)	2 - 3 (high)	2 - 3 (high)
QSPI	x	1 - 2 (low)	2 - 3 (high)
SD Card	1 - 2 (low)	2 - 3 (high)	2 - 3 (high)

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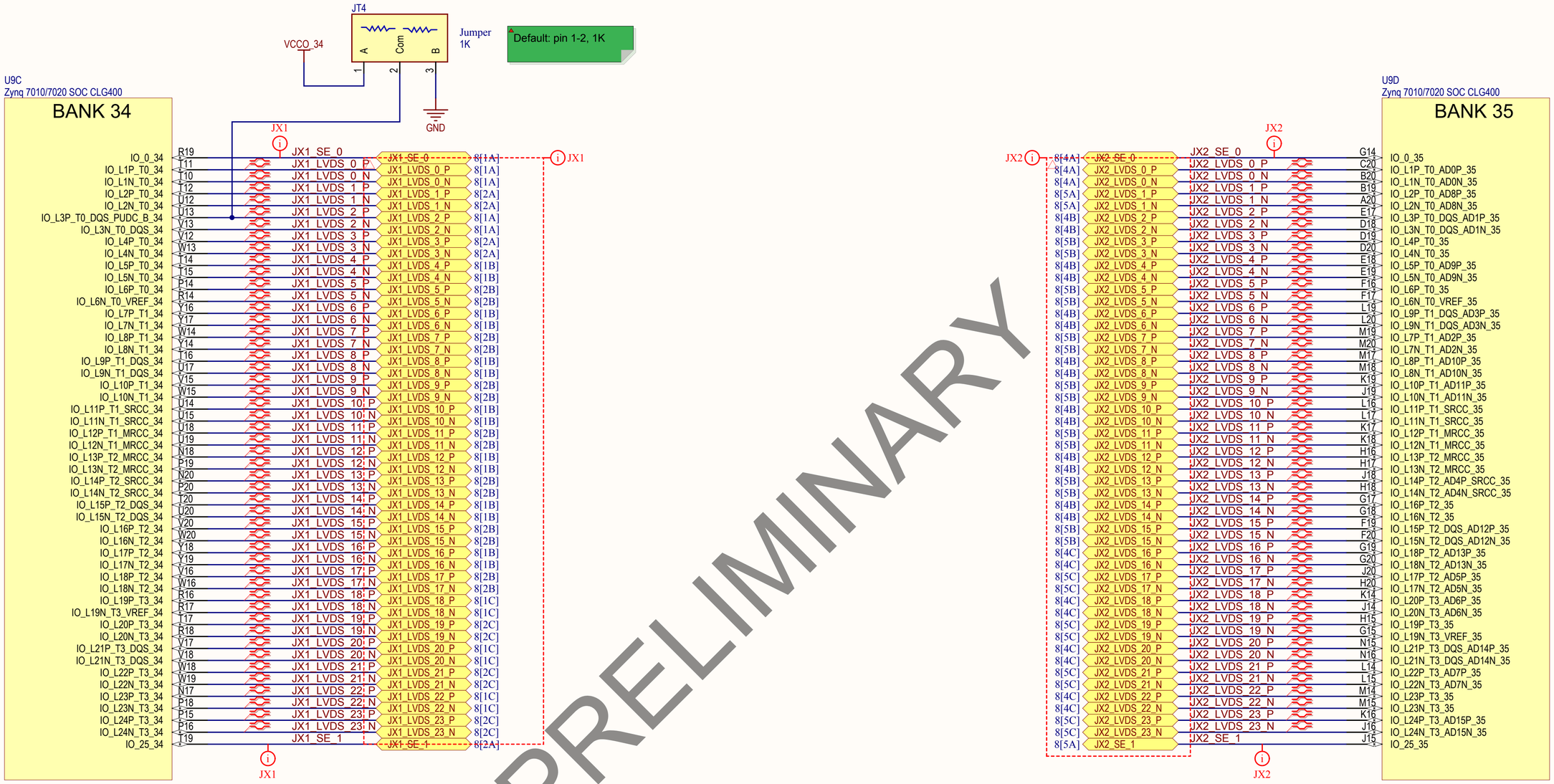
Title: 04 - QSPI FLASH, MicroSD.SchDoc

Size: B | Document Number: MicroZed 7010 | Rev: F

Date: 10/29/2013 | Sheet 4 of 11

Ethernet PHY
USB 2.0 OTG
USB UART
BANK 501
PRELIMINARY
U9F Zynq 7010/7020 SOC CLG400
U3 88E1512-XX-NNP2I000
U4 USB3320-EZK
U2 CP2104-F03-GM
U18 TLV62150RGT DNP
J1 0821-1X1T-43-F
RJ-45
USB-A
J2 10104111-0001LF
USB Micro AB
Layout Note: USB differential signal impedance target is 90 ohms.
Layout Note: USB_VBUS_OTG net must be 500mA or more capable.
Component Notes: In USB Device Mode: 1) C1 & C3 not required 2) R50 Removed In USB Host Mode: 1) C1 & C3 required 2) R50 0603 0 Ohm or PTC placed
R51: Host/OTG Mode = 1K Device Mode = 10K Default = Host Mode.
Design Note: R50 is a 0603 footprint. Generic PTCs can be placed, not to exceed 500mA withholding, can be a selectable PTC value, pending customer requirements.
NOTE: The components in the purple outlined areas MUST be placed if greater than +5.0 Vin is applied to the power jack! By Default these components are NOT placed and the board is powered via the USB UART port with +5.0V.
Operational Notes: USB Bus powered mode: 1) JT7 0 ohm pads 1-2. 2) DNP: D10, D11, R97, R98. USB Self powered mode: 1) JT7 0 ohm on pads 2-3. 2) R97, R98 populated. 3) DNP: D10, D11. USB Self powered, no backfeed: 1) JT7 0 ohm on pads 2-3. 2) D10, D11 populated. 3) DNP: R97, R98.
Layout Note: USB_VBUS_UART net must be 1A or more capable.
Default: 0 ohm pins 1-2
Avnet Engineering Services
Title: 05 - ETHERNET, USB.SchDoc
Size: C
Document Number: MicroZed 7010
Rev: F
Date: 10/29/2013
Sheet 5 of 11



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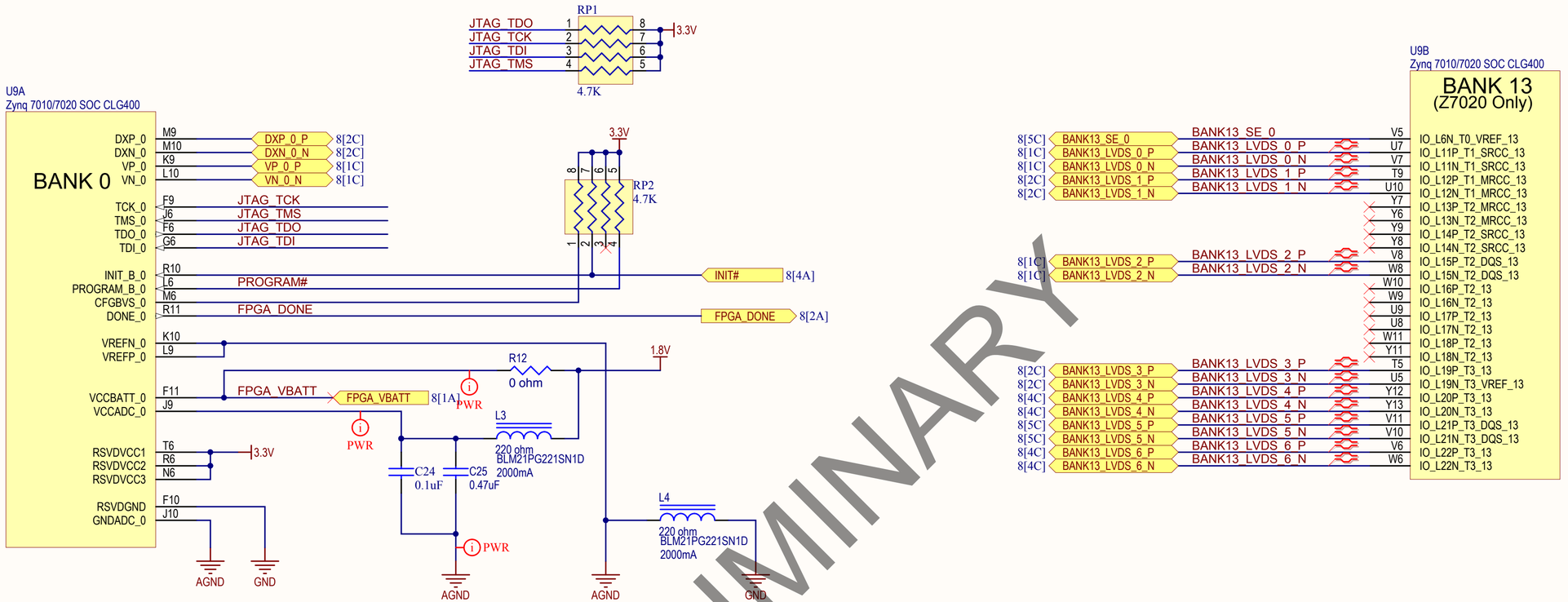
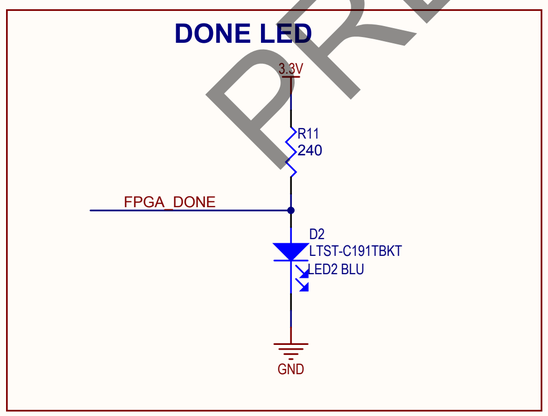
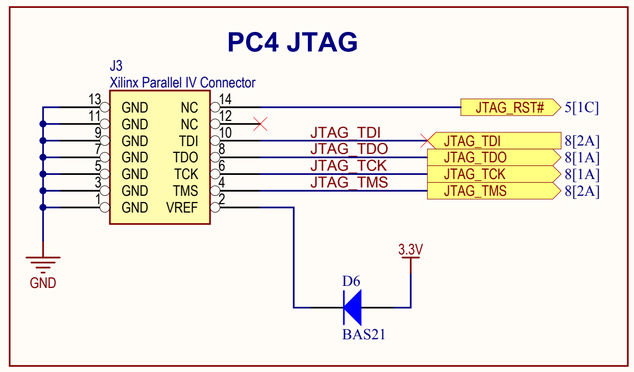
Rev:	F
Date: 10/29/2013	Sheet 6 of 11







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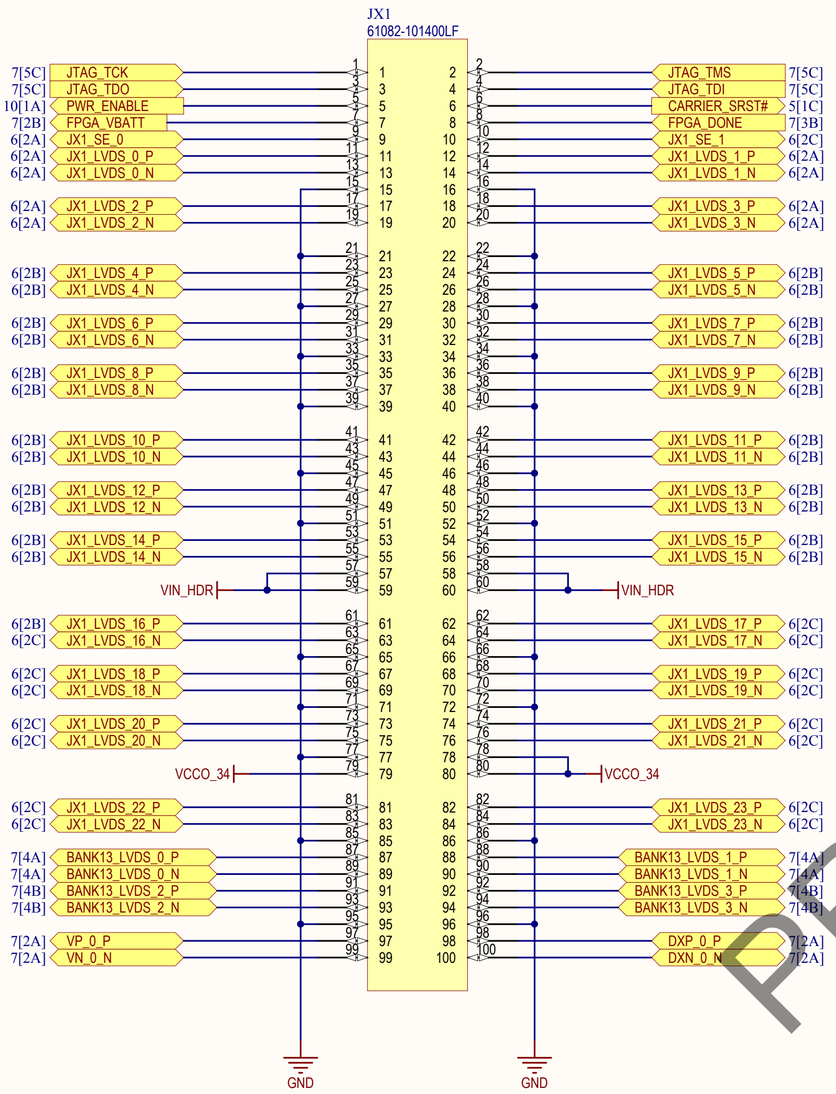
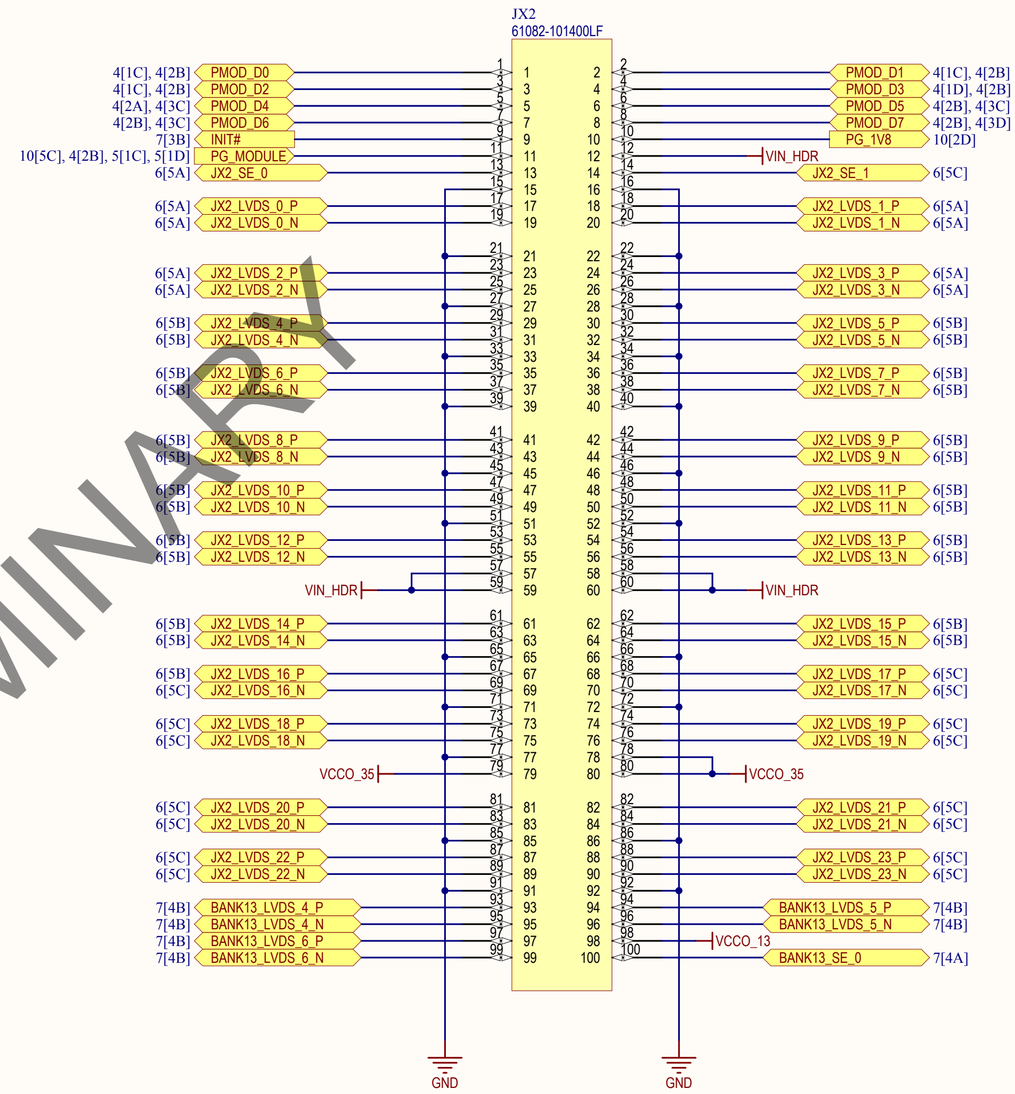
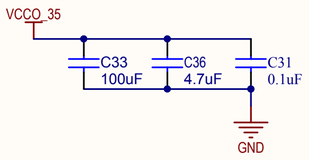
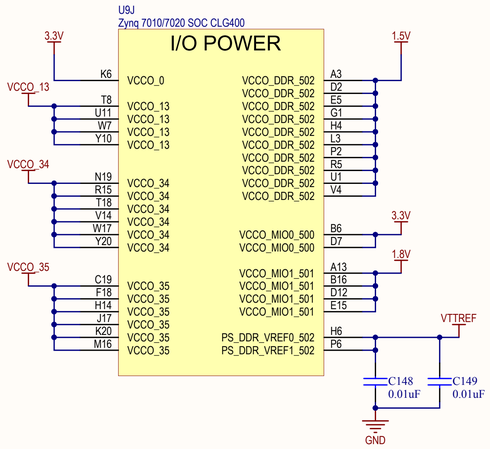
Rev:	F
Date: 10/29/2013	Sheet 7 of 11

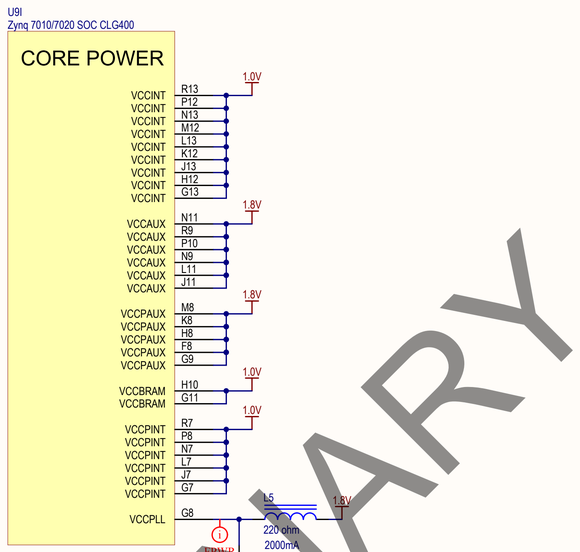


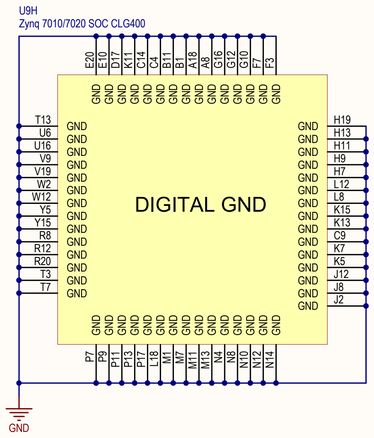


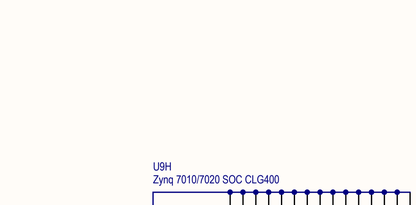


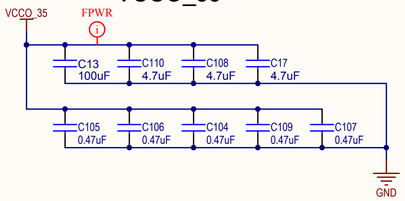
Title:	Avnet Engineering Services 08 - MICROHEADERS.SchDoc
Size: B	Document Number: MicroZed 7010
Rev: F	
Date: 10/29/2013	Sheet 8 of 11

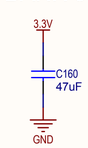


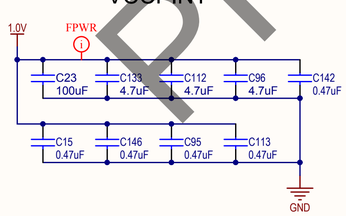


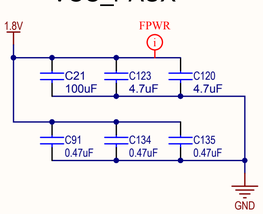


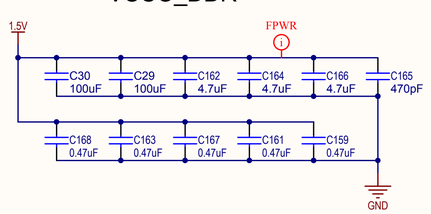


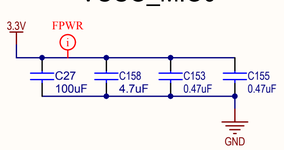


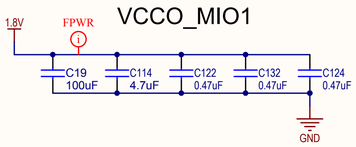


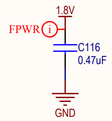




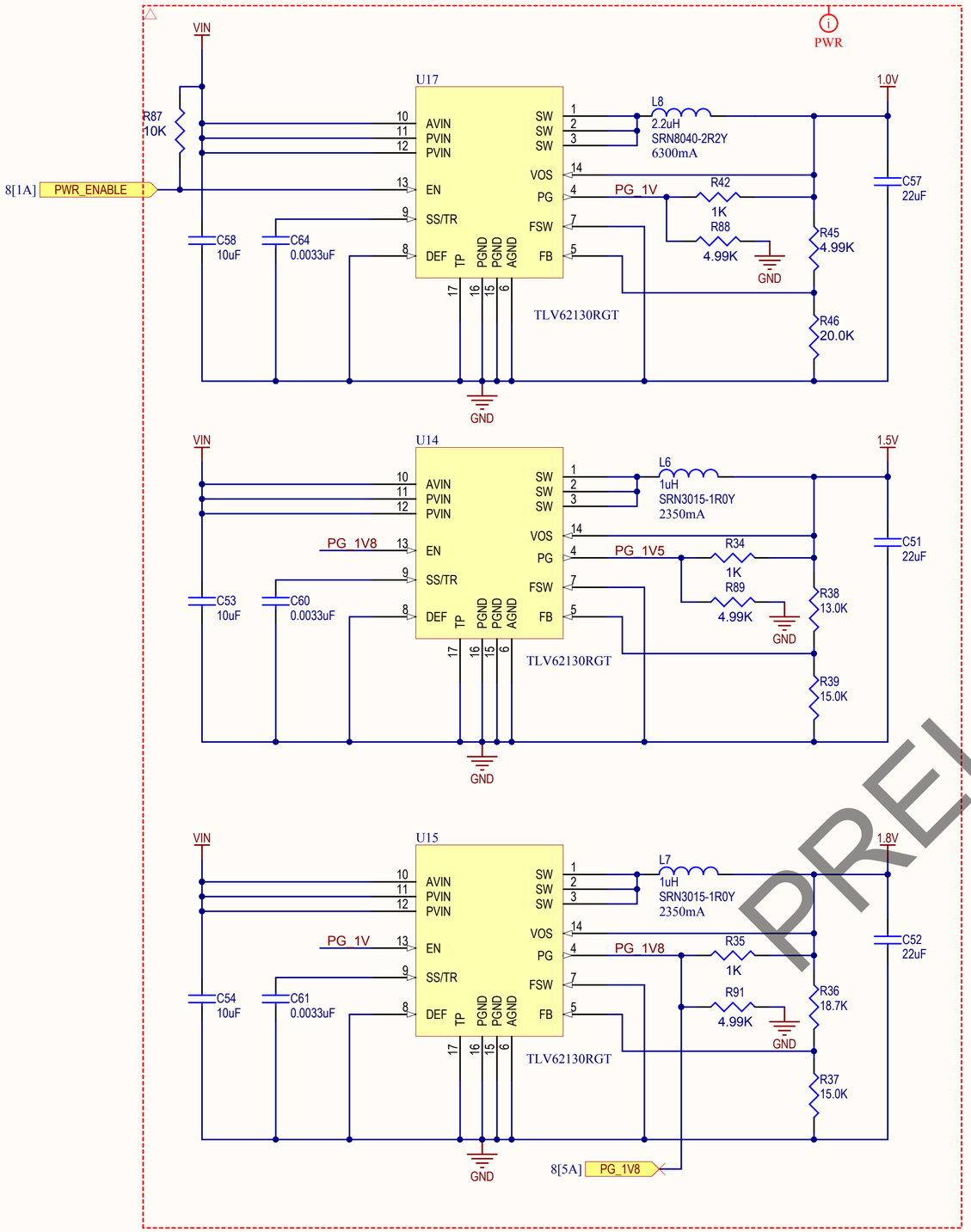


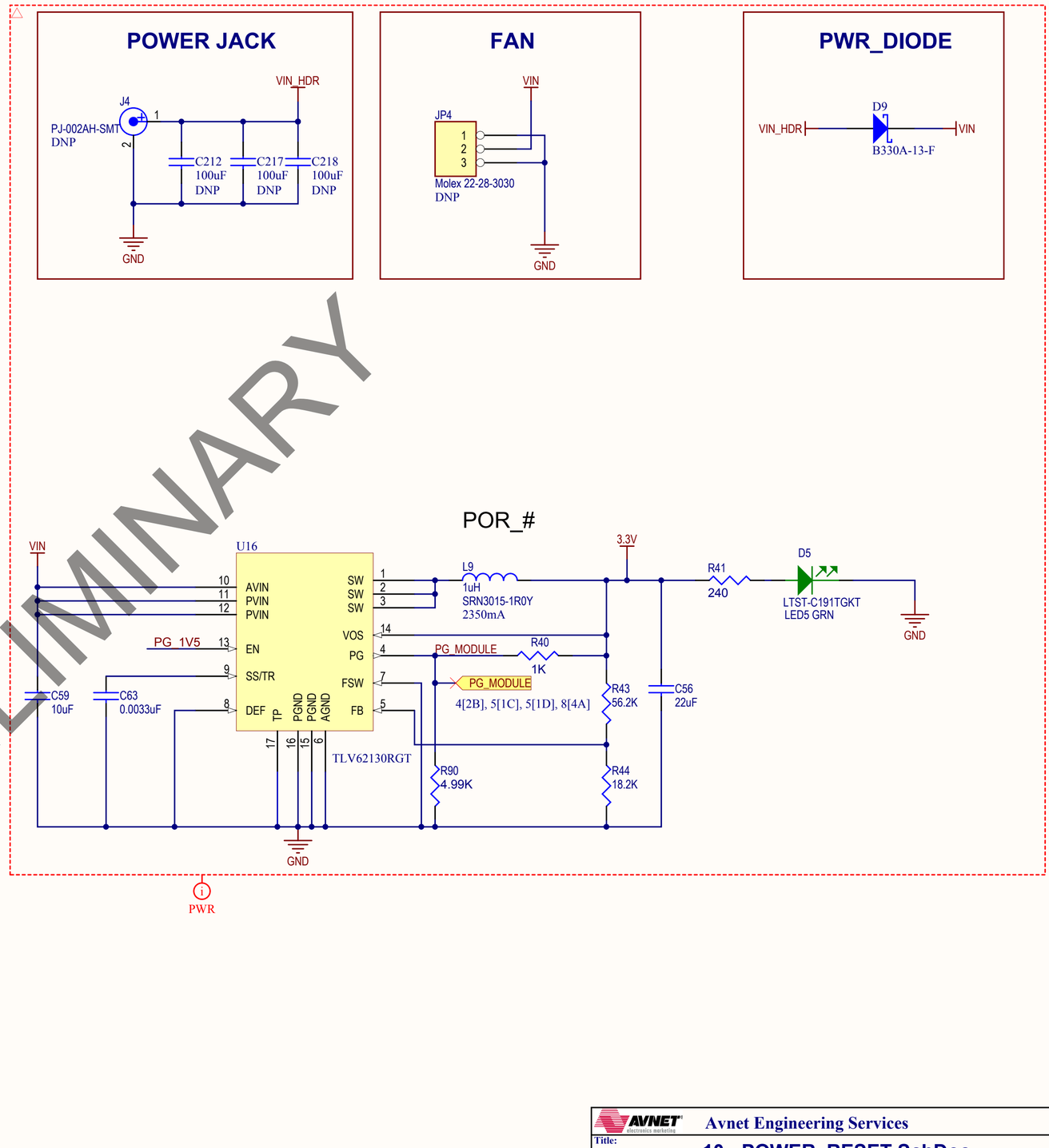






Avnet Engineering Services	
Title:	09 - FPGA POWER.SchDoc
Size: C	Document Number: MicroZed 7010
Rev: F	
Date: 10/29/2013	Sheet 9 of 11





Avnet Engineering Services	
Title:	10 - POWER, RESET.SchDoc
Size: B	Document Number: MicroZed 7010
Rev:	F
Date: 10/29/2013	Sheet 10 of 11

Revision Notes:

Revision C Changes:
1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board
2) Reduce R34, 35, (40), 42 from 100K to 1K
3) Add pulldown resistors to R34, 35, (40), 42 - Value 2.2K - 5.00K
4) Fuse (PTC) recommendation note for R50, 12V input
5) Connect: U8.6 to U20.2
6) Connect: U3.16 to U8.3
7) Connect: JX2.10 to U15.4
8) Change 4.75K resistors to 4.99K
9) Added rubber feet to BOM
10) Add staple point vias for J2 USB connector.

Revision D Changes (no production):
1) Attached JX2.10 to U15.4

Revision E Changes (no production):
1) Replaced U1 from MAX13035EETE+ to TI TXS02612ZQSR part.
2) Added Sheet 11.
3) Moved mechanical information to back page.

Revision F Changes:
1) Changed USB UART default power to bus power. Attach VBUS power net to U2.7 REGIN pin. Disconnect Vdd pin from +3.3V.
2) Added Ethernet LED drive buffer circuit to reduce 3.3V PHY backfeed.
3) Added: D10, D11, JT7, R97, R98 to allow user to configure USB Bus or Self power mode.
4) Removed two fansink mounting holes. Removed ground attribute to mounting holes (in layout files).
5) Added D12 PolyZen (PTC+Zen) USB UART protection component as configurable option.
6) Added R99 0 ohm resistor for D12 bypass (default).
7) Added C221 2.2uF capacitor for USB transient and flyback voltage protection.
8) Revised notes (above).

Mechanicals:

PCB
MMP-7Z045-PCB-F

PCB Mounting Holes

MTG5 0
MOUNTING HOLE 125mil

MTG2 0
MOUNTING HOLE 125mil

MTG1 0
MOUNTING HOLE 125mil

MTG6 0
MOUNTING HOLE 125mil

Fansink Mounting Holes

MTG4
MOUNTING HOLE

MTG3
MOUNTING HOLE

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Title:	11 - Back Page.SchDoc	
Size: B	Document Number: MicroZed 7010	Rev: F
Date: 10/29/2013	Sheet 11 of 11	