

LCFC Confidential


KENOBI NM-A821 Rev2.0 Schematic

Intel KabyLake Processor with DDR4 + PCH-LP

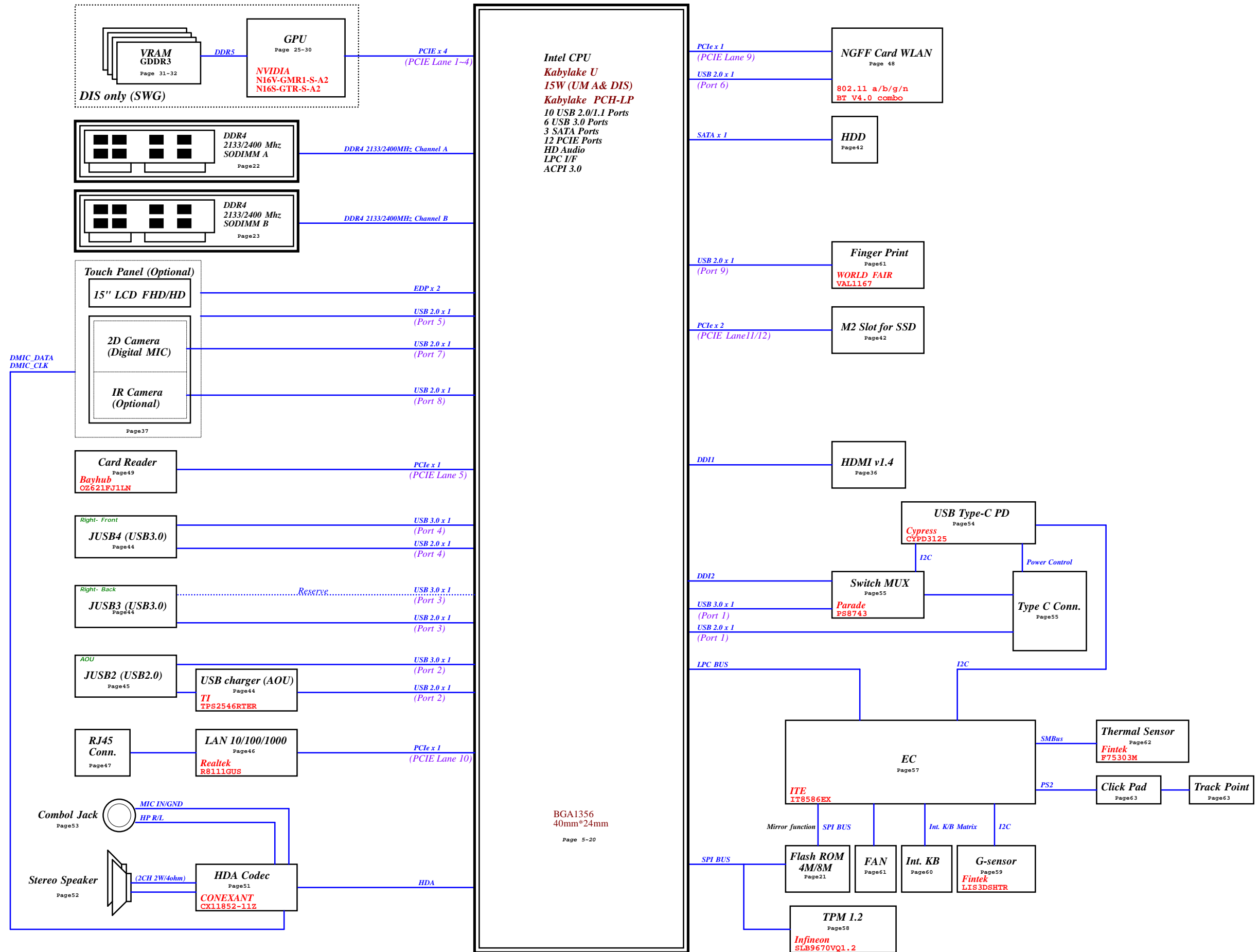
NVIDIA N16V-GMR GDDR3 2GB

2016-08-24 Rev2.0

| | | | | | |
|--|------------------------------|-----------------|------------|-------------------|---------------------------|
| Security Classification | LC Future Center Secret Data | | | Title | |
| Issued Date | 2015/10/5 | Deciphered Date | 2016/12/31 | COVER PAGE | |
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| | | | | Custom | Number |
| | | | | Date: | Thursday, August 25, 2016 |
| | | | | Sheet | 1 of 82 |



Kenobi KBL U Block Diagram



Voltage Rails (O --> Means ON , X --> Means OFF)

| Power Plane / State | B+ +3VL | +3VALW +5VALW +1VALW +1.8VALW | +2.5V +1.2V +VCC_STG | +5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.5VS_VGA +3VS_AON +1VS_VGA +0.6VS |
|--------------------------------|------------|--|----------------------------|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC Only | O | O | X | X |
| S5 S4 Battery only | O | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X |

| STATE \ SIGNAL | SLP_A# | SLP_S3# | SLP_S4# | SLP_S5# | EC_ON2 | EC_ON | SUSP# | SYSON |
|----------------------|--------|---------|---------|---------|--------|-------|-------|-------|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | HIGH |
| S1(Power On Suspend) | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | HIGH |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | HIGH |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | ON | OFF | LOW |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | ON | OFF | LOW |

SMBUS Control Table

| | SOURCE | Main VGA | BATT (Charger) | SODIMM | WLAN WiMAX | Thermal Sensor | PCH | CP Module | LAN PHY | G sensor | USB Type-C |
|-----------------------------|-----------------|---------------|----------------|-----------|------------|----------------|--------------|-----------|---------|--------------|----------------|
| EC_SMB_CK1 EC_SMB_DA1 | IT8580F +3VL | X | V +3VALW | X | X | X | X | X | X | X | X |
| EC_SMB_CK2 EC_SMB_DA2 | IT8580F +3VL | X | X | X | X | X | X | X | X | X | V +3VPD_VDD |
| EC_SMB_CK3 EC_SMB_DA3 | IT8580F +3VS | V +3VS_VGA | X | X | X | V +3VS | V +3V_PCH | X | X | V +3VS_GS | X |
| PCH_SMB_CLK PCH_SMB_DATA | PCH +3V_PCH | X | X | V +3VS | X | X | X | V +5VS | X | X | X |
| PCH_SML1CLK PCH_SML1DAT | PCH +3V_PCH | X | X | X | X | X | X | X | X | X | X |

BOM Structure Table

| BOM Structure | NOTE |
|---------------|-------------------------------|
| PCB@ | For PCB load BOM |
| XDP@ | Debug port |
| UMA@ | UMA SKU ID |
| DIS@ | Optimus SKU ID |
| SSD@ | SSD setting |
| FRP@ | Finger printer setting |
| TYPEC@ | For USB Type-C function |
| ME@ | ME Connector |
| EMC@ | For EMC function |
| EMC_2D@ | For EMC function |
| EMC_NS@ | For EMC function |
| RF_NS@ | For RF function |
| S2G@ | For VRAM Strap |
| CHA@ | For VRAMA function |
| CHB@ | For VRAMB function |
| RANKA@ | GPU DDR5 Setting |
| X76@ | GPU VRAM Setting |
| 3DCCD@ | 3D Camera Setting |
| VGA@ | VGA Setting |
| MUX@ | MUX Setting |
| ODD@ | ODD Setting |
| TPM@ | Trusted Platform Module (TPM) |
| MIRROR@ | For mirror function |
| NGC6@ | For VGA Non GC6 function |
| GC6@ | For VGA GC6 function |

USB2 Port

| Port | Device |
|------|--------------|
| 1 | JUSB1 TYPE-C |
| 2 | JUSB2 |
| 3 | JUSB3 |
| 4 | JUSB4 |
| 5 | Touch Panel |
| 6 | BT |
| 7 | CMOS |
| 8 | IR CAMERA |
| 9 | FP/Smart |

USB3 Port


| Port | Device |
|------|--------------|
| 1 | JUSB1 TYPE-C |
| 2 | JUSB2 |
| 3 | JUSB3 |
| 4 | JUSB4 |

PCIE Port

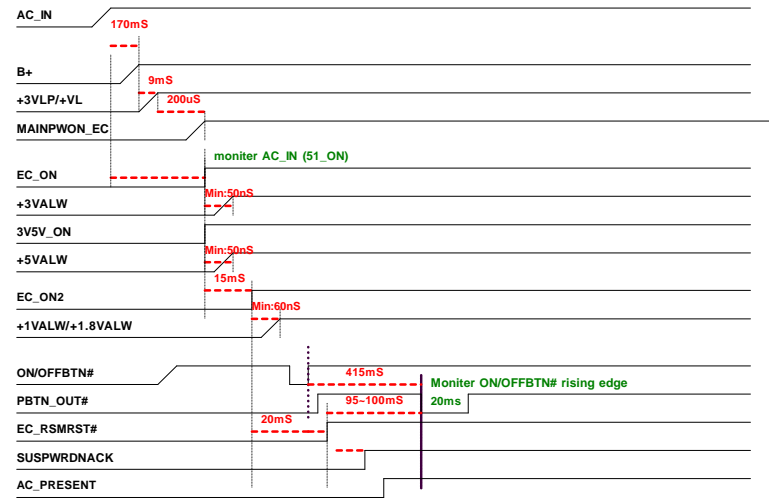
| Port | Device |
|------|------------|
| 1 | GPU |
| 2 | GPU |
| 3 | GPU |
| 4 | GPU |
| 5 | CardReader |
| 6 | X |
| 7 | X |
| 8 | X |
| 9 | WLAN |
| 10 | LAN |
| 11 | M.2 SSD |
| 12 | M.2 SSD |

SATA Port

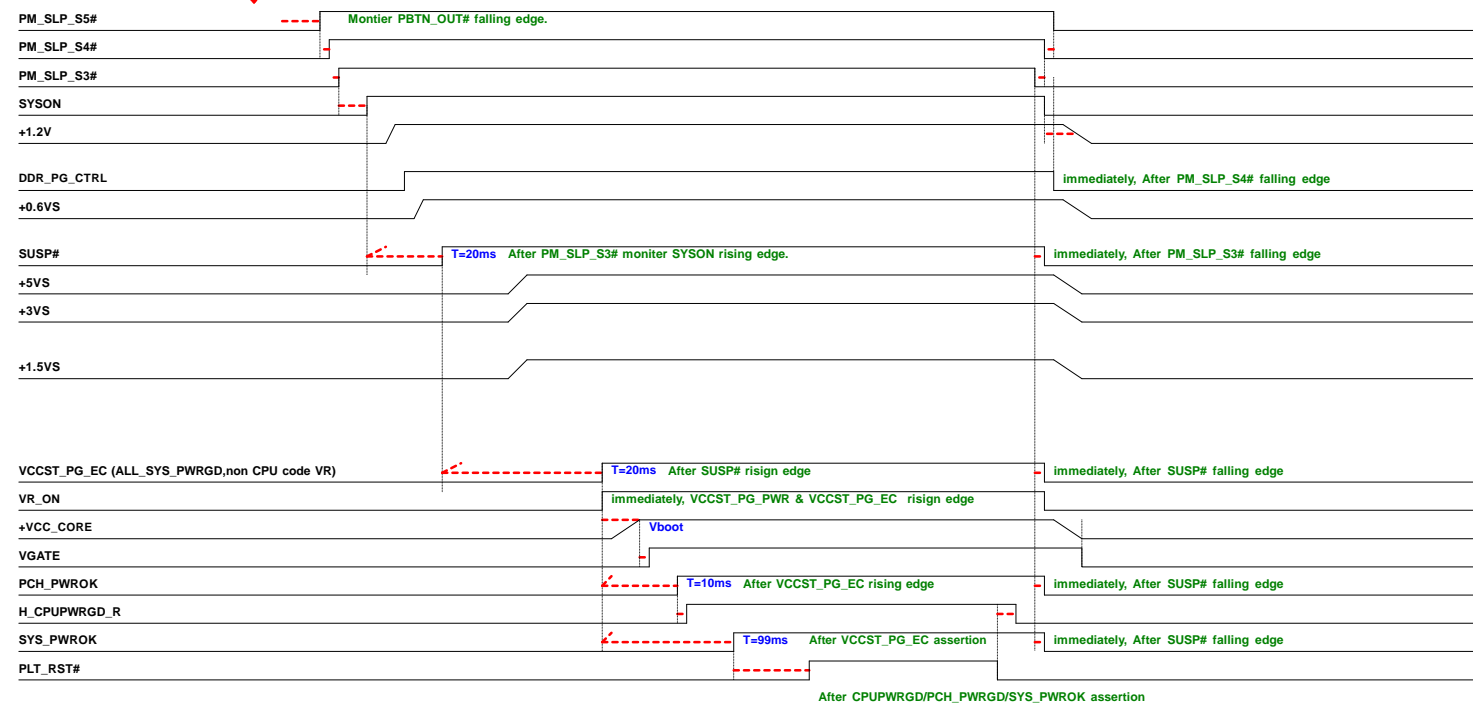
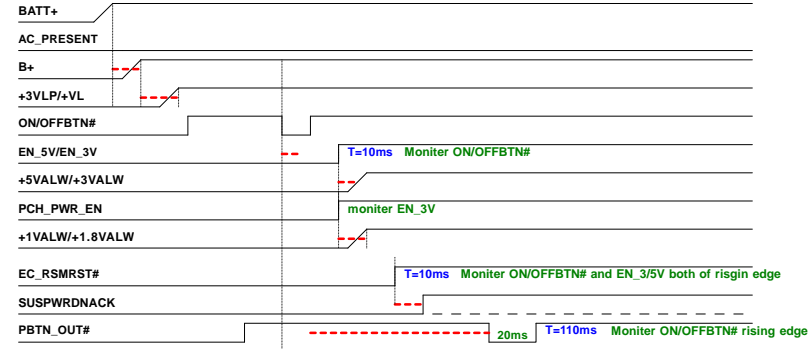
| Port | Device |
|------|--------|
| 1 | HDD |
| 2 | X |
| 3 | X |
| 4 | X |

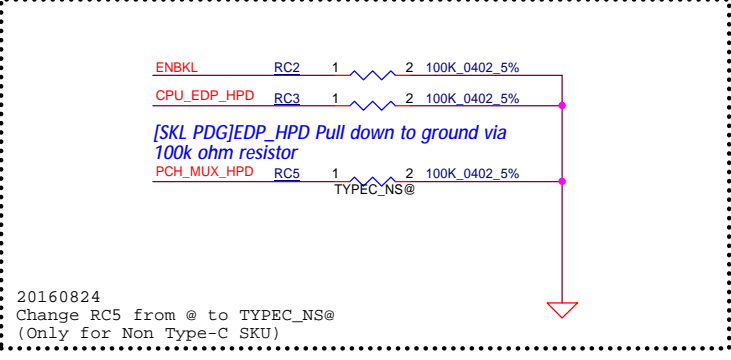
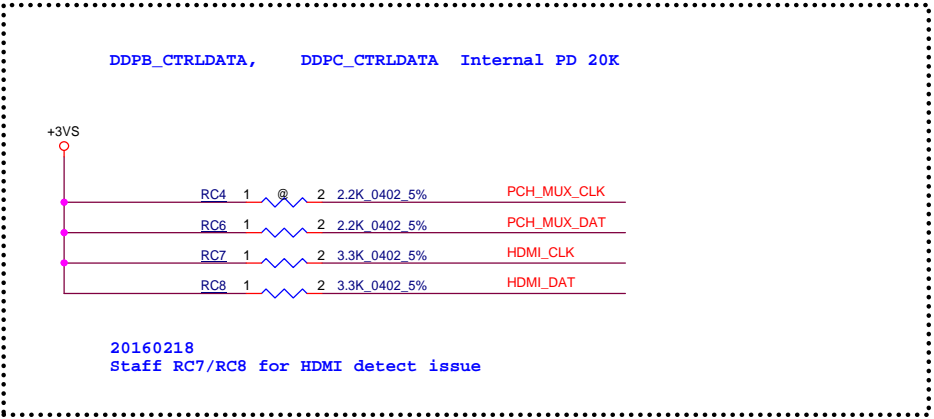
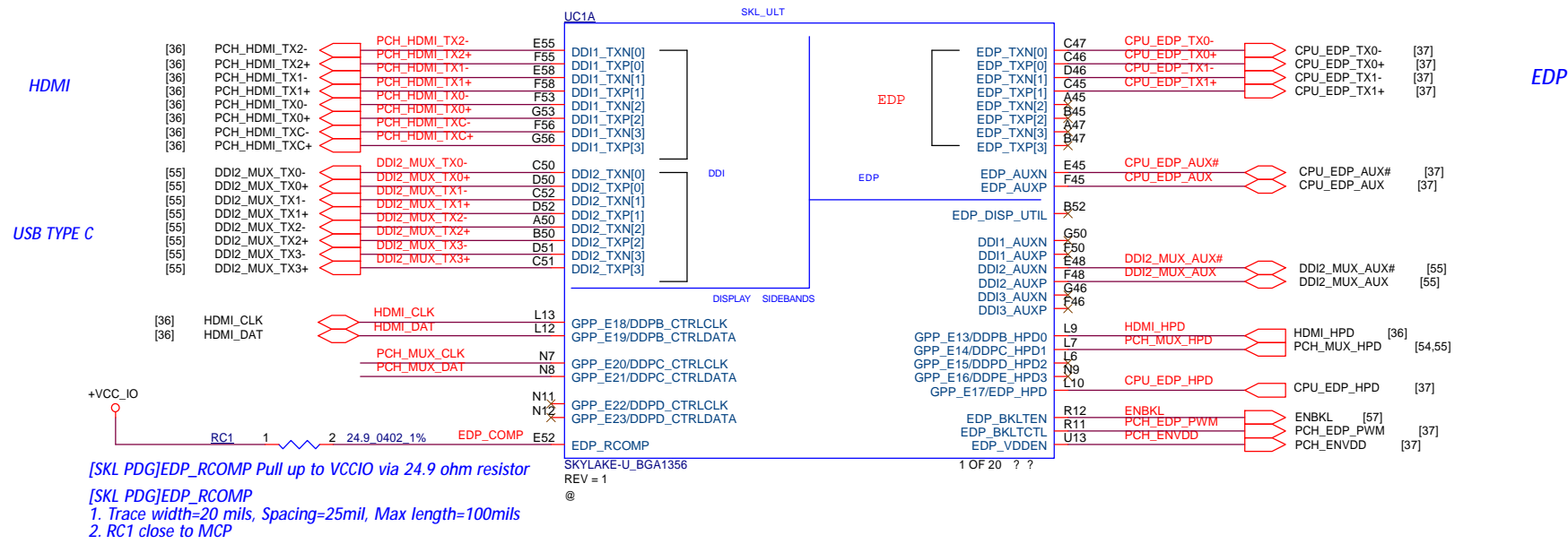
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[AC Mode]

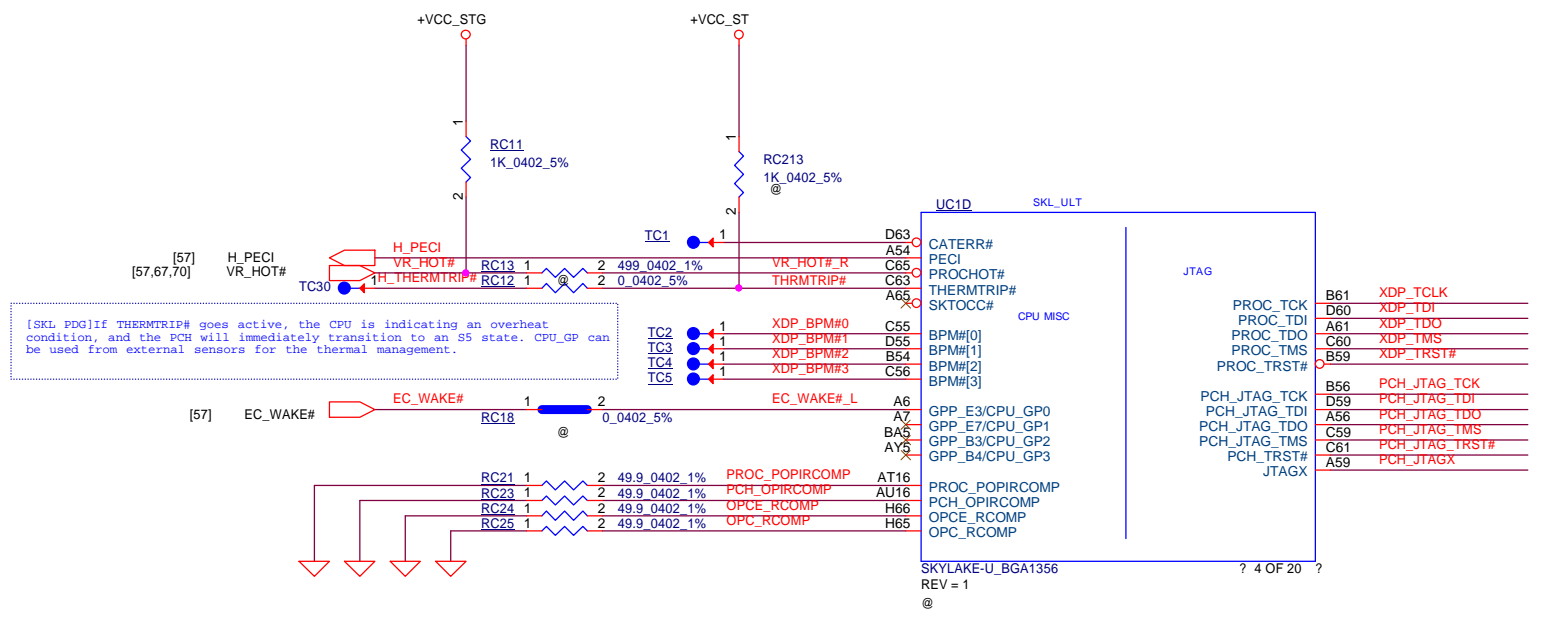


[DC Mode]



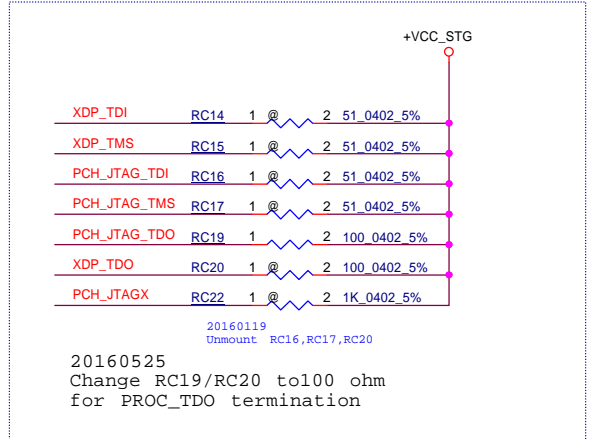
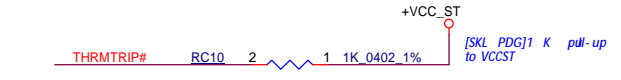


| | | |
|---------------|-----------------|---|
| DDPB_CTRLDATA | Port B Detected | This signal has an integrated weak pull-down (20 K Ω nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 K Ω \pm 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected. |
| DDPC_CTRLDATA | Port C Detected | This signal has an integrated weak pull-down (20 K Ω nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 K Ω \pm 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected. |

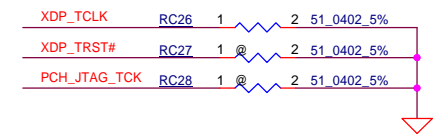


[SKL_PDG] If THERMTRIP# goes active, the CPU is indicating an overheat condition, and the PCH will immediately transition to an S5 state. CPU_GP can be used from external sensors for the thermal management.

[SKL_PDG] PROC_OPI_RCOMP: Signal should be pulled down to ground with a resistance of 50 ohm ±1%
 [SKL_PDG] PCH_OPI_RCOMP: Signal should be pulled down to ground with a resistance of 50 ohm ±1%
 [SKL_PDG] On Package Interface Compensation (OPI) Guidelines should be referenced to VSS plane only. VSS reference planes must be continuous. Require low DC resistance routing <0.2 ohm. Avoid routing next to clock pins or noisy signals.



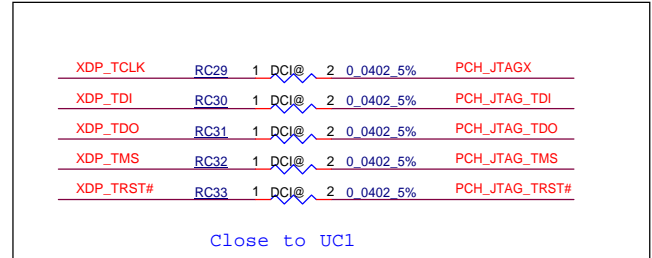
20160119
 Unmount RC16,RC17,RC20
 20160525
 Change RC19/RC20 to 100 ohm for PROC_TDO termination



Termination option

XDP_TCLK
 PROC_TCK Termination:
 51 ohm +/- 5% pull down to GNG (Ground)
 Placed to within 200ps (1100 mil) or PROC_TCK pin

PCH_JTAG_TDO
 PCH_JTAG_TDO Termination:
 51ohm +/- 5% pull up to VccSTG or equivalent.
 Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin



Close to UC1

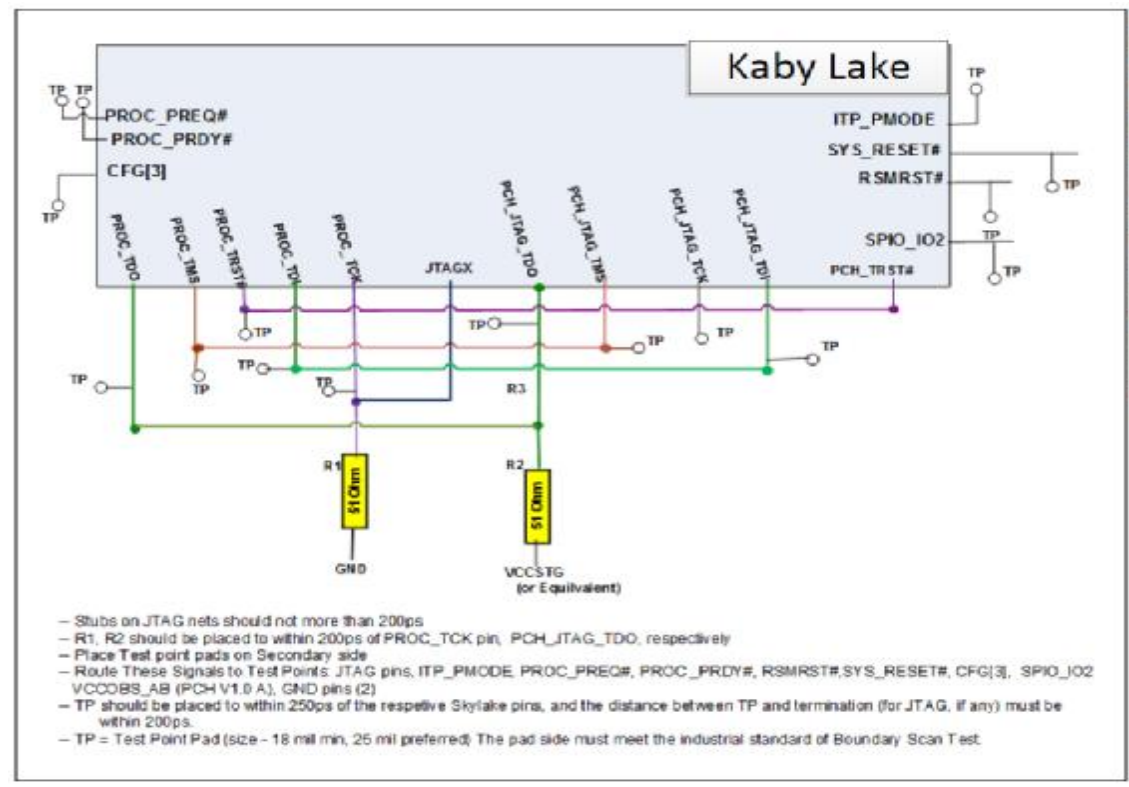


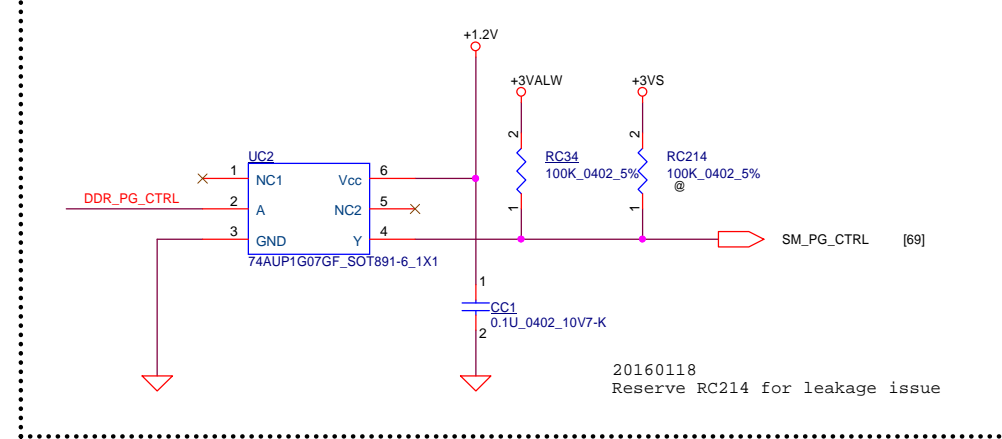
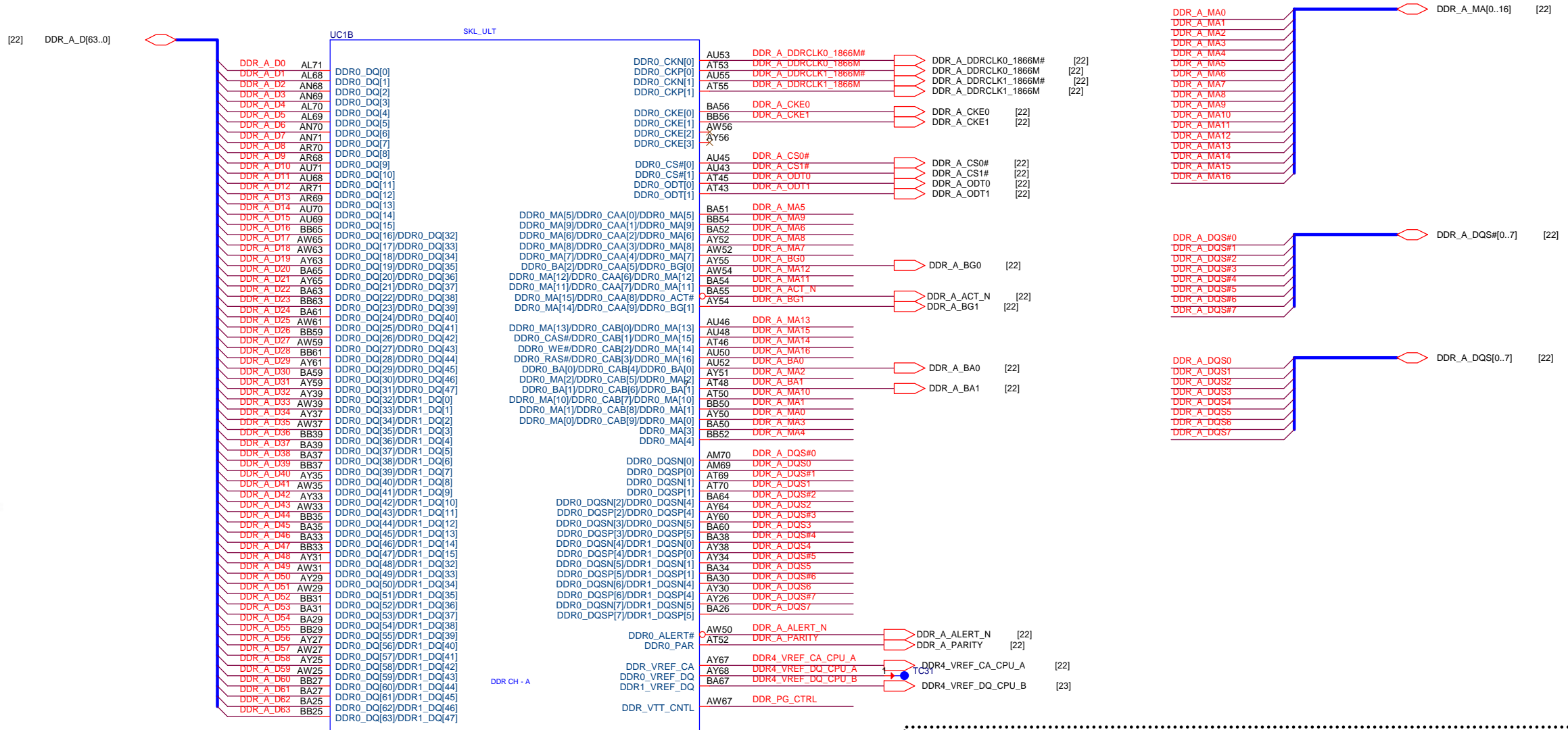
Figure 44-6: Connector Less Routing Topology

- Stubs on JTAG nets should not more than 200ps
- R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
- Place Test point pads on Secondary side
- Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#, SYS_RESET#, CFG[3], SPIO_IO2, VCCOBS_AB (PCH V1.0 A), GND pins (2)
- TP should be placed to within 250ps of the respective Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
- TP = Test Point Pad (size - 18 mil min, 25 mil preferred). The pad side must meet the industrial standard of Boundary Scan Test.

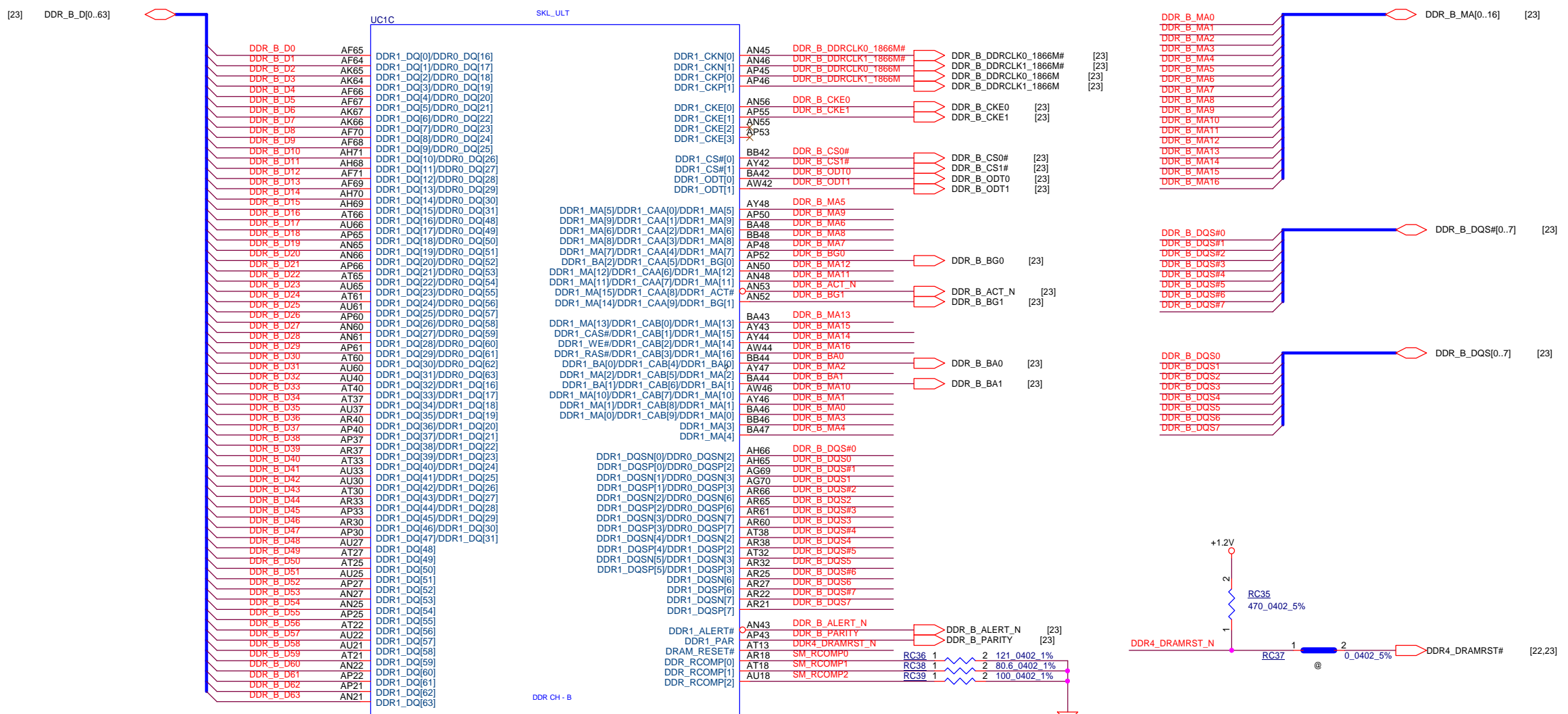
| TABLE | Pin | Interleave | Non-Interleave |
|---------|------|-------------|----------------|
| Block 0 | AL71 | DDR0_DQ[0] | DDR0_DQ[0] |
| | AL88 | DDR0_DQ[1] | DDR0_DQ[1] |
| | AN68 | DDR0_DQ[2] | DDR0_DQ[2] |
| | AN69 | DDR0_DQ[3] | DDR0_DQ[3] |
| | AL70 | DDR0_DQ[4] | DDR0_DQ[4] |
| | AL89 | DDR0_DQ[5] | DDR0_DQ[5] |
| | AN70 | DDR0_DQ[6] | DDR0_DQ[6] |
| | AN71 | DDR0_DQ[7] | DDR0_DQ[7] |
| | AR70 | DDR0_DQ[8] | DDR0_DQ[8] |
| | AR88 | DDR0_DQ[9] | DDR0_DQ[9] |
| | AU71 | DDR0_DQ[10] | DDR0_DQ[10] |
| | AU88 | DDR0_DQ[11] | DDR0_DQ[11] |
| | AR71 | DDR0_DQ[12] | DDR0_DQ[12] |
| | AR89 | DDR0_DQ[13] | DDR0_DQ[13] |
| | AU70 | DDR0_DQ[14] | DDR0_DQ[14] |
| | AU89 | DDR0_DQ[15] | DDR0_DQ[15] |
| Block 2 | BB66 | DDR0_DQ[16] | DDR0_DQ[16] |
| | AW66 | DDR0_DQ[17] | DDR0_DQ[17] |
| | AY63 | DDR0_DQ[18] | DDR0_DQ[18] |
| | BA66 | DDR0_DQ[19] | DDR0_DQ[19] |
| | AY66 | DDR0_DQ[20] | DDR0_DQ[20] |
| | BA63 | DDR0_DQ[21] | DDR0_DQ[21] |
| | BA83 | DDR0_DQ[22] | DDR0_DQ[22] |
| | BB83 | DDR0_DQ[23] | DDR0_DQ[23] |
| | BA81 | DDR0_DQ[24] | DDR0_DQ[24] |
| | AW81 | DDR0_DQ[25] | DDR0_DQ[25] |
| | BB81 | DDR0_DQ[26] | DDR0_DQ[26] |
| | BB69 | DDR0_DQ[27] | DDR0_DQ[27] |
| | AW69 | DDR0_DQ[28] | DDR0_DQ[28] |
| | AY61 | DDR0_DQ[29] | DDR0_DQ[29] |
| | BA59 | DDR0_DQ[30] | DDR0_DQ[30] |
| | AY59 | DDR0_DQ[31] | DDR0_DQ[31] |
| Block 4 | AY39 | DDR0_DQ[32] | DDR0_DQ[32] |
| | AW39 | DDR0_DQ[33] | DDR0_DQ[33] |
| | AY37 | DDR0_DQ[34] | DDR0_DQ[34] |
| | AW37 | DDR0_DQ[35] | DDR0_DQ[35] |
| | BB39 | DDR0_DQ[36] | DDR0_DQ[36] |
| | BA39 | DDR0_DQ[37] | DDR0_DQ[37] |
| | BA37 | DDR0_DQ[38] | DDR0_DQ[38] |
| | BB37 | DDR0_DQ[39] | DDR0_DQ[39] |
| | AY36 | DDR0_DQ[40] | DDR0_DQ[40] |
| | AW36 | DDR0_DQ[41] | DDR0_DQ[41] |
| | AY33 | DDR0_DQ[42] | DDR0_DQ[42] |
| | AW33 | DDR0_DQ[43] | DDR0_DQ[43] |
| | BB36 | DDR0_DQ[44] | DDR0_DQ[44] |
| | BA36 | DDR0_DQ[45] | DDR0_DQ[45] |
| | BA33 | DDR0_DQ[46] | DDR0_DQ[46] |
| | BB33 | DDR0_DQ[47] | DDR0_DQ[47] |
| Block 6 | AY31 | DDR0_DQ[48] | DDR0_DQ[48] |
| | AW31 | DDR0_DQ[49] | DDR0_DQ[49] |
| | AY29 | DDR0_DQ[50] | DDR0_DQ[50] |
| | AW29 | DDR0_DQ[51] | DDR0_DQ[51] |
| | BB31 | DDR0_DQ[52] | DDR0_DQ[52] |
| | BA31 | DDR0_DQ[53] | DDR0_DQ[53] |
| | AA29 | DDR0_DQ[54] | DDR0_DQ[54] |
| | BB29 | DDR0_DQ[55] | DDR0_DQ[55] |
| | AY27 | DDR0_DQ[56] | DDR0_DQ[56] |
| | AW27 | DDR0_DQ[57] | DDR0_DQ[57] |
| | AY26 | DDR0_DQ[58] | DDR0_DQ[58] |
| | AW26 | DDR0_DQ[59] | DDR0_DQ[59] |
| | BB27 | DDR0_DQ[60] | DDR0_DQ[60] |
| | BA27 | DDR0_DQ[61] | DDR0_DQ[61] |
| | BA26 | DDR0_DQ[62] | DDR0_DQ[62] |
| | BB26 | DDR0_DQ[63] | DDR0_DQ[63] |

| TABLE | Pin | Interleave | Non-Interleave |
|---------|------|--------------|----------------|
| Block 0 | AM70 | DDR0_DQSN[0] | DDR0_DQSN[0] |
| | AM69 | DDR0_DQSP[0] | DDR0_DQSP[0] |
| | AT69 | DDR0_DQSN[1] | DDR0_DQSN[1] |
| | AT70 | DDR0_DQSP[1] | DDR0_DQSP[1] |
| Block 2 | BA64 | DDR0_DQSN[2] | DDR0_DQSN[2] |
| | AY64 | DDR0_DQSP[2] | DDR0_DQSP[2] |
| | AY60 | DDR0_DQSN[3] | DDR0_DQSN[3] |
| | BA60 | DDR0_DQSP[3] | DDR0_DQSP[3] |
| Block 4 | BA38 | DDR0_DQSN[4] | DDR0_DQSN[4] |
| | AY38 | DDR0_DQSP[4] | DDR0_DQSP[4] |
| | AY34 | DDR0_DQSN[5] | DDR0_DQSN[5] |
| | BA34 | DDR0_DQSP[5] | DDR0_DQSP[5] |
| Block 6 | BA30 | DDR0_DQSN[6] | DDR0_DQSN[6] |
| | AY30 | DDR0_DQSP[6] | DDR0_DQSP[6] |
| | AY26 | DDR0_DQSN[7] | DDR0_DQSN[7] |
| | BA26 | DDR0_DQSP[7] | DDR0_DQSP[7] |

| TABLE | Pin | DDR3L | LPDDR3 | DDR4 |
|-------|-------------|-------------|-------------|------|
| BA51 | DDR0_MA[5] | DDR0_CAA[0] | DDR0_MA[5] | |
| BB54 | DDR0_MA[3] | DDR0_CAA[1] | DDR0_MA[3] | |
| BA52 | DDR0_MA[6] | DDR0_CAA[2] | DDR0_MA[6] | |
| AY52 | DDR0_MA[8] | DDR0_CAA[3] | DDR0_MA[8] | |
| AW52 | DDR0_MA[7] | DDR0_CAA[4] | DDR0_MA[7] | |
| AY55 | DDR0_BA[2] | DDR0_CAA[5] | DDR0_BG[6] | |
| AW54 | DDR0_MA[12] | DDR0_CAA[6] | DDR0_MA[12] | |
| BA54 | DDR0_MA[11] | DDR0_CAA[7] | DDR0_MA[11] | |
| BA55 | DDR0_MA[15] | DDR0_CAA[8] | DDR0_ACT# | |
| AY54 | DDR0_MA[14] | DDR0_CAA[9] | DDR0_BG[1] | |
| AU46 | DDR0_MA[13] | DDR0_CAB[0] | DDR0_MA[13] | |
| AU48 | DDR0_CAS# | DDR0_CAB[1] | DDR0_MA[15] | |
| AT46 | DDR0_WE# | DDR0_CAB[2] | DDR0_MA[14] | |
| AU50 | DDR0_RAS# | DDR0_CAB[3] | DDR0_MA[16] | |
| AU52 | DDR0_BA[0] | DDR0_CAB[4] | DDR0_BA[0] | |
| AY51 | DDR0_MA[2] | DDR0_CAB[5] | DDR0_MA[2] | |
| AT48 | DDR0_BA[1] | DDR0_CAB[6] | DDR0_BA[1] | |
| AT50 | DDR0_MA[10] | DDR0_CAB[7] | DDR0_MA[10] | |
| BB50 | DDR0_MA[1] | DDR0_CAB[8] | DDR0_MA[1] | |
| AY50 | DDR0_MA[0] | DDR0_CAB[9] | DDR0_MA[0] | |
| BA50 | DDR0_MA[3] | Not Used | DDR0_MA[3] | |
| BB52 | DDR0_MA[4] | Not Used | DDR0_MA[4] | |



| TABLE | Pin | Interleave | Non-Interleave |
|---------|-------------|-------------|----------------|
| Block 1 | AF66 | DDR1_DQ[0] | DDR0_DQ[16] |
| | AF64 | DDR1_DQ[1] | DDR0_DQ[17] |
| | AK64 | DDR1_DQ[2] | DDR0_DQ[18] |
| | AK64 | DDR1_DQ[3] | DDR0_DQ[19] |
| | AF68 | DDR1_DQ[4] | DDR0_DQ[20] |
| | AF67 | DDR1_DQ[5] | DDR0_DQ[21] |
| | AK67 | DDR1_DQ[6] | DDR0_DQ[22] |
| | AK68 | DDR1_DQ[7] | DDR0_DQ[23] |
| | AF70 | DDR1_DQ[8] | DDR0_DQ[24] |
| | AF68 | DDR1_DQ[9] | DDR0_DQ[25] |
| | AH71 | DDR1_DQ[10] | DDR0_DQ[26] |
| | AH68 | DDR1_DQ[11] | DDR0_DQ[27] |
| | AF71 | DDR1_DQ[12] | DDR0_DQ[28] |
| | AF68 | DDR1_DQ[13] | DDR0_DQ[29] |
| AH70 | DDR1_DQ[14] | DDR0_DQ[30] | |
| AH68 | DDR1_DQ[15] | DDR0_DQ[31] | |
| Block 3 | AT66 | DDR1_DQ[16] | DDR0_DQ[32] |
| | AU66 | DDR1_DQ[17] | DDR0_DQ[33] |
| | AK66 | DDR1_DQ[18] | DDR0_DQ[34] |
| | AK66 | DDR1_DQ[19] | DDR0_DQ[35] |
| | AN68 | DDR1_DQ[20] | DDR0_DQ[36] |
| | AP68 | DDR1_DQ[21] | DDR0_DQ[37] |
| | AT66 | DDR1_DQ[22] | DDR0_DQ[38] |
| | AU66 | DDR1_DQ[23] | DDR0_DQ[39] |
| | AT61 | DDR1_DQ[24] | DDR0_DQ[40] |
| | AU61 | DDR1_DQ[25] | DDR0_DQ[41] |
| | AP60 | DDR1_DQ[26] | DDR0_DQ[42] |
| | AN60 | DDR1_DQ[27] | DDR0_DQ[43] |
| | AN61 | DDR1_DQ[28] | DDR0_DQ[44] |
| | AF61 | DDR1_DQ[29] | DDR0_DQ[45] |
| AT60 | DDR1_DQ[30] | DDR0_DQ[46] | |
| AU60 | DDR1_DQ[31] | DDR0_DQ[47] | |
| Block 5 | AU40 | DDR1_DQ[32] | DDR1_DQ[16] |
| | AT40 | DDR1_DQ[33] | DDR1_DQ[17] |
| | AT37 | DDR1_DQ[34] | DDR1_DQ[18] |
| | AU37 | DDR1_DQ[35] | DDR1_DQ[19] |
| | AR40 | DDR1_DQ[36] | DDR1_DQ[20] |
| | AP40 | DDR1_DQ[37] | DDR1_DQ[21] |
| | AP37 | DDR1_DQ[38] | DDR1_DQ[22] |
| | AR37 | DDR1_DQ[39] | DDR1_DQ[23] |
| | AT33 | DDR1_DQ[40] | DDR1_DQ[24] |
| | AU33 | DDR1_DQ[41] | DDR1_DQ[25] |
| | AU30 | DDR1_DQ[42] | DDR1_DQ[26] |
| | AT30 | DDR1_DQ[43] | DDR1_DQ[27] |
| | AR33 | DDR1_DQ[44] | DDR1_DQ[28] |
| | AP33 | DDR1_DQ[45] | DDR1_DQ[29] |
| AR30 | DDR1_DQ[46] | DDR1_DQ[30] | |
| AP30 | DDR1_DQ[47] | DDR1_DQ[31] | |
| Block 7 | AU27 | DDR1_DQ[48] | DDR1_DQ[16] |
| | AT27 | DDR1_DQ[49] | DDR1_DQ[17] |
| | AT26 | DDR1_DQ[50] | DDR1_DQ[18] |
| | AU25 | DDR1_DQ[51] | DDR1_DQ[19] |
| | AP27 | DDR1_DQ[52] | DDR1_DQ[20] |
| | AN27 | DDR1_DQ[53] | DDR1_DQ[21] |
| | AN26 | DDR1_DQ[54] | DDR1_DQ[22] |
| | AP26 | DDR1_DQ[55] | DDR1_DQ[23] |
| | AT22 | DDR1_DQ[56] | DDR1_DQ[24] |
| | AU22 | DDR1_DQ[57] | DDR1_DQ[25] |
| | AU21 | DDR1_DQ[58] | DDR1_DQ[26] |
| | AT21 | DDR1_DQ[59] | DDR1_DQ[27] |
| | AN22 | DDR1_DQ[60] | DDR1_DQ[28] |
| | AP22 | DDR1_DQ[61] | DDR1_DQ[29] |
| AP21 | DDR1_DQ[62] | DDR1_DQ[30] | |
| AN21 | DDR1_DQ[63] | DDR1_DQ[31] | |



| TABLE | Pin | Interleave | Non-Interleave |
|---------|------|--------------|----------------|
| Block 1 | AH66 | DDR1_DQSN[0] | DDR0_DQSN[2] |
| | AH65 | DDR1_DQSP[0] | DDR0_DQSP[2] |
| | AG69 | DDR1_DQSN[1] | DDR0_DQSN[3] |
| Block 3 | AR66 | DDR1_DQSN[2] | DDR0_DQSN[6] |
| | AR65 | DDR1_DQSP[2] | DDR0_DQSP[6] |
| | AR61 | DDR1_DQSN[3] | DDR0_DQSN[7] |
| Block 5 | AT38 | DDR1_DQSN[4] | DDR1_DQSN[2] |
| | AR38 | DDR1_DQSP[4] | DDR1_DQSP[2] |
| | AR32 | DDR1_DQSN[5] | DDR1_DQSN[3] |
| Block 7 | AR25 | DDR1_DQSN[6] | DDR1_DQSN[6] |
| | AR27 | DDR1_DQSP[6] | DDR1_DQSP[6] |
| | AR21 | DDR1_DQSN[7] | DDR1_DQSN[7] |

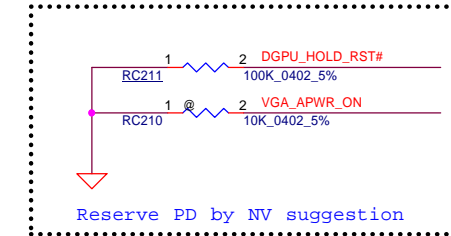
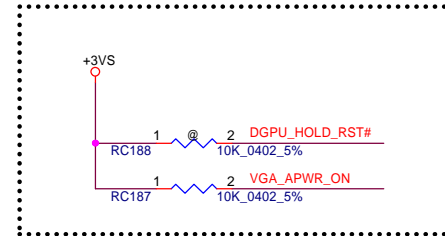
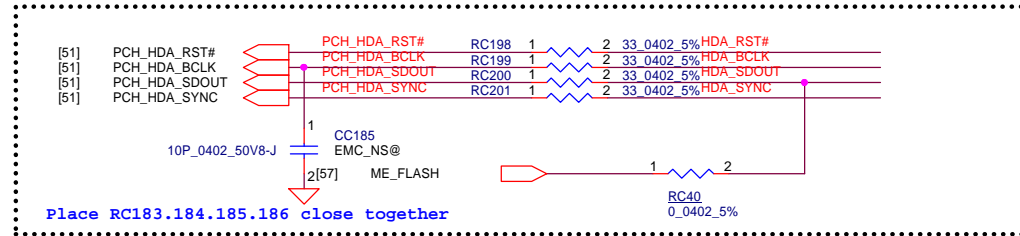
| TABLE | Pin | DDR3L | LPDDR3 | DDR4 |
|---------|------|-------------|-------------|-------------|
| Block 1 | AY48 | DDR1_MA[5] | DDR1_CAA[0] | DDR1_MA[5] |
| | AP90 | DDR1_MA[8] | DDR1_CAA[1] | DDR1_MA[8] |
| | BA48 | DDR1_MA[6] | DDR1_CAA[2] | DDR1_MA[6] |
| | BS48 | DDR1_MA[8] | DDR1_CAA[3] | DDR1_MA[8] |
| | AP48 | DDR1_MA[7] | DDR1_CAA[4] | DDR1_MA[7] |
| | AP52 | DDR1_BA[2] | DDR1_CAA[5] | DDR1_BG[0] |
| | AN50 | DDR1_MA[12] | DDR1_CAA[6] | DDR1_MA[12] |
| | AN48 | DDR1_MA[11] | DDR1_CAA[7] | DDR1_MA[11] |
| | AN53 | DDR1_MA[15] | DDR1_CAA[8] | DDR1_ACT# |
| | AN52 | DDR1_MA[14] | DDR1_CAA[9] | DDR1_BG[1] |
| Block 2 | BA43 | DDR1_MA[13] | DDR1_CAB[0] | DDR1_MA[13] |
| | AY43 | DDR1_CAS# | DDR1_CAB[1] | DDR1_MA[15] |
| | AY44 | DDR1_WE# | DDR1_CAB[2] | DDR1_MA[14] |
| | AW44 | DDR1_RAS# | DDR1_CAB[3] | DDR1_MA[16] |
| | BS44 | DDR1_BA[0] | DDR1_CAB[4] | DDR1_BA[0] |
| | AY47 | DDR1_MA[2] | DDR1_CAB[5] | DDR1_MA[2] |
| | BA44 | DDR1_BA[1] | DDR1_CAB[6] | DDR1_BA[1] |
| | AW46 | DDR1_MA[10] | DDR1_CAB[7] | DDR1_MA[10] |
| | AY46 | DDR1_MA[11] | DDR1_CAB[8] | DDR1_MA[11] |
| | BA46 | DDR1_MA[0] | DDR1_CAB[9] | DDR1_MA[0] |
| Block 3 | BB46 | DDR1_MA[3] | Not Used | DDR1_MA[3] |
| | BA47 | DDR1_MA[4] | Not Used | DDR1_MA[4] |

(KBL PDG) for DDR4 COMPENSATION
 DDR_RCOMP[0] Pull down 121 ohm resistor
 DDR_RCOMP[1] Pull down 80.6 ohm resistor
 DDR_RCOMP[2] Pull down 100 ohm resistor

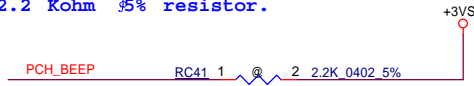
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[KBL PDG] Manufacturing Mode Jumper
 1. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default)
 2. If sampled high, the Flash Descriptor Security will be overridden.

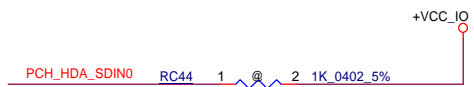
20160408
 1. Unstaff RC188 and Staff RC211 with 100K resistor



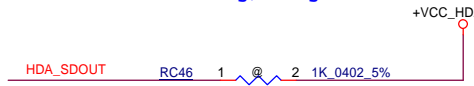
Note:
 SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Sway by default.
 To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm 5% resistor.



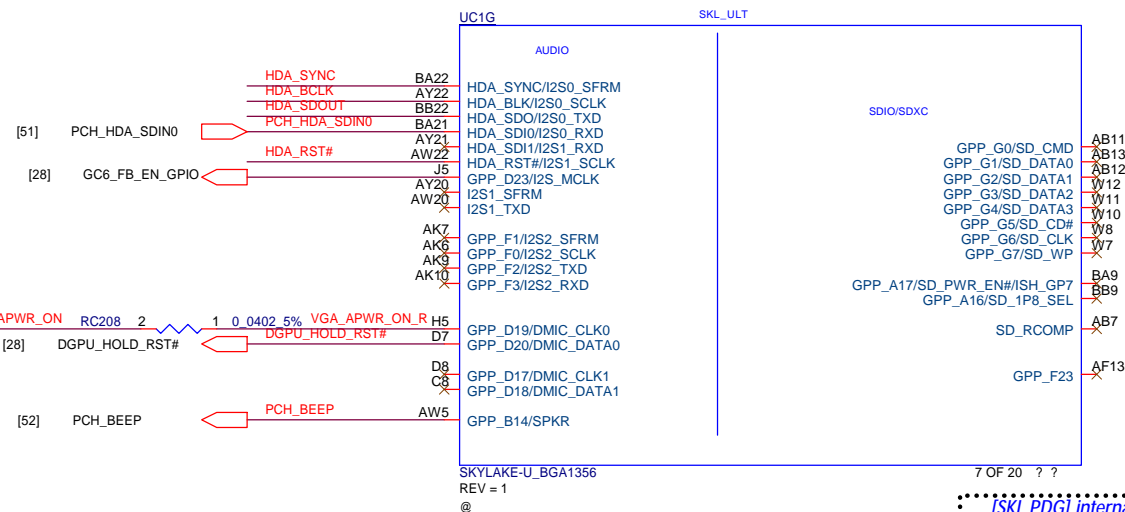
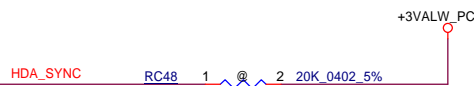
Note:
 Internal PD 20K



Note:
 HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.



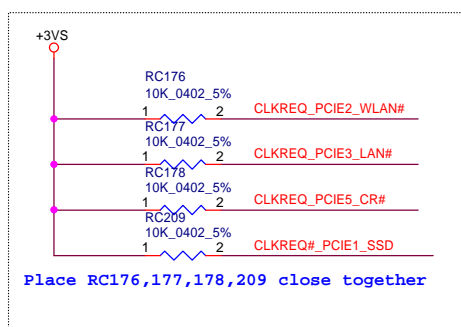
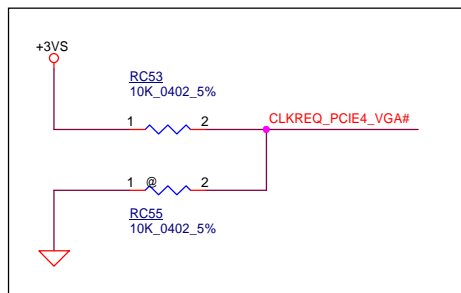
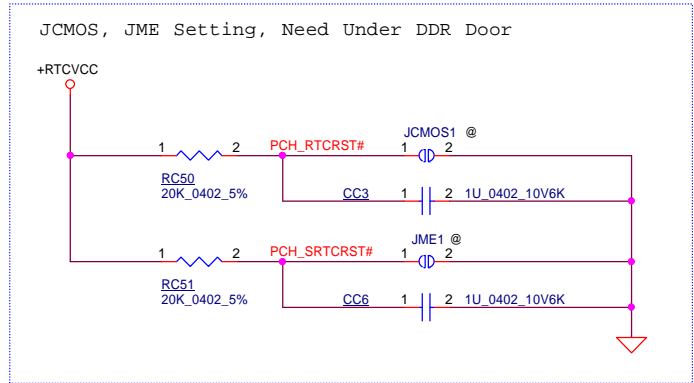
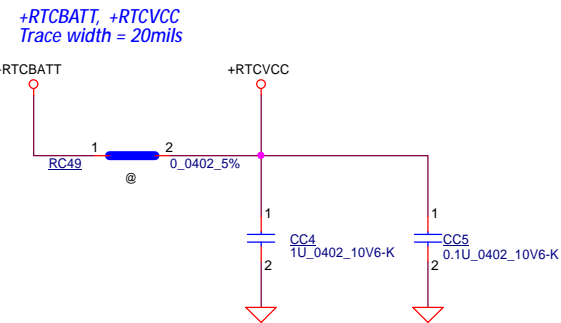
Note:
 Internal PD 20K



[SKL PDG] internal SD card
 Not support internal SD card. Remove SD_RCOMP

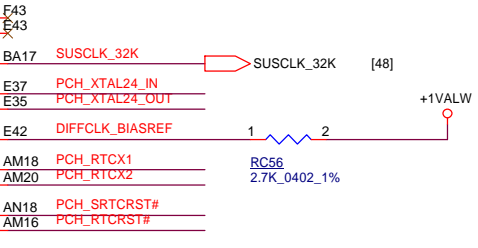
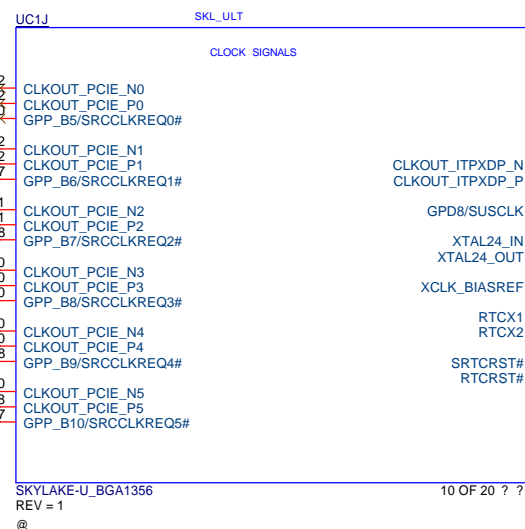
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| | | | | Rev: 2.0 Sheet: 9 of 82 |

RTC External Circuit

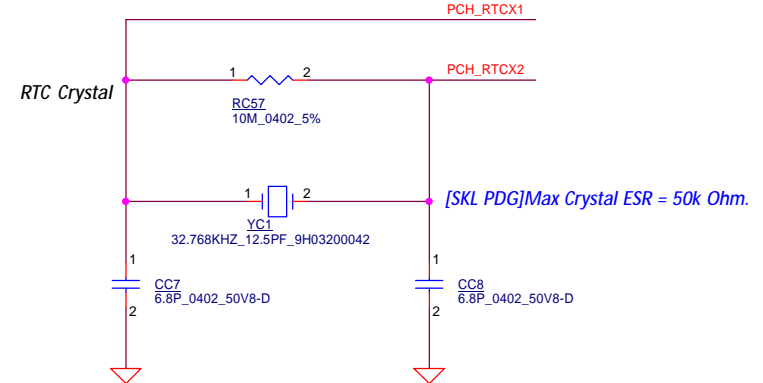


| Signal | Pin | Component |
|---------|------|--------------------|
| M.2 SSD | [42] | CLK_PCIE_SSD# |
| | [42] | CLK_PCIE_SSD |
| | [42] | CLKREQ_PCIE1_SSD |
| WLAN | [48] | CLK_PCIE_WLAN# |
| | [48] | CLK_PCIE_WLAN |
| | [48] | CLKREQ_PCIE2_WLAN# |
| LAN | [46] | CLK_PCIE_LAN# |
| | [46] | CLK_PCIE_LAN |
| | [46] | CLKREQ_PCIE3_LAN# |
| VGA | [25] | CLK_PCIE_VGA# |
| | [25] | CLK_PCIE_VGA |
| | [25] | CLKREQ_PCIE4_VGA# |
| CR | [49] | CLK_PCIE_CR# |
| | [49] | CLK_PCIE_CR |
| | [49] | CLKREQ_PCIE5_CR# |

[SKL PDG] External pull-up resistor required if used for CLKREQ# functionality.

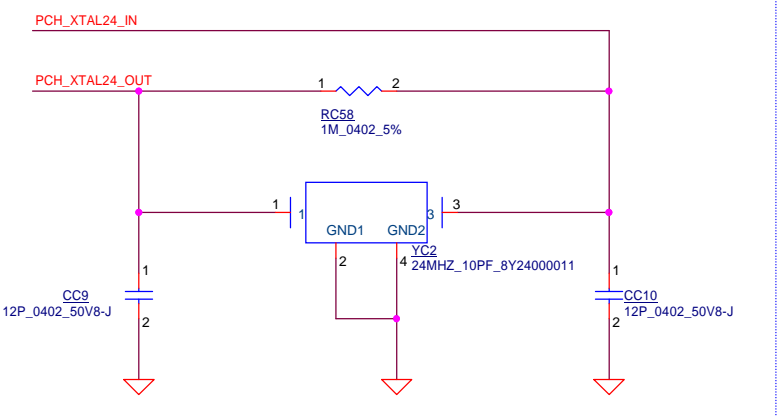


[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on opposite side of MCP for temp influence
4.The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.



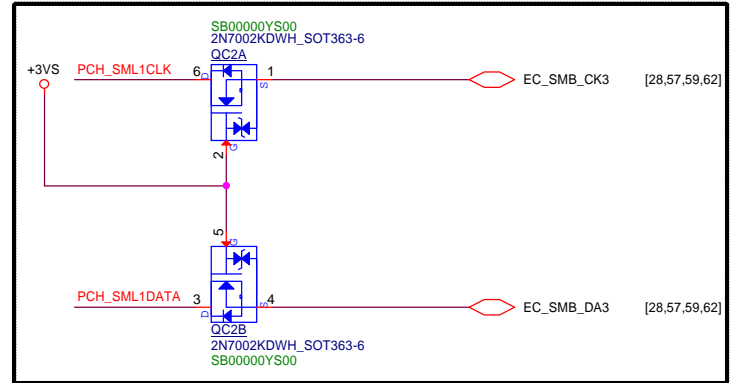
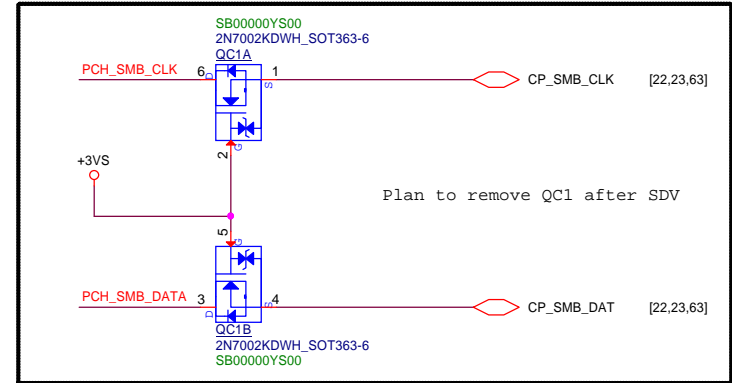
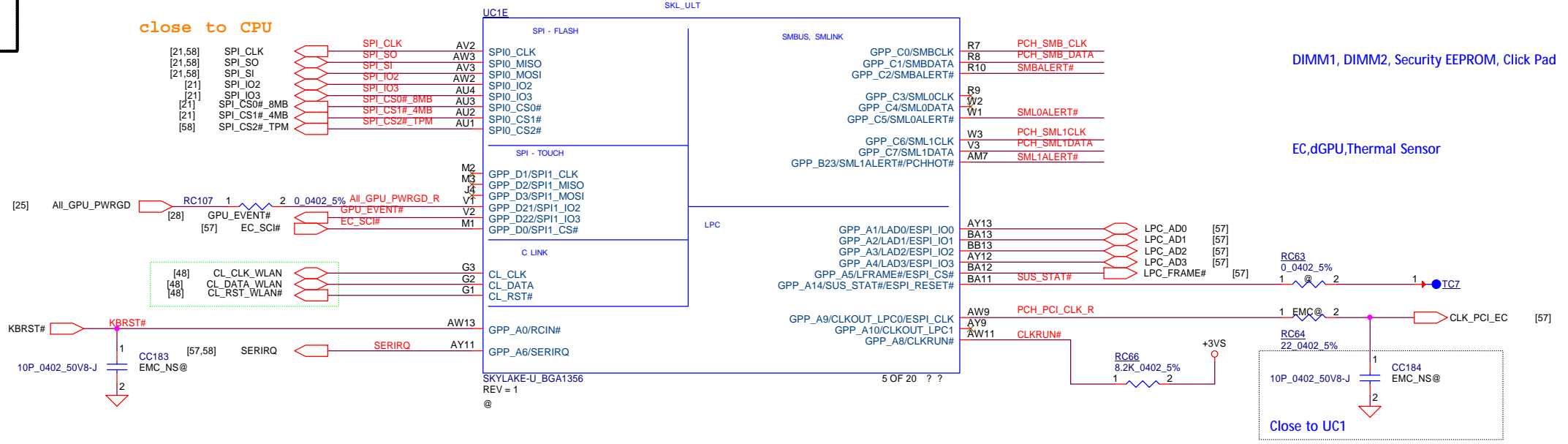
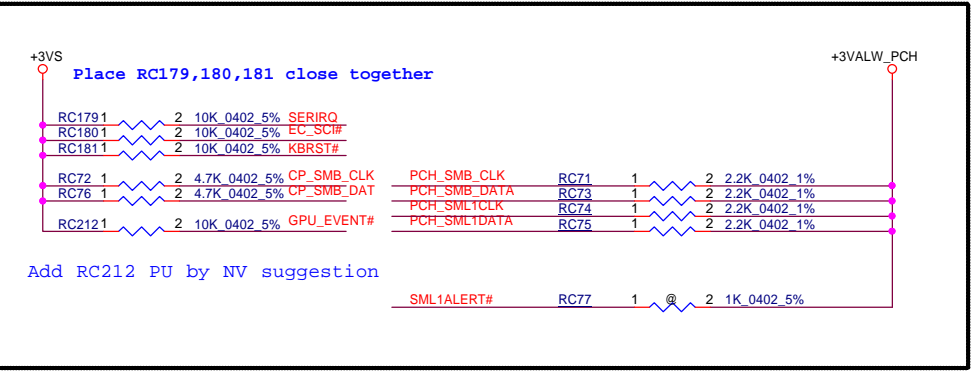
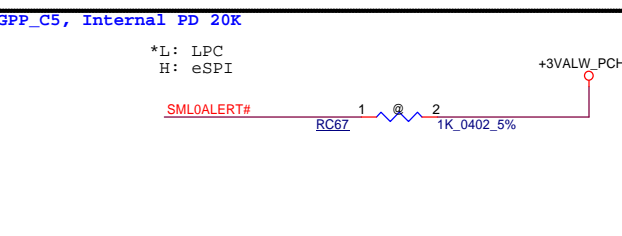
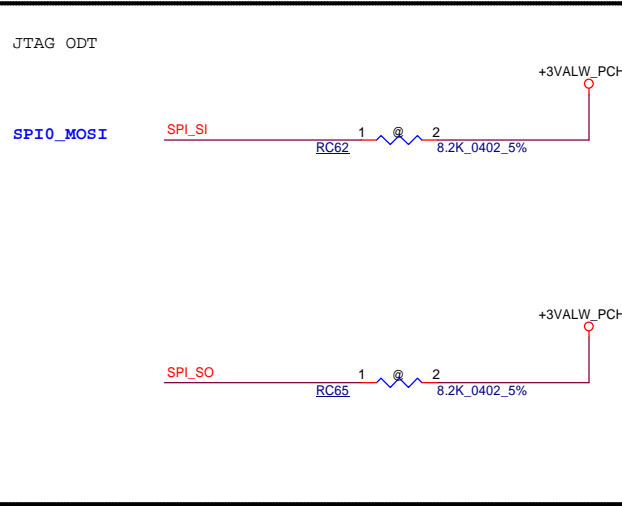
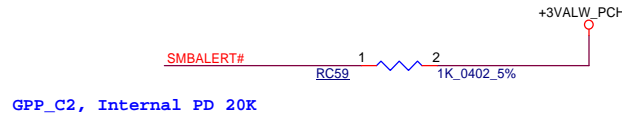
20160127
Change CC7/CC8 to 6.8p by vander suggestion

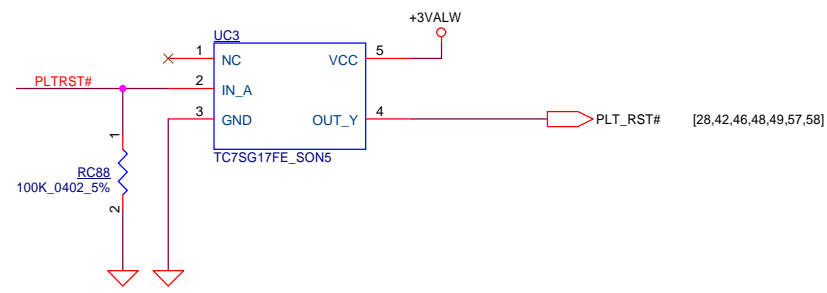
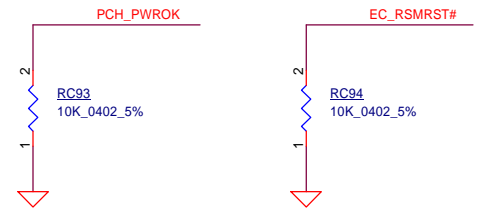
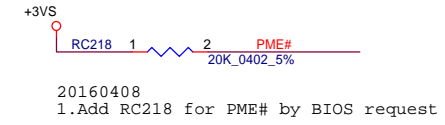
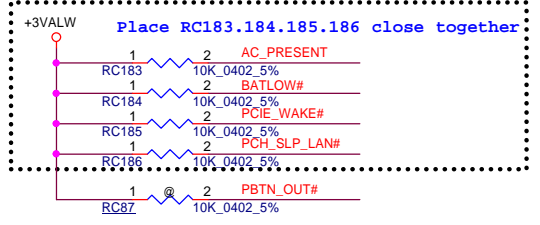
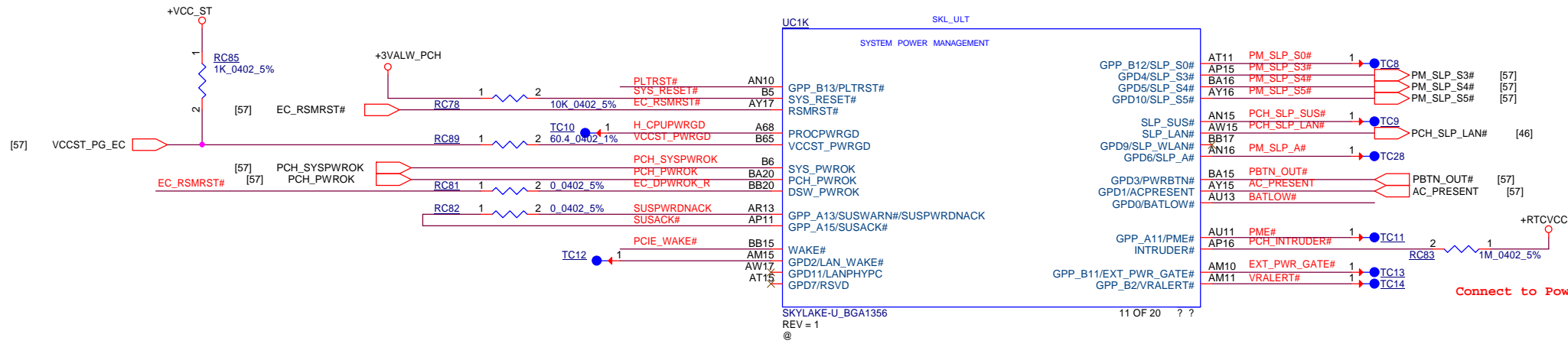
[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)




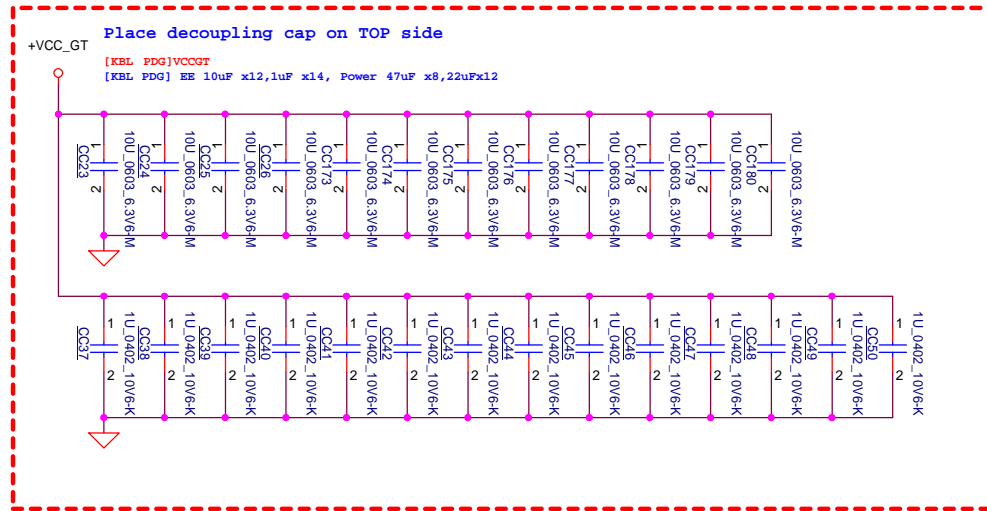
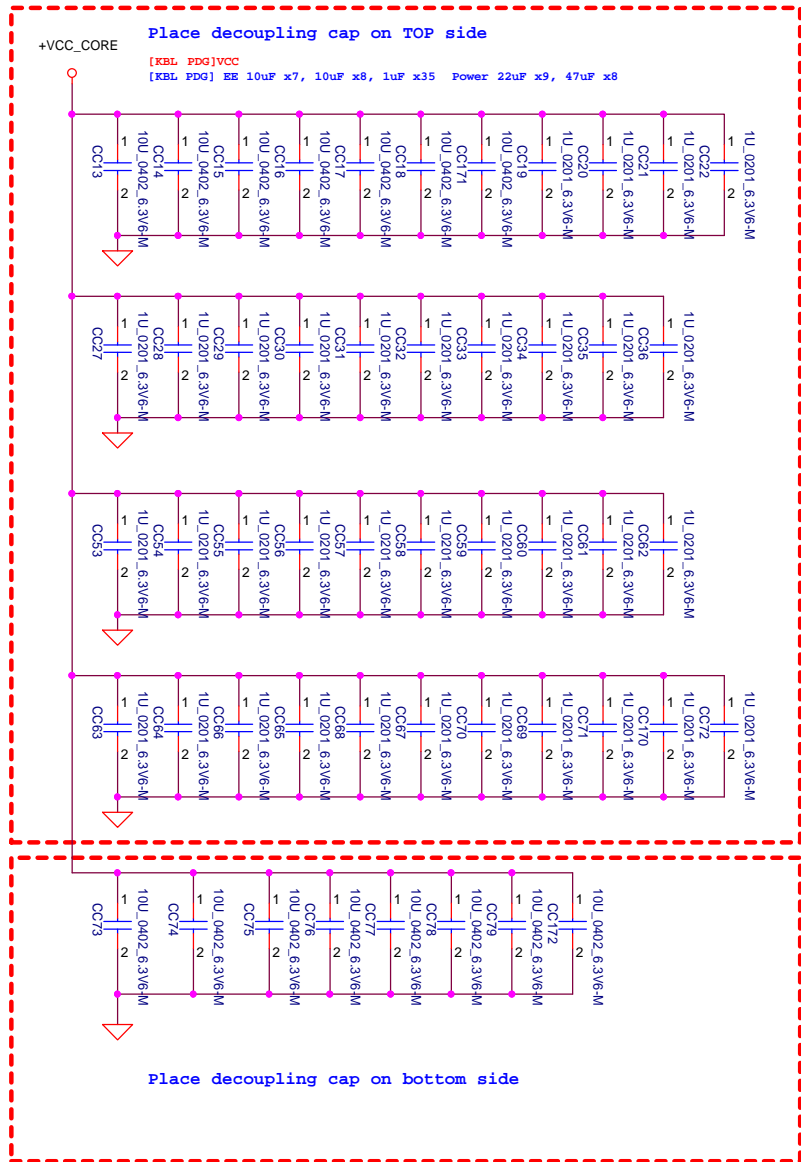
Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
 *H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



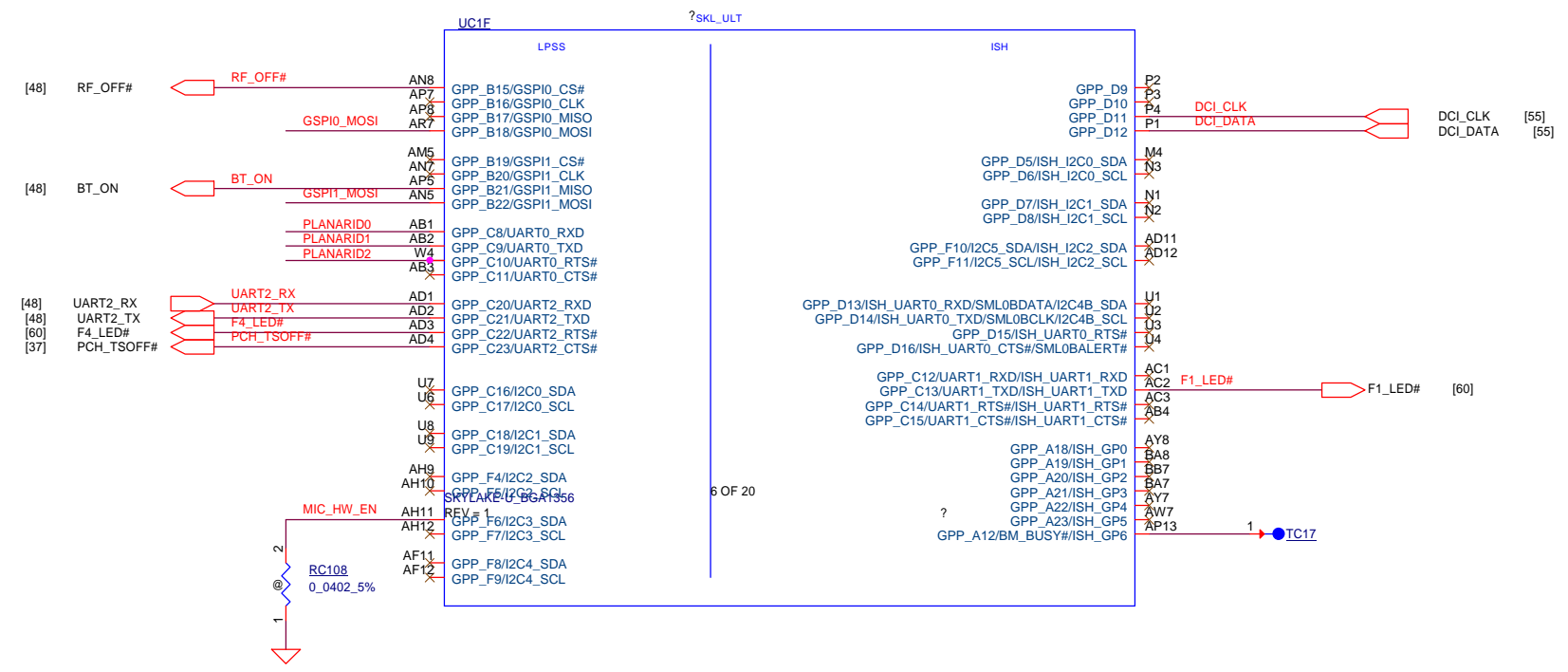
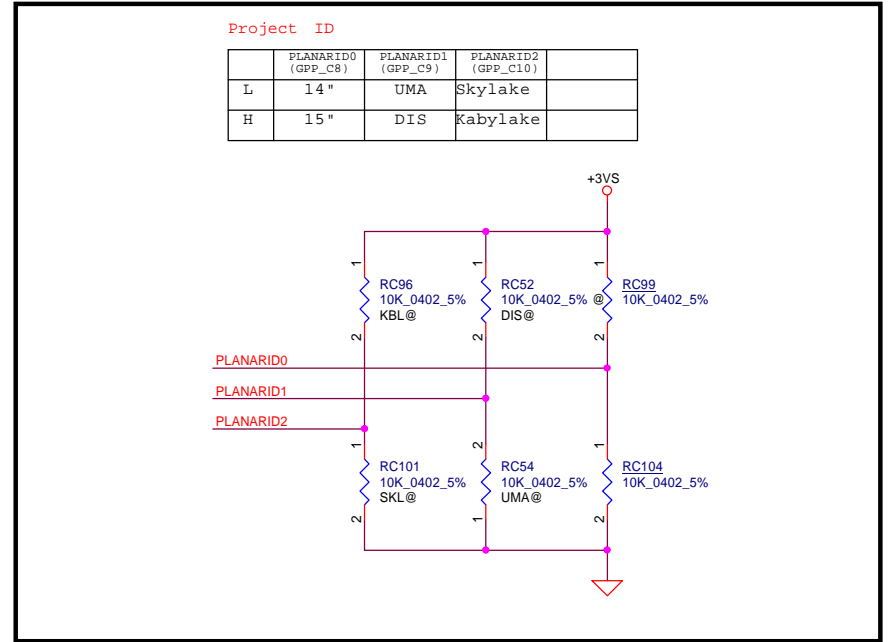
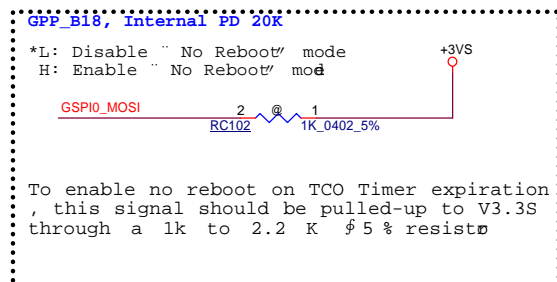
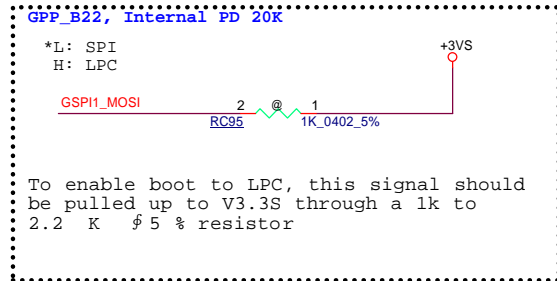


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| Date: | Thursday, August 25, 2016 | Sheet | 12 of 82 |



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| | | | | Sheet | 13 of 82 |
| | | | | Rev | 2.0 |

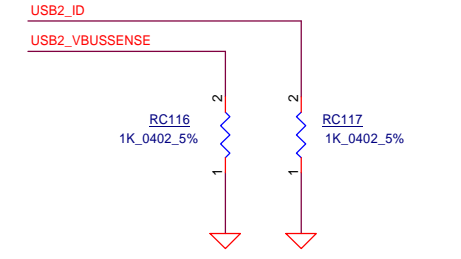
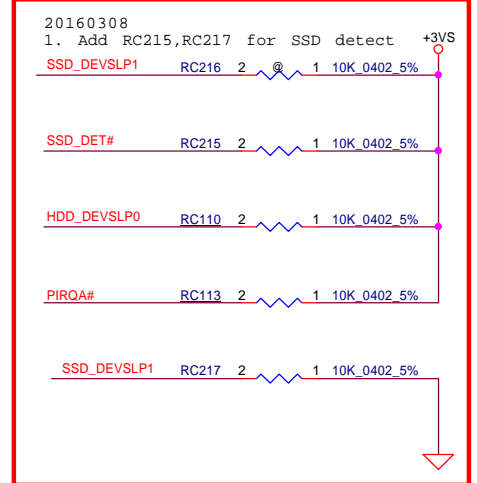
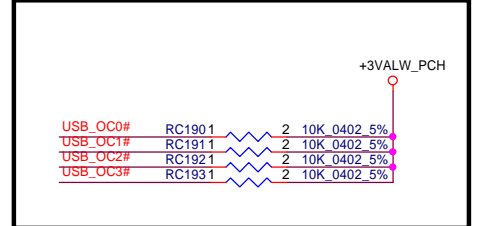




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| USB_OC# | USB Port Number |
|----------|-----------------|
| USB_OC0# | Reserve |
| USB_OC1# | Port2 |
| USB_OC2# | Port3 |
| USB_OC3# | Port4 |



TYPE C

On Board (Left)

On Board (Right-Front)

TYPE C

On Board (AOU)

On Board (Right-Back)

On Board (Right-Front)

Touch Panel

BT

CAMERA

IR CAMERA

FPR

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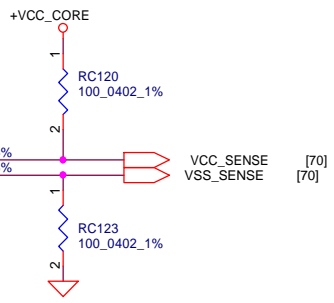
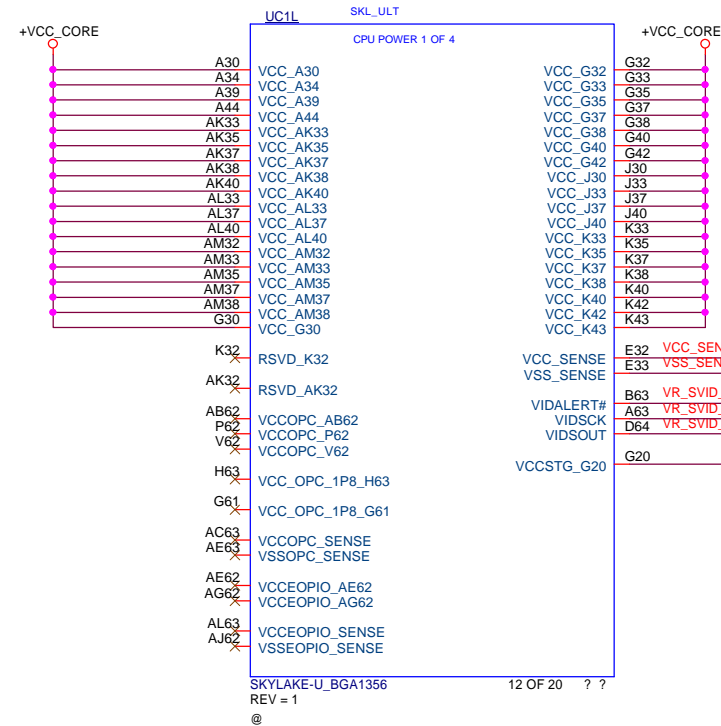
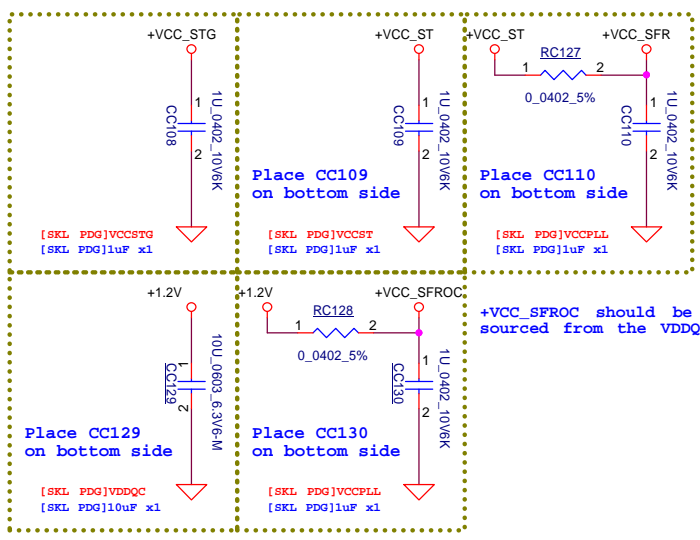
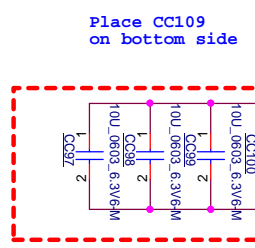
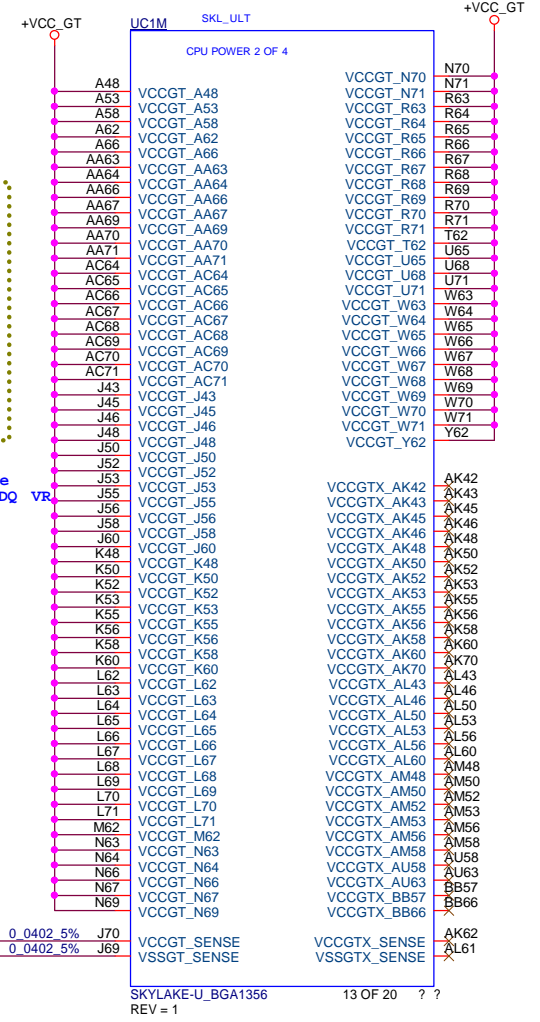
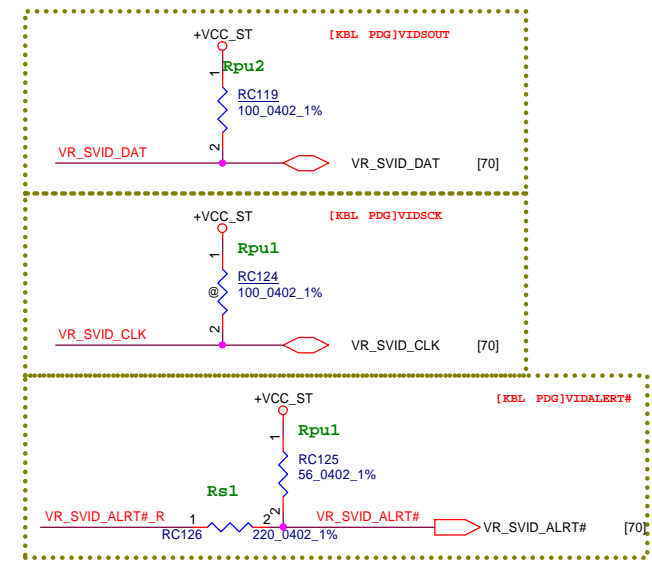
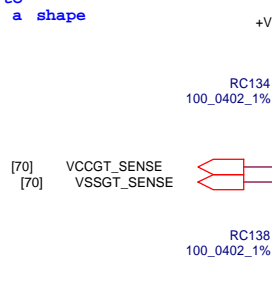
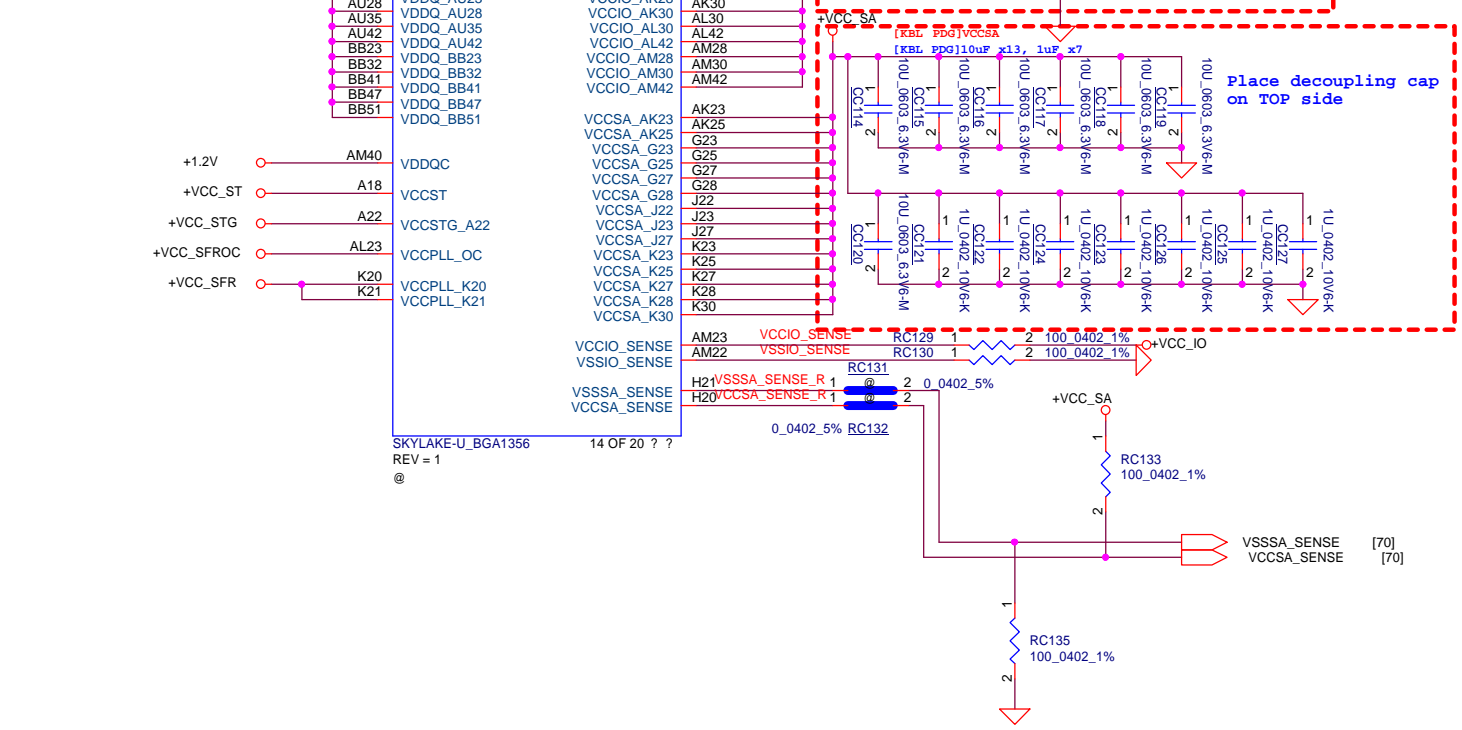


Table 10-10. SVID Bus Routing Guidelines

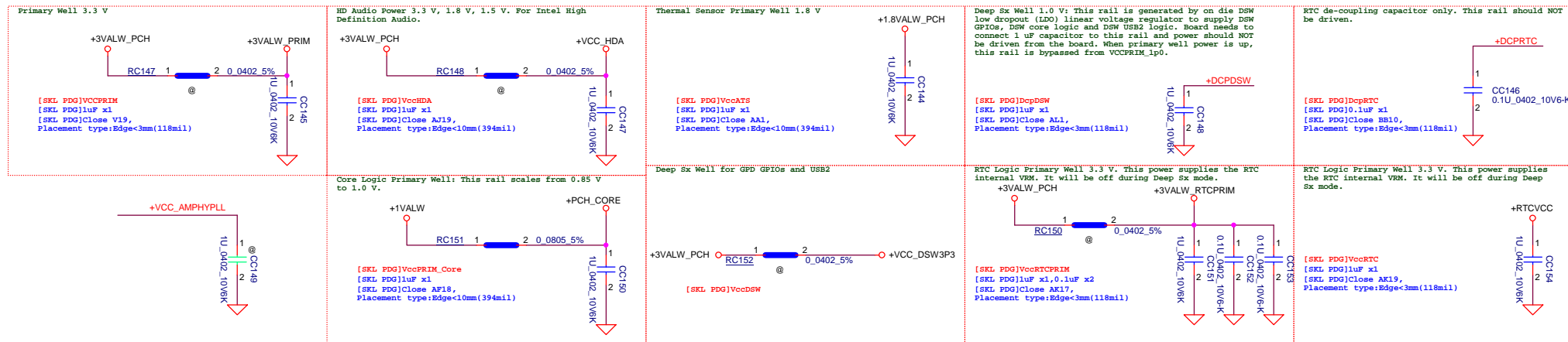
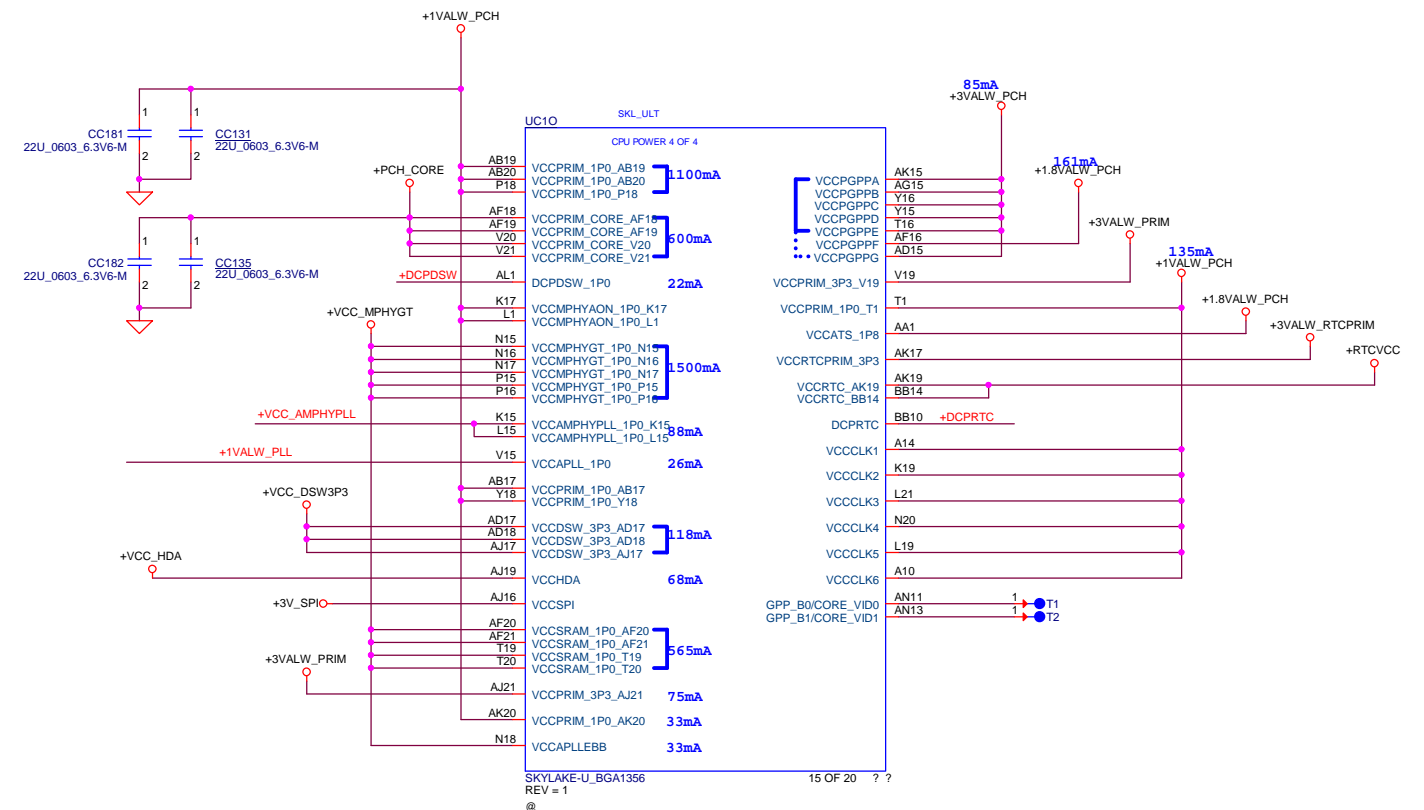
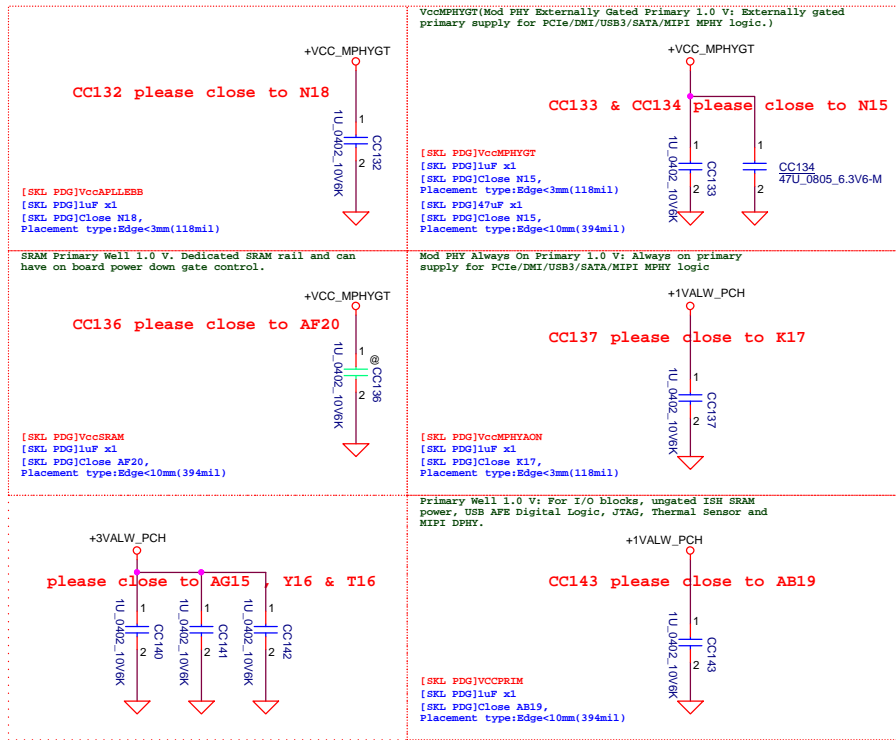
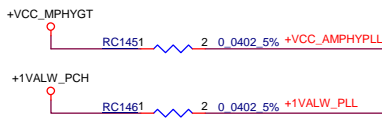
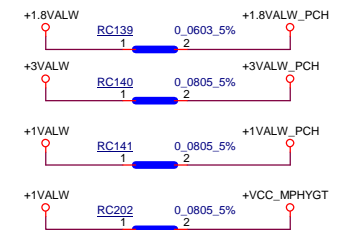
| Signal | W1 [inches] | W2 [inches] | W3/4/5 [inches] | W2+W3+W4+W5 [inches] | WS1 [inches] | WS2 [inches] | R _{P1} [Ω] | R _{P2} [Ω] | R _S [Ω] | R _{S2} [Ω] | VCC _{GT} [V] |
|------------|-------------|-------------|-----------------|----------------------|--------------|--------------|---------------------|---------------------|--------------------|---------------------|-----------------------|
| VIDSOUT | | | | | | | 100 | 100 | 0 | 10 | 1.0 |
| VIDSCK | 0.5-3 | 1-15 | 0.5-4 | 3-17 | <0.1 | <0.1 | Empty | 45 | 0 | 50 | |
| VIDALERT # | | | | | | | 55 | Empty | 220 | 0 | |

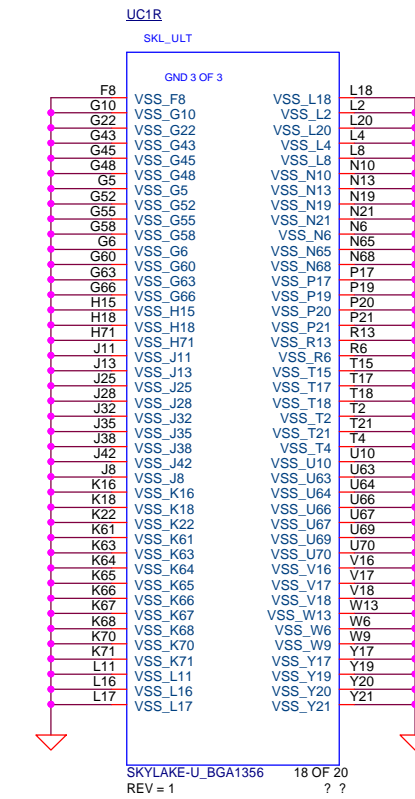
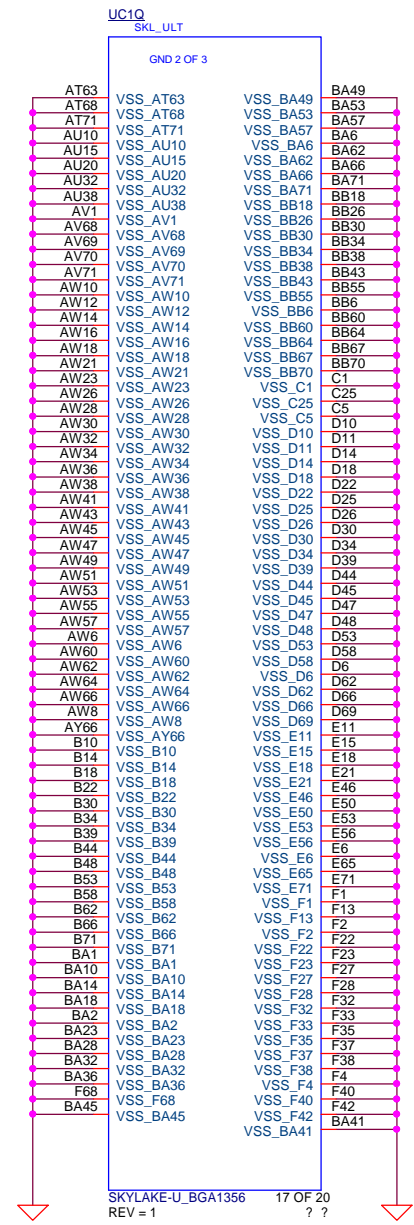
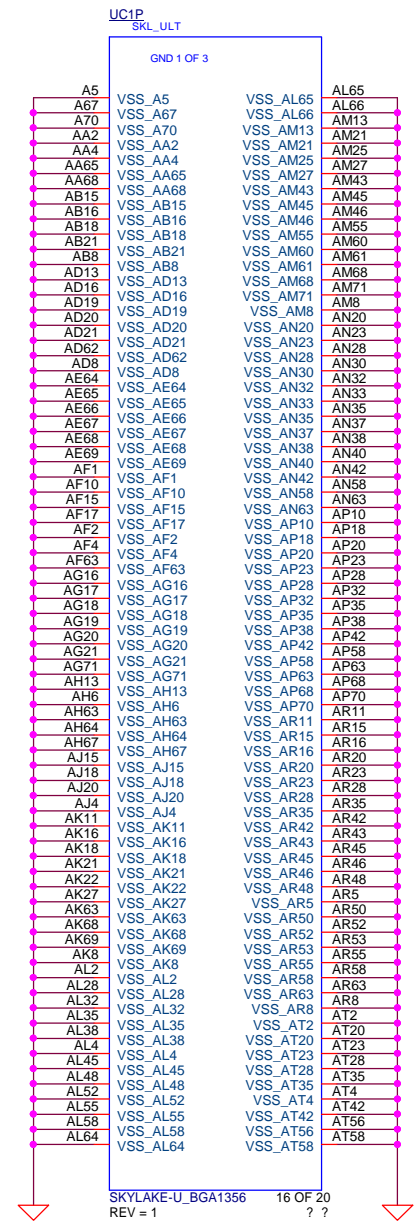


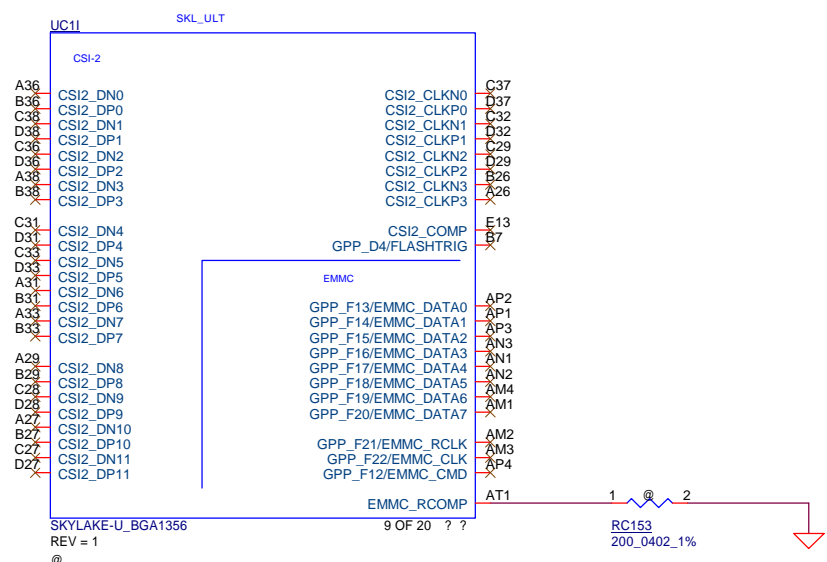
Preferred to place the 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape




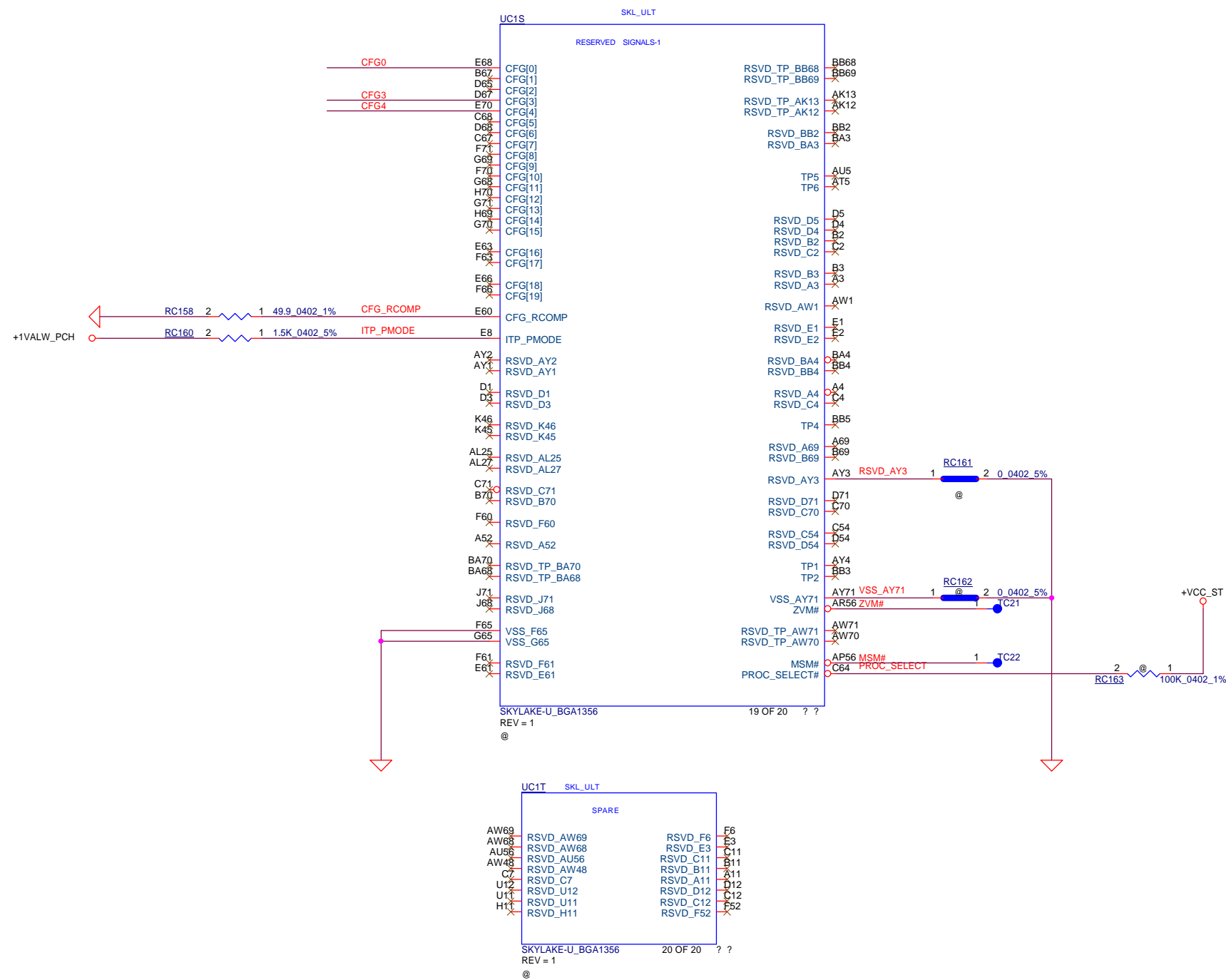
Reserve for Sense Resistor



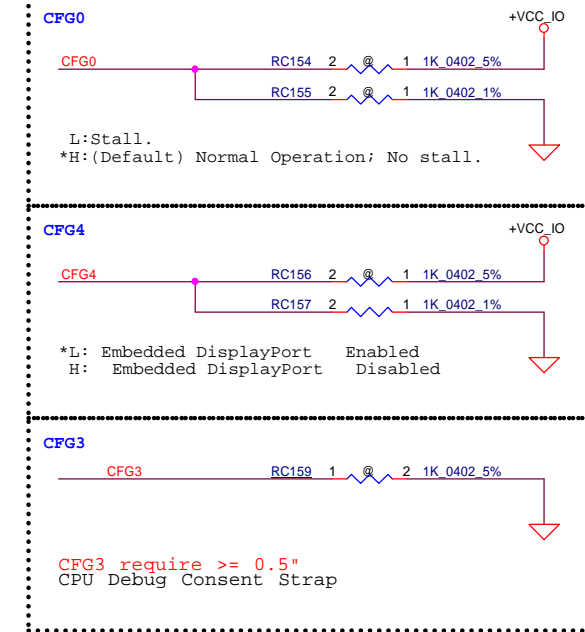




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| | | | | Document Number KENOBI |
| | | | | Rev 2.0 |
| | | | | Date: Thursday, August 25, 2016 |
| | | | | Sheet 19 of 82 |

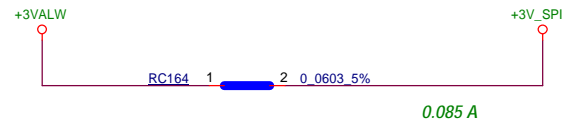


[SKL_EDS]

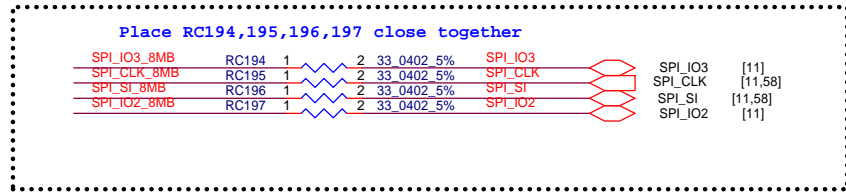
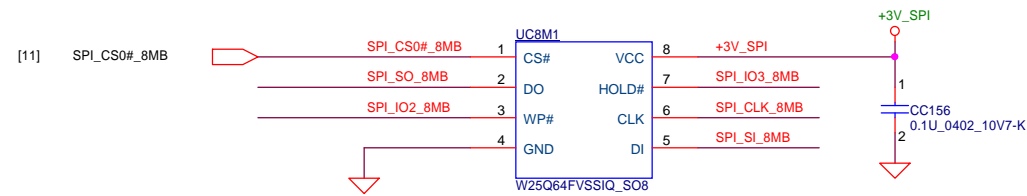


TABLE

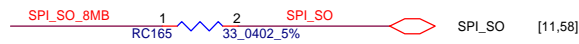
| |
|---|
| <p>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall</p> |
| <p>CFG4 : eDP Enable 1 : Disabled 0 : Enabled</p> |



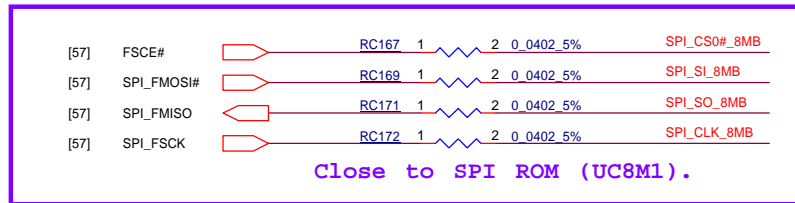
4MB(32Mb) Reserve



Near SPI ROM

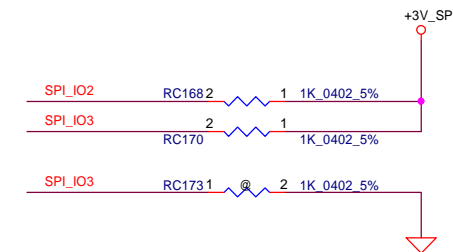
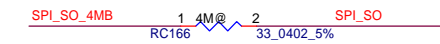
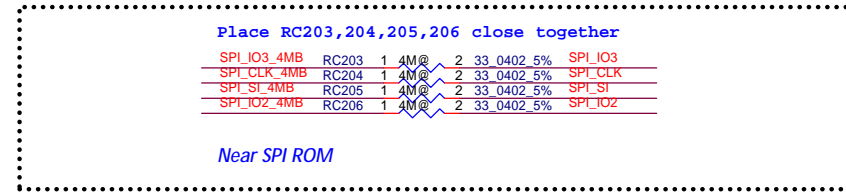
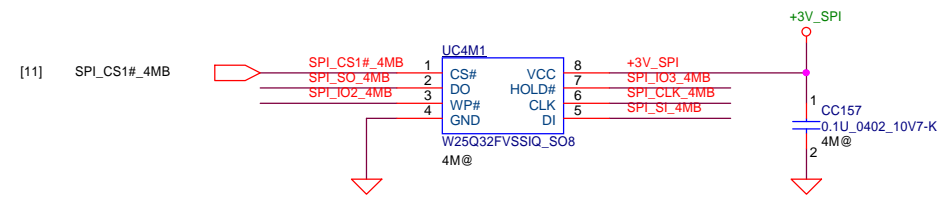


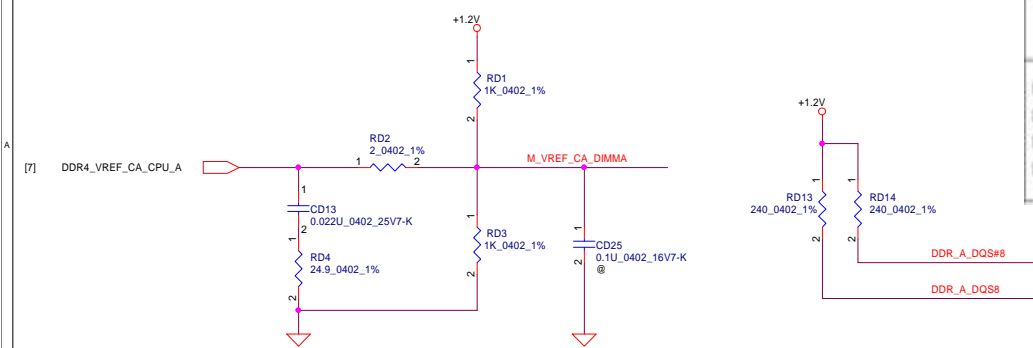
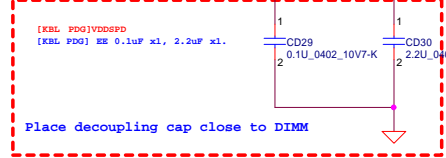
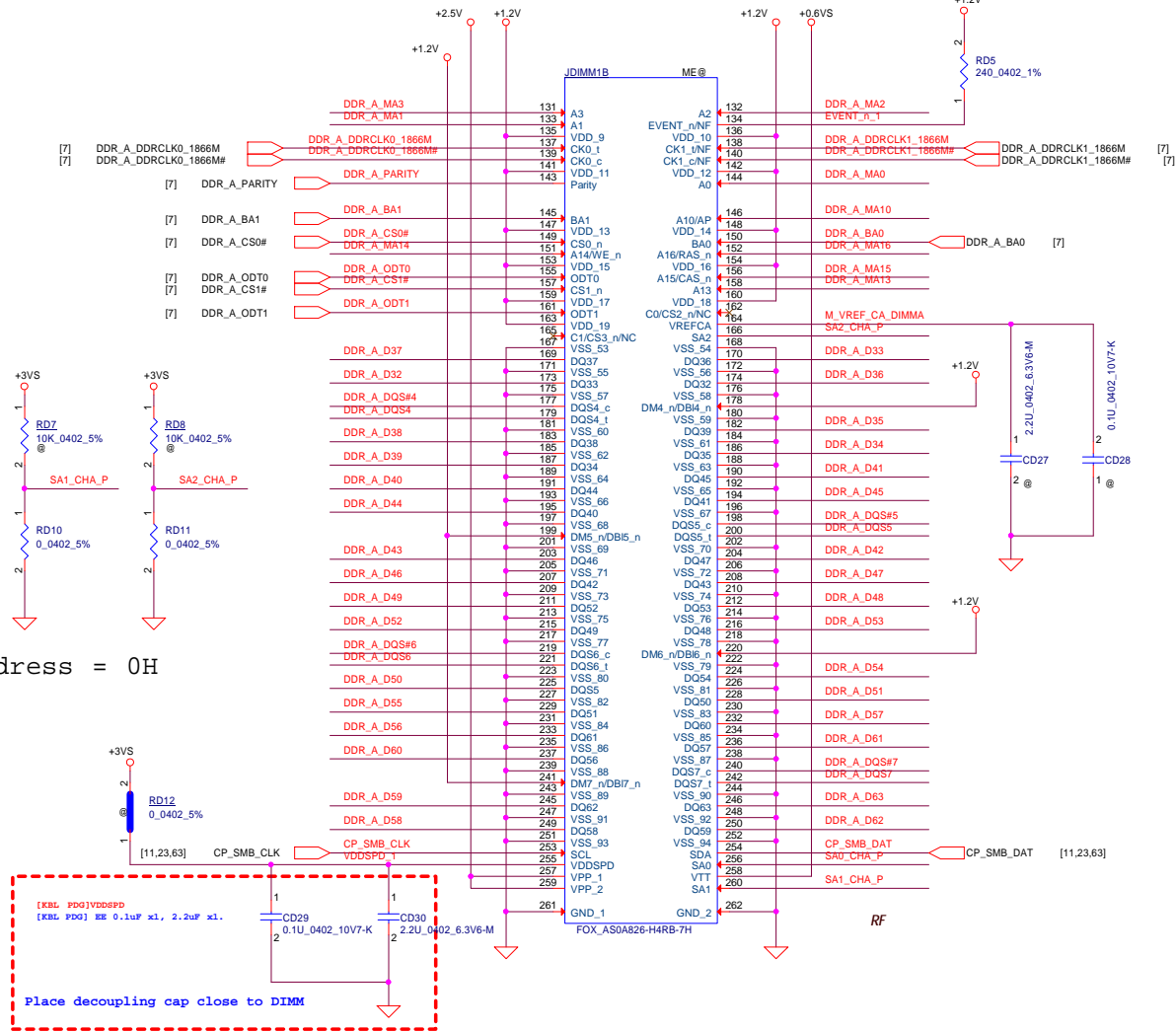
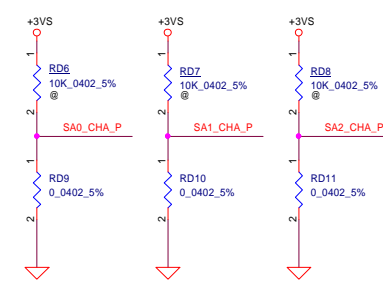
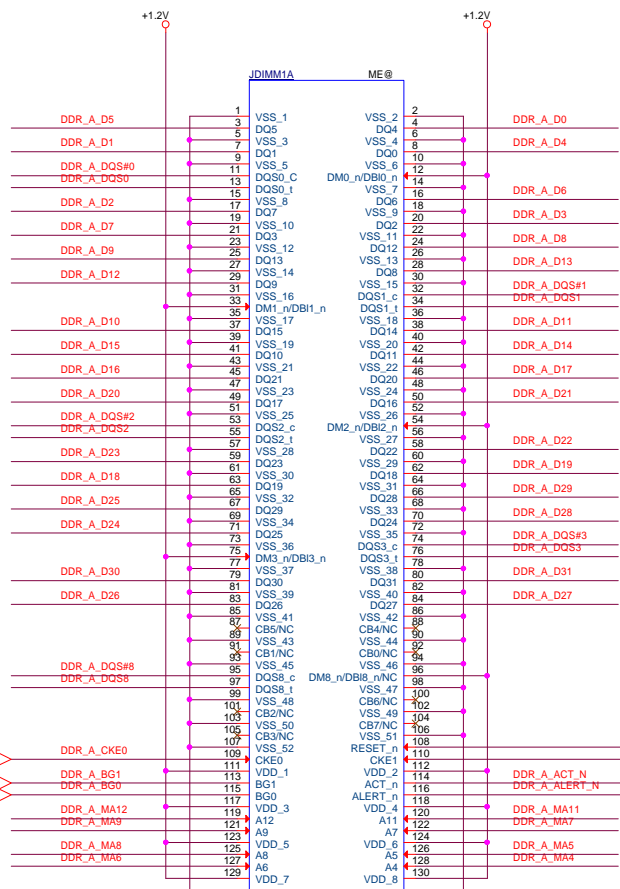
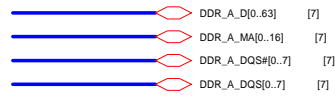
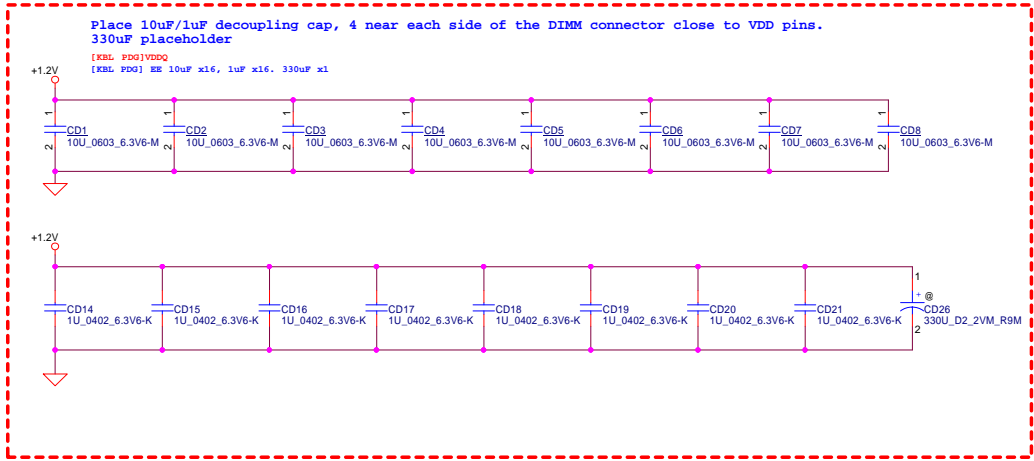
Mirror Code



8MB(64Mb)

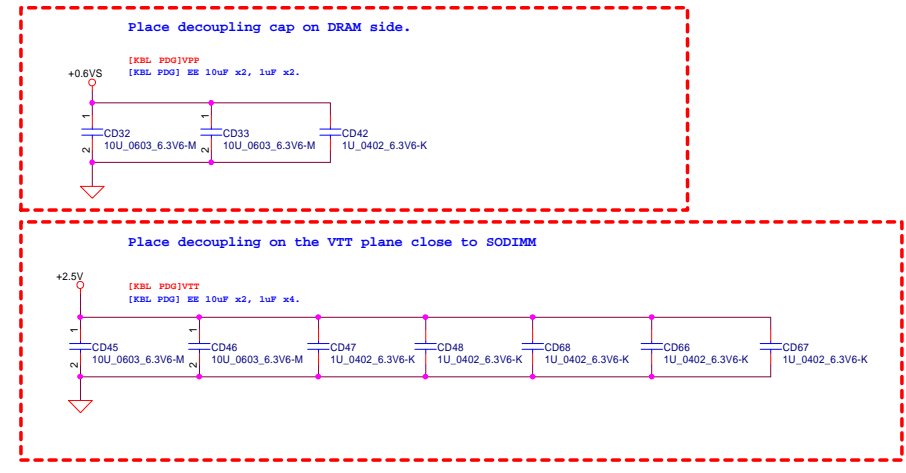
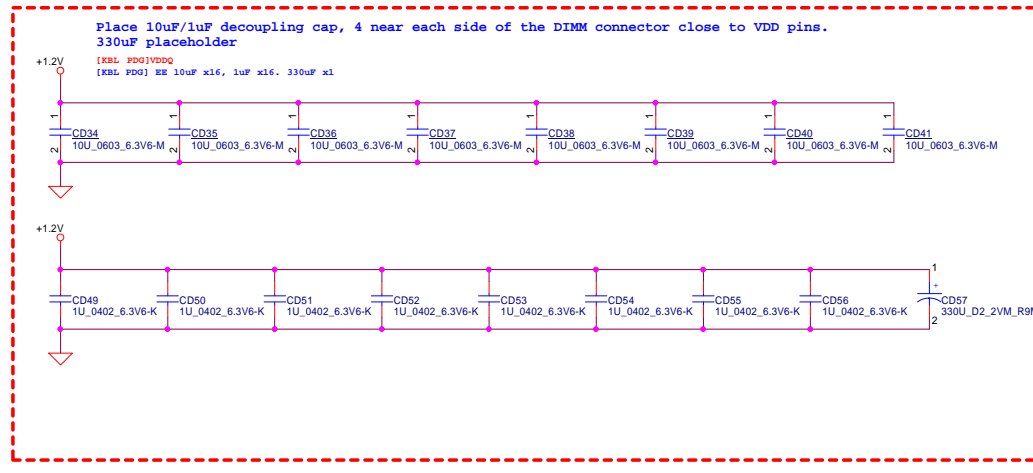
[SKL]SPI0_CS0#: SPI FLASH
 SPI0_CS1#: SPI FLASH
 SPI0_CS2#: SPI TPM





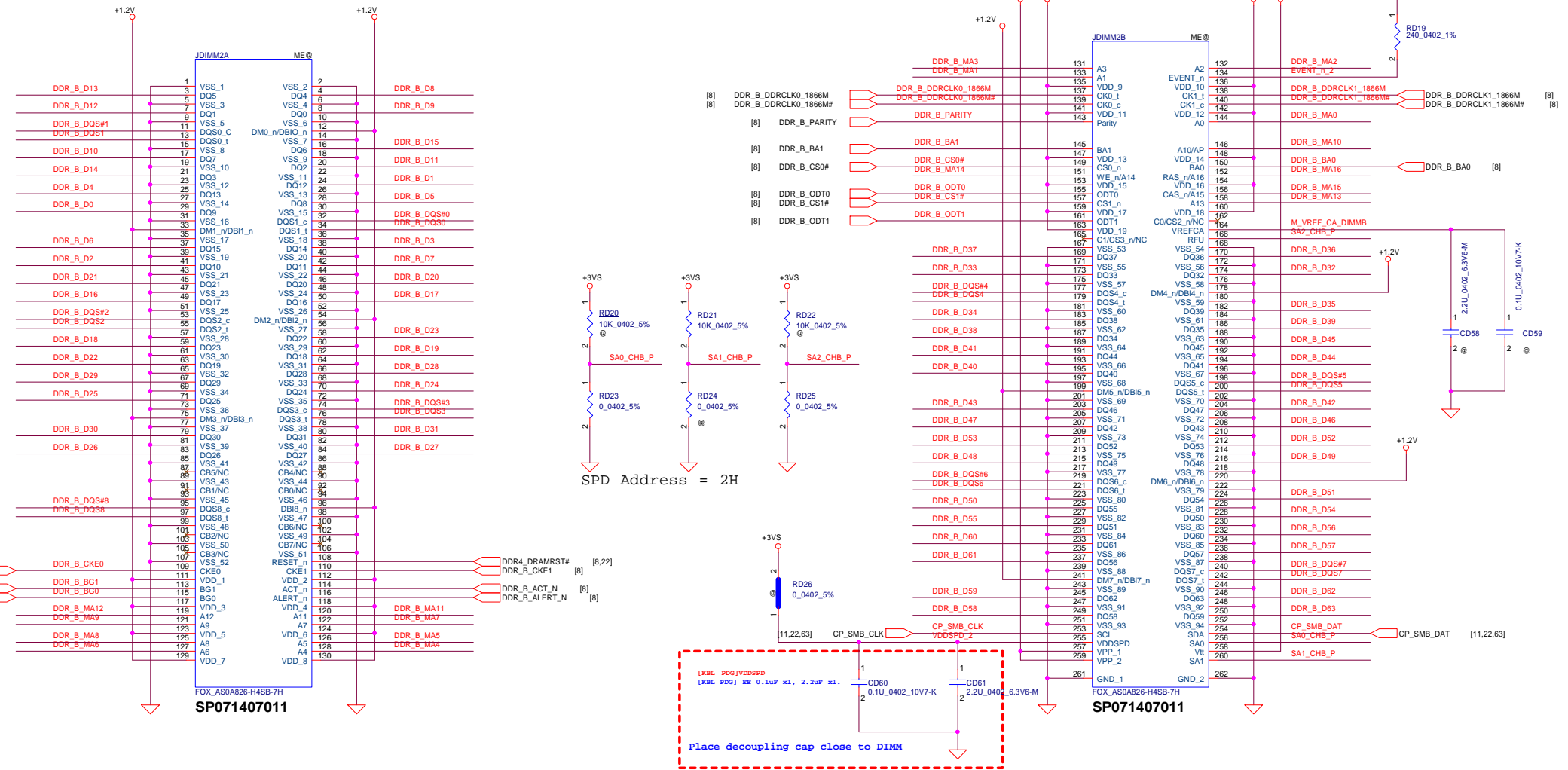
| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|--|---|------|-------------|-----------|--|
| DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0] | Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions. | I/O | DDR4/-R5 | Dif | The 9th signals[8] are applicable for UDIMM/SODIM module with ECC in S and H-processor line processors |

| | | | |
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| Size | Document Number | Date | Rev |
| Custom | Thursday, August 25, 2016 | Sheet 22 of 82 | 2.0 |



Layout Node:
Place Close DIMMs

- DDR_B_DQ[0..63] [8]
- DDR_B_MA[0..16] [8]
- DDR_B_DQS[0..7] [8]
- DDR_B_DQS[0..7] [8]



| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|----------------|--|------|-------------|-----------|--|
| DDR0_DQSP[8:0] | Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions. | I/O | DDR4/R5 | DIFF | The 9th signals(8) are applicable for UDIMM/SODIM module with ECC in S and H-processor line processors |
| DDR0_DQSN[8:0] | | | | | |
| DDR1_DQSP[8:0] | | | | | |
| DDR1_DQSN[8:0] | | | | | |

| Resistor Values | Pull-up to +3VGS | Pull-down to Gnd |
|-----------------|------------------|------------------|
| 4.99K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 24.9K | 1100 | 0100 |
| 30.1K | 1101 | 0101 |
| 34.8K | 1110 | 0110 |
| 45.3K | 1111 | 0111 |

| DEVID_SEL | |
|-----------|-----------|
| 0 | (Default) |
| 1 | |

| SMBUS_ALT_ADDR | |
|----------------|------------------------|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

| PCIE_CFG | |
|----------|-----------|
| 0 | (Default) |
| 1 | |


| VGA_DEVICE | |
|------------|-----------------------------|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|---|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VS_AON | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SI | +3VS_AON | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_AON | DEVID_SEL | PCIE_CFG | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_AON | Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up) | | | |
| STRAP1 | +3VS_AON | Reserved(keep pull-up and pull-down footprint and not stuff by default) | | | |
| STRAP2 | +3VS_AON | | | | |
| STRAP3 | +3VS_AON | | | | |
| STRAP4 | +3VS_AON | | | | |

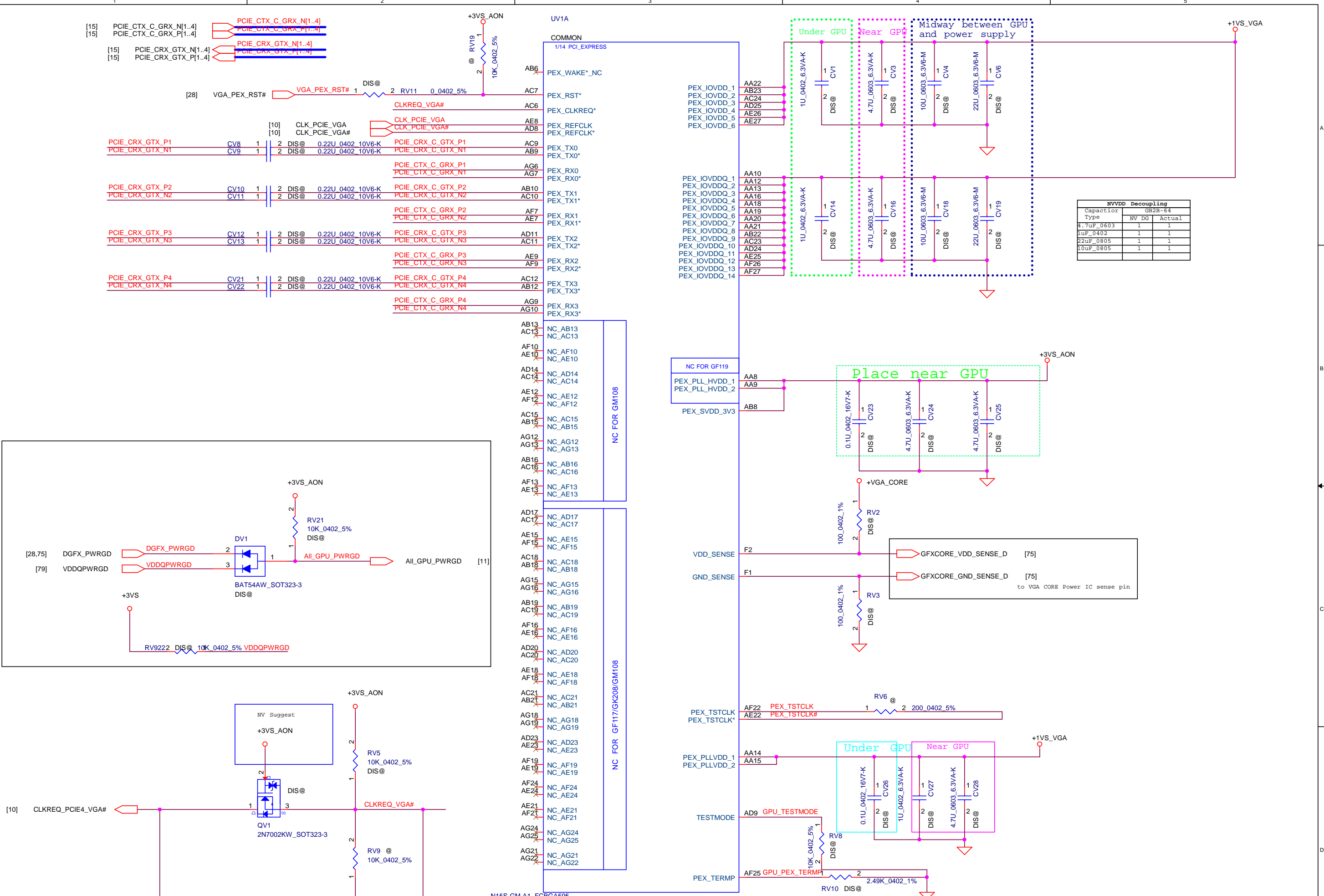
X76

| GPU | FB Memory (GDDR3) | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|----------------------|---------------------------------------|-------------------------|--------|----------|--------|--------|--------|--------|--------|
| N16S-GTR N16V-GMR | Samsung K4W4G1646E-BC1A(E-Die)256MX16 | PD 24.9K SD03424928T | PD 5K | PD 5K | PU 50K | NC | NC | NC | NC |
| | Hynix H5TC4G63CFR-N0C(C-Die)256Mx16 | PD 30.1K SD03430128T | | | | | | | |
| | Micron MT41J256M16LY-091G:N | PD 20K SD02820028T | | | | | | | |

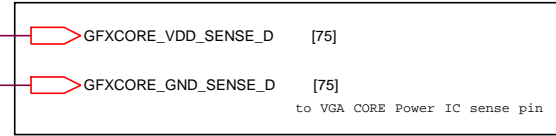
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| Title | |  |
| VGA NOTE | | |
| Size B | Document Number | Rev 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet 24 of 82 |

KENOBI

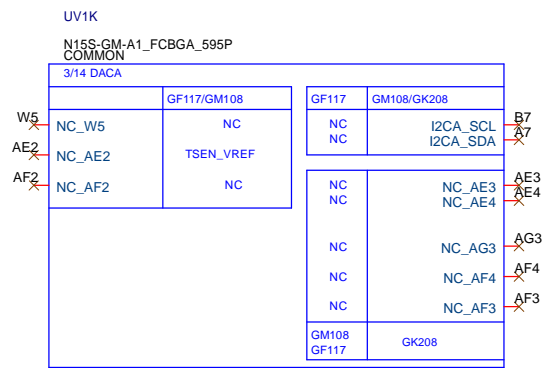


| Capacitor Type | GB2B-64 | |
|----------------|---------|--------|
| | NV DG | Actual |
| 4.7uF_0603 | 1 | 1 |
| 1uF_0402 | 1 | 1 |
| 22uF_0805 | 1 | 1 |
| 10uF_0805 | 1 | 1 |

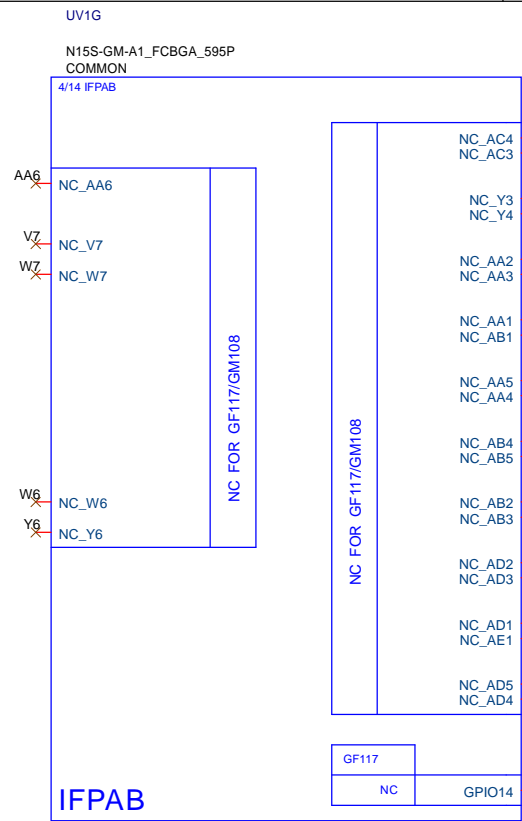


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| | | 2016/08/27 |
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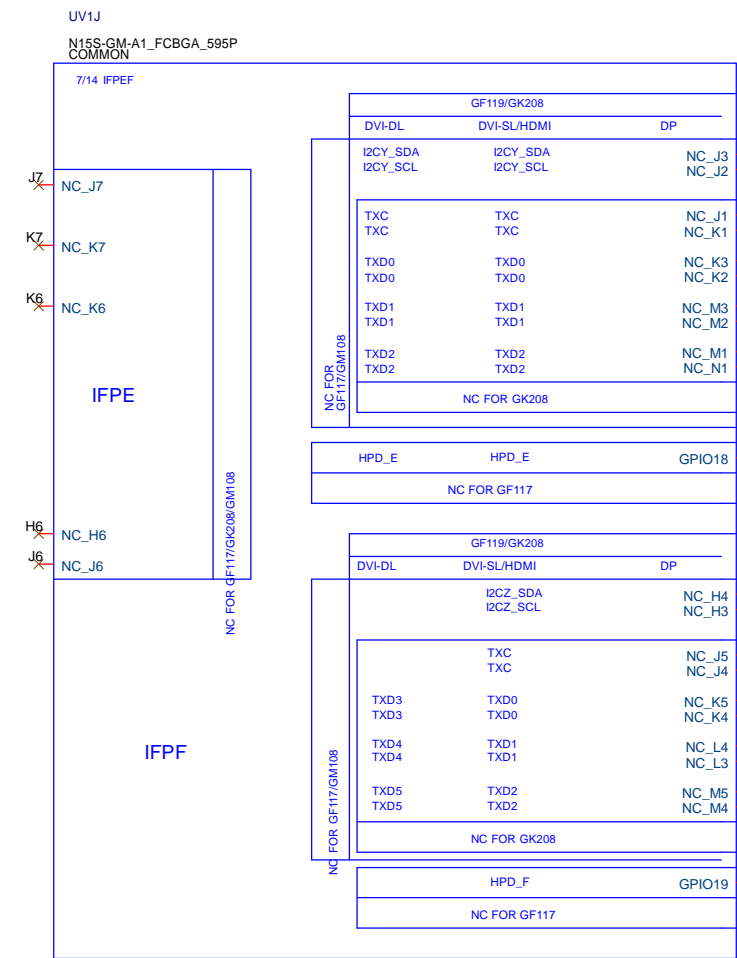
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| Title | | |
| N16S-GT PCIe | | |
| Size | Document Number | KENOBI |
| Custom | | |
| Date: | Thursday, August 25, 2016 | Sheet 25 of 82 |
| | | Rev 2.0 |



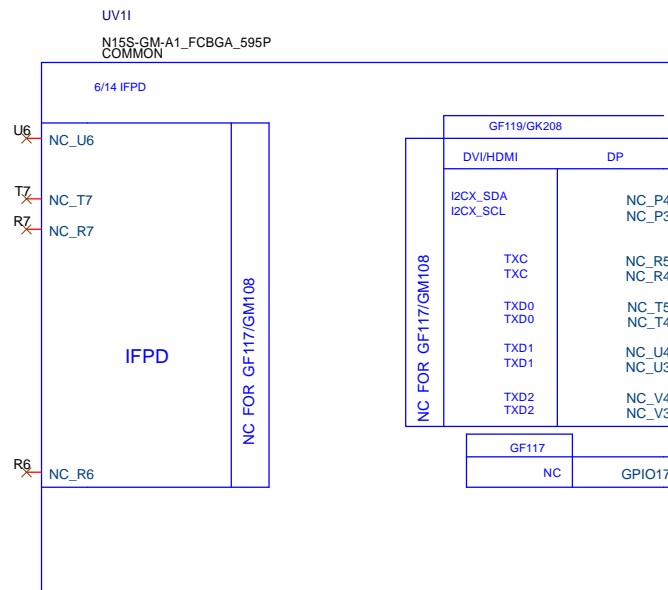
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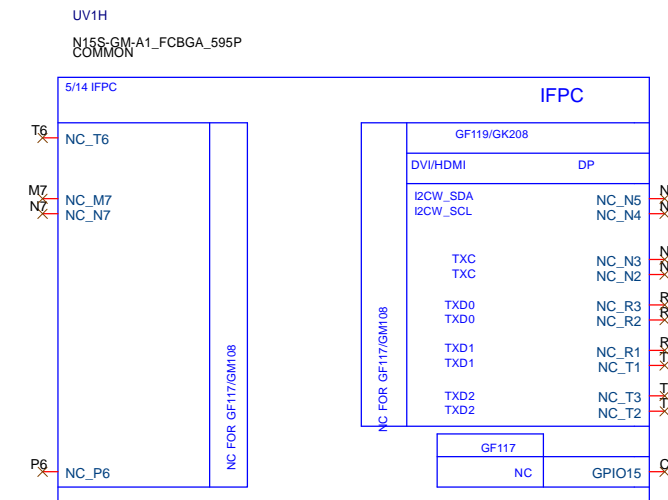
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N155-GM-A1_FCBGA595





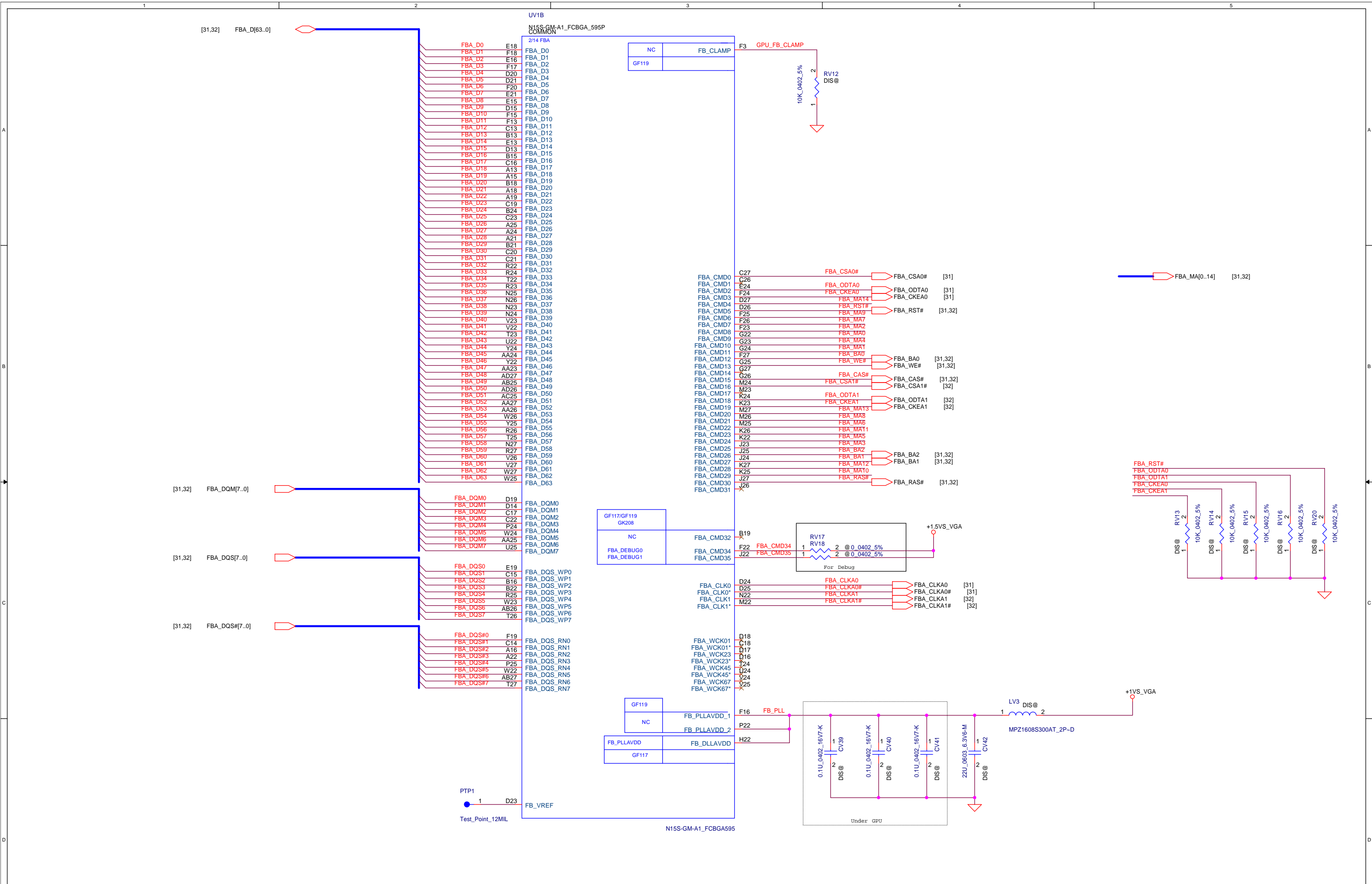
N155-GM-A1_FCBGA595



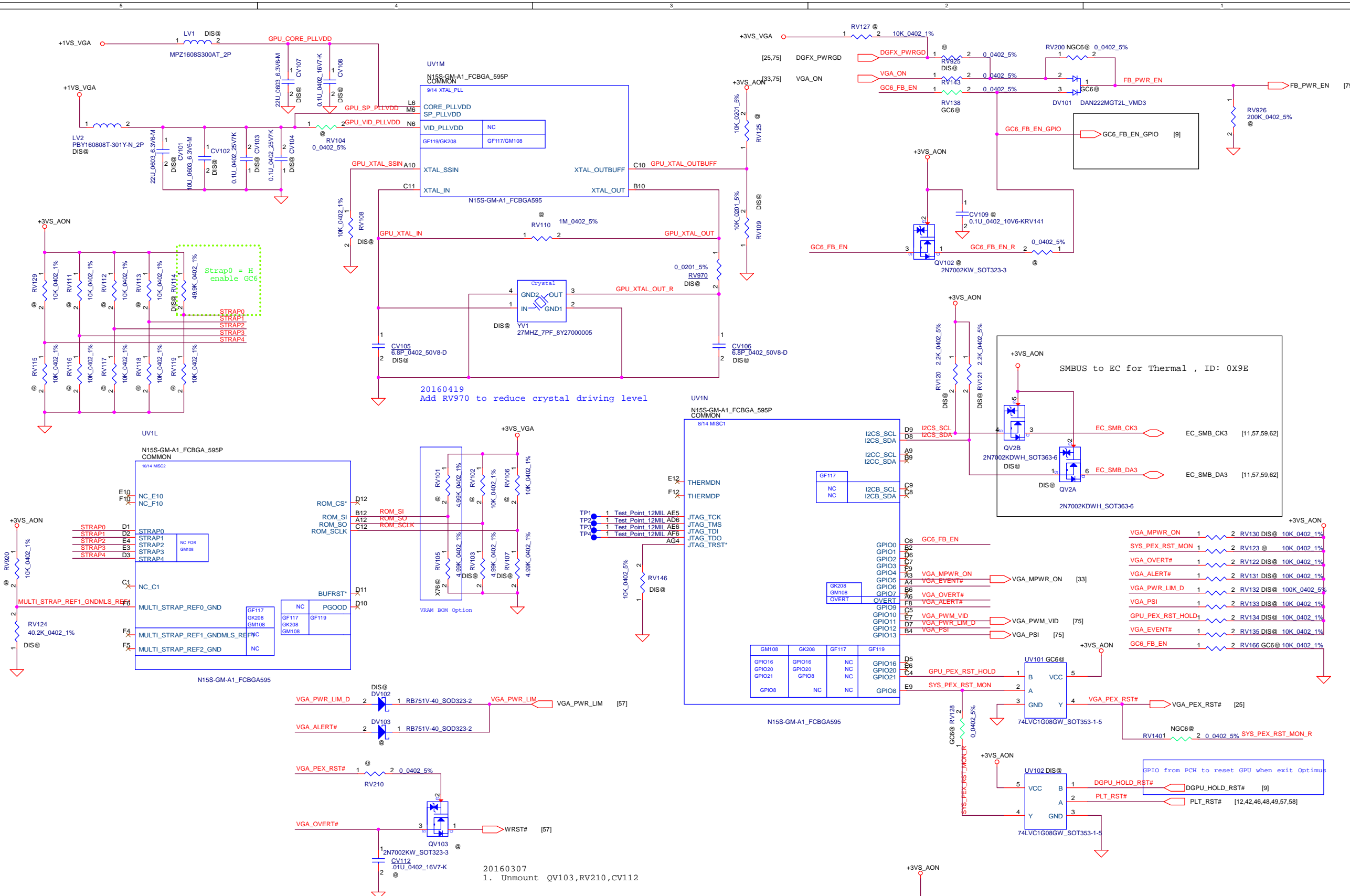
N155-GM-A1_FCBGA595

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|--|------------|------------------------------|------------|
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| Issued Date | 2015/08/28 | Deciphered Date | 2016/08/27 |
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| Size | Document Number |  |
| Custom | | |
| Date: | Thursday, August 25, 2016 | Sheet 26 of 82 |
| | | Rev 2.0 |



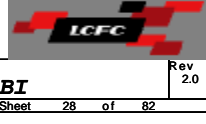
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| Issued Date | 2015/08/28 | Deciphered Date | 2016/08/27 |
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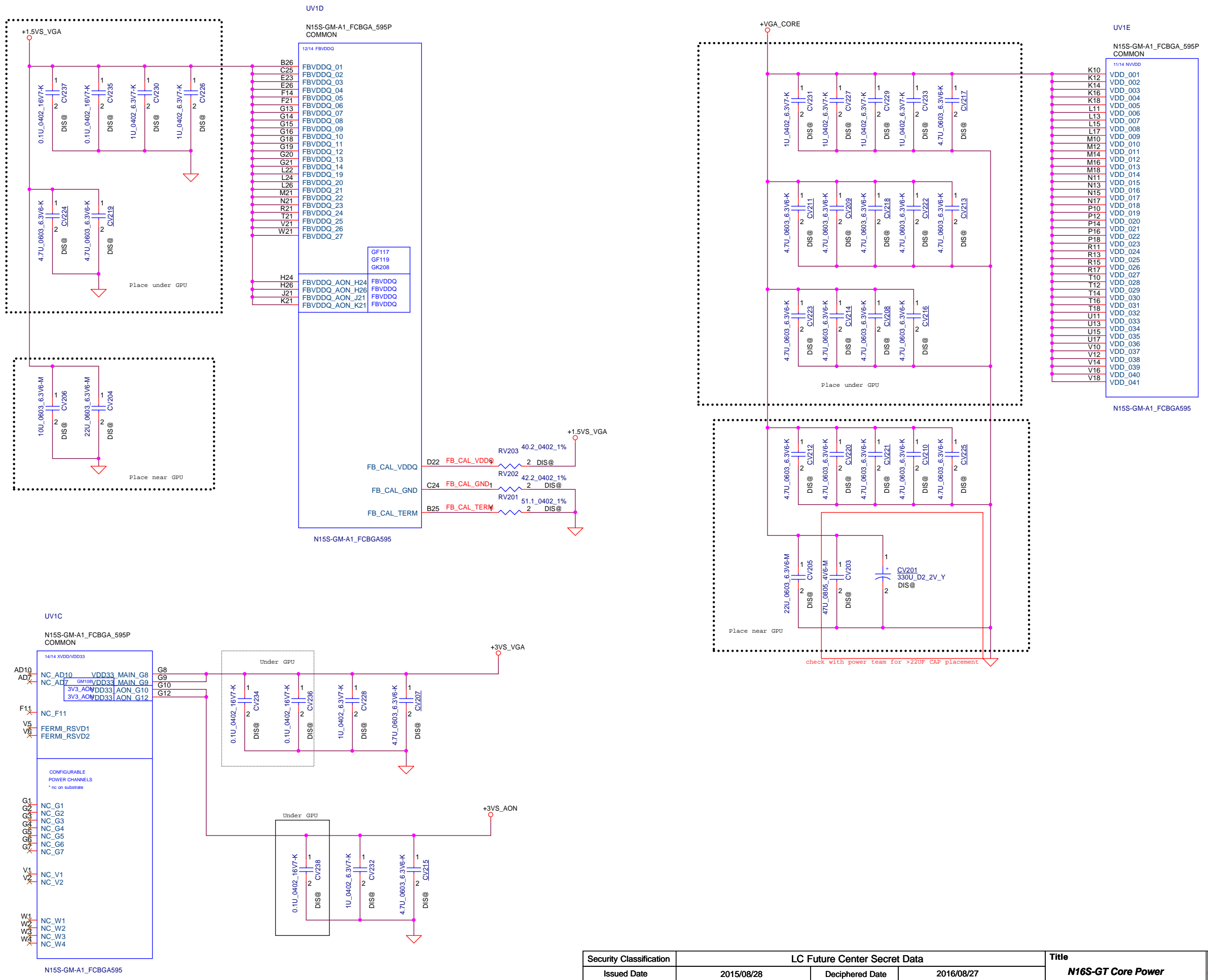


X76


| GPU | FB Memory (GDDR3) | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|----------------------|--|-------------------------|--------|----------|--------|--------|--------|--------|--------|
| N16S-GTR N16V-GMR | Samsung K4W4G1646E-BC1A(E-Die)256MX16 | PD 24.9K SD03424928T | | PD 5K | PD 5K | PU 50K | NC | NC | NC |
| | Hynix H5TC4G63CFR-N0C(C-Die)256Mx16 | PD 30.1K SD03430128T | | | | | | | |
| | Micron MT41J256M16LY-091G:N | PD 20K SD02820028T | | | | | | | |

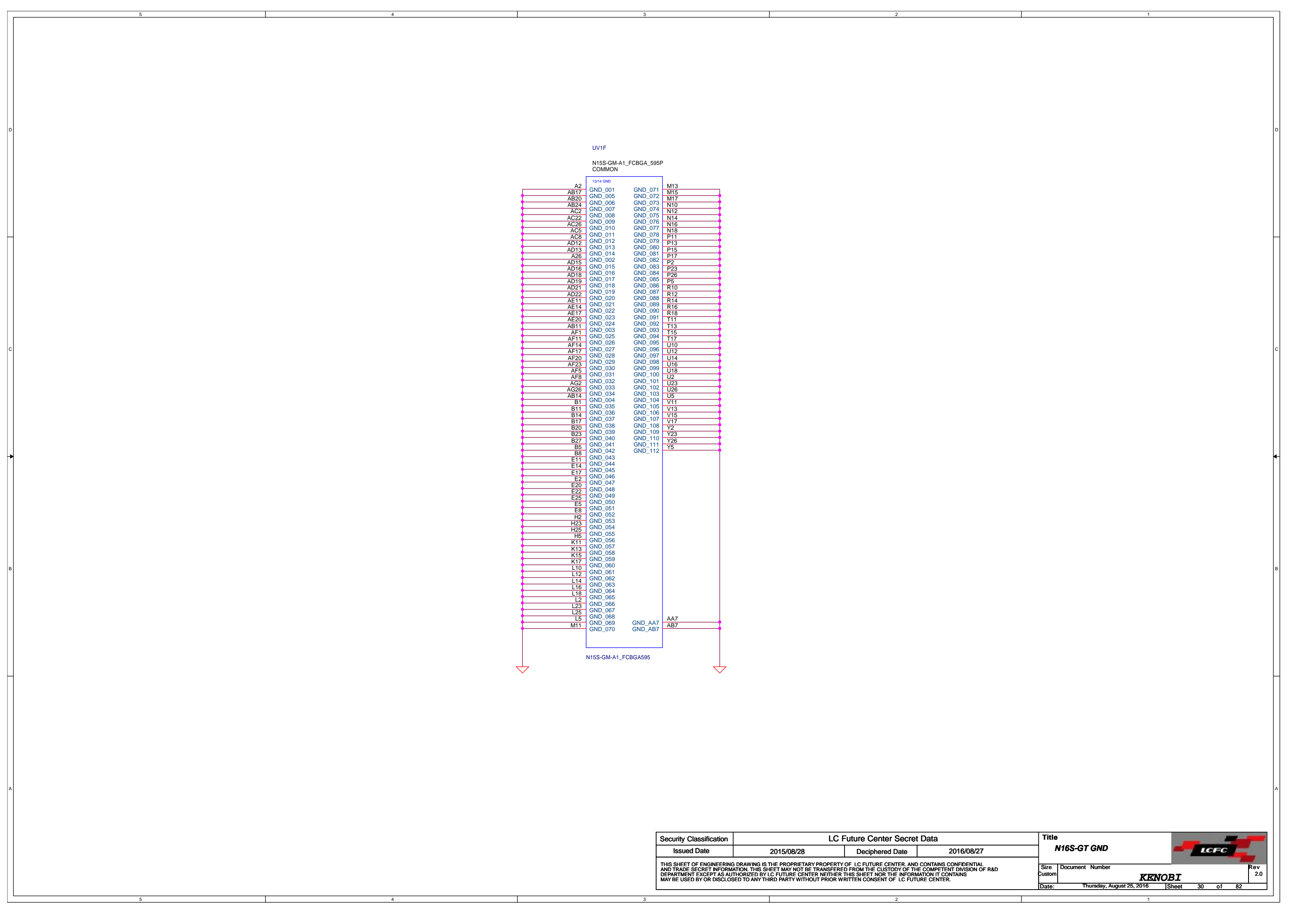
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| Date: | Thursday, August 25, 2016 | Sheet | 28 of 82 |






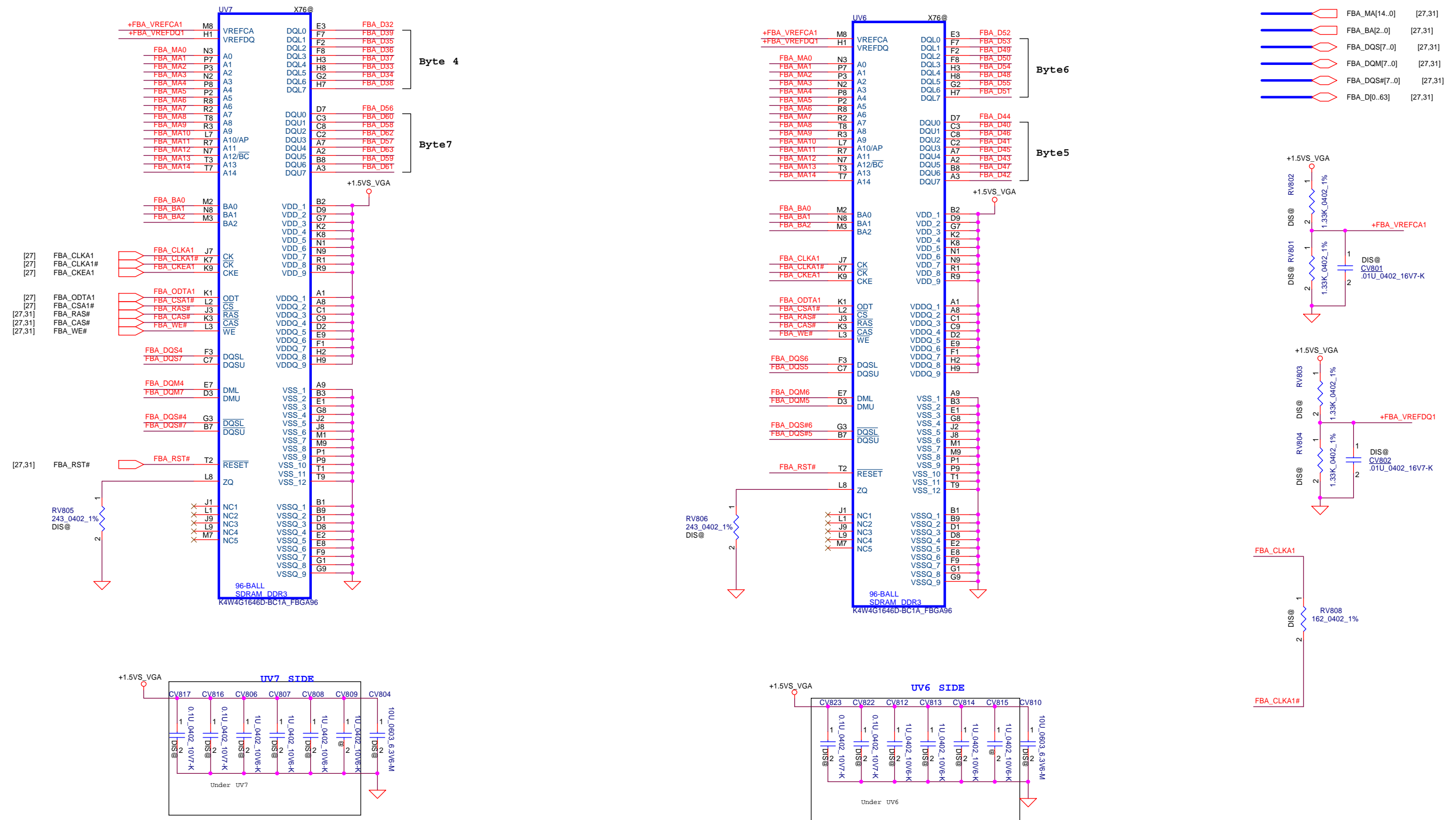
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| N16S-GT Core Power | | |
| Size | Document Number | Rev |
| Custom | KENOBI | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet 29 of 82 |



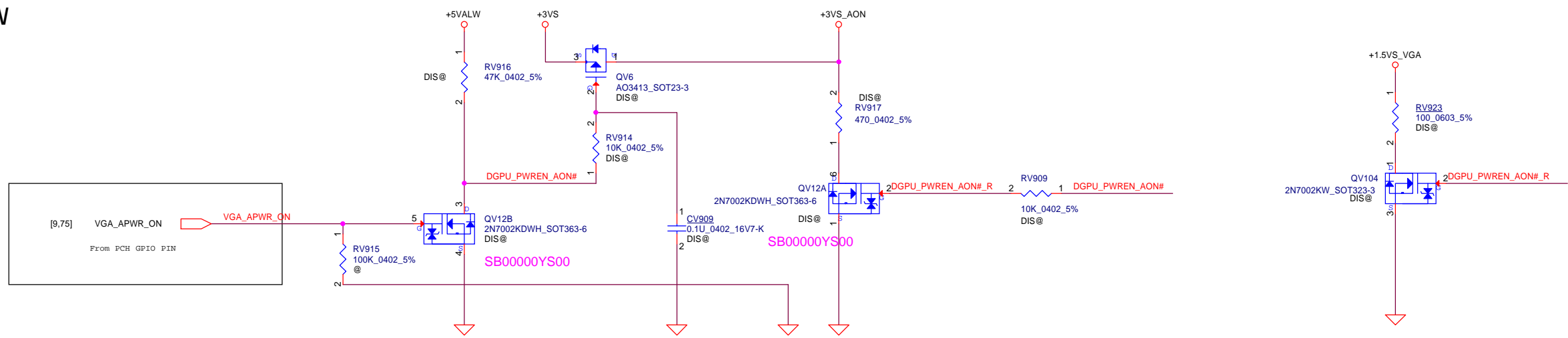
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| | | | | Date: Thursday, August 25, 2016 | Rev 2.0 |
| | | | | Sheet 30 | of 82 |

Memory Partition A - Upper 32 bits

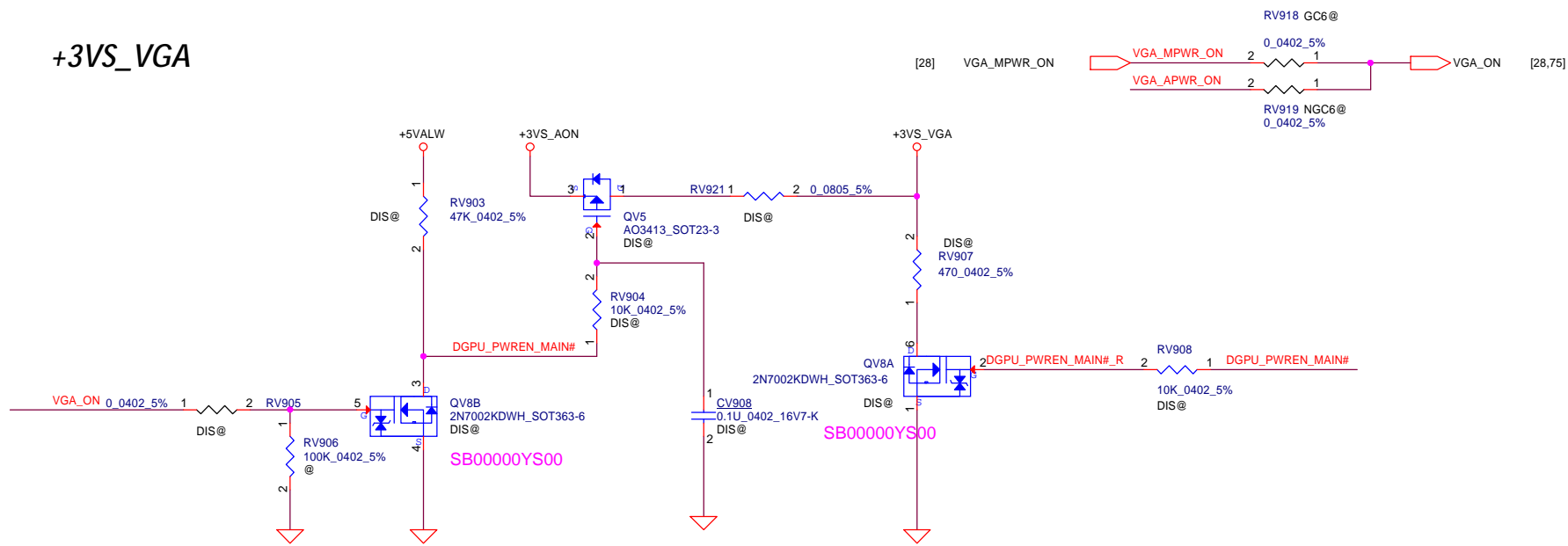


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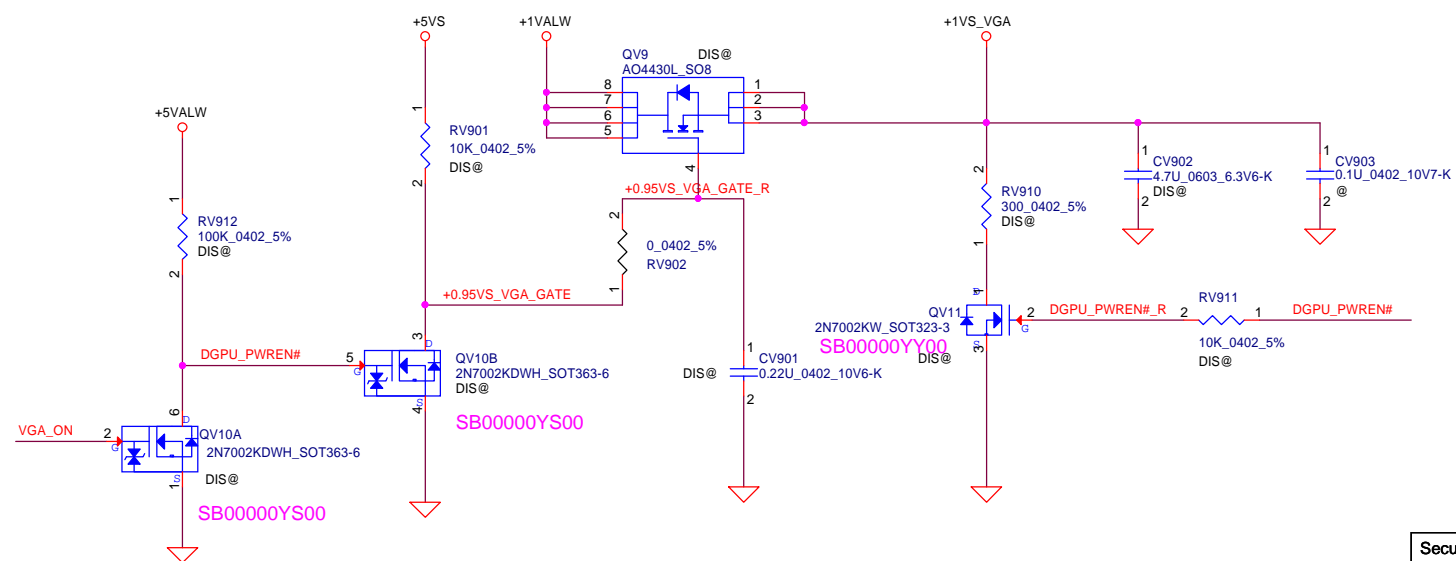
+3VS to +3VS_AON




+3VS_VGA

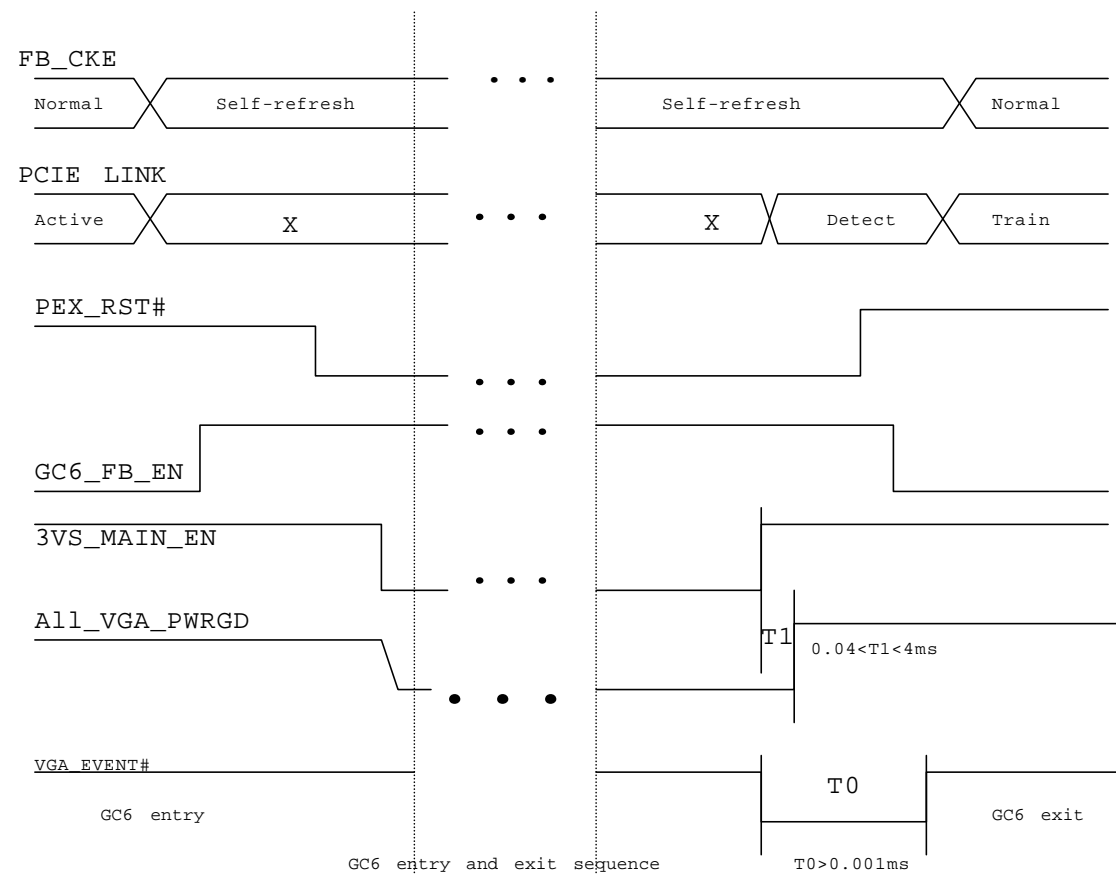
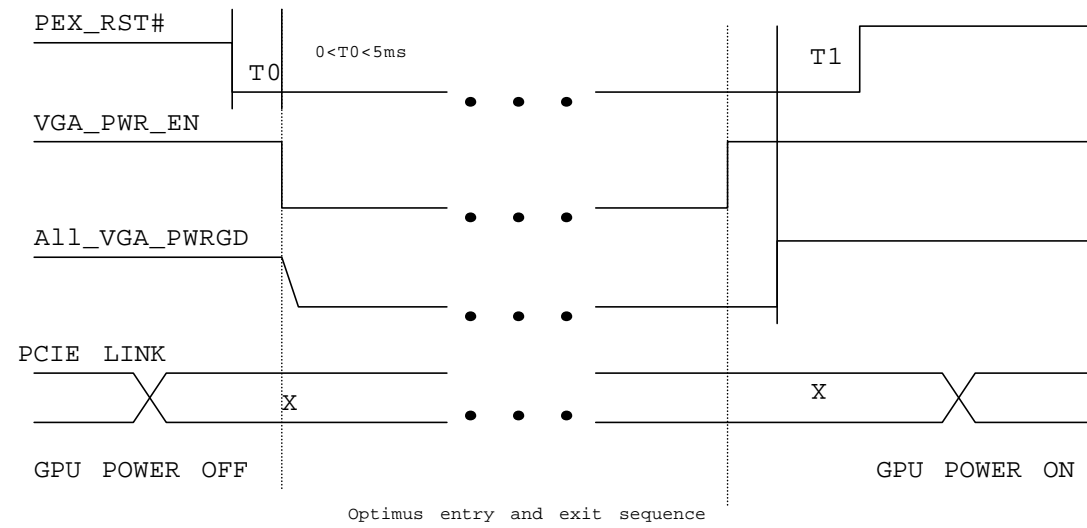
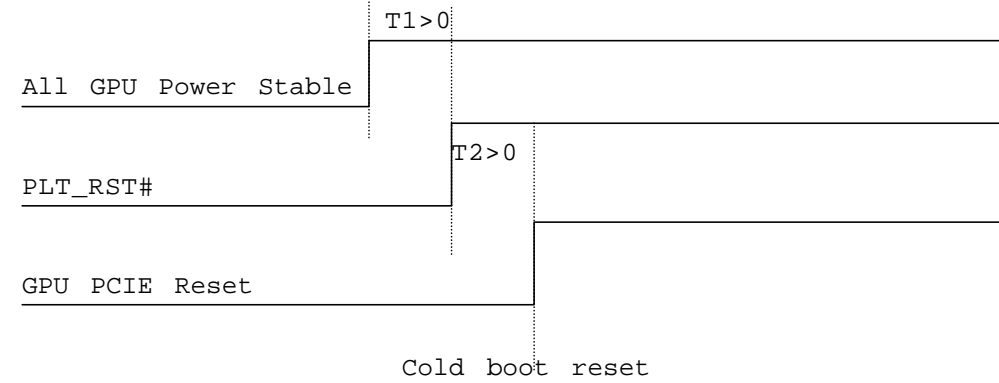



+1VALW to +1VS_VGA




| | | | | |
|--|------------------------------|-----------------|------------|--|
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| | | | | Rev 2.0 |

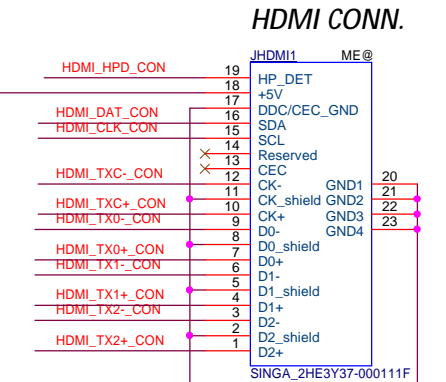
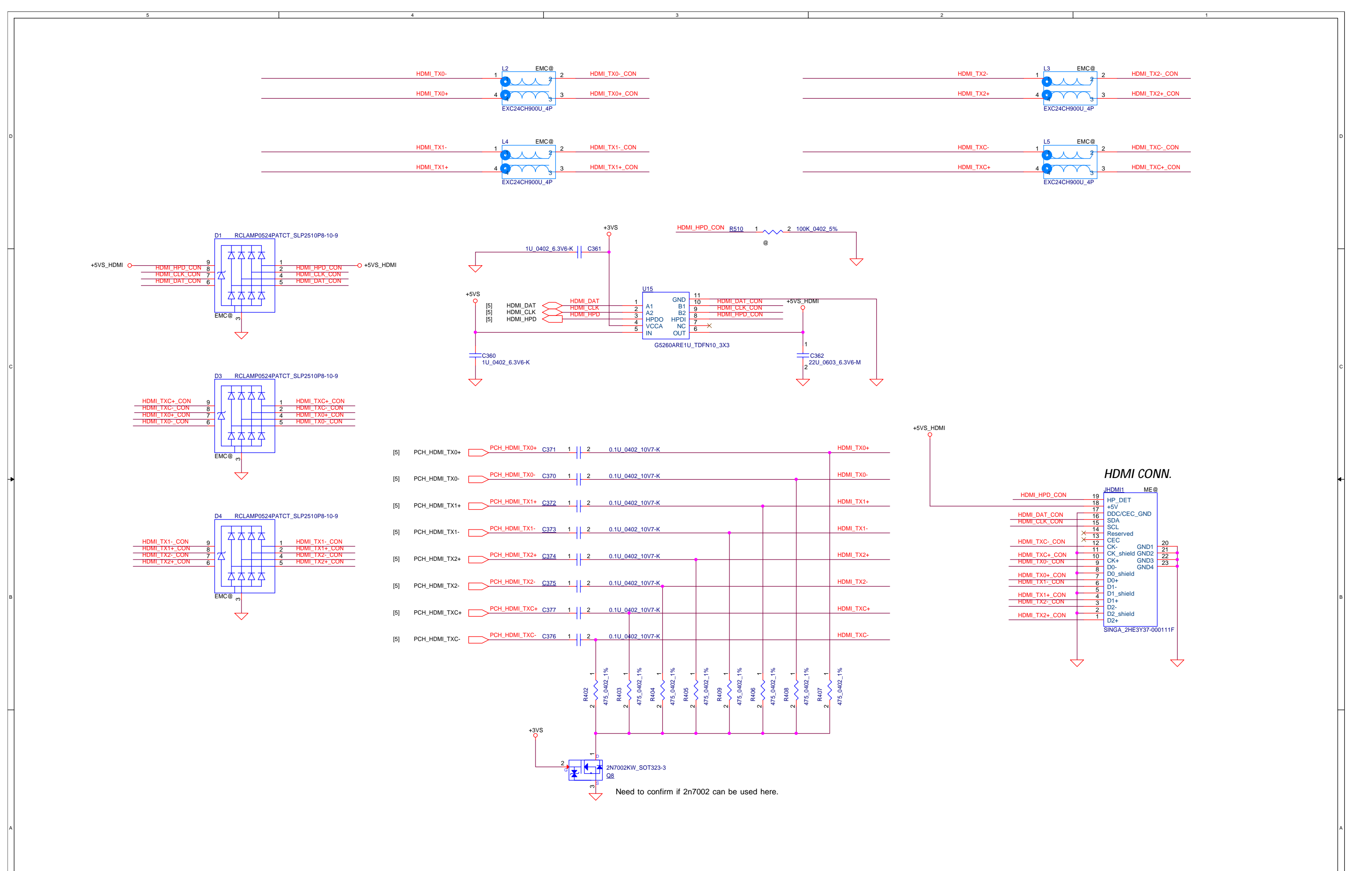
| GPIO | I/O | Functional Description | I/O Termination |
|--------|-----|---|---|
| GPI00 | O | FB Enable for GC6 2.0, Open source | 10K pull-down |
| GPI01 | O | Memory voltage control | Pull-up/pull down to set the FBVDD/Q boot voltage |
| GPI02 | O | Panel Backlight PWM Brightness Control | 100K pull down |
| GPI03 | O | Panel Power Enable | 100K pull down |
| GPI04 | O | Panel Backlight Enable | 100K pull down |
| GPI05 | O | GPU Power Sequence for GC6 2.0, Open Drain | 10k pull-up to 3V3_AON |
| GPI06 | I | GPU wake signal for GC6 2.0 | 10k pull-up to 3V3_AON |
| GPI07 | O | 3D Vision L/R signal | 100K pull down |
| GPI08 | O | System side PCIe rest monitor | 10k pull-up to 3V3_AON |
| GPI09 | I/O | Active low thermal alert, open drain | 10k pull-up to 3V3_AON |
| GPI010 | O | Memory VREF Control | 100K pull down |
| GPI011 | O | GPU Core VDD PWM control signal | |
| GPI012 | I | AC power detect or power supply overdraw input | 100k pull-up to 3V3_AON |
| GPI013 | O | Phase Shedding | 10k pull-up to 3V3_AON to enable two phase |
| GPI014 | I | Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI | |
| GPI015 | I | Hot Plug Detect for IFPC | |
| GPI016 | I | Active Low Frame Lock, Open Drain | 10k pull-up to 3V3_AON |
| GPI017 | I | Hot Plug Detect for IFPD | |
| GPI018 | I | Hot Plug Detect for IFPE | |
| GPI019 | I | Hot Plug Detect for IFPF or for IPPB when used as DisplayPort | |
| GPI020 | O | Reserved | |
| GPI021 | O | GPU PCIe self-reset control, Open Drain | 10k pull-up to 3V3_AON |
| OVERT | I/O | Catastrophic Over Temperature | 100k pull-up to 3V3_AON |



| | | | | | | |
|--|------------------------------|-----------------|------------|---|---------------------------|----------------|
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| Issued Date | 2015/08/28 | Deciphered Date | 2016/08/27 | | GPU GPIO table & sequence | |
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| | | | | Custom | KENOBI | 2.0 |
| | | | | Date: | Thursday, August 25, 2016 | Sheet 34 of 82 |

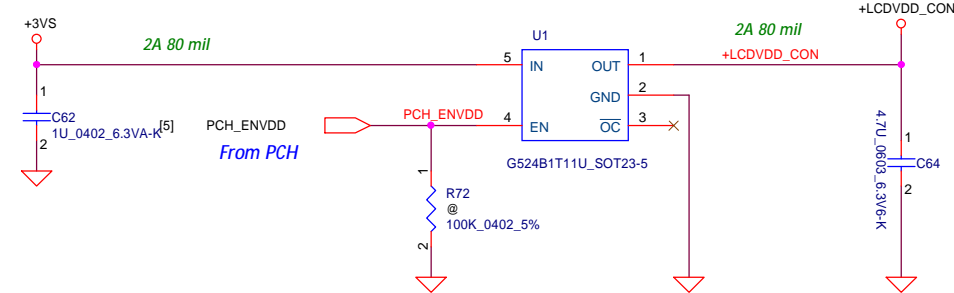
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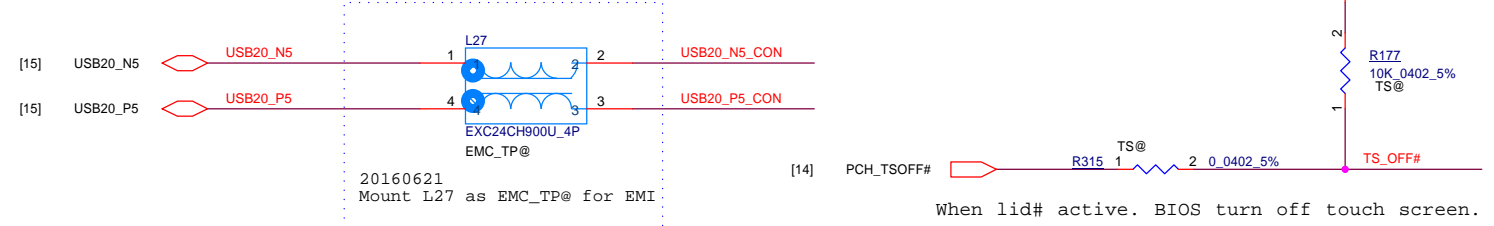


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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | HDMI CONN | |
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| Date: | Thursday, August 25, 2016 | Sheet | 36 | of | 82 |

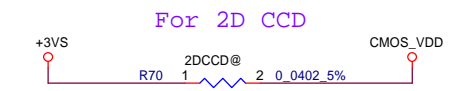
LCDVDD Circuit



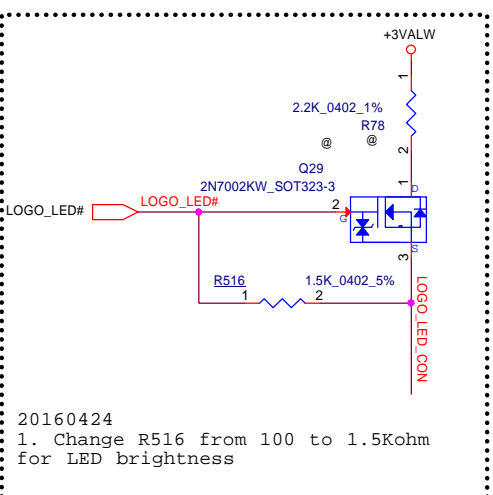
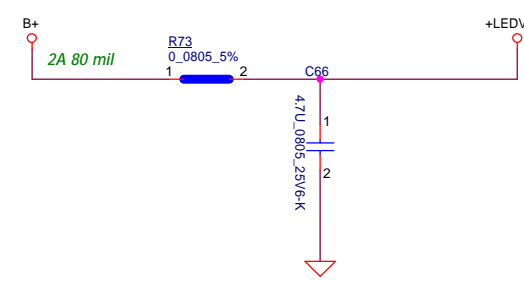
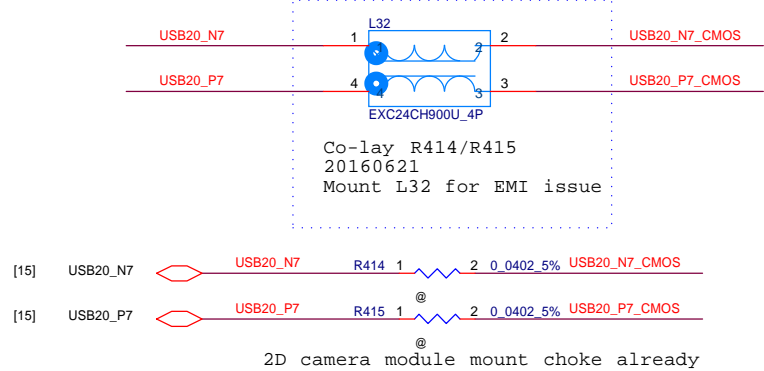
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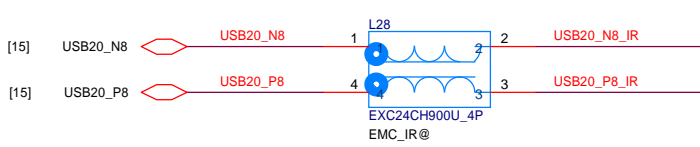
CMOS Camera



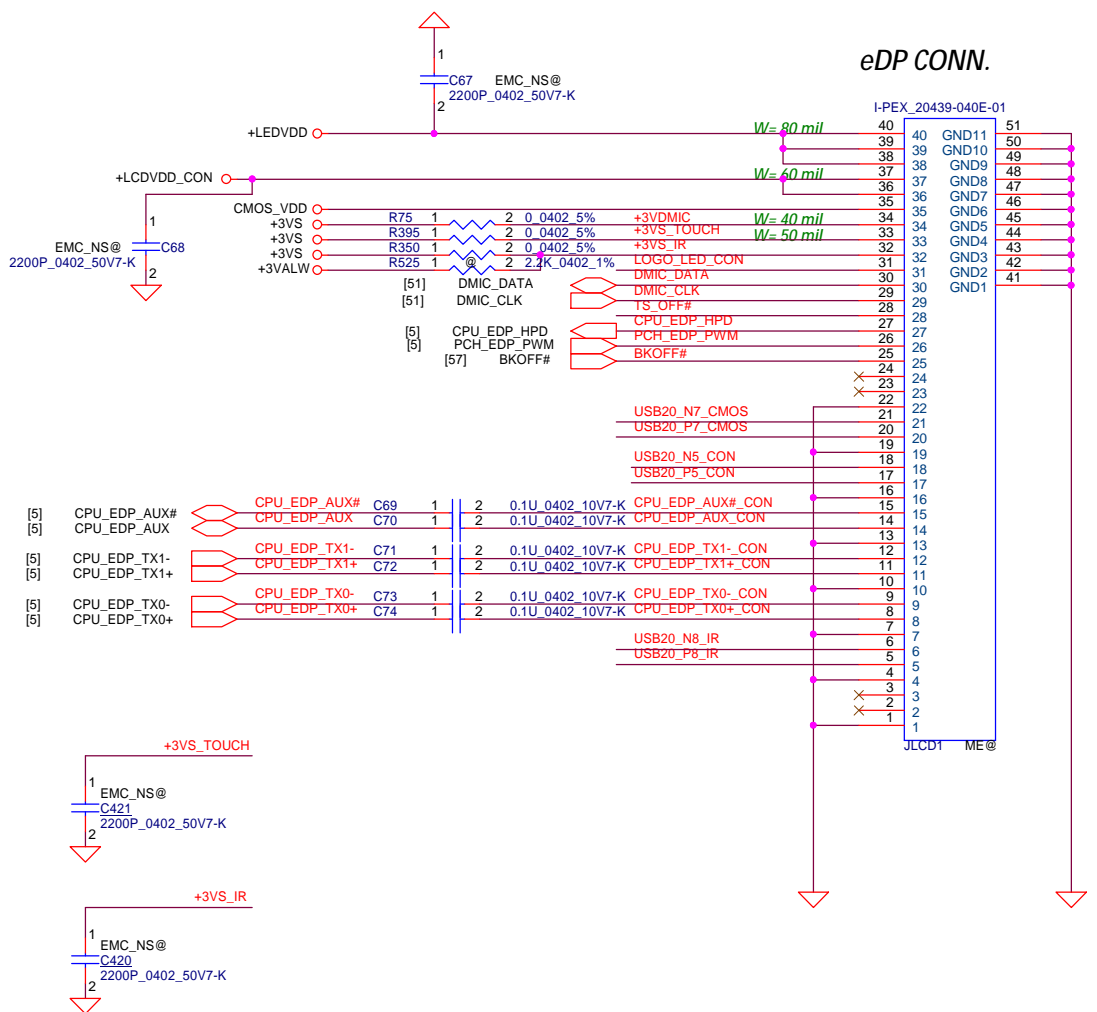
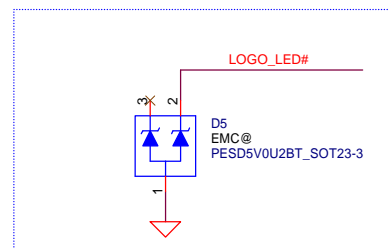
CMOS USB Port




IR camera USB Port




ESD request




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|---|------------------------------|-----------------|------------|--|
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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | |
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| Security Classification | LC Future Center Secret Data | | | Title |  | | |
| Issued Date | 2015/10/5 | Deciphered Date | 2014/09/07 | HDMI RP | | | |
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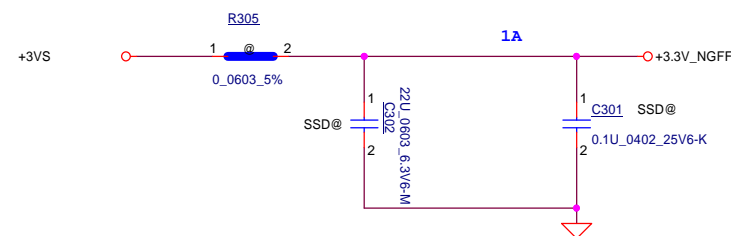
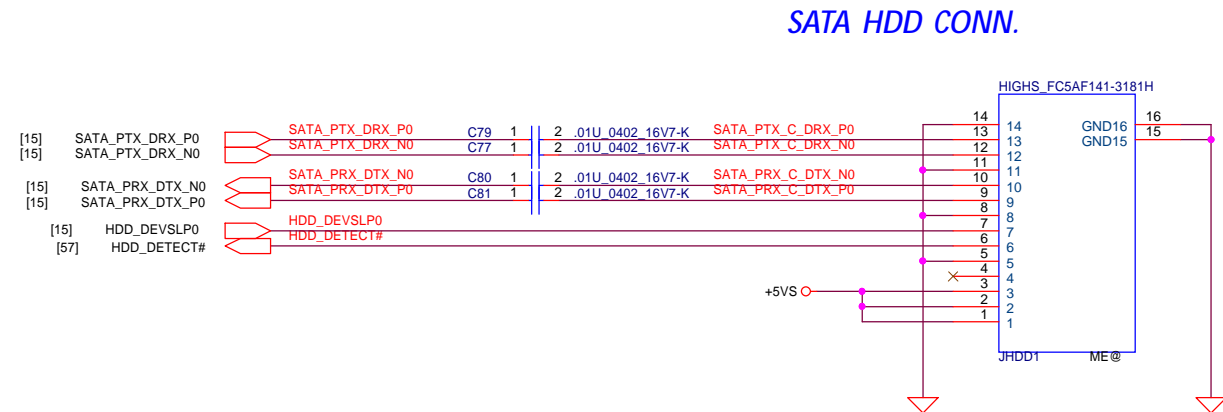
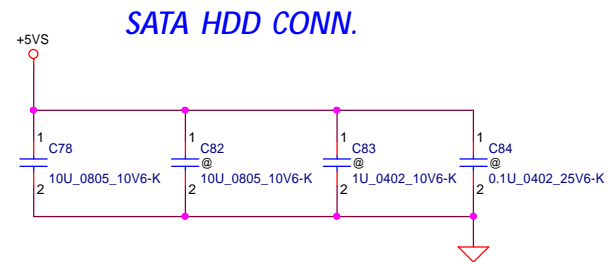
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| | | | | Custom | KENOBI |
| Date: | | | | Thursday, August 25, 2016 | Sheet 39 of 82 |

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| Security Classification | LC Future Center Secret Data | | | Title |  | |
| Issued Date | 2015/10/5 | Deciphered Date | 2016/12/31 | DP to VGA | | |
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| | | | | Date: | Thursday, August 25, 2016 | Sheet 40 of 82 |

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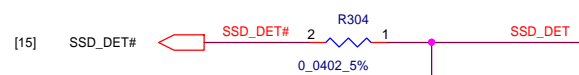
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M.2 SSD(SATA/PCIE)

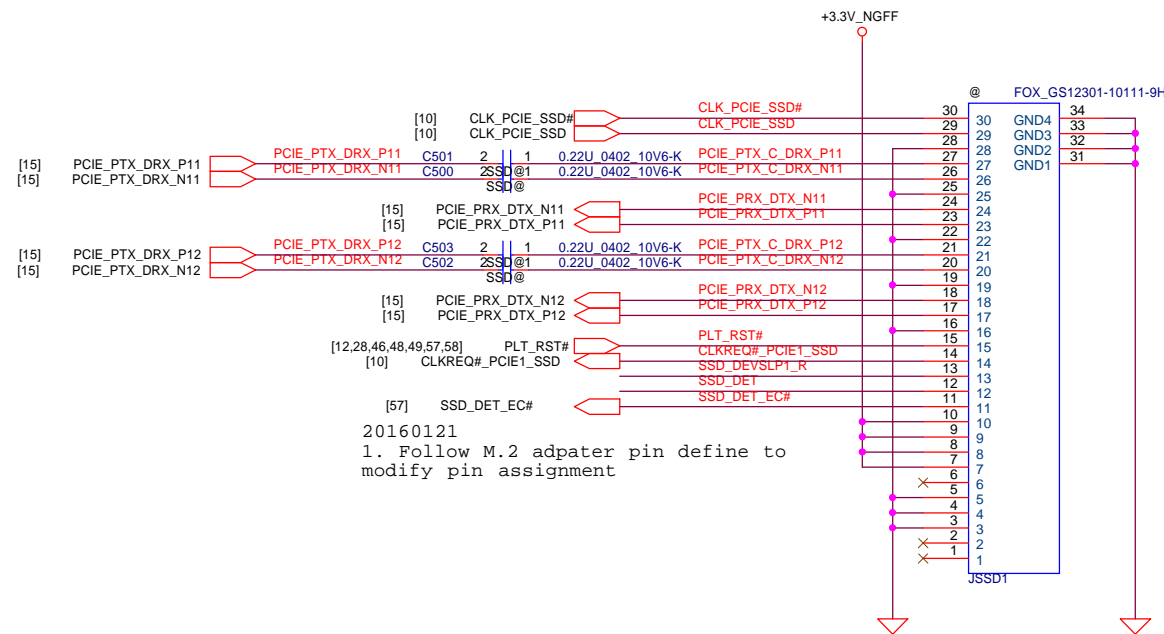


20160308
1. Remove R300,R301,R302 and put it to CPU side



PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open


SSD_DET#
0 - SATA
1 - PCIE



20160121
1. Follow M.2 adapter pin define to modify pin assignment

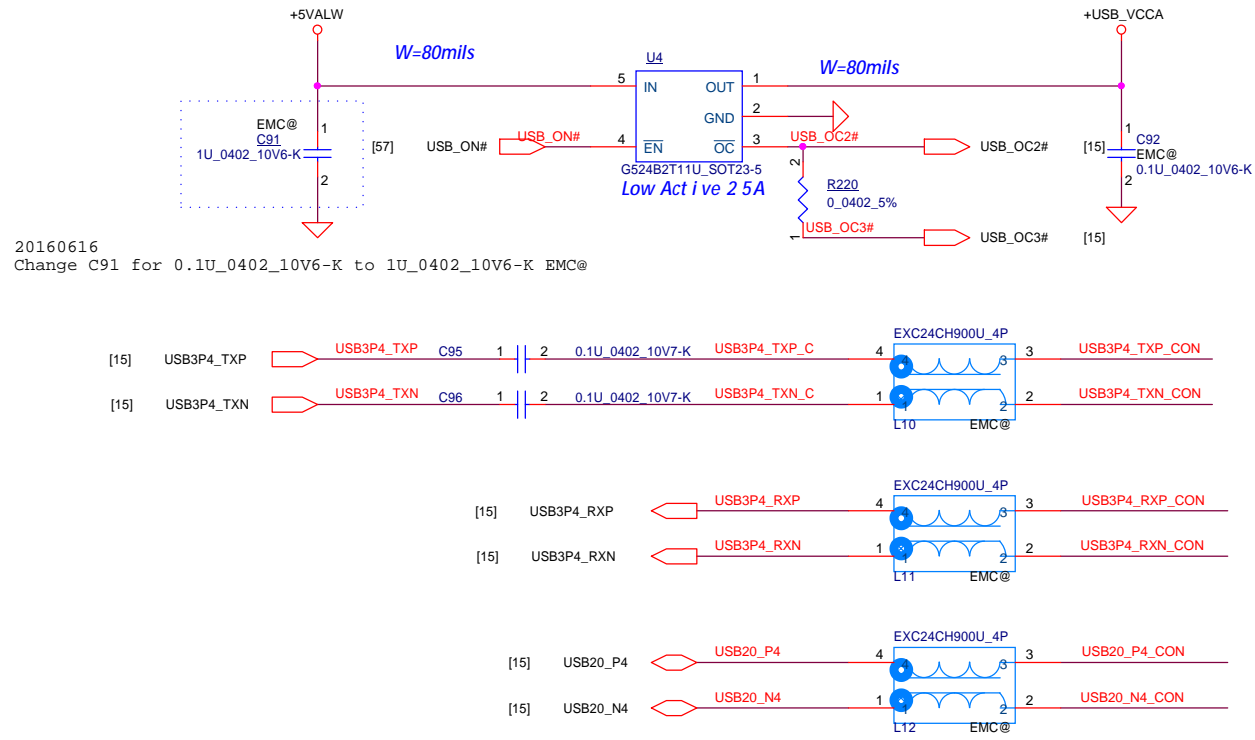
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| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | SATA HDD | |
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| Size | Document Number | KENOBI | | Rev | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet | 42 of 82 | | |

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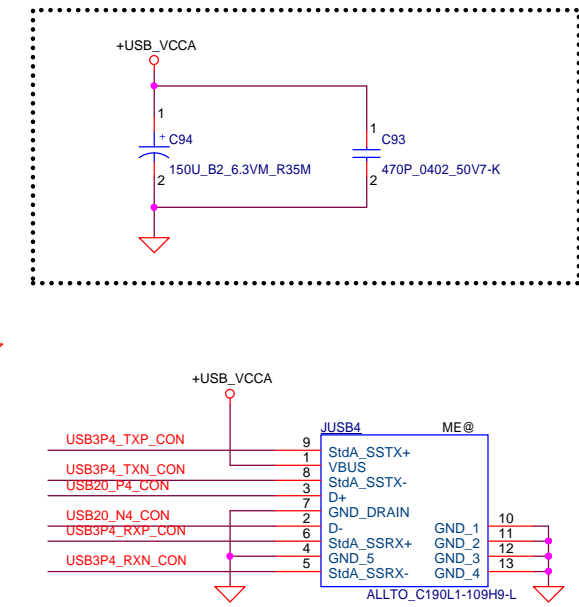
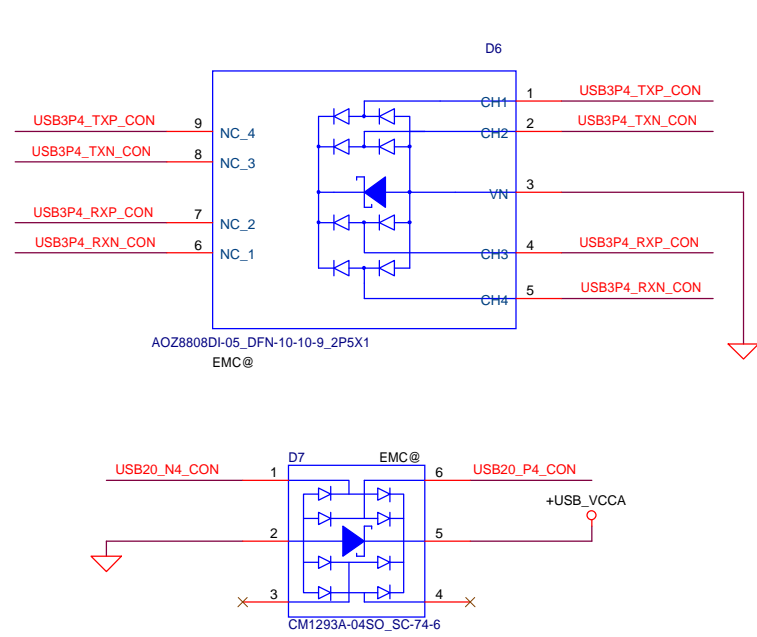
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| Issued Date | 2015/10/5 | Deciphered Date | 2016/12/31 | Size | |
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| | | | | KENOBI | |
| Date: | | | | Thursday, August 25, 2016 | Sheet 43 of 82 |

USB3 PORT4

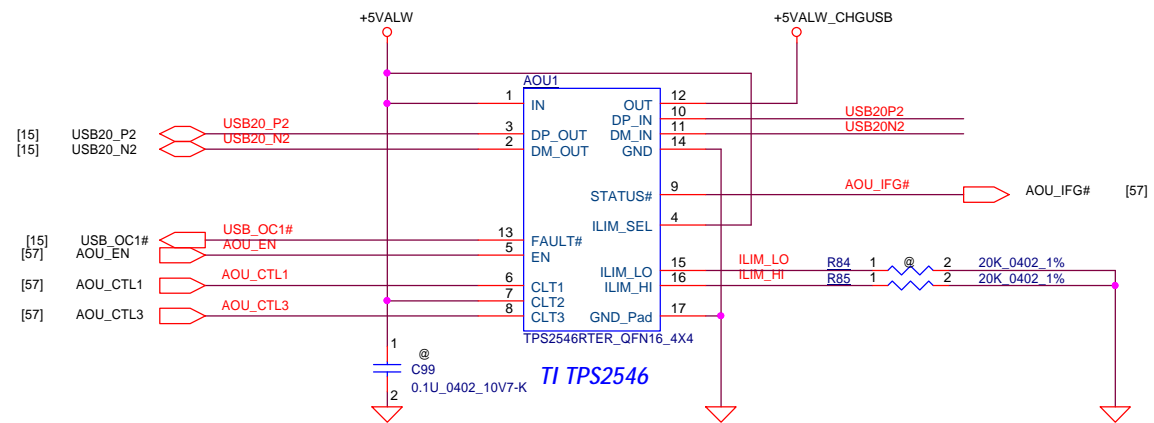
POWER SWITCH



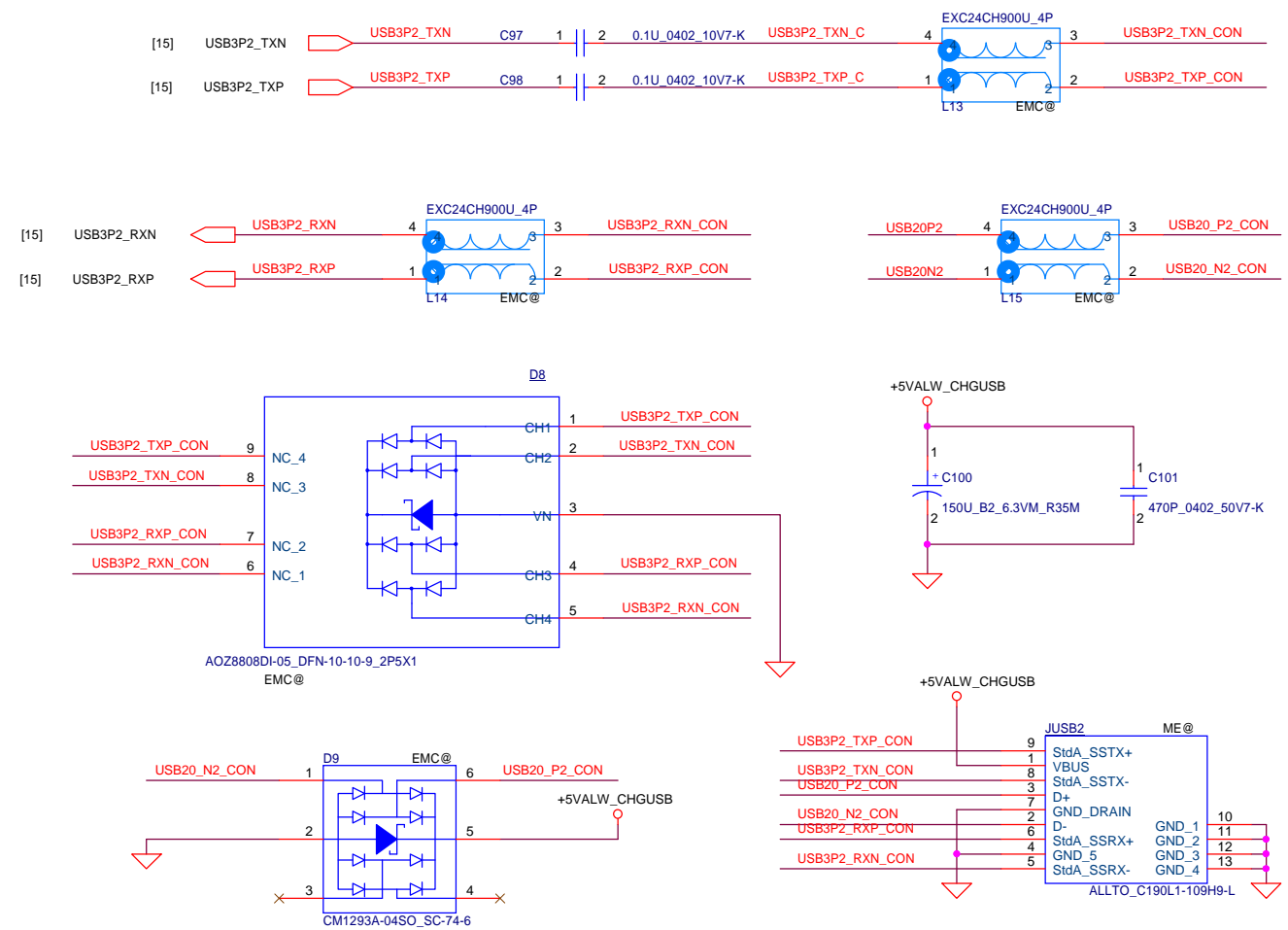
20160616
Change C91 for 0.1U_0402_10V6-K to 1U_0402_10V6-K EMC@



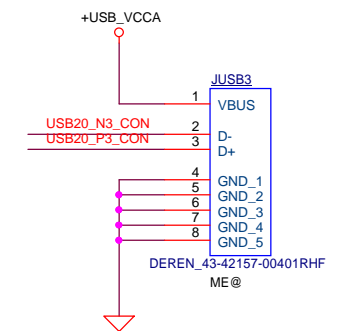
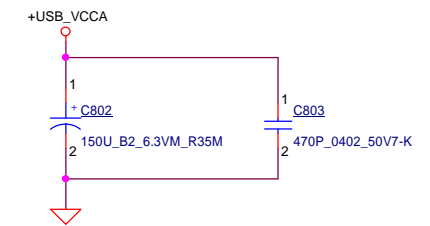
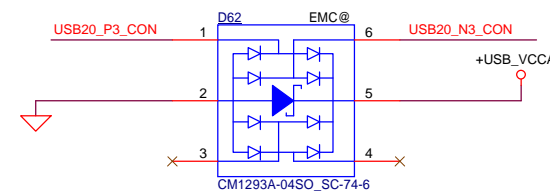
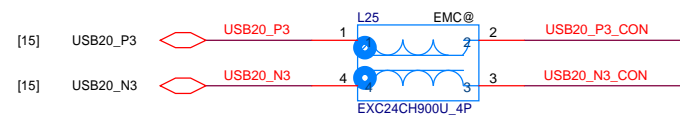
PORT2 (AOU)




| CLT1 | CLT2 | CLT3 | ILIM_SEL | MOD |
|------|------|------|----------|--|
| 0 | 0 | 0 | X | DCH OUT held low |
| * | 1 | 1 | 1 | CDP Data Connected and Port Power Mgt. Function Active |
| * | 1 | 1 | 0 | SDP2 Data Connected |
| * | 1 | 1 | X | SDP1 Data Connected |
| * | 0 | 1 | 0 | SDP1 Data Connected |
| | 1 | 0 | 0 | DCP_Short Device Forced to stay in DCP BC 1.2 charging mode |
| | 1 | 0 | 1 | DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode |
| * | 0 | 1 | 1 | DCP_Auto Data Disconnected and Port Power Mgt. Function Active |
| * | 0 | 0 | 1 | DCP_Auto Data Disconnected and Power Wake Function Active |



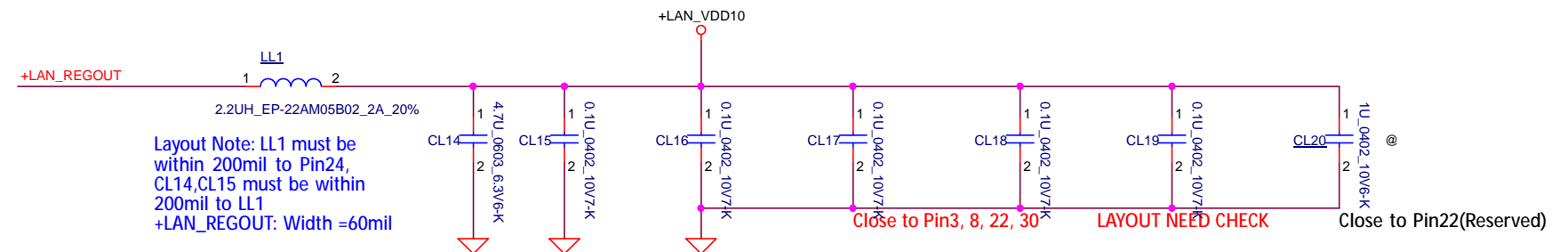
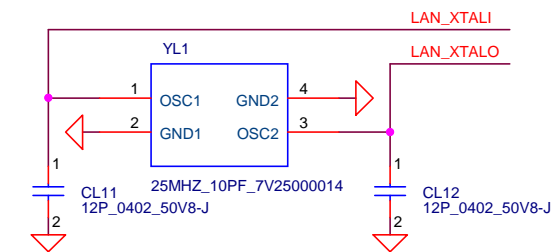
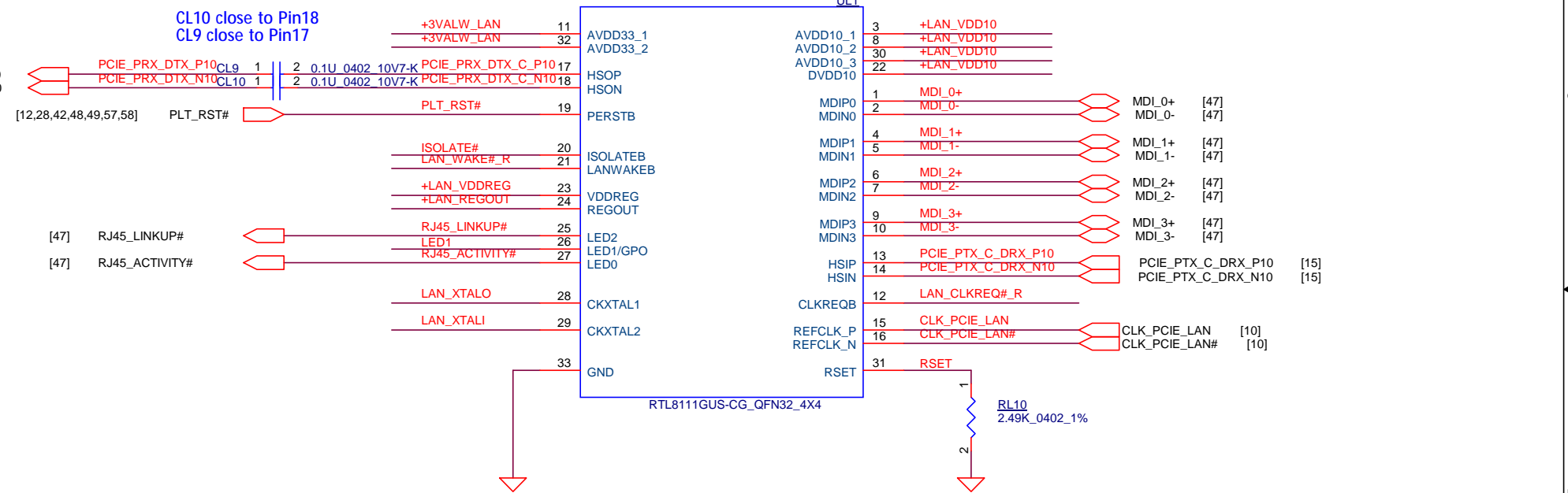
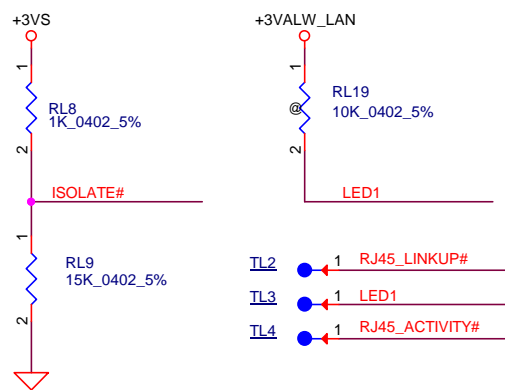
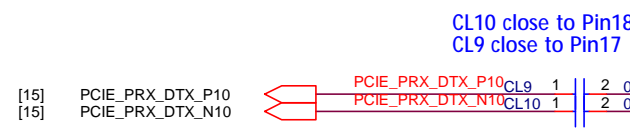
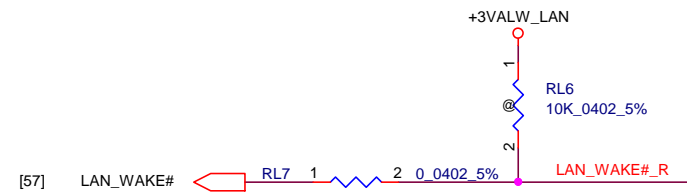
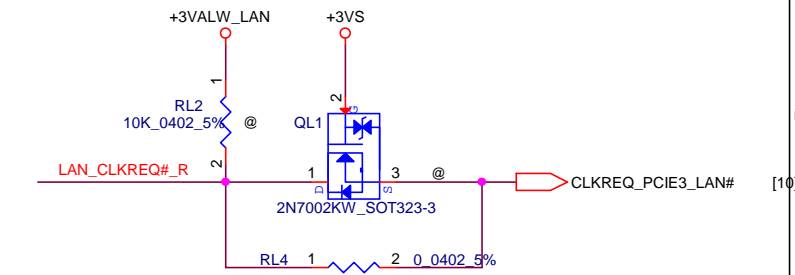
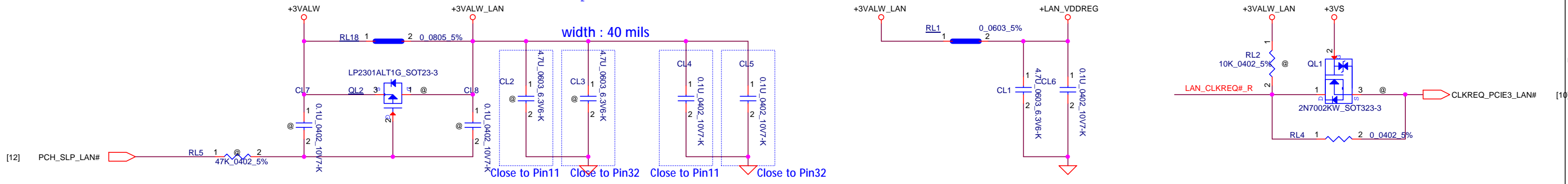
USB3 PORT3




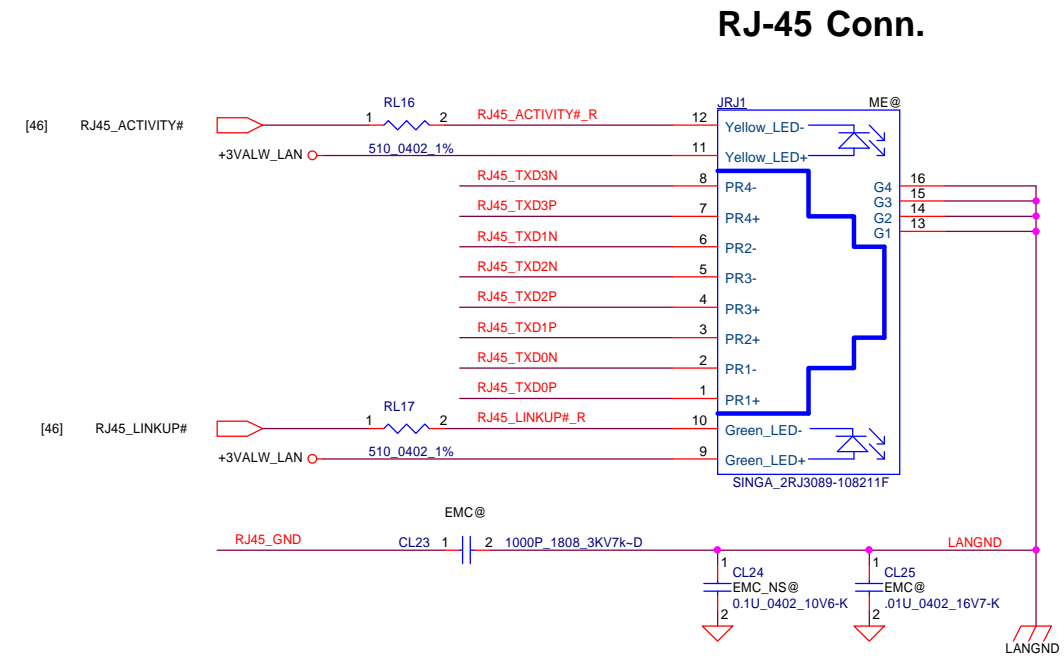
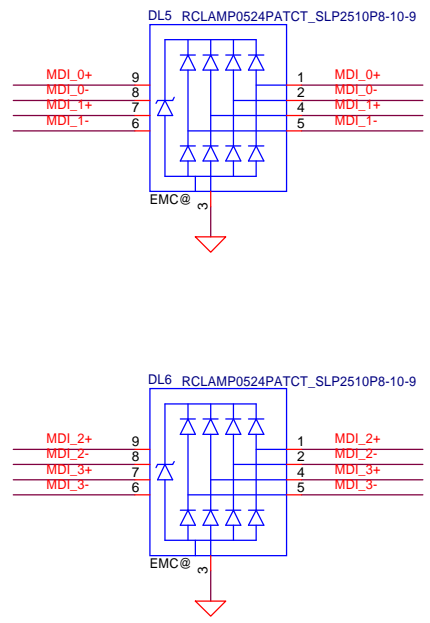
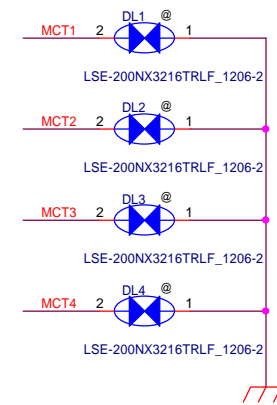
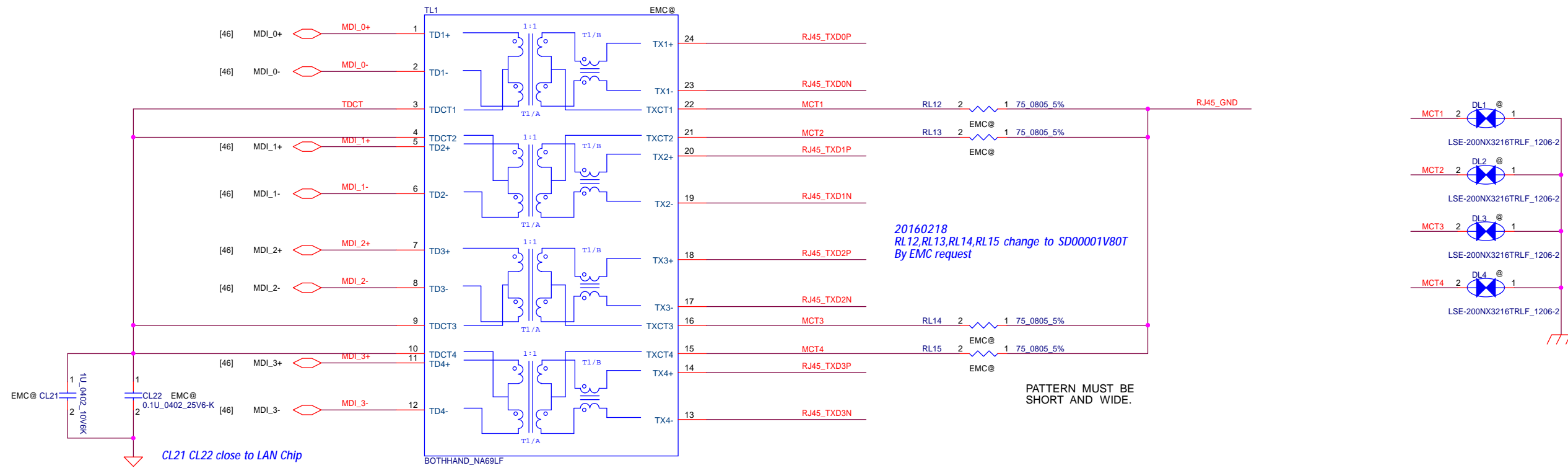
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| | | | | Rev: 2.0 Sheet: 45 of 82 |

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100ms

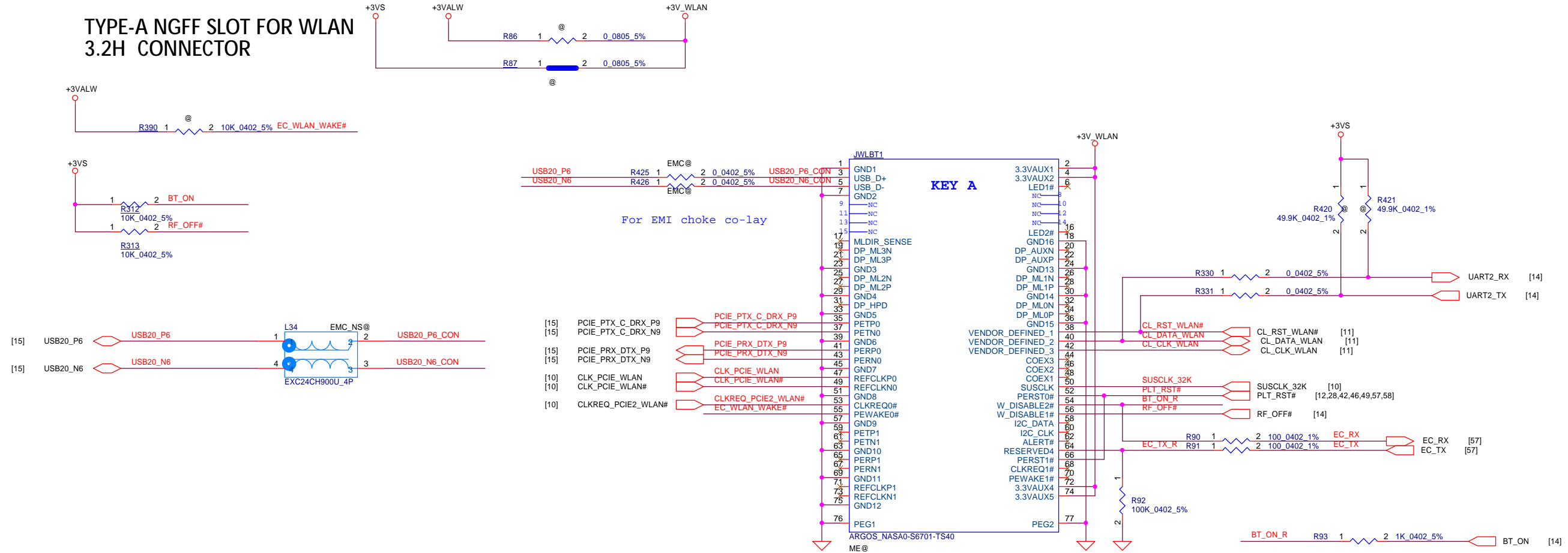



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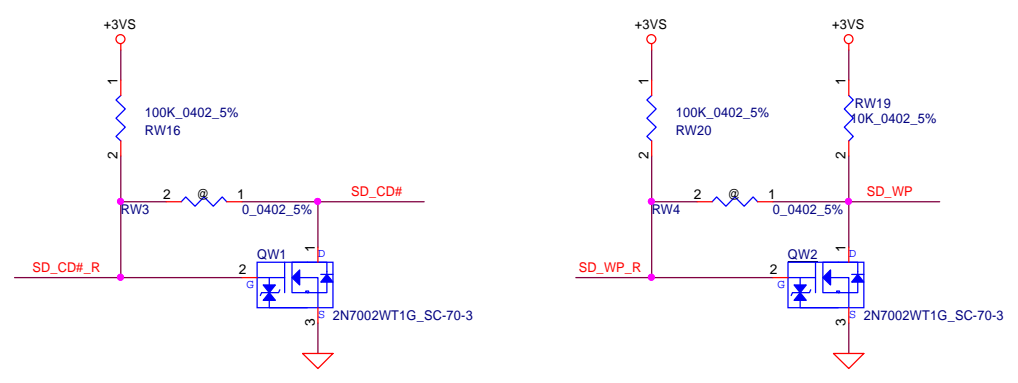
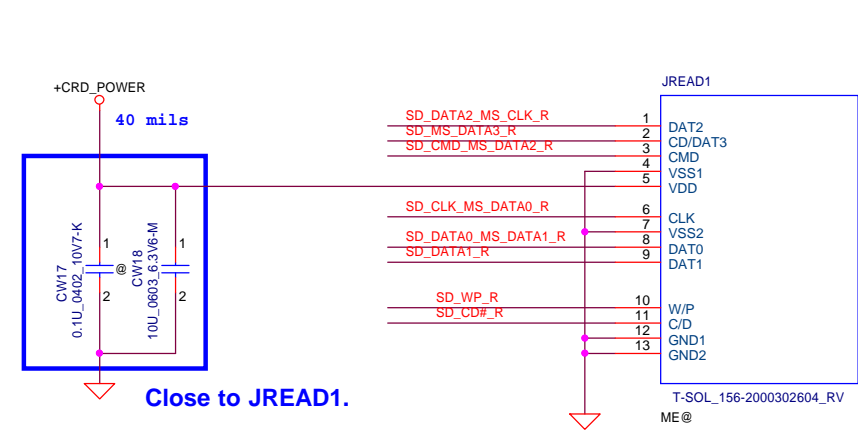
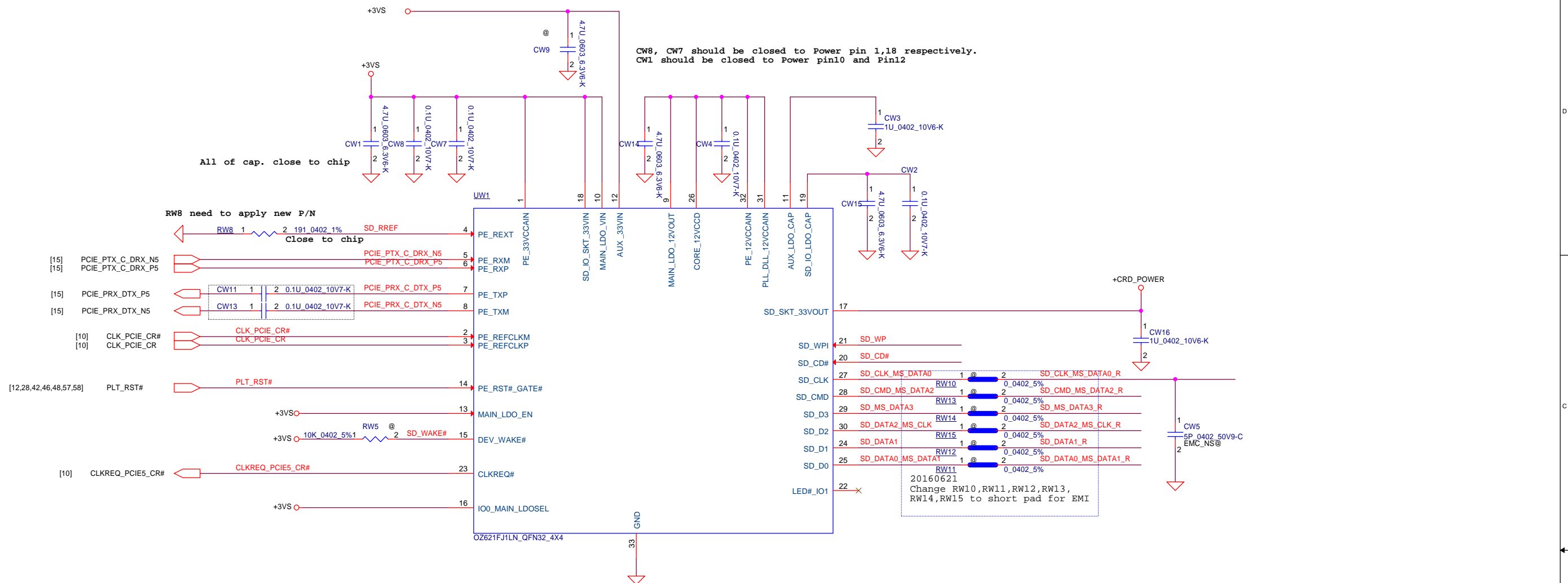


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TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR

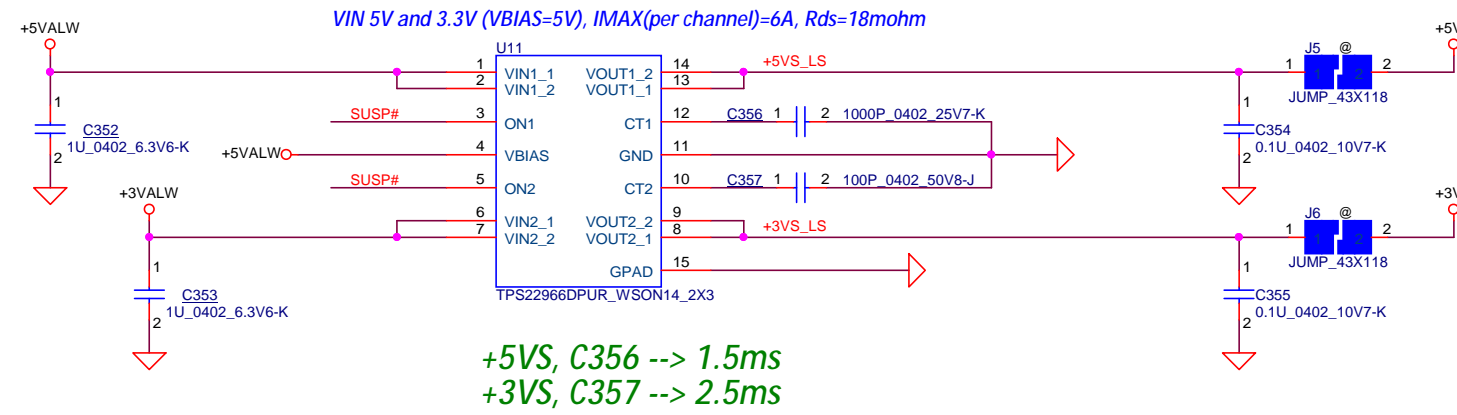


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| Date: | Thursday, August 25, 2016 | Sheet | 48 | of 82 |

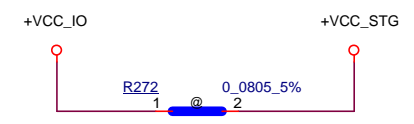
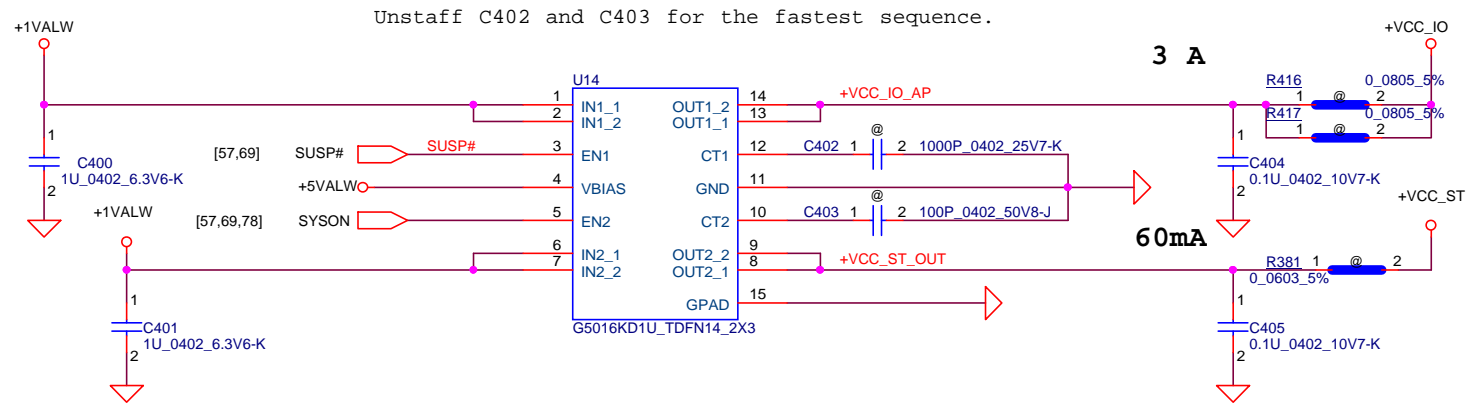


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Load Switch
+5VALW To +5VS
+3VALW To +3VS

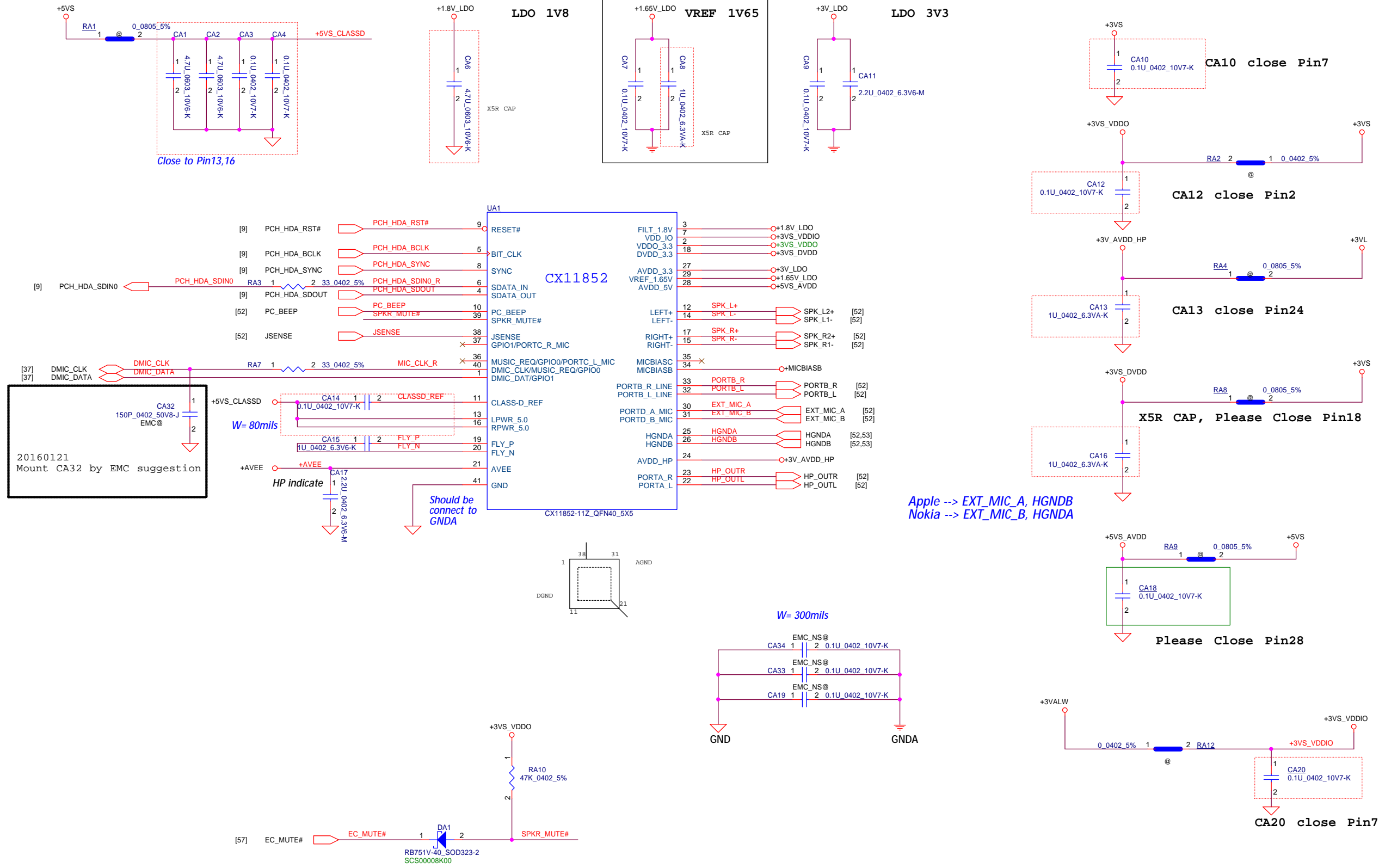


+1VALW to +VCC_IO_AP & +VCC_ST



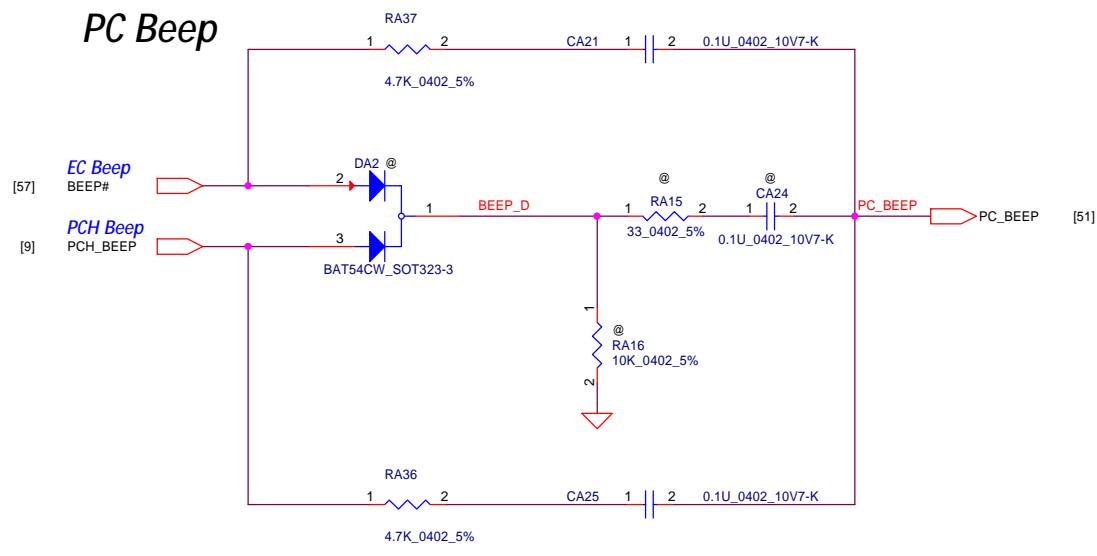
Slew Rate=10uS<TR<65us

| | | | |
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| Size Custom | | Document Number | Rev 2.0 |
| | | KENOBI | |
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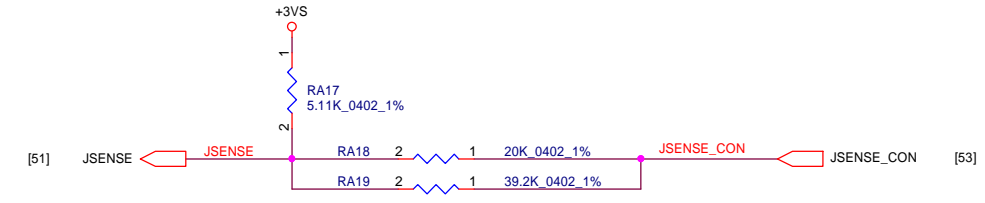
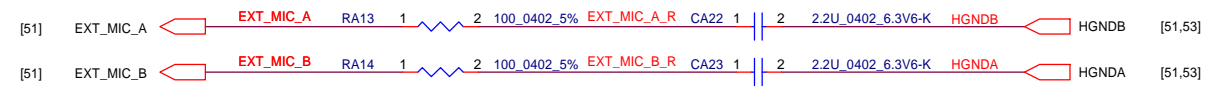
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PC BEEP

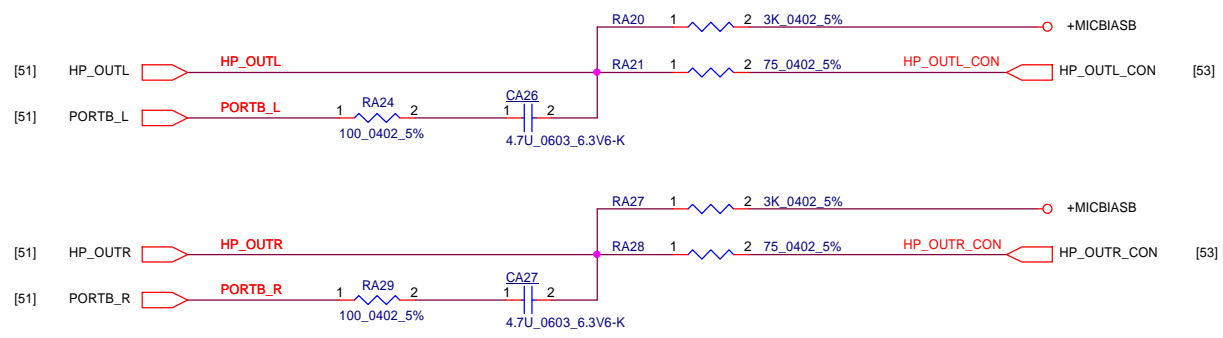


EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A

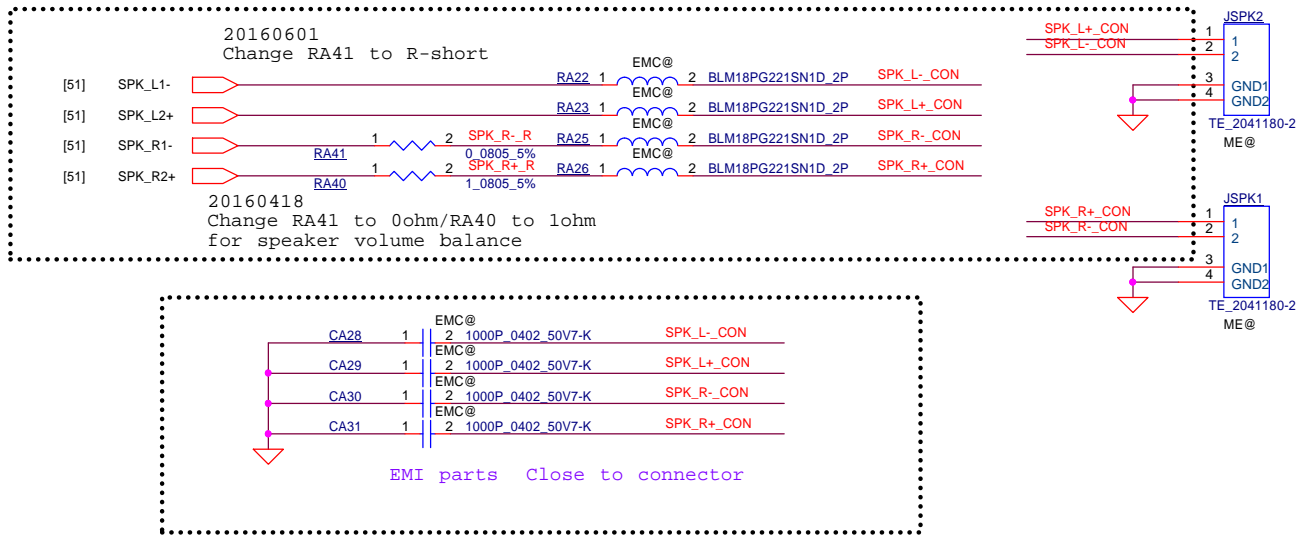


HeadPhone/LINE OUT

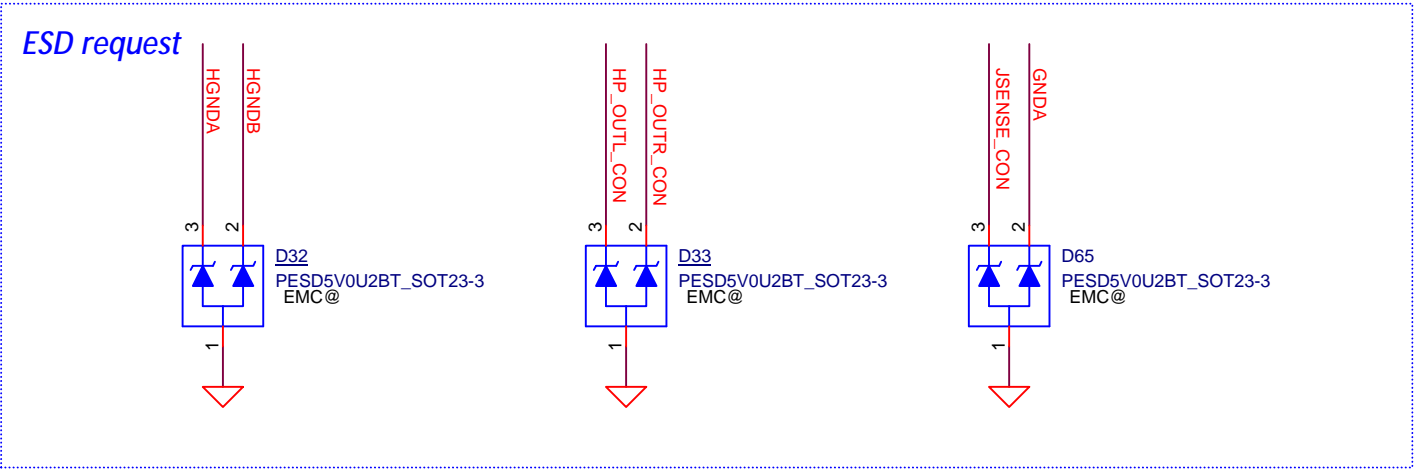
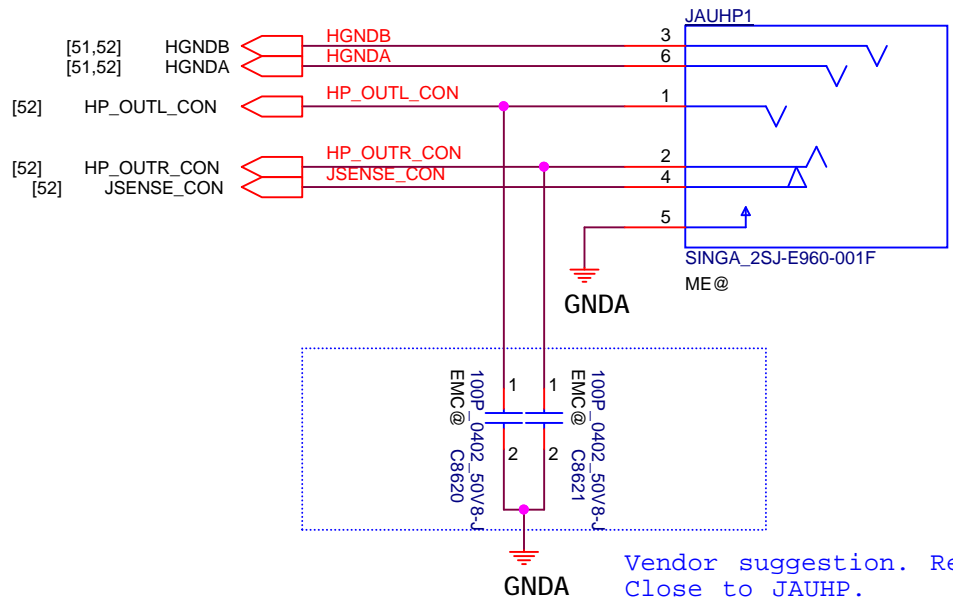


Speaker OUT

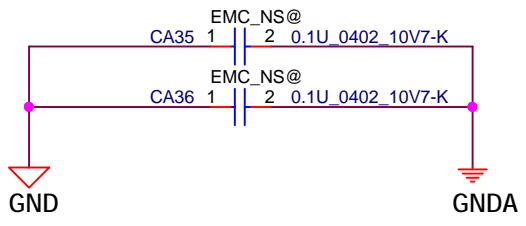
Need Length Match




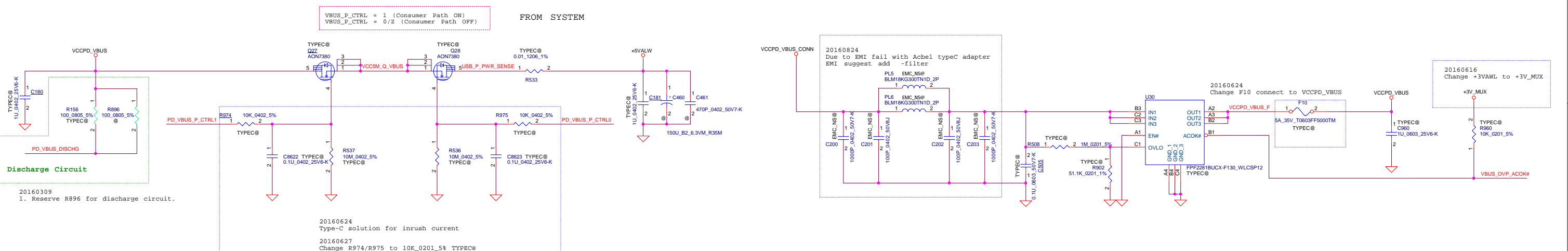
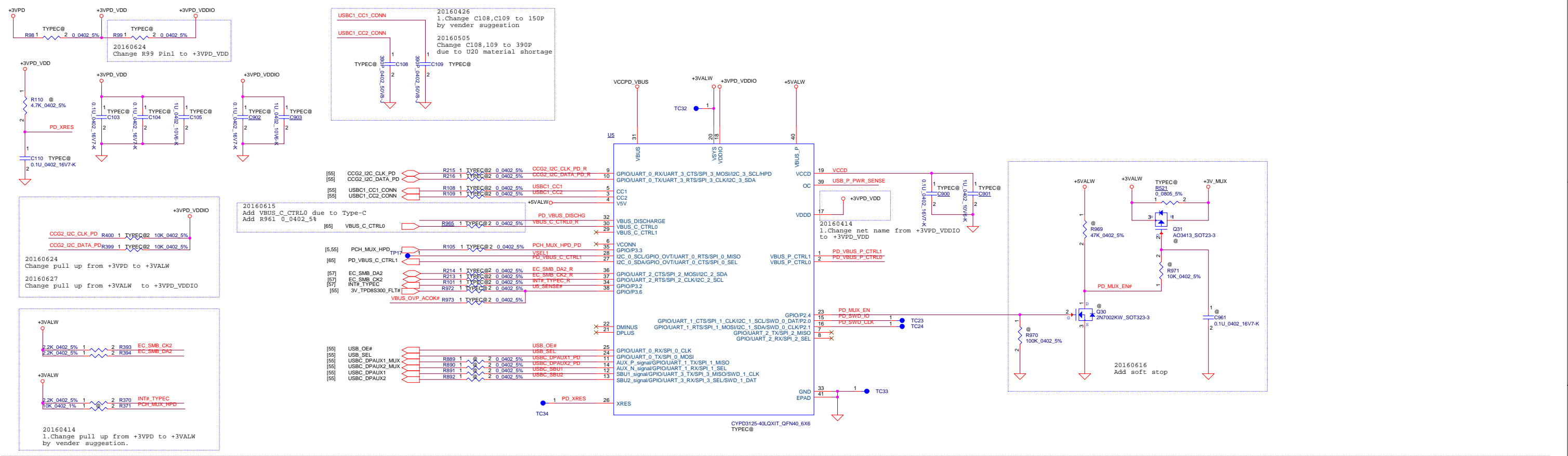
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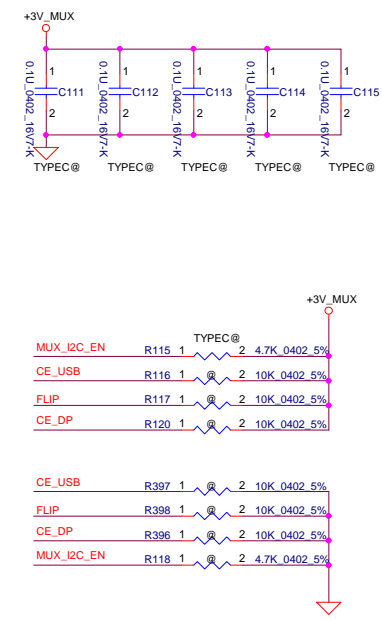
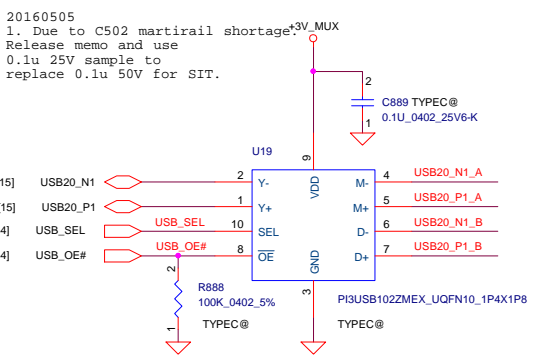
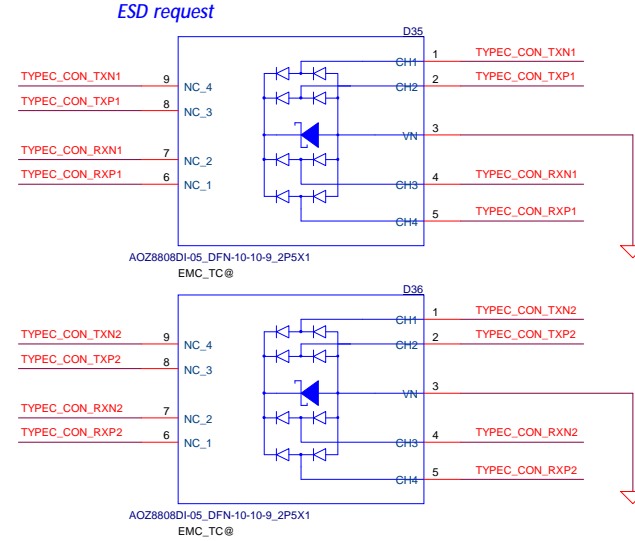
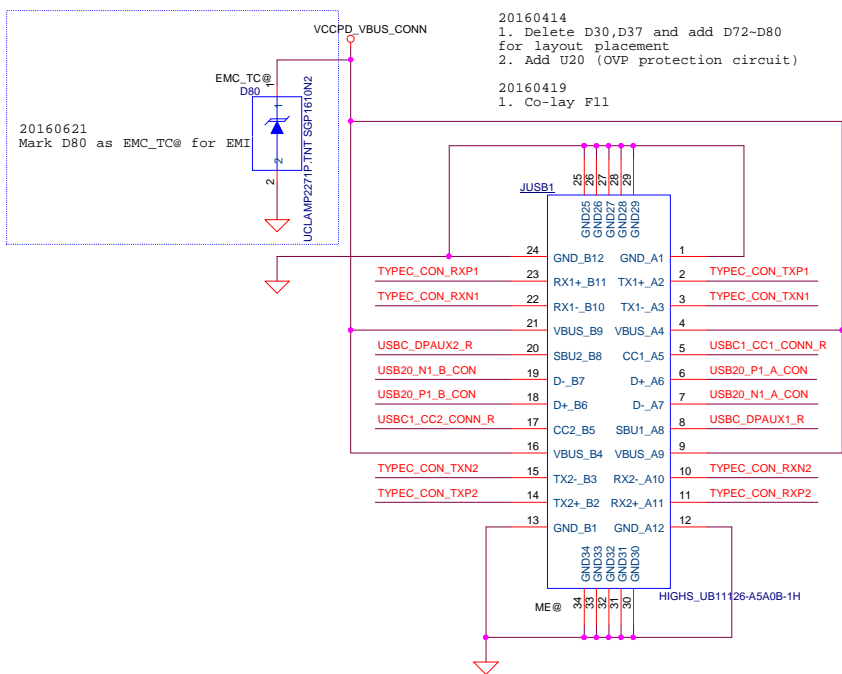
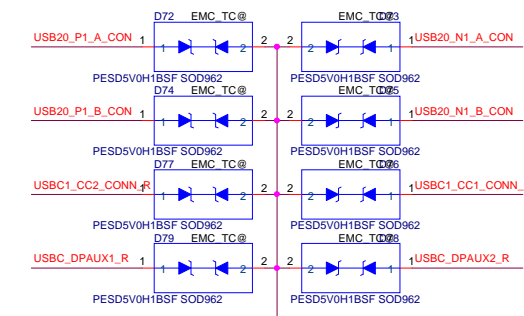
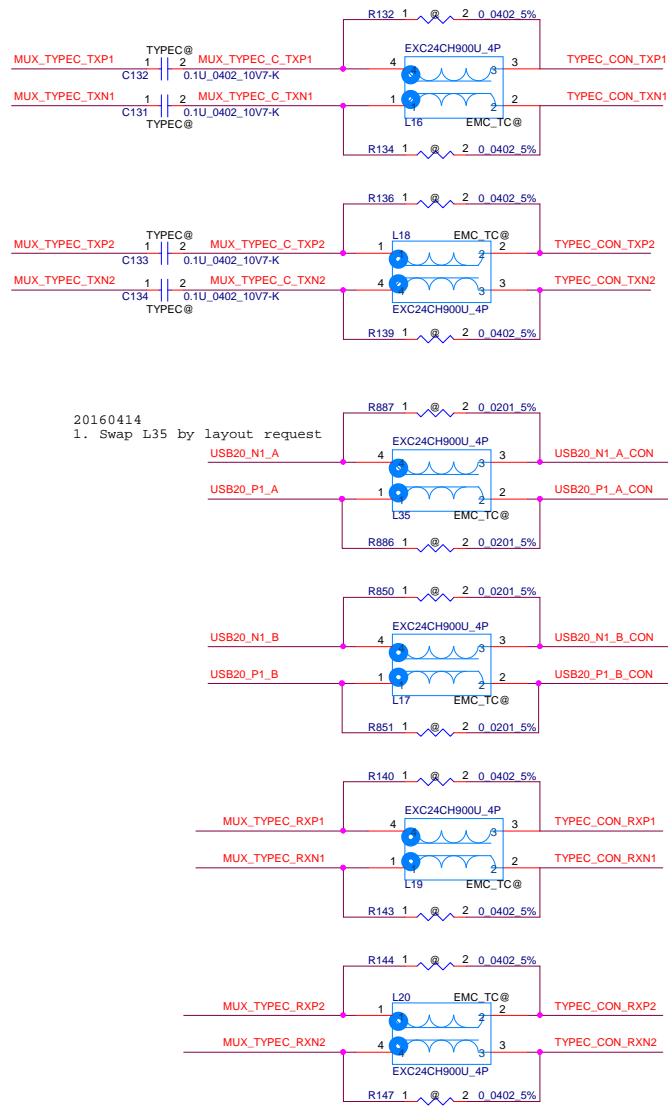
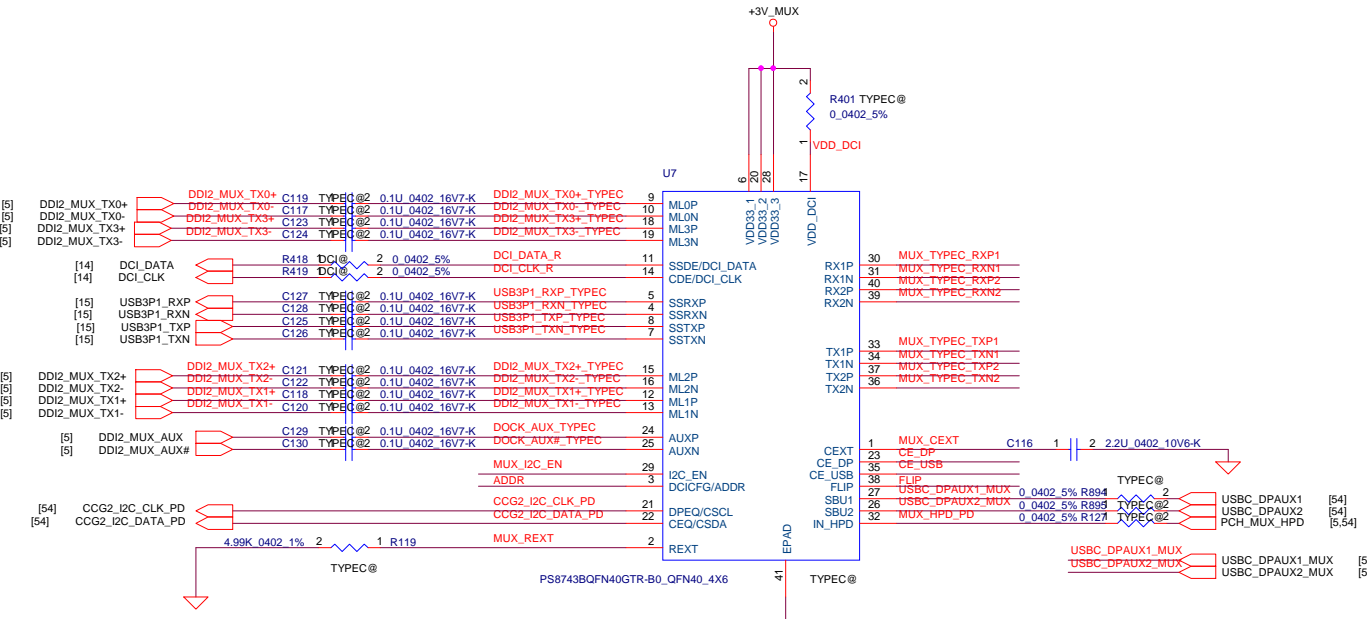
Vendor suggestion. Reserve for EMI. Close to JAUHP.



| | | | | | | |
|---|-----------|------------------------------|------------|------------|---------------------------|---|
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| Size | Document | Number | Rev | | 2.0 |
| Customer | KENOBI | | Date: | Thursday, August 25, 2016 | Sheet 54 of 82 |



20160414
1. Swap L35 by layout request

20160414
1. Delete D30, D37 and add D72-D80 for layout placement
2. Add U20 (OVP protection circuit)

20160419
1. Co-lay F11

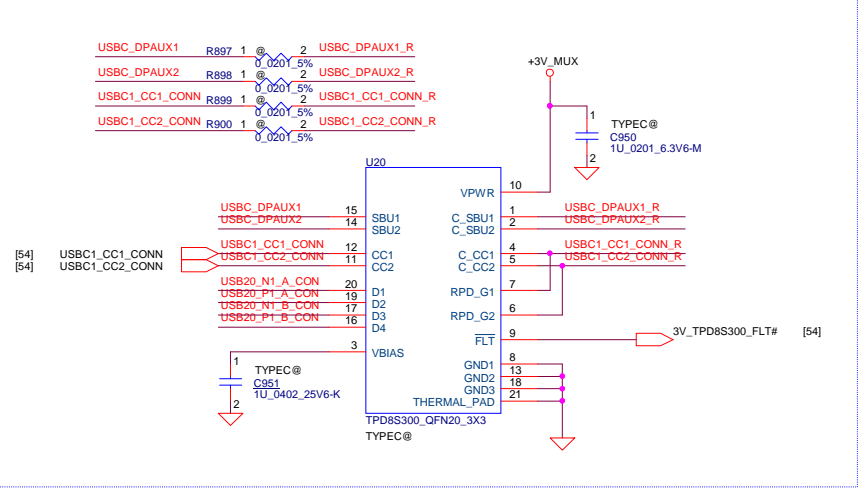
20160330
1. Add CC/SBU protection solution

20160505
1. Unstaff U20 and staff R897, R898, R899, R900 due to U20 martirail shortage.

201616
FLT pin into U5 pin30


20160624
1. Change VPER to +3V_MUX

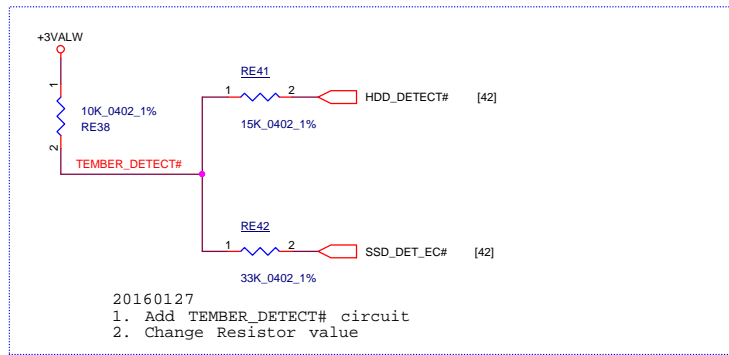
20160719
1. U20 martirail prepare ready.



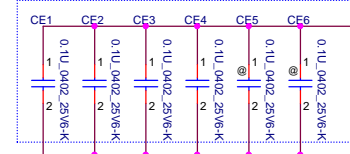
| | | | | |
|--|------------------------------|-----------------|------------|---------------------------|
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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | |
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| | | | Sheet | 55 of 82 |

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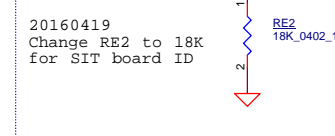
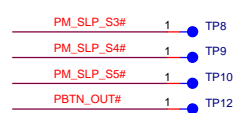
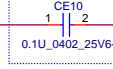
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| Issued Date | 2015/10/5 | Deciphered Date | 2016/12/31 | DOCKING/ DCIN CONN | |
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| | | | | Size Custom | 2.0 |
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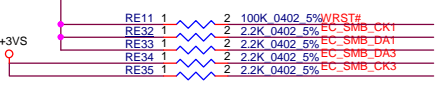
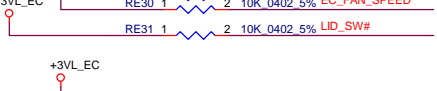
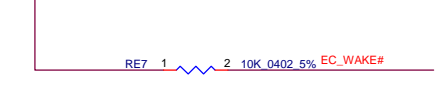
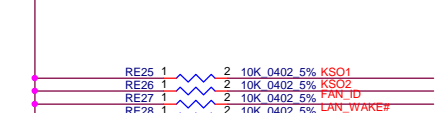
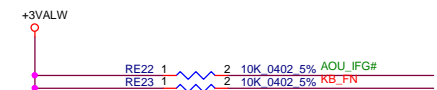
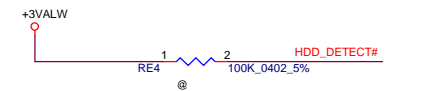
All capacitors close to EC



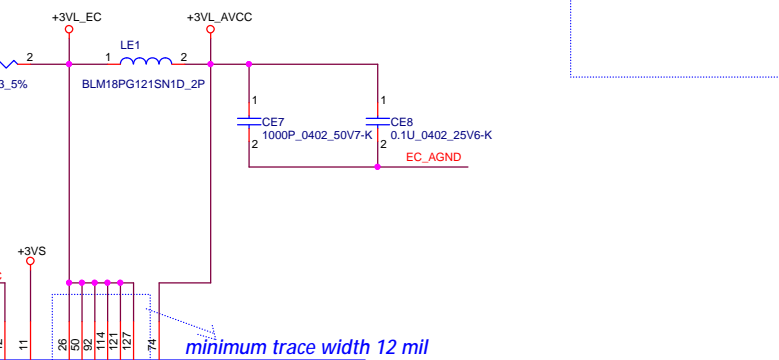
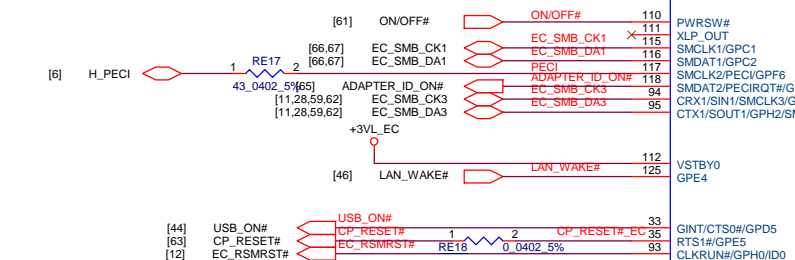
Close to EC



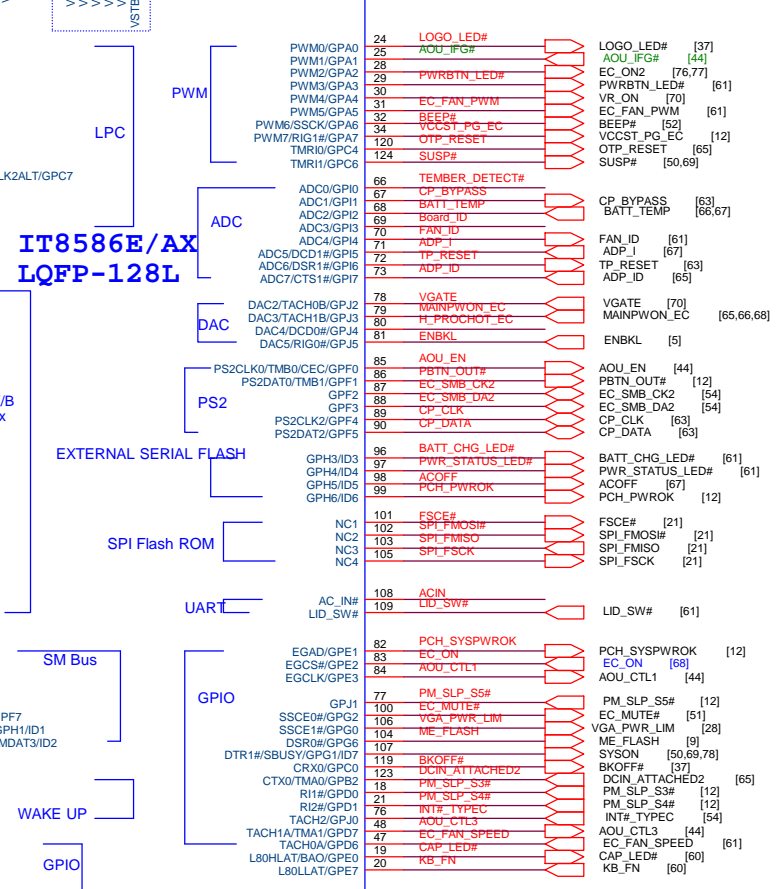
| Vcc | RE1 | RE2 | V _{AD_BID} min | V _{AD_BID} typ | V _{AD_BID} max | Phase |
|-------------|-------------|-------------|-------------------------|-------------------------|-------------------------|-------|
| 3.3V +/- 5% | 100K +/- 1% | 0K +/- 5% | 0 V | 0 V | 0 V | SDV |
| | | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | FVT |
| | | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | SIT |
| | | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | SVT |
| | | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V | |
| | | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V | |



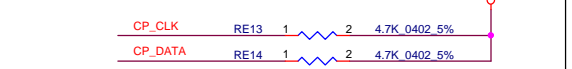
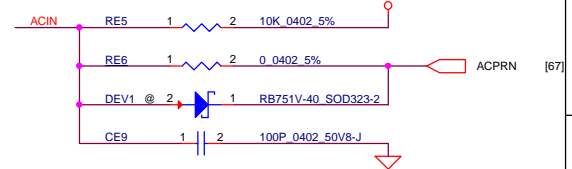
20160307
Stuff CE11 for WRST signal



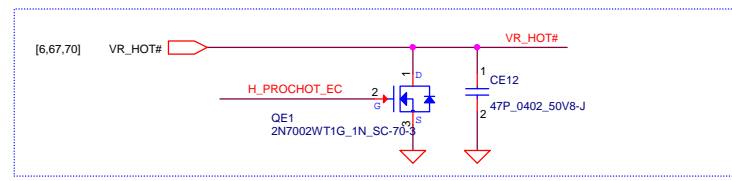
minimum trace width 12 mil



Please don't place any PU Resistor on GPG[7:2] (Reserve hardware strapping)



Un-stuff if not necessary.



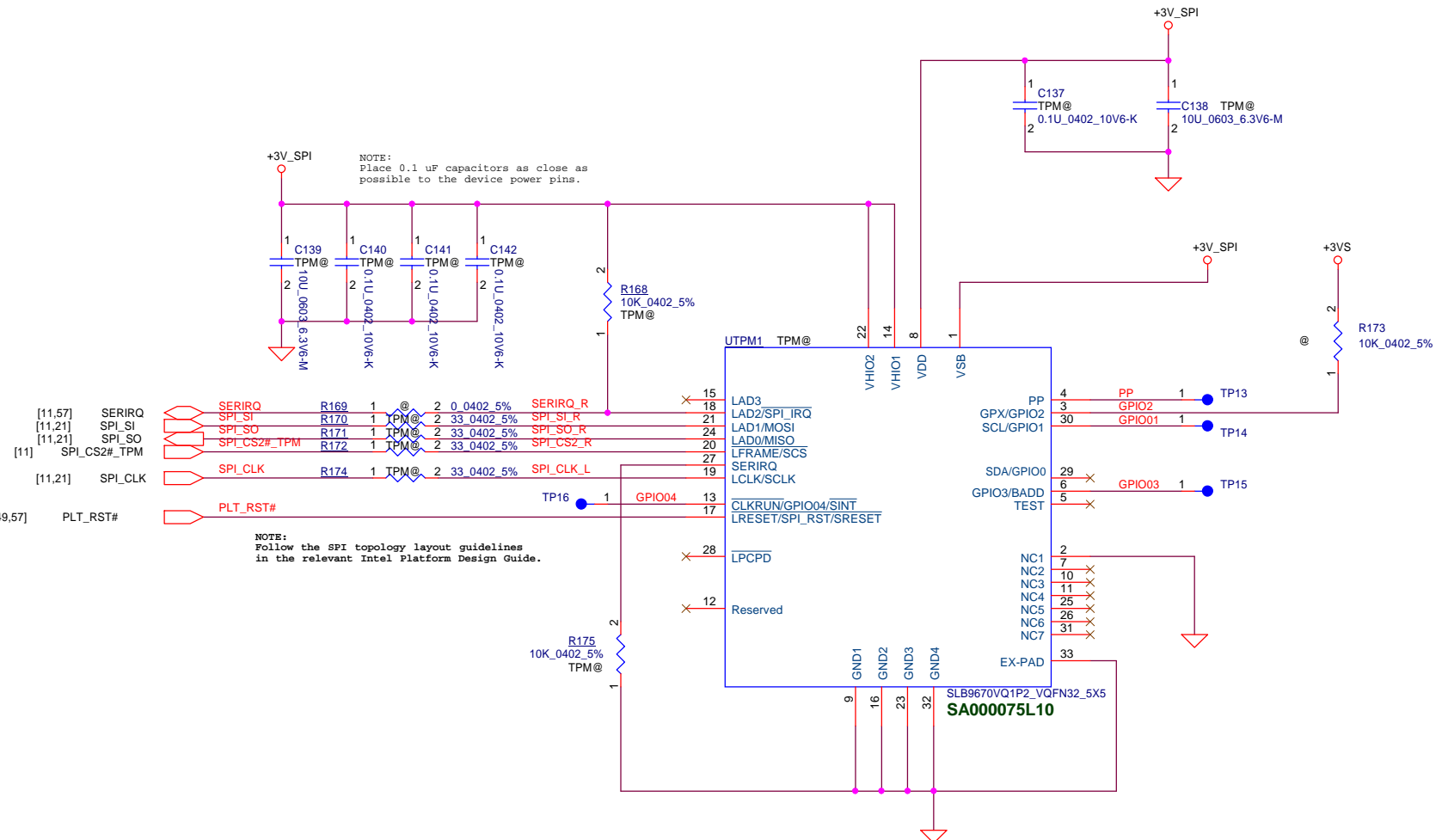
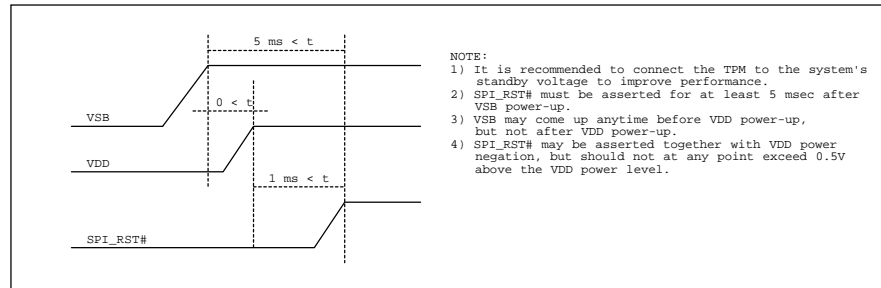
1. Version CX : Don't Support Mirror Code
Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)

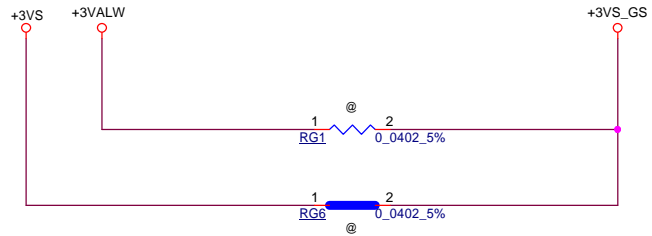
TPM IC

| Pin No | TCG PTP 9pins (+36) | Infineon SLB967VQ1.2 FW 6.10 | ST Micro ST32HTPM2E32AAB9 | Navteon NFCT63LD0YX |
|--------|---------------------|------------------------------|---------------------------|---------------------|
| 1 | VDD | VDD | NC | VSS |
| 2 | GND | GND | GND | NC |
| 3 | GPIO | NC | NC | GP3/GPIO2 |
| 4 | GPIO | NC | PP | PP |
| 5 | NC | NC | NC | TEST |
| 6 | VNC/GPIO | GPIO | NC | GPIO3 |
| 7 | GPIO/VDD | PP | GPIO | NC |
| 8 | VDD | VDD | NC | VDD |
| 9 | GND | GND | NC | GND |
| 10 | VNC | NC | NC | NC |
| 11 | NC | NC | NC | NC |
| 12 | NC | NC | NC | Reserved |
| 13 | VNC/GPIO | NC | NC | GPIO4 |
| 14 | VDD | NC | NC | VDD |
| 15 | NC | NC | NC | DNC |
| 16 | GND | NC | NC | GND |
| 17 | SPI_RST# | RST# | SPI_RST# | SPI_RST# |
| 18 | SPI_PIRQ# | PIRQ# | SPI_PIRQ# | SPI_IRQ# |
| 19 | SPI_CLK | SCLK | SPI_CLK | SCLK |
| 20 | SPI_CS# | CS# | SPI_CS# | SCS# |
| 21 | MOSI | MOSI | MOSI | MOSI |
| 22 | VDD | VDD | VPS | VDD |
| 23 | GND | GND | NC | GND |
| 24 | MISO | MISO | MISO | MISO |
| 25 | NC | NC | NC | NC |
| 26 | NC | NC | NC | NC |
| 27 | NC | NC | NC | (SERIRQ) |
| 28 | NC | NC | NC | DNC |
| 29 | VNC/GPIO | NC | NC | GPIO0 |
| 30 | VNC/GPIO | NC | NC | GPIO1 |
| 31 | VNC | NC | NC | NC |
| 32 | GND | GND | NC | GND |

Follow THP1_SWG_SIT_EC005, update TPM table

NOTE:
Check timing sequence in SDV phase.

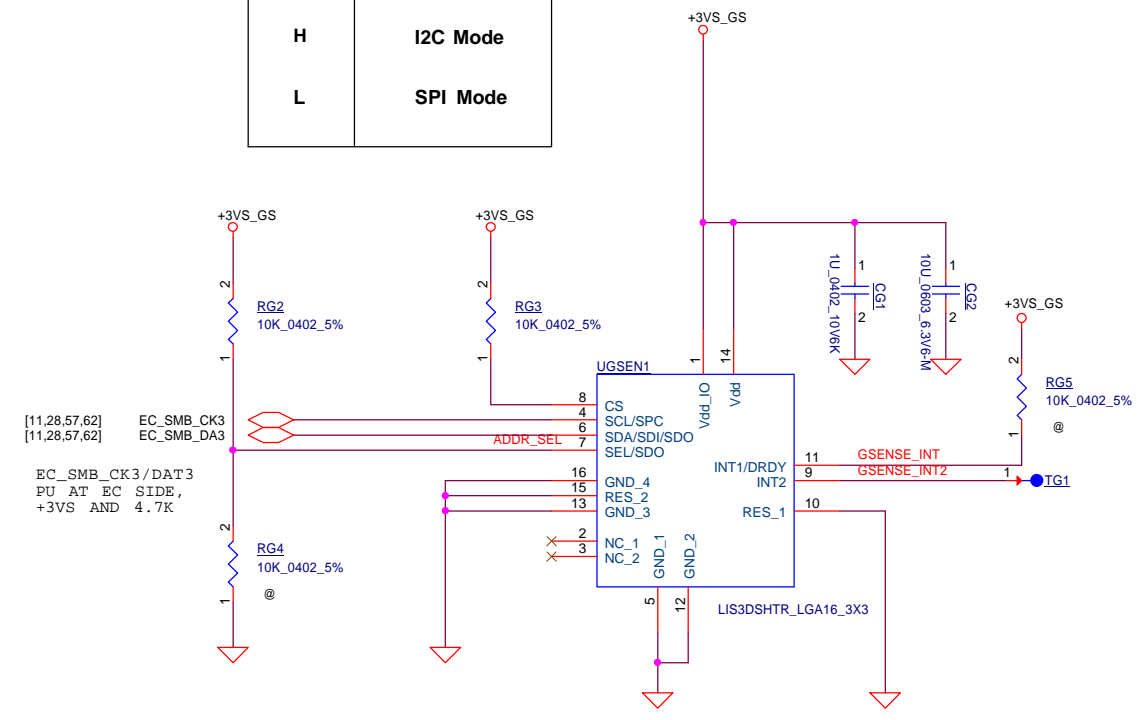




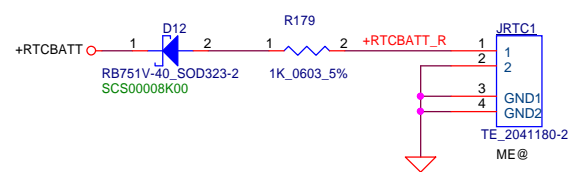
APS G-Sensor

| P/N | ADDR_SEL | Address |
|------------|----------|-------------------|
| LIS3DSHTR | H | 32h (W) & 33h (R) |
| | L | 30h (W) & 31h (R) |
| KX023-1025 | H | 3Eh (W) & 3Fh (R) |
| | L | 3Ch (W) & 3Dh (R) |

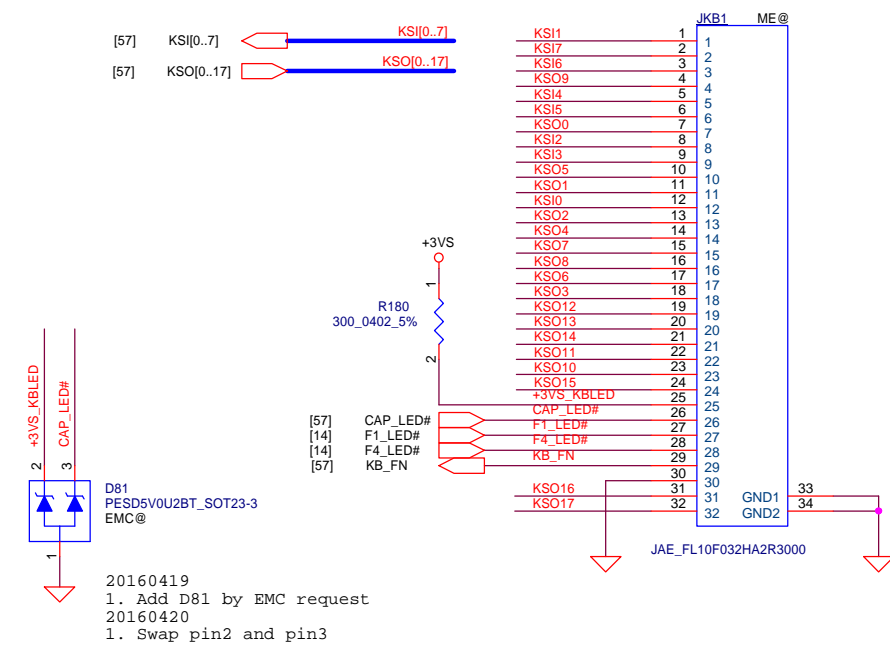
| P/N | Mode Selection |
|-----|----------------|
| H | I2C Mode |
| L | SPI Mode |



RTC CONN.

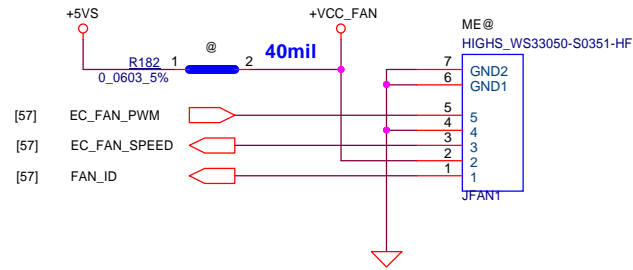


KB CONN

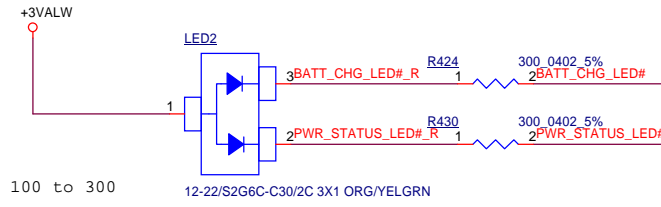


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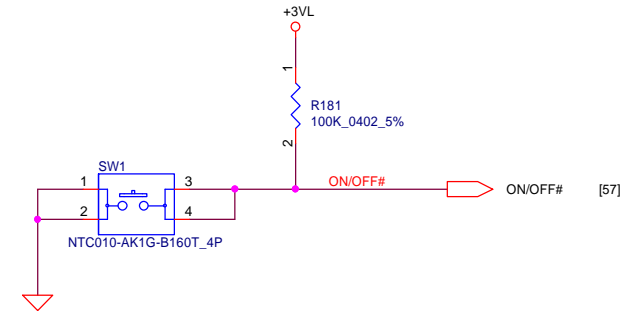
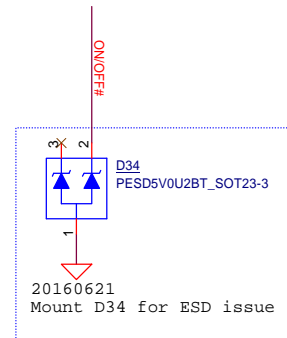
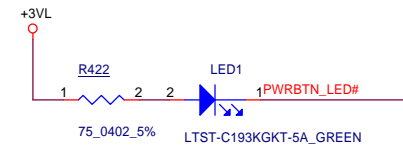
FAN CONN.



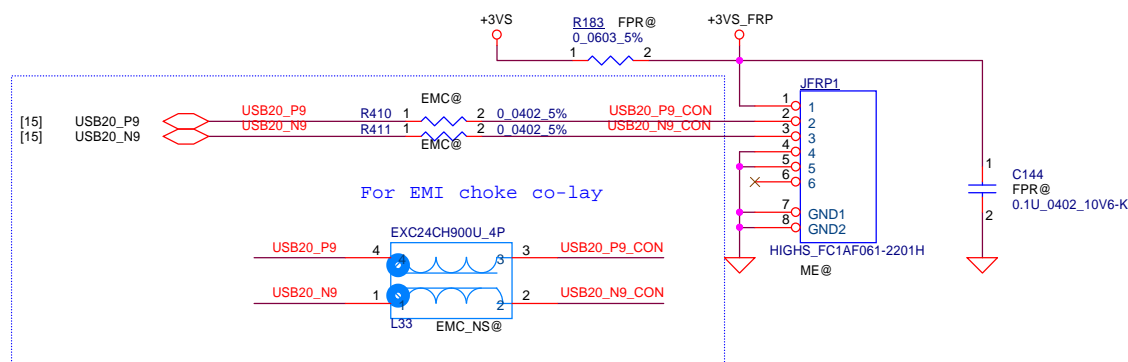
20160424
 1. Change R430/R423 from 100 to 300 ohm for LED brightness
 2. Change R422 from 100 to 75 ohm for LED brightness



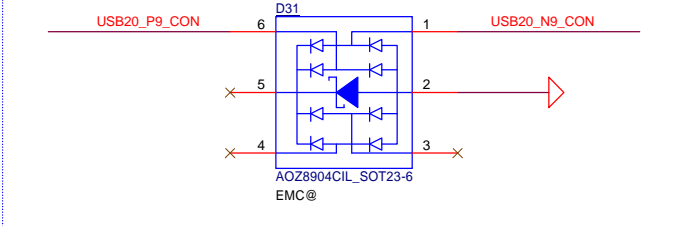
- [57] PWRBTN_LED# PWRBTN_LED#
- [57] BATT_CHG_LED# BATT_CHG_LED#
- [57] PWR_STATUS_LED# PWR_STATUS_LED#



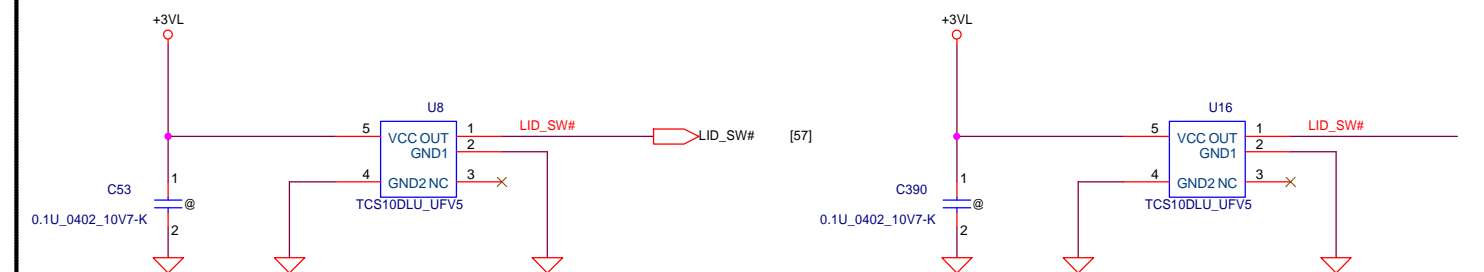
FingerPrint CONN.




ESD request

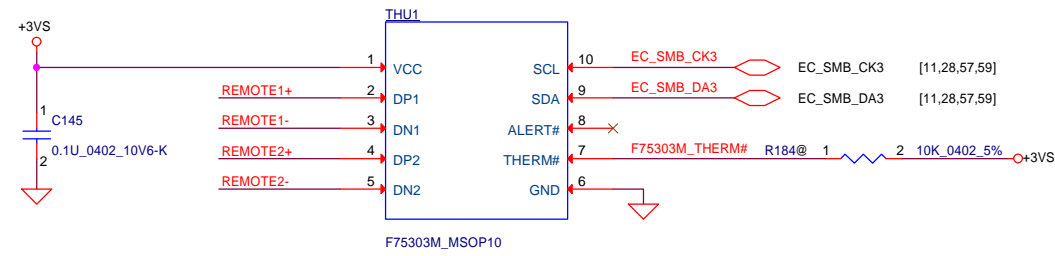


Lid Switch



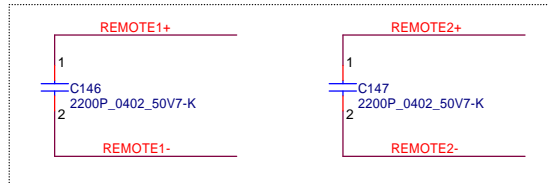
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|--|------------------------------|-----------------|------------|--|
| Security Classification | LC Future Center Secret Data | | Title |  |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | |
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| | | | | Rev 2.0 |

**Thermal Sensor
placed near by VRAM**

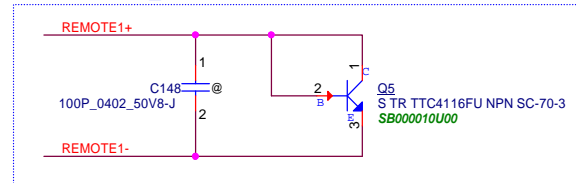


Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for init i d t her m# sh ut do wnt e mp

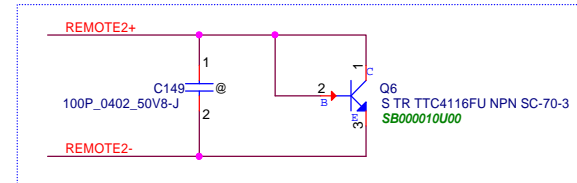
Close to U1



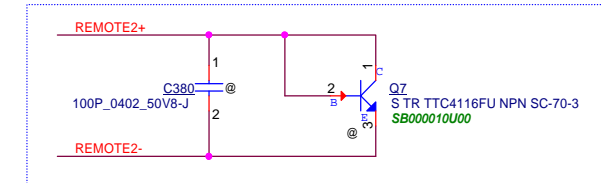
Close to +VCC_CORE



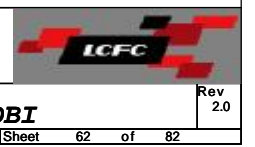
Close JDIMM1&JDIMM2

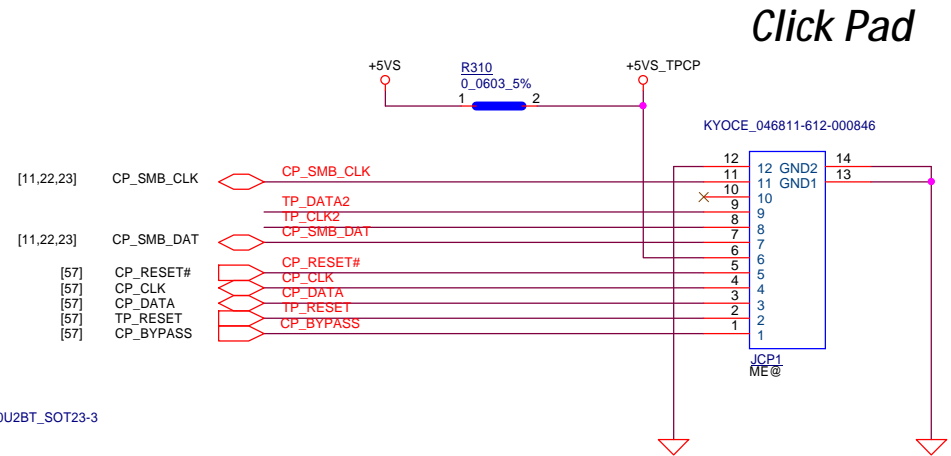
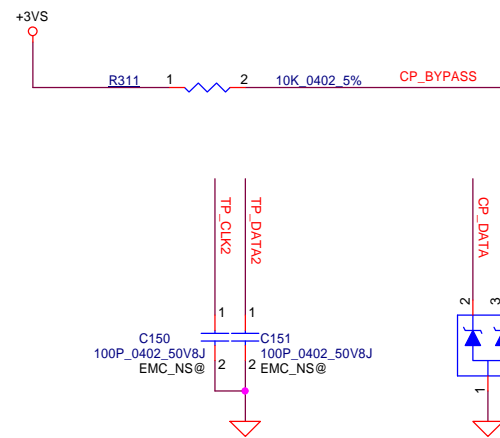
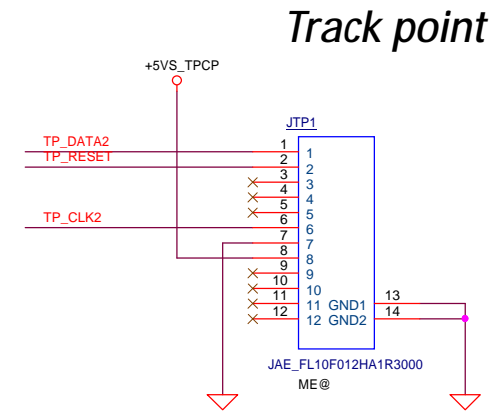
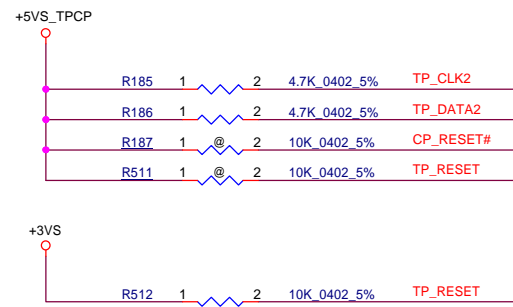


*REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"*



| | | | | | |
|---|------------------------------|-----------------|------------|--------------------------------|------------------------------------|
| Security Classification | LC Future Center Secret Data | | | Title Thermal Sensor | Rev 2.0 |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | | |
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| | | | | Sheet 62 | of 82 |

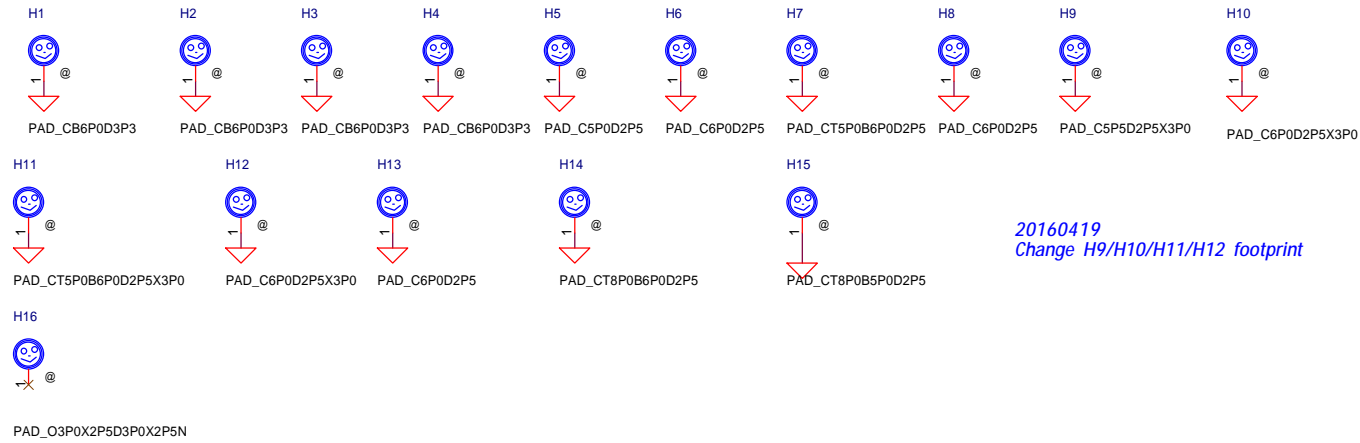




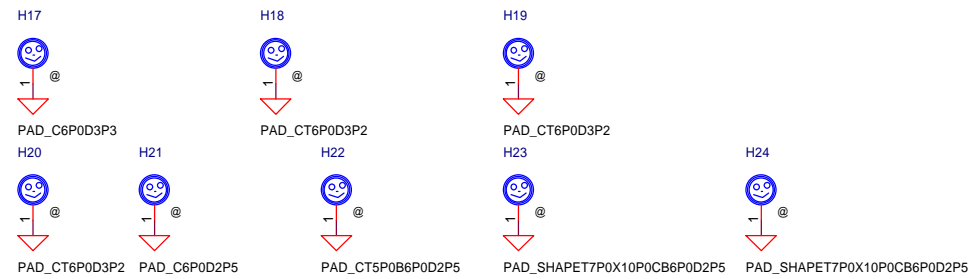
20160419
 1. Add D81 by EMC request
 2. Delete D66 and connect to C150/C151

20160414
 1. Change JCP1 foot print

Screw Hole



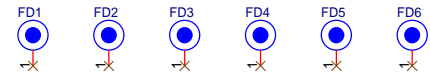
20160419
Change H9/H10/H11/H12 footprint



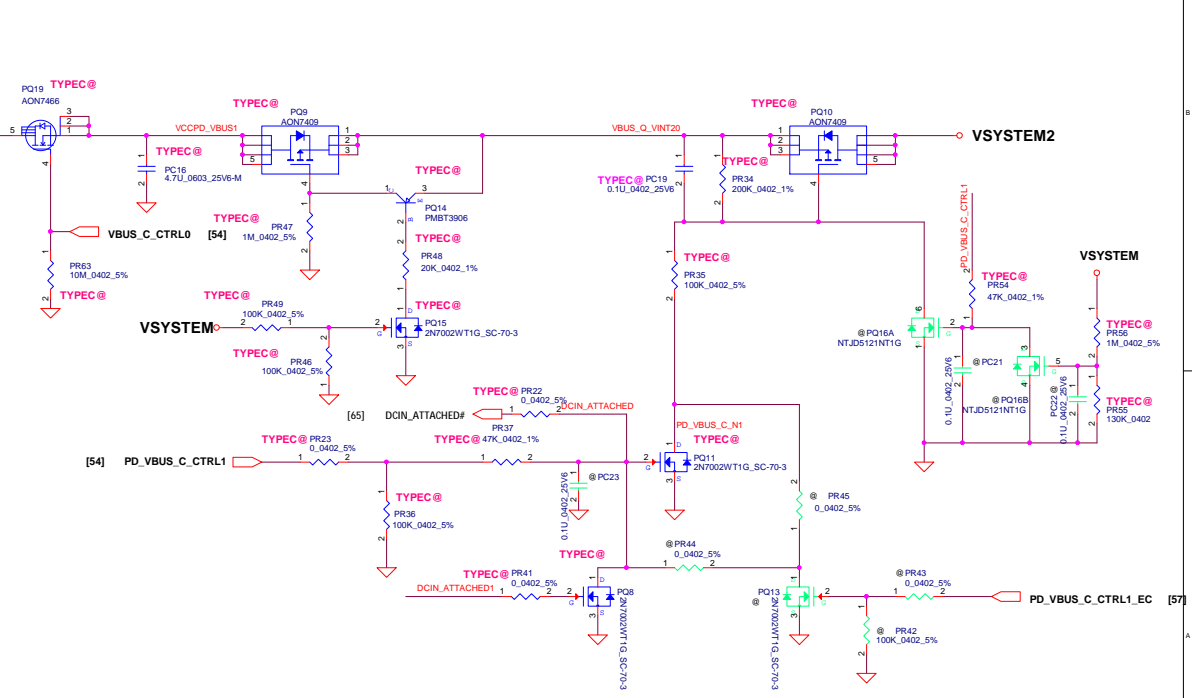
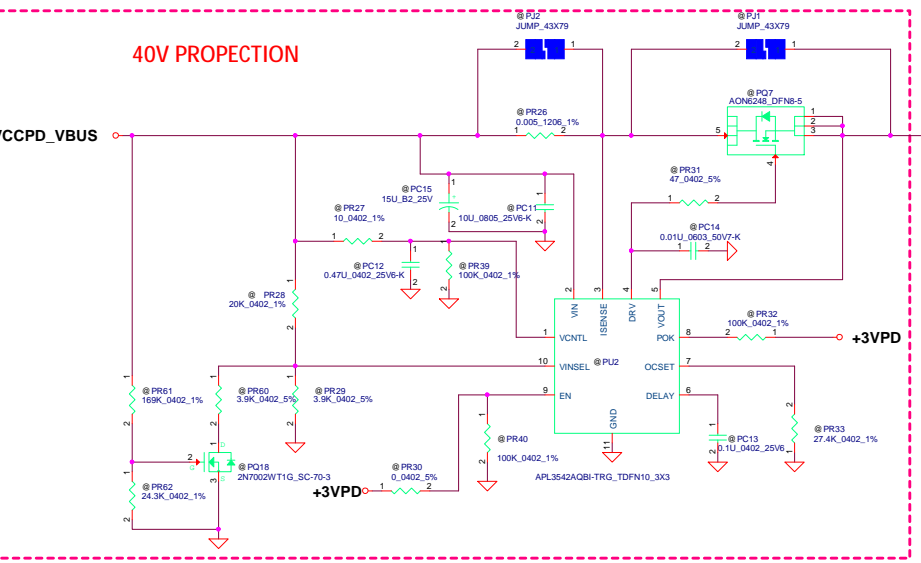
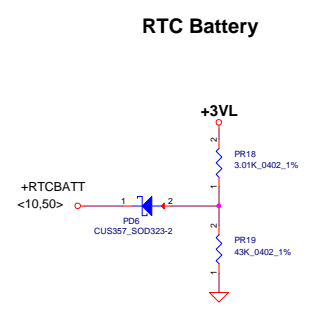
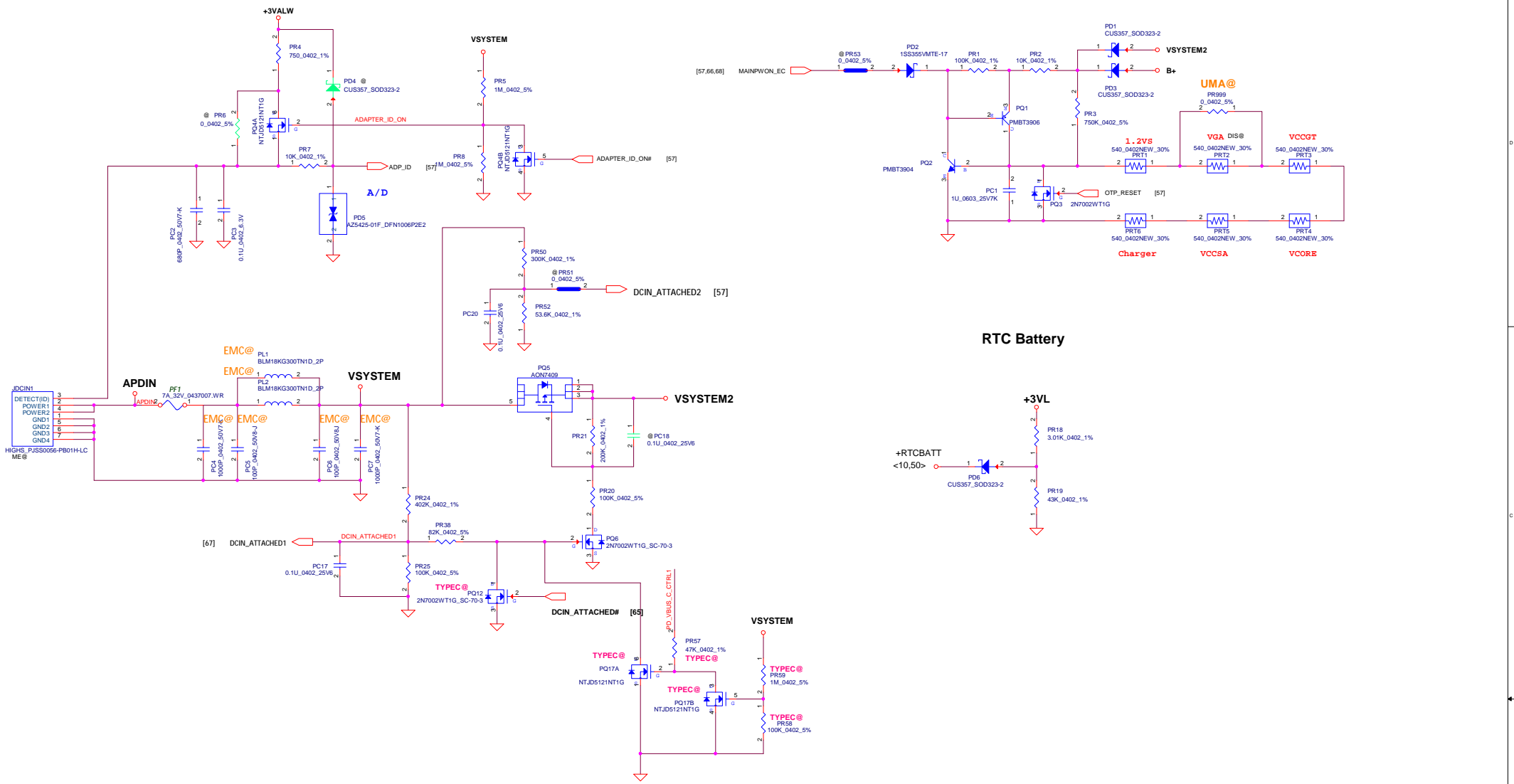
Center Zero

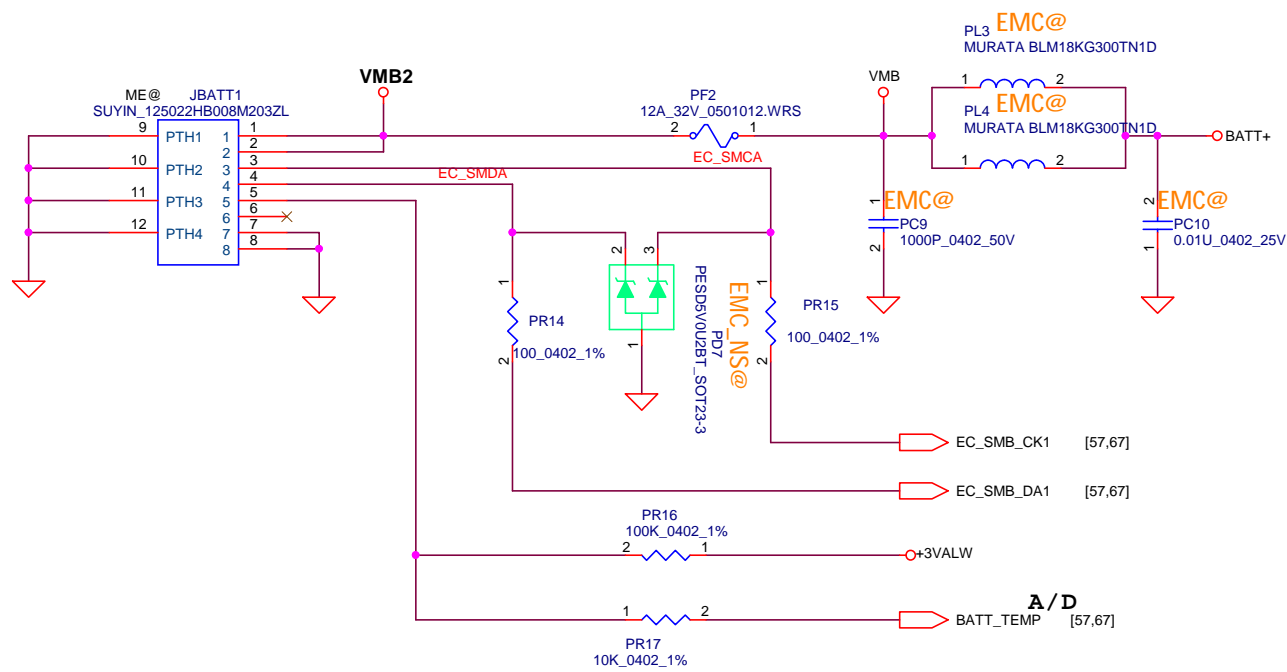


PCB Fedical Mark PAD

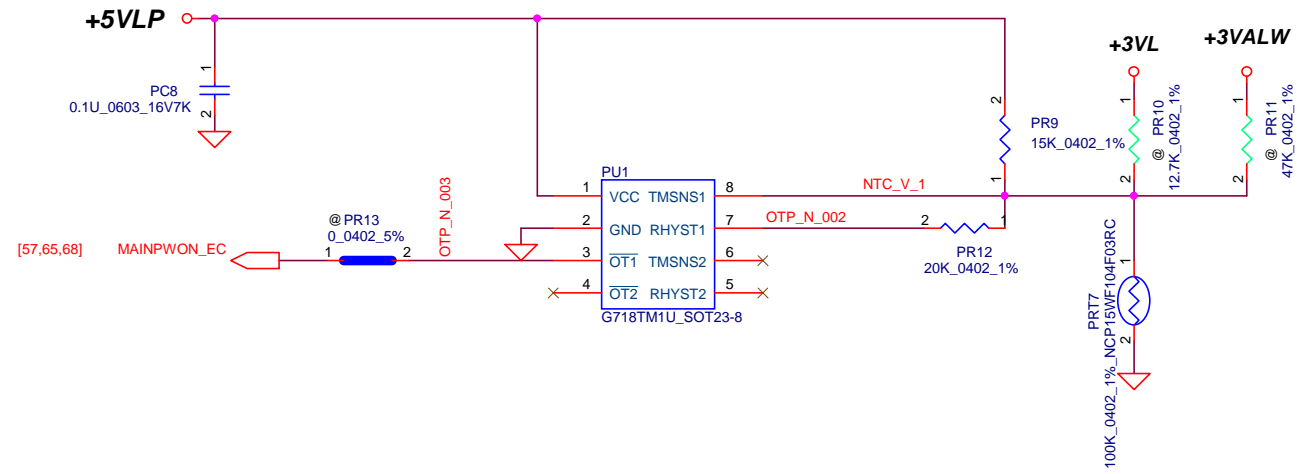



| | | | | |
|---|------------------------------|-----------------|------------|--|
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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 | |
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| | | | | Document Number KENOBI |
| | | | | Rev 2.0 |
| | | | | Date: Thursday, August 25, 2016 Sheet 64 of 82 |

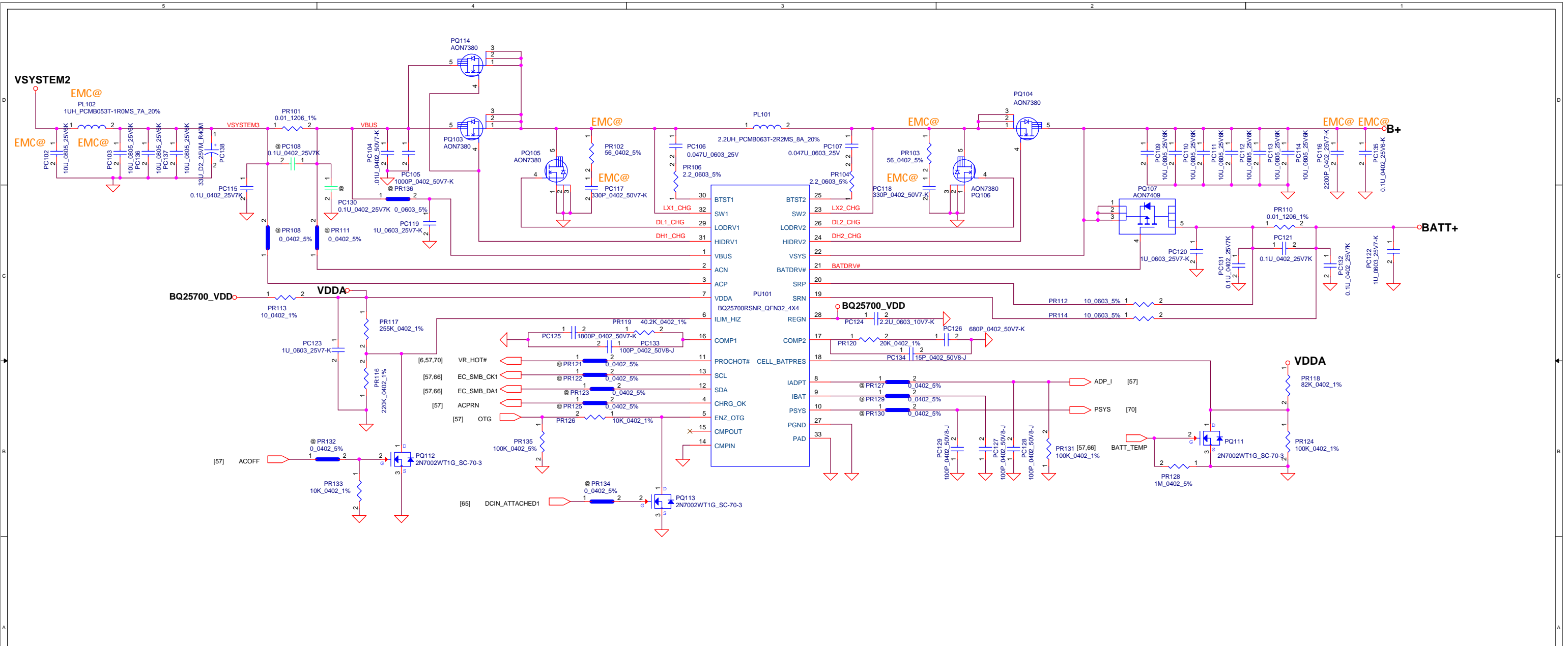





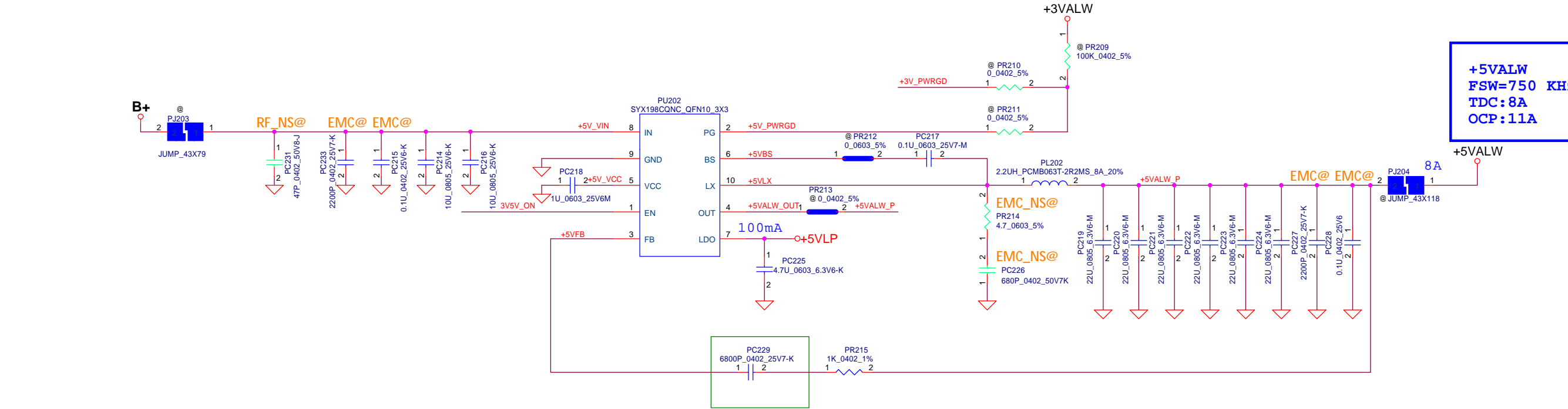
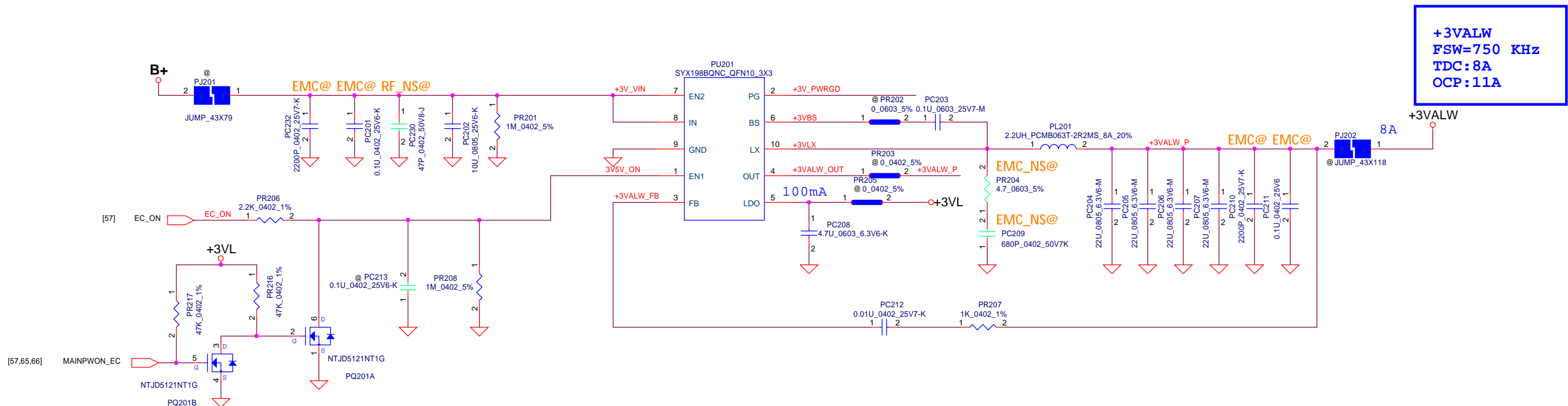
**PRT7 under CPU bottom side for CPU thermal protection.
This is for thermal team request.**



| | | | | | | | |
|---|------------------------------|-----------------|------------|------------------|---|---------------------------|----------------|
| Security Classification | LC Future Center Secret Data | | | Title |  | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 | BATTERY CONN/OTP | | | |
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| | | | | | Custom | KENOBI | 2.0 |
| | | | | | Date: | Thursday, August 25, 2016 | Sheet 66 of 82 |

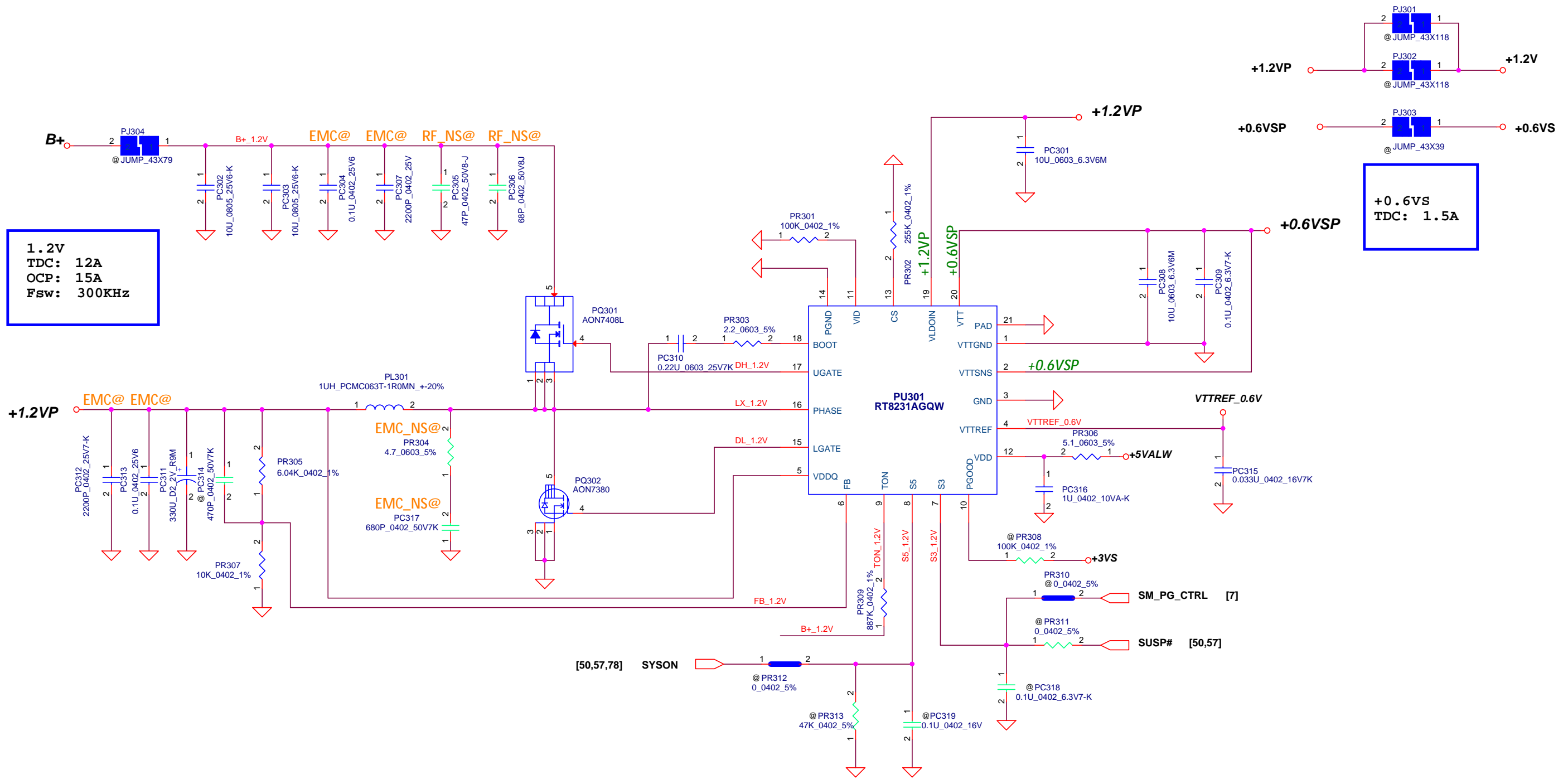


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|---|------------------------------|-----------------|------------|--|
| Security Classification | LC Future Center Secret Data | | Title |  |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 | |
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| | | | | Rev: 2.0 |



6800pf soft start 2ms
47nf soft start 7ms

| | | | | | |
|---|-----------------|------------------------------|------------|---------------------------|----------------|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | 3VALWP/5VALWP | |
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| Size | Document Number | Rev | | 2.0 | |
| Custom | KENOBI | Date: | | Thursday, August 25, 2016 | Sheet 68 of 82 |

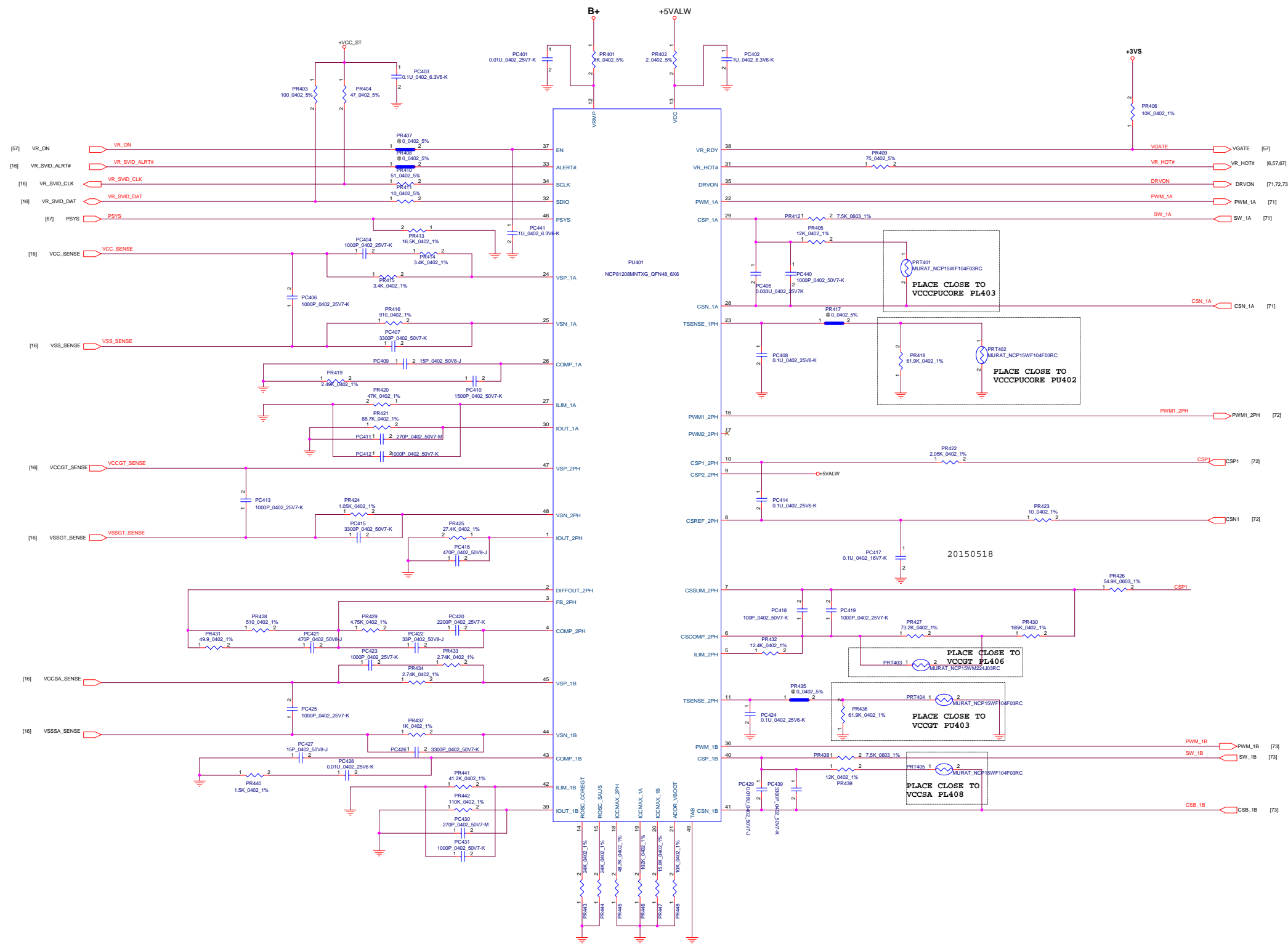


1.2V
TDC: 12A
OCP: 15A
Fsw: 300KHz

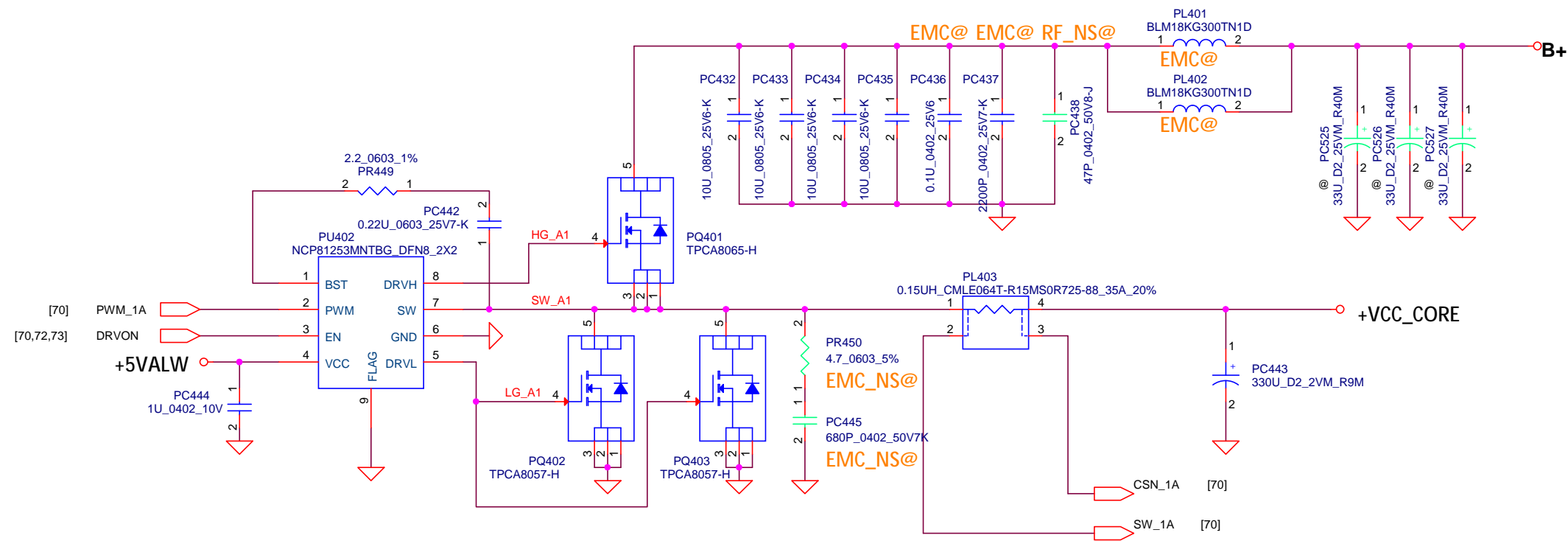
+0.6VS
TDC: 1.5A

| | | | |
|--|------------------------------|-----------------|--|
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| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |
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| | | | Document Number KENOBI |
| | | | Rev 2.0 |
| | | | Date: Thursday, August 25, 2016 Sheet 69 of 82 |




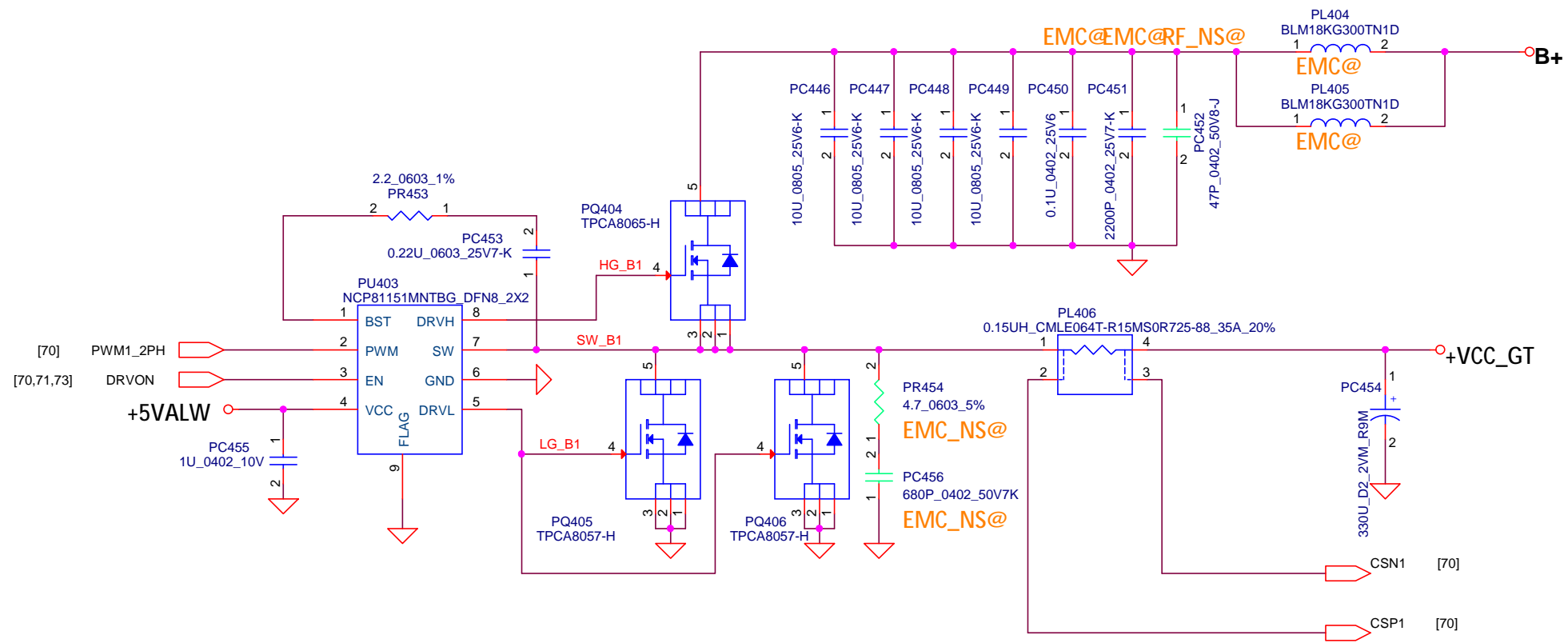


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|---|------------------------------|-----------------|------------|--------------------------------|
| Security Classification | LC Future Center Secret Data | | Title | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 | |
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| Date: Thursday, August 26, 2013 | | | | Sheet 70 of 82 |



+VCC_CORE
 TDC= 21A
 IccMAX=31A
 OCP = 36A


| | | | | |
|--|------------------------------|-----------------|------------|---|
| Security Classification | LC Future Center Secret Data | | Title |  |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 | |
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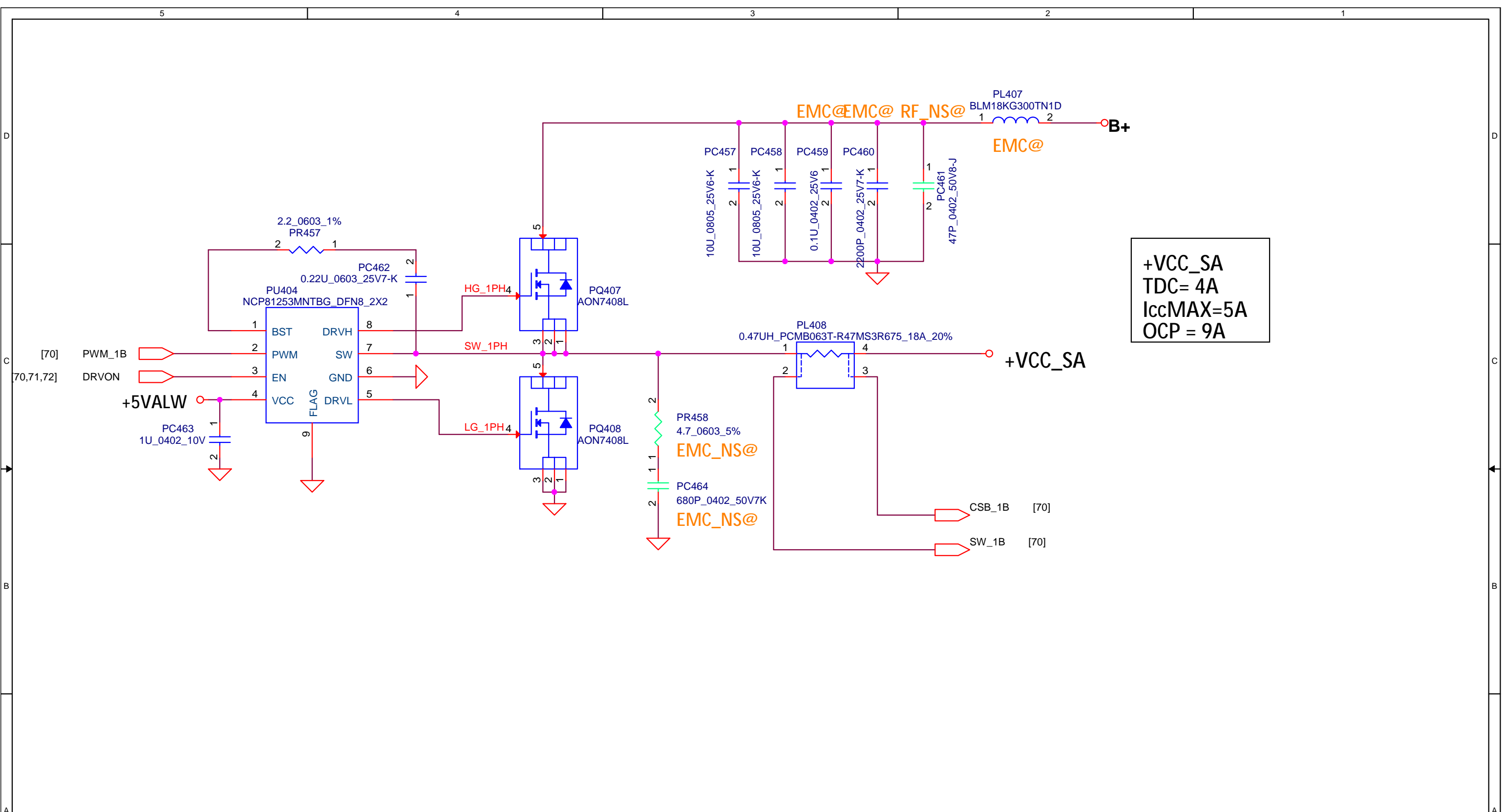
+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

| | | |
|-------------------------|------------------------------|----------------------------|
| Security Classification | LC Future Center Secret Data | |
| Issued Date | 2013/08/05 | Deciphered Date 2014/12/31 |


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| | | |
|---------------------------------|-----------------|---|
| Title | |  |
| +VCC_GT | | |
| Size Custom | Document Number | Rev 2.0 |
| Date: Thursday, August 25, 2016 | | Sheet 72 of 82 |

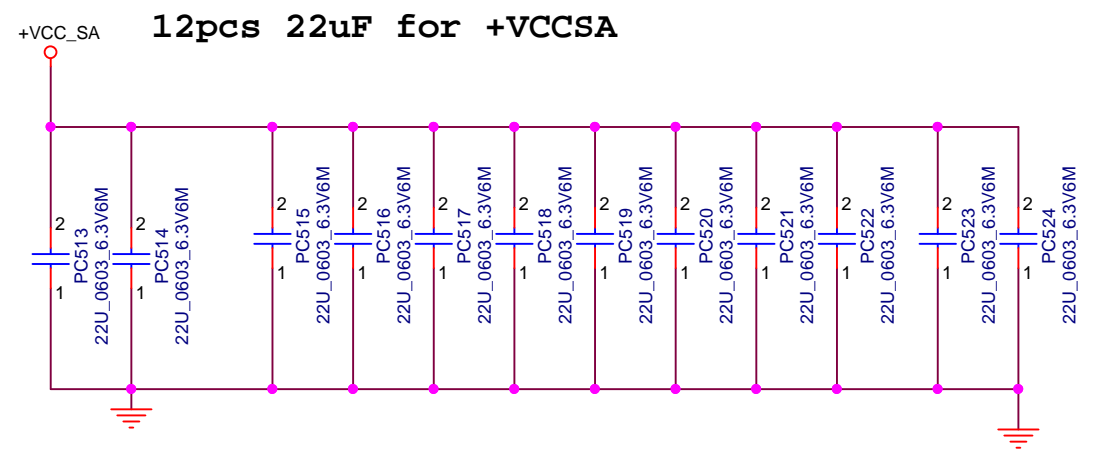
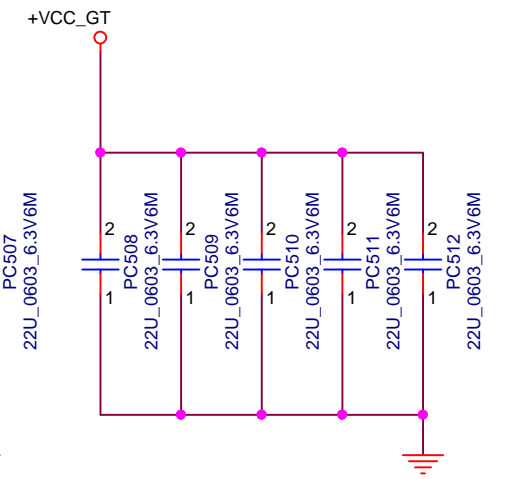
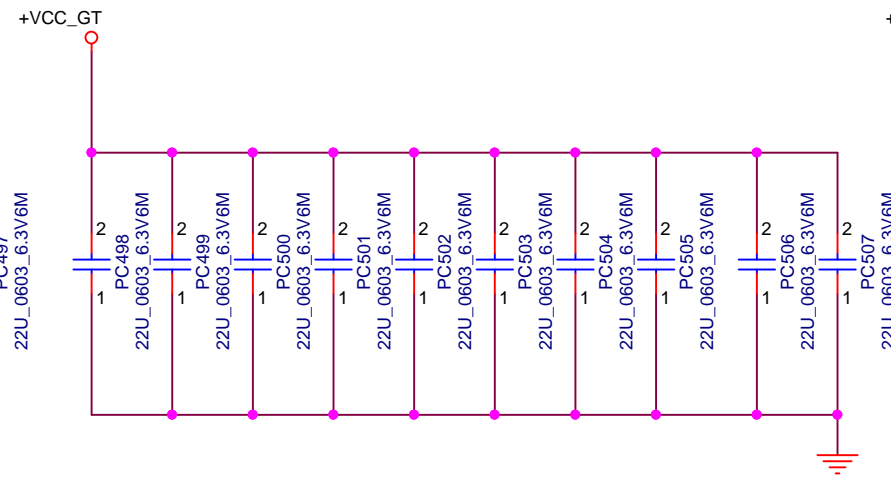
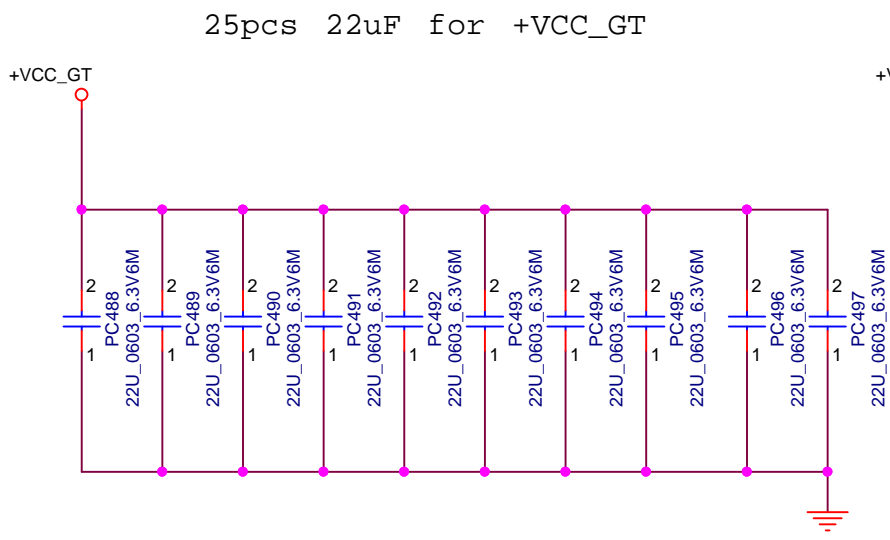
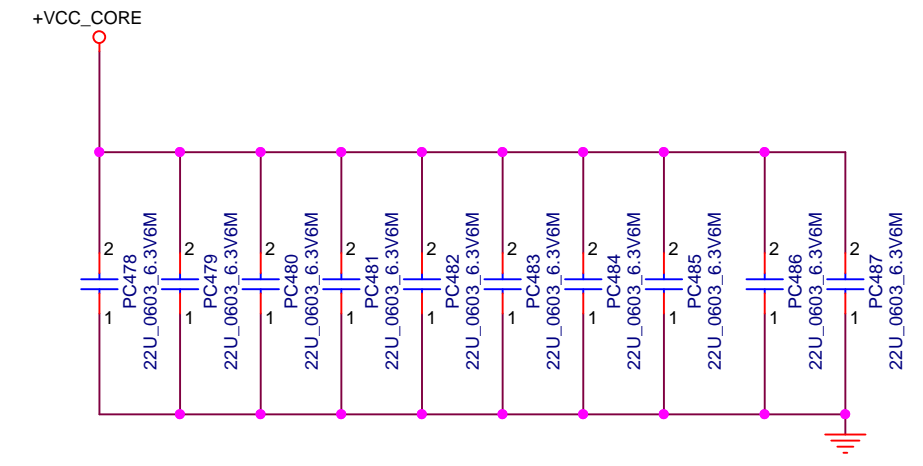
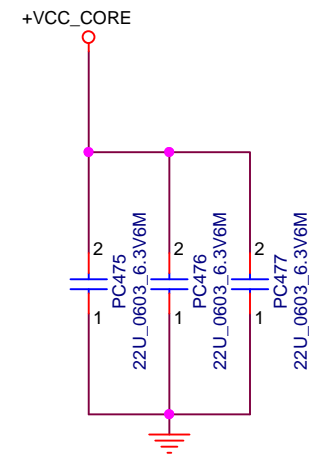
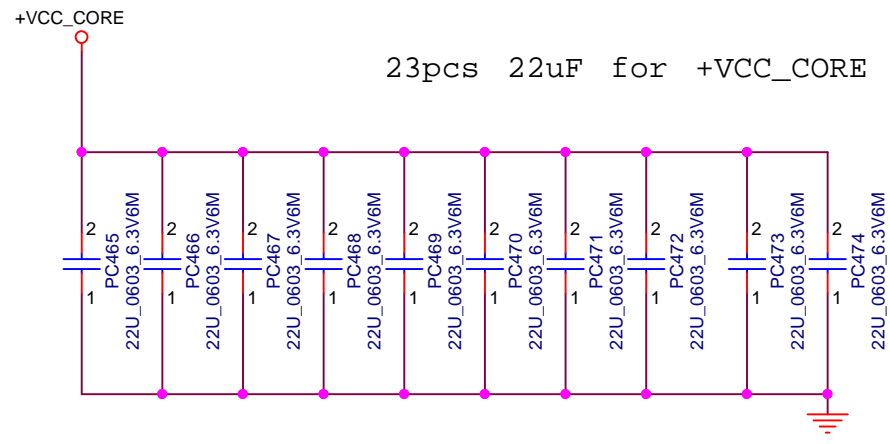
KENOBI




+VCC_SA
TDC= 4A
IccMAX=5A
OCP = 9A

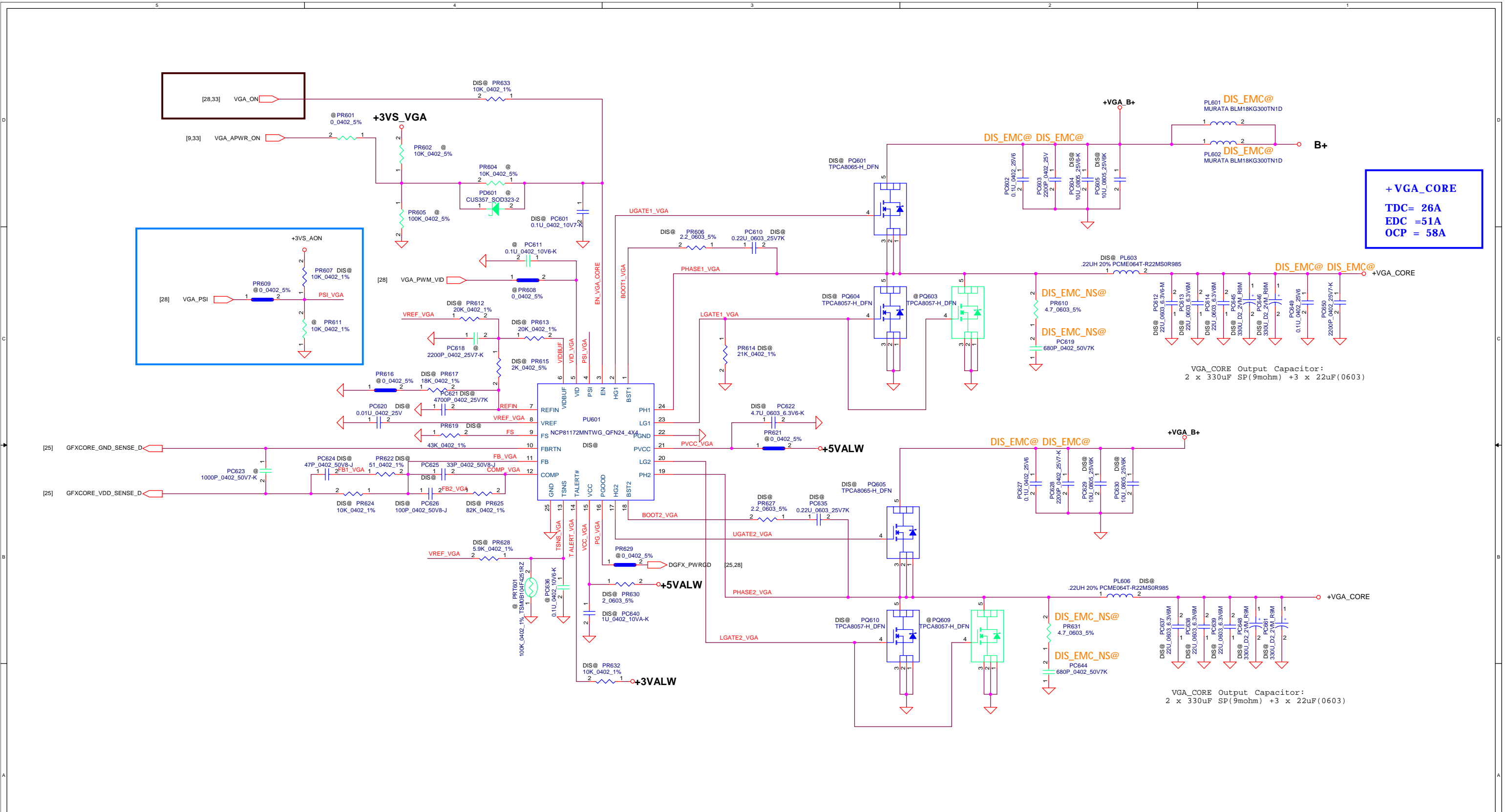
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|--|---------------------------|------------------------------|------------|---------|---------|---|
| Security Classification | | LC Future Center Secret Data | | Title | |  |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 | +VCC_SA | | |
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| Size Custom | Document Number | | | | Rev 2.0 | |
| Date: | Thursday, August 25, 2016 | | Sheet | 73 | of | 82 |


Based on PDDG rev 0.7 Table 5-1.

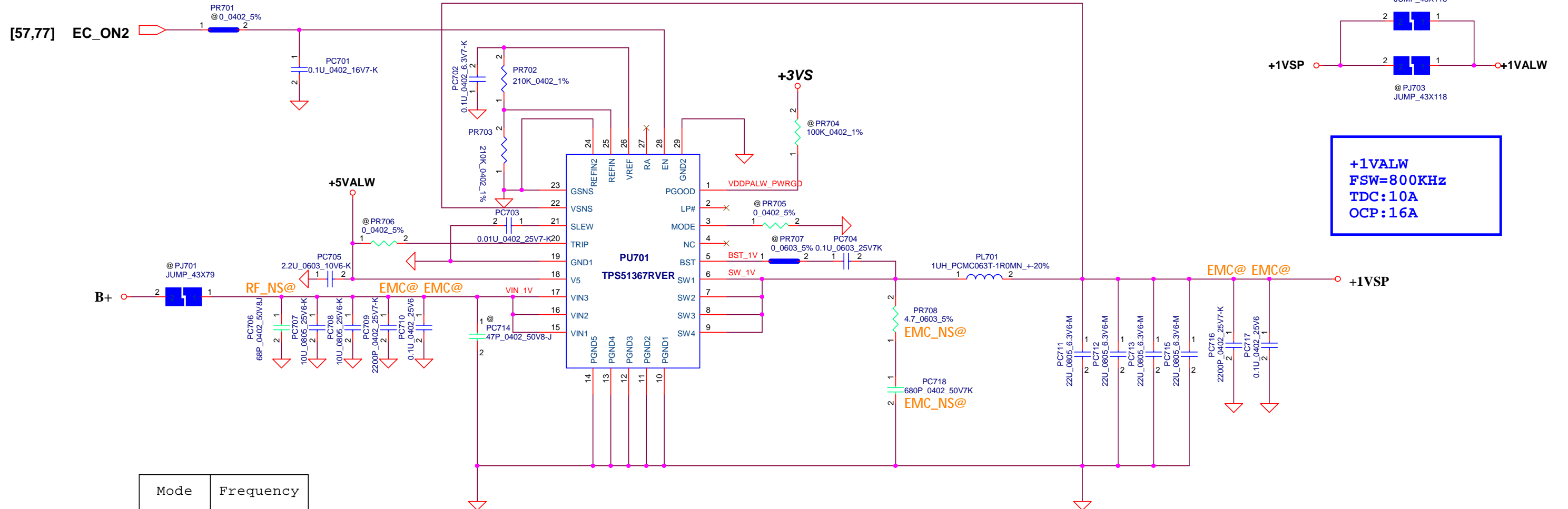


| | | |
|---|------------------------------|-----------------|
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| Issued Date | 2013/08/05 | Deciphered Date |
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| | | |
|----------------------|---------------------------|---|
| Title | |  |
| PROCESSOR DECOUPLING | | |
| Size | Document Number | Rev |
| B | | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet 74 of 82 |

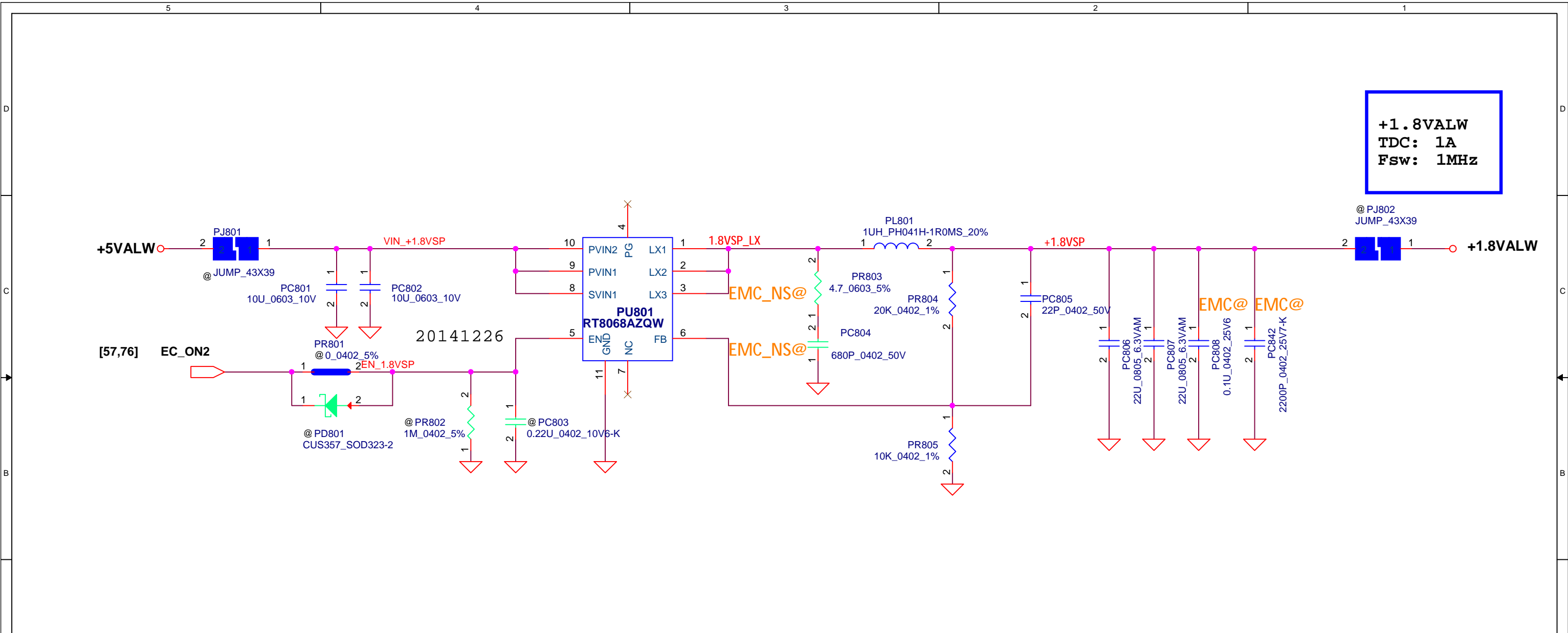


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|---|------------------------------|-----------------|------------|--|
| Security Classification | LC Future Center Secret Data | | Title |  VGA_CORE(NCP81174) |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | |
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| Mode | Frequency |
|-------|-----------|
| GND | 400KHz |
| Float | 800KHz |

| | | | | |
|--|------------------------------|-----------------|------------------------|---|
| Security Classification | LC Future Center Secret Data | | Title +1VALW |  |
| Issued Date | 2013/08/01 | Deciphered Date | | |
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| Size Custom | Document Number | KENOBI | | Rev 2.0 |
| Date: | Thursday, August 25, 2016 | | Sheet | 76 of 82 |

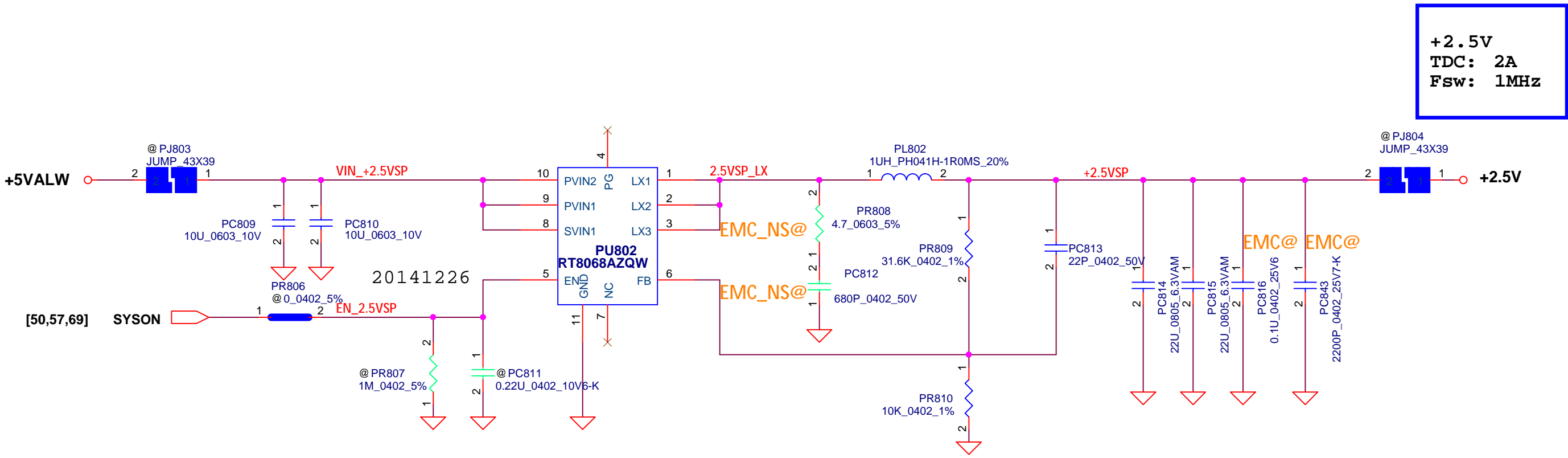


+1.8VALW
TDC: 1A
Fsw: 1MHz


| | | |
|-------------------------|------------------------------|-----------------|
| Security Classification | LC Future Center Secret Data | |
| Issued Date | 2013/08/05 | Deciphered Date |
| | | 2014/12/31 |

| | | |
|----------|---------------------------|---|
| Title | |  |
| +1.8VALW | | |
| Size | Document Number | Rev |
| Custom | KENOBI | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet 77 of 82 |

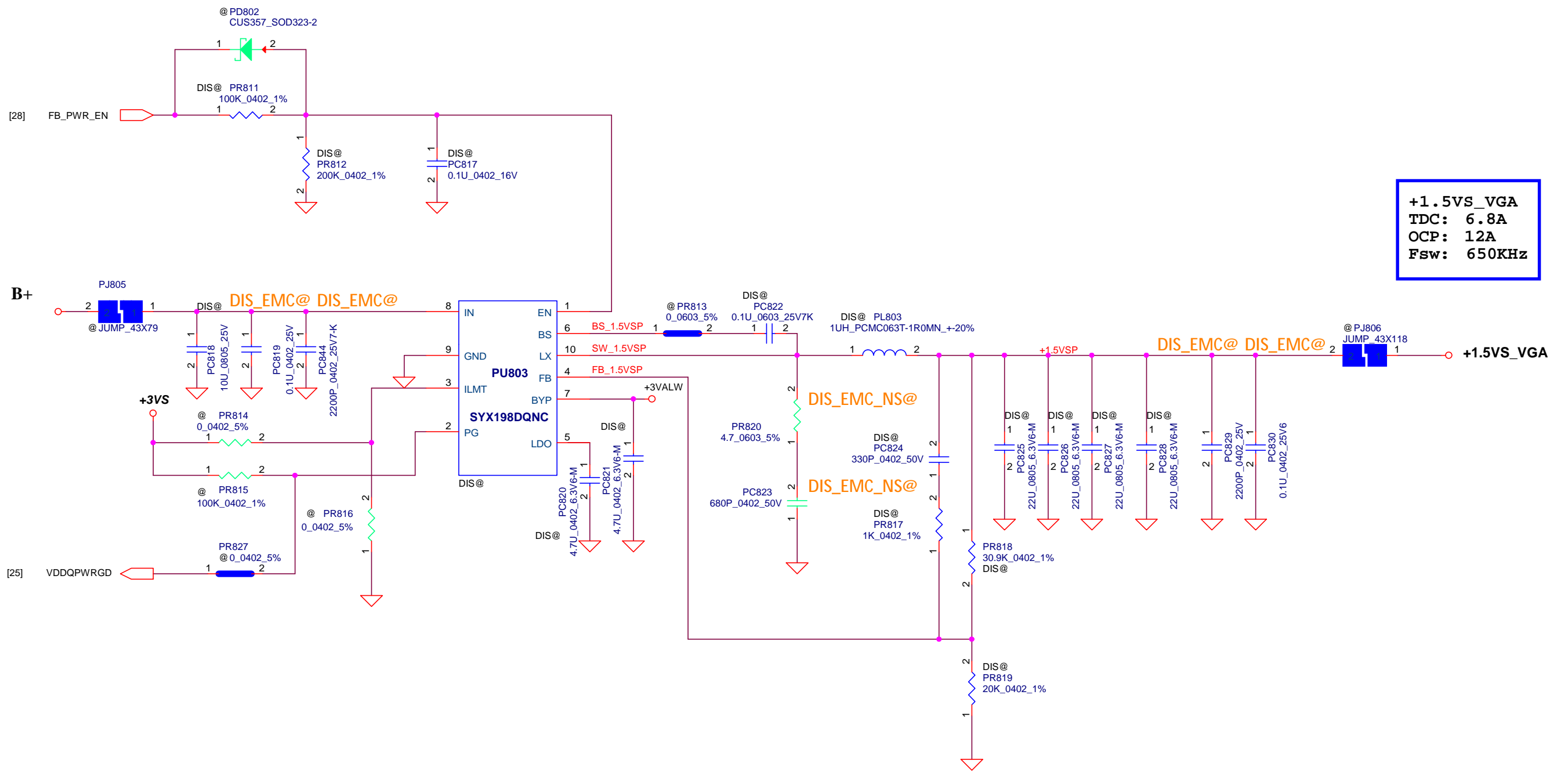
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| Security Classification | LC Future Center Secret Data | |
| Issued Date | 2013/08/05 | Deciphered Date |
| | | 2014/12/31 |

| | | |
|--------|---------------------------|---|
| Title | |  |
| +2.5V | | |
| Size | Document Number | Rev |
| Custom | KENOBI | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet 78 of 82 |

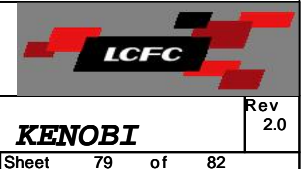
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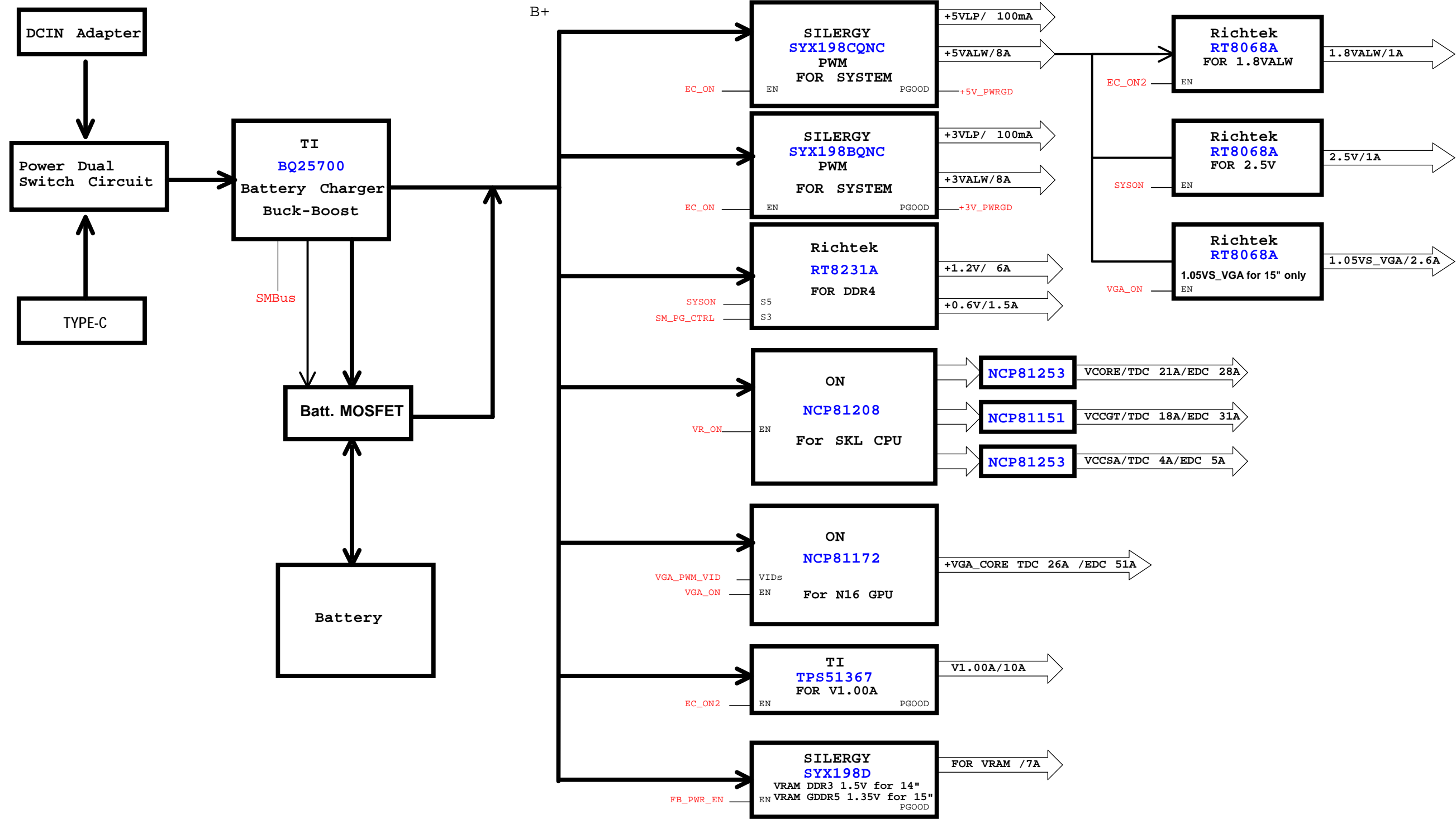


+1.5VS_VGA
 TDC: 6.8A
 OCP: 12A
 Fsw: 650KHz

| | | |
|---|------------------------------|-----------------|
| Security Classification | LC Future Center Secret Data | |
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