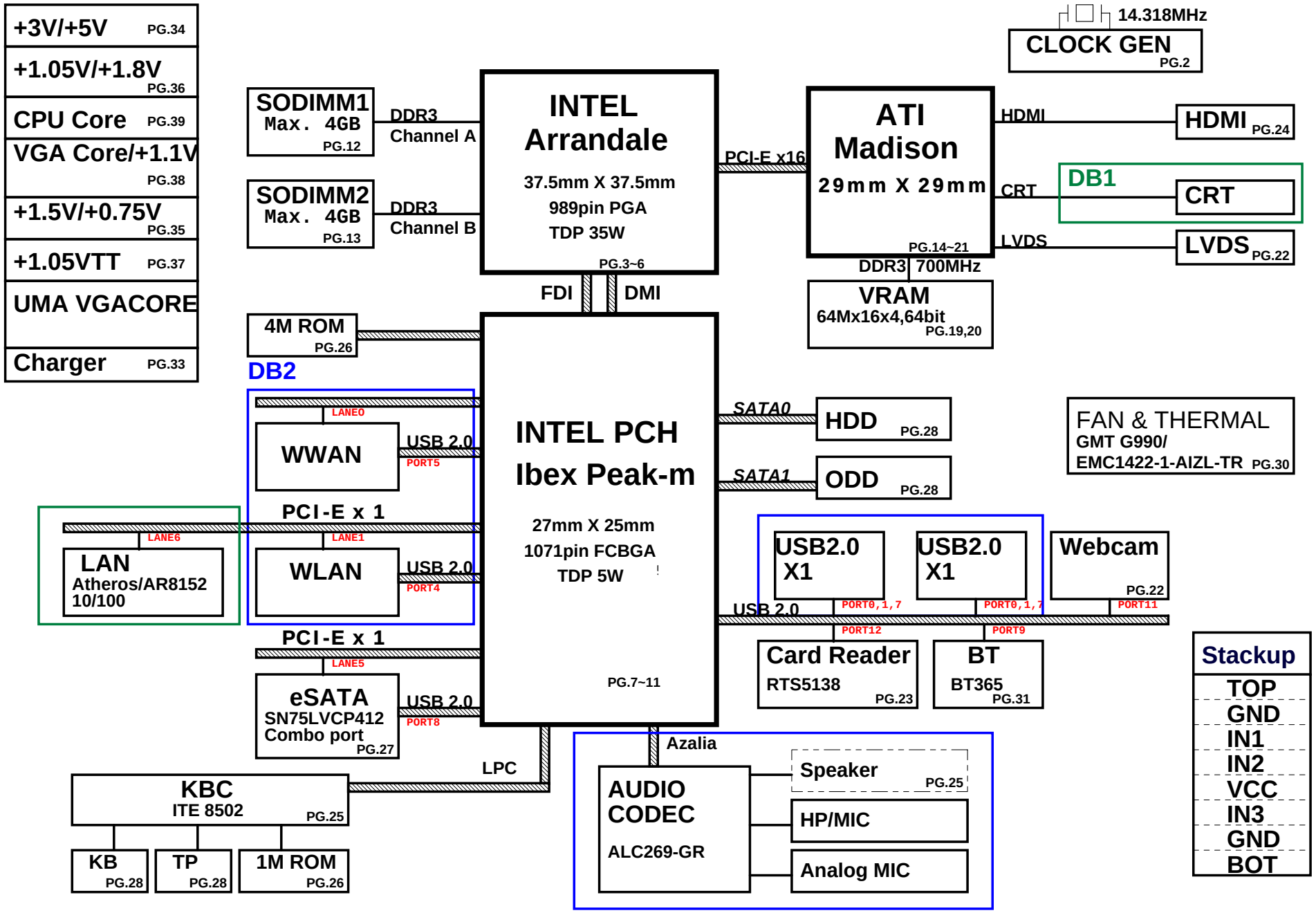
UM8B DIS SYSTEM DIAGRAM



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Wednesday, February 10, 2010 Sheet 1 of 46

02

25mA

+1.05V_PCH — L25 HCB1608KF-181T15_6 — +VDDIO_CLK

C327 0.1U/ 10V/X7R
C320 0.1U/ 10V/X7R
C323 10U/6.3V 8/X5R

Place each 0.1uF cap close to pin

8/20 Wait Victor check

300mA

+3.3V_RUN — L27 HCB1608KF-181T15_6 — +VDDSE_CLK

C352 10U/6.3V 8/X5R
C336 0.1U/ 10V/X7R
C353 0.1U/ 10V/X7R
C354 0.1U/ 10V/X7R
C322 0.1U/ 10V/X7R
C321 0.1U/ 10V/X7R

Place each 0.1uF cap close to pin

PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint

58

U10 — 9LRS3197 — QFN32

+VDDSE_CLK → VDD_LCD, VDD_REF
+VDDIO_CLK → VDD_CPU_IO, VDD_SRC_IO
VDD_USB, VDD_SRC, VDD_CPU

18,25,30 SMBDAT2 → SDATA
18,25,30 SMBCLK2 → SCLK

+3.3V_RUN — R196 10K — R213 33/J_4 — CPU_SEL
8 CLK_PCH_14M → CLK_PCH_14M — C338 *10P/50V_4_NC/COG

Place R8044 within 0.5" of C/G

CK_PWRGD_R → CK_PWRGD/PD#_3.3
XTAL_OUT, XTAL_IN → XOUT, XIN
CPU_STOP#, REF_0/CPU_SEL
VSS_SATA, VSS_USB, VSS_LCD

CPU-0, CPU-0# → CLK_BUF_BCLKP_R, CLK_BUF_BCLKN_R
CPU-1, CPU-1#
DOT96T_LPR, DOT96C_LPR → CLK_BUF_DREFCLKP_R, CLK_BUF_DREFCLKN_R
SRC-1, SRC-1# → CLK_BUF_PCIE_3GPLLP_R, CLK_BUF_PCIE_3GPLLN_R
SATA, SATA# → CLK_BUF_DREFSSCLKP_R, CLK_BUF_DREFSSCLKN_R
27MHz_nonSS, 27MHz_SS → CLK_VGA_27M_NOSS, CLK_VGA_27M_SS
GND, VSS_REF, VSS_CPU, VSS_SRC

Place within 0.5" of C/G

RP5 0X2 → CLK_BUF_BCLKP 8, CLK_BUF_BCLKN 8
RP8 0X2 → CLK_BUF_DREFCLKP 8, CLK_BUF_DREFCLKN 8
RP6 0X2 → CLK_BUF_PCIE_3GPLLP 8, CLK_BUF_PCIE_3GPLLN 8
RP7 0X2 → CLK_BUF_DREFSSCLKP 8, CLK_BUF_DREFSSCLKN 8

R217 33/J_4
R216 *33/J_4_NC
EVGA-XTALI 15
CLK_27M_SS 15

Discrete only

C351 *10P/50V_4_NC/COG

+3.3V_RUN — R212 *10K_NC — CPU_SEL — R209 10K

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

BOM check

+3.3V_RUN — R199 1K/J_4 — CK_PWRGD_R
Q13 FDN357N
39 VR_PWRGD_CLKEN# → 2
R201 *100K/F_4_NC

Y1 14.318MHZ
XTAL_IN — C330 33P/50V_4/NPO
XTAL_OUT — C328 33P/50V_4/NPO

SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

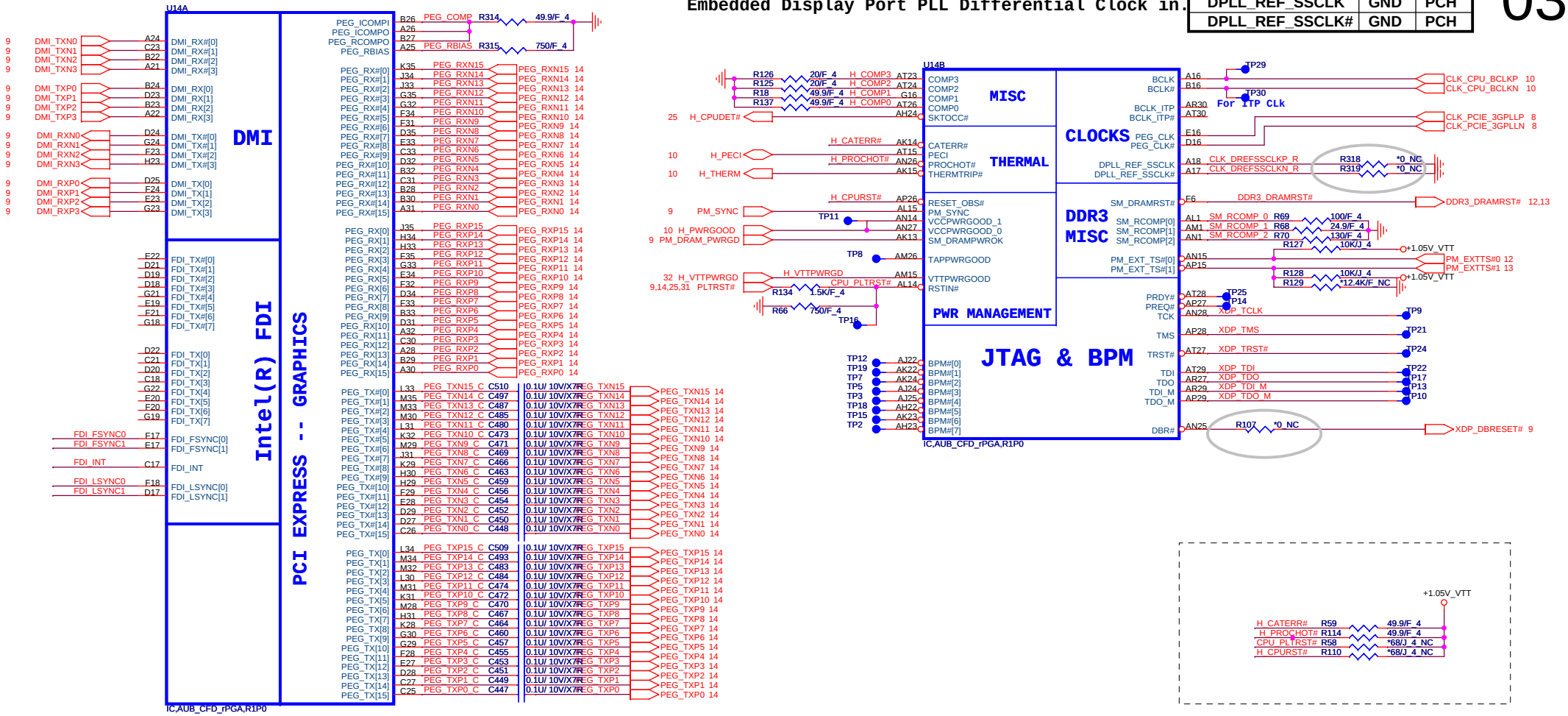
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Clock Gen(9LRS3197)/HOLES	1A
Date: Wednesday, February 10, 2010	Sheet 2 of 46	

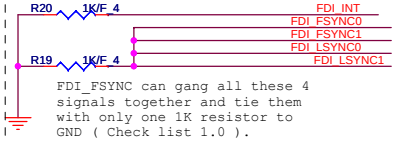
DPLL_REF_SSCLK/DPLL_REF_SSCLK#:
Embedded Display Port PLL Differential Clock in.

	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

03



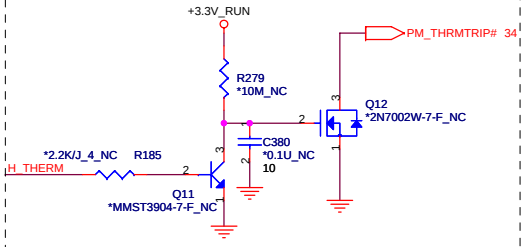
Discrete Only

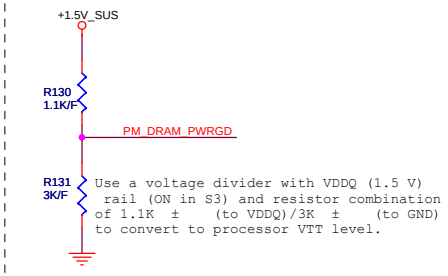


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1],FDI_LSYN[0],FDI_LSYN[1] can be ganged together with one resistor.

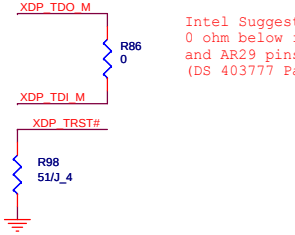
CPU THERMTRIP





Use a voltage divider with VDDQ (1.5 V) rail (ON in S3) and resistor combination of 1.1K ± (to VDDQ)/3K ± (to GND) to convert to processor VTT level.

JTAG MAPPING



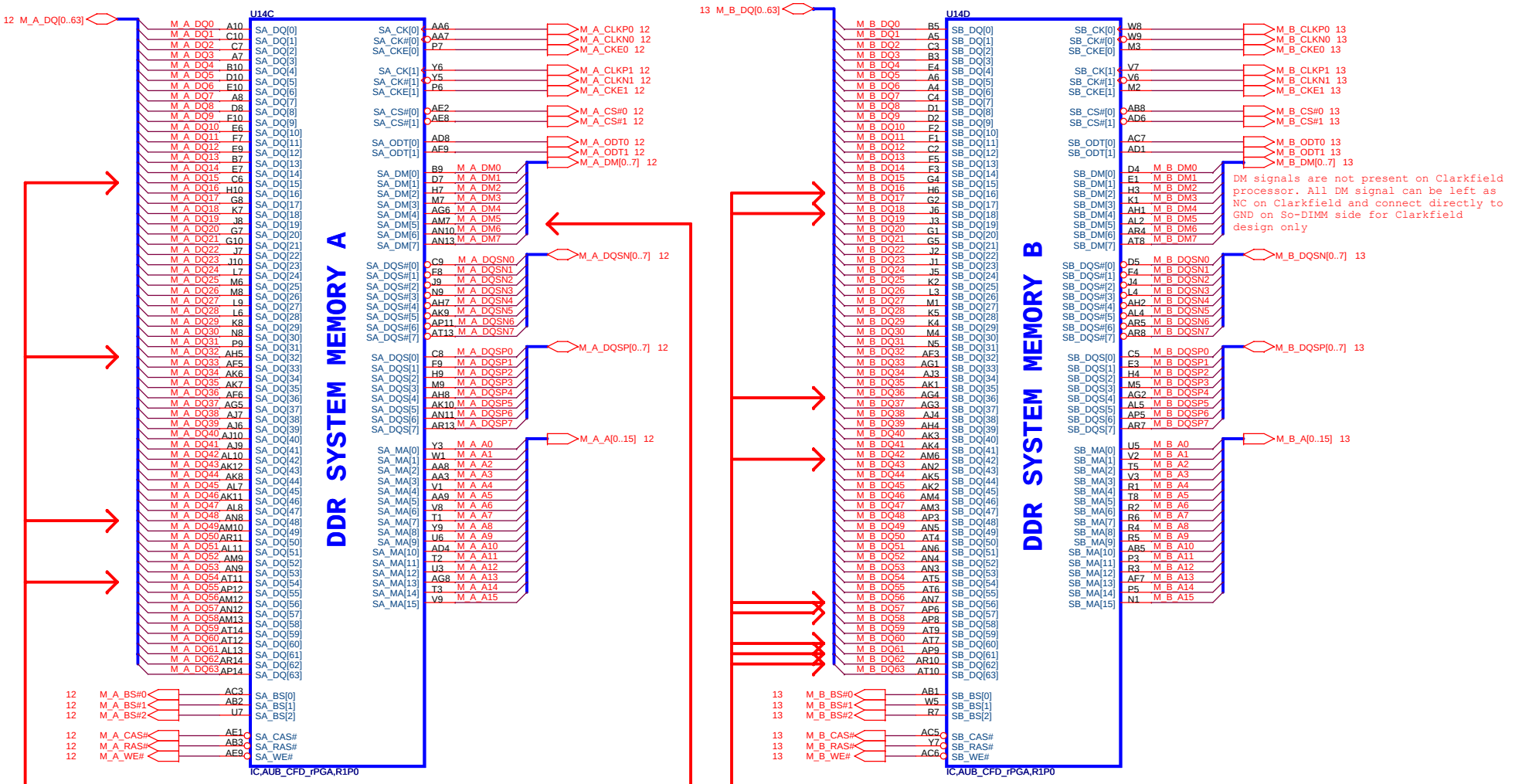
Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins. (DS 403777 Page 81)

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A

Date: Wednesday, February 10, 2010 Sheet 3 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A
Date: Wednesday, February 10, 2010	Sheet 4 of 46	

18A

Name different with power

+VCC_CORE

C491 *22U/6.3V_8/X5R_NC
C490 *22U/6.3V_8/X5R_NC
C92 *22U/6.3V_8/X5R_NC
C70 *22U/6.3V_8/X5R_NC
C521 *22U/6.3V_8/X5R_NC
C125 22U/6.3V_8/X5R
C103 22U/6.3V_8/X5R
C121 22U/6.3V_8/X5R
C126 22U/6.3V_8/X5R
C77 22U/6.3V_8/X5R
C124 22U/6.3V_8/X5R
C129 22U/6.3V_8/X5R
C78 10U/6.3V_8/X5R
C488 10U/6.3V_8/X5R
C505 10U/6.3V_8/X5R
C445 10U/6.3V_8/X5R
C520 10U/6.3V_8/X5R
C60 10U/6.3V_8/X5R
C516 10U/6.3V_8/X5R
C122 10U/6.3V_8/X5R
C515 *10U/6.3V_8/X5R_NC
C489 *10U/6.3V_8/X5R_NC
C120 10U/6.3V_8/X5R
C117 10U/6.3V_8/X5R
C522 *10U/6.3V_8/X5R_NC
C518 *10U/6.3V_8/X5R_NC
C108 *10U/6.3V_8/X5R_NC
C123 *10U/6.3V_8/X5R_NC

C446 *470U_NC/
C18 *470U_NC

U14F

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

CPU VIDS

SENSE LINES

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.05V_VTT

C519 10U/6.3V_8/X5R
C503 10U/6.3V_8/X5R
C478 10U/6.3V_8/X5R
C73 10U/6.3V_8/X5R
C46 *10U/6.3V_0805/X5R_NC
C481 *10U/6.3V_0805/X5R_NC
C47 *10U/6.3V_0805/X5R_NC
C119 *10U/6.3V_0805/X5R_NC
C114 *10U/6.3V_0805/X5R_NC
C524 22U/6.3V_8/X5R
C48 22U/6.3V_8/X5R
C514 *22U/6.3V_8/X5R_NC

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05V_VTT

C43 22U/6.3V_8/X5R
C84 22U/6.3V_8/X5R

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

PSI# AN33 H_PSI# 39

VID[0] AK35 VID0 39
VID[1] AK33 VID1 39
VID[2] AK34 VID2 39
VID[3] AL35 VID3 39
VID[4] AL33 VID4 39
VID[5] AM33 VID5 39
VID[6] AM35 VID6 39
PROC_DPRSLPVR AM34 DPRSLPVR 39

VTT_SELECT G15 TP1

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

ISENSE AN35 I_MON 39

VTT_SENSE B15 VTT_SENSE 37
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT T34

VCC_SENSE AJ34
VSS_SENSE AJ35

VCCSENSE 39
VSSSENSE 39

+VCC_CORE
R64 100/F
R61 100/F/

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options
in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors
will depend on the POC configuration of AUB
and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

Please note that +VCC_GFX_CORE
should be 1.05V in Auburndale

U14G

POWER

GRAPHICS

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

FDI

PEG & DMI

1.1V

1.8V

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

Pop it when Arrandale Graphics disable.

R118 1K/J_4

2A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_SUS

C44 1U/6.3V/X5R
C90 1U/6.3V/X5R
C116 1U/6.3V/X5R
C53 1U/6.3V/X5R
C38 1U/6.3V/X5R
C55 22U/6.3V_8/X5R
C61 *22U/6.3V_8/X5R_NC
C20 330U/2V_7343

+1.05V_VTT

C49 22U/6.3V_8/X5R
C475 *22U/6.3V_8/X5R_NC

J24 J23 H25

VTT1_45 VTT1_46 VTT1_47

+1.05V_VTT

C56 22U/6.3V_8/X5R
C62 22U/6.3V_8/X5R
C98 *22U/6.3V_8/X5R_NC
C37 *22U/6.3V_8/X5R_NC

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

P10 N10 L10 K10 J22 J20 J18 H21 H20 H19

+1.05V_VTT

C486 10U/6.3V_8/X5R
C495 *10U/6.3V_0805/X5R_NC
C476 22U/6.3V_8/X5R
C477 *22U/6.3V_8/X5R_NC

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

+1.8V_RUN

C45 22U/6.3V_8/X5R
C34 4.7U/6.3V/X5R
C42 2.2U/ 6.3V/X5R
C36 1U/6.3V/X5R
C479 1U/6.3V/X5R

IC,AUB_CFD_rPGA,R1P0

VID0 R96 1K/J_4 R313 *1K/J_4_NC
VID1 R84 1K/J_4 R312 *1K/J_4_NC
VID2 R104 1K/J_4 R311 *1K/J_4_NC
VID3 R111 1K/J_4 R310 *1K/J_4_NC
VID4 R115 1K/J_4 R309 *1K/J_4_NC
VID5 R148 1K/J_4 R308 *1K/J_4_NC
VID6 R124 1K/J_4 R307 *1K/J_4_NC
DPRSLPVR R139 1K/J_4 R306 *1K/J_4_NC
H_PSI# R140 1K/J_4 R305 *1K/J_4_NC

+1.05V_VTT

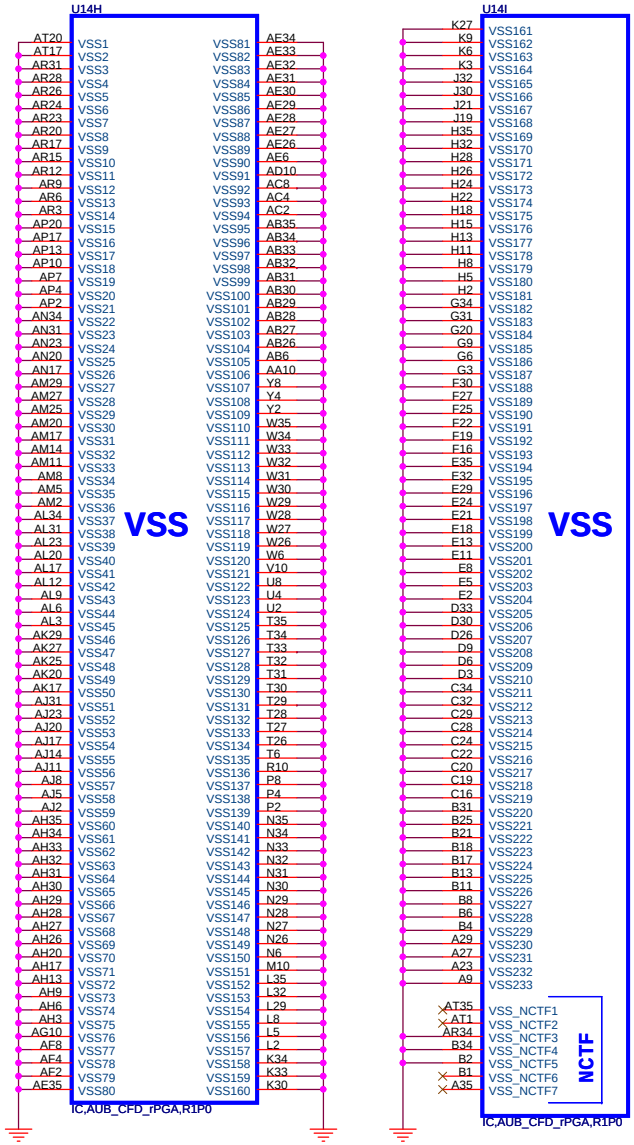
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A

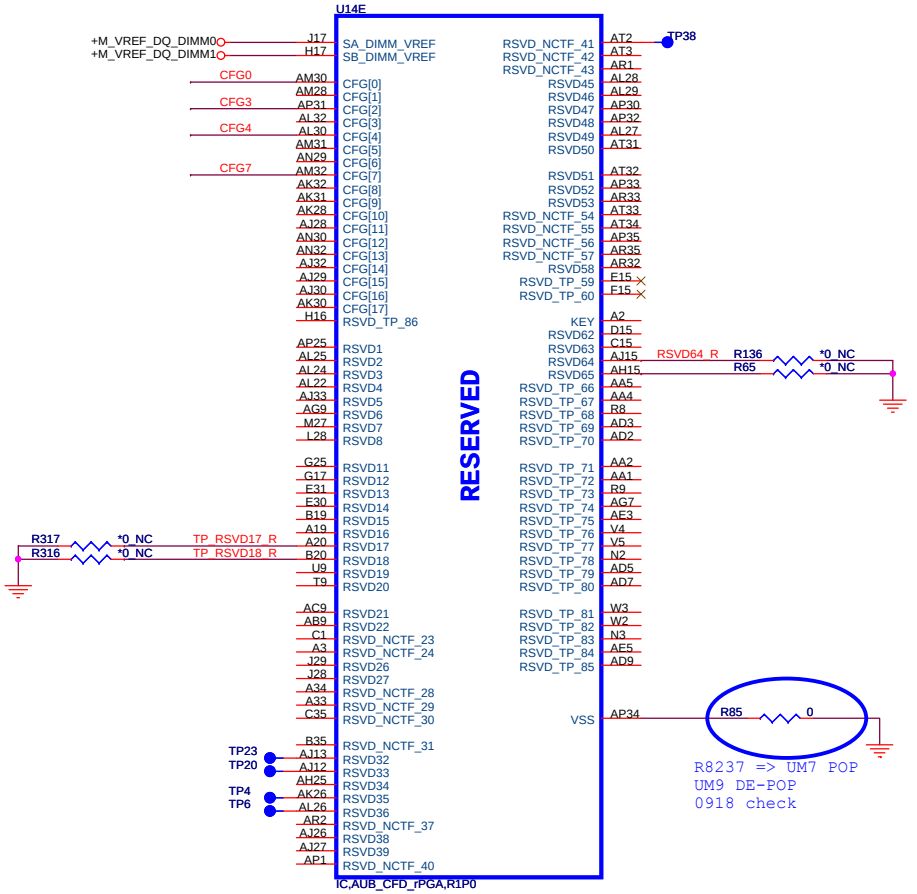
Date: Wednesday, February 10, 2010 Sheet 5 of 46

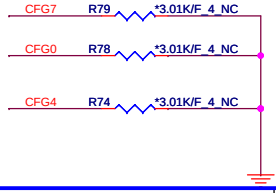
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



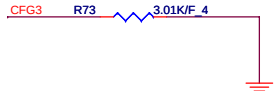
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

Date: Wednesday, February 10, 2010 Sheet 6 of 46

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U21A

Ibex-M 1 OF 10

C422 18P/50V_4/COG
Y3 32.768KHZ
R268 10M/J_4
C421 18P/50V_4/COG
RTC_X1 B13
RTC_X2 D13

RTC

T46 PAD RTC_RST# C14 RTCRST#
T45 PAD SRTC_RST# D17 SRTCRST#
SM_INTRUDER# A16 INTRUDER#
+RTC_CELL R440 330K/J_6 PCH_INVRMEN A14 INTVRMEN
T47 PAD

IHDA

ACZ_BITCLK A30 HDA_BCLK
ACZ_SYNC D29 HDA_SYNC
31 ACZ_SPKR P1 SPKR
ACZ_RST# C30 HDA_RST#
31 ACZ_SDIN0 G30 HDA_SDIN0
F30 HDA_SDIN1
E32 HDA_SDIN2
F32 HDA_SDIN3
ACZ_SDOUT B29 HDA_SDO
25 PCH_MELOCK R452 *0_NC PCH_GPIO33 H32 HDA_DOCK_EN# / GPIO33 (+3V)
J30 HDA_DOCK_RST# / GPIO13 (+3V_S5)

JTAG

TP43 PCH_JTAG_TCK_BUF M3 JTAG_TCK
TP44 PCH_JTAG_TMS K3 JTAG_TMS
TP45 PCH_JTAG_TDI K1 JTAG_TDI
TP46 PCH_JTAG_TDO J2 JTAG_TDO
TP47 PCH_JTAG_RST# J4 TRST#
must add test point.

SPI

26 SPI_CLK TP39 SPI_CLK BA2 SPI_CLK
26 SPI_CS0# TP40 SPI_CS0# AV3 SPI_CS0#
TP41 SPI_CS1# AY3 SPI_CS1#
26 SPI_SI TP28 SPI_SI AY1 SPI_MOSI
26 SPI_SO TP42 SPI_SO AV1 SPI_MISO
C602 *100P/NPO_NC
36
ibexPeak-M_Rev1_0

LPC

FWH0 / LAD0 D33 LAD0 25,31
FWH1 / LAD1 B33 LAD1 25,31
FWH2 / LAD2 C32 LAD2 25,31
FWH3 / LAD3 A32 LAD3 25,31
FWH4 / LFRAME# C34 LFRAME# 25,31
LDRQ0# A34
(+3V) LDRQ1# / GPIO23 E34
SERIRQ AB9 SERIRQ 25

HDD

SATA0RXN AK7 SATA_RXN0 28
SATA0RXP AK6 SATA_RXP0 28
SATA0TXN AK11 SATA_TXN0 28
SATA0TXP AK9 SATA_TXP0 28

SATA1RXN AH6 SATA_RXN1 28
SATA1RXP AH5 SATA_RXP1 28
SATA1TXN AH9 SATA_TXN1 28
SATA1TXP AH8 SATA_TXP1 28

ODD

SATA2RXN AF11 DG: Place TX cap close to connector
SATA2RXP AF9
SATA2TXN AF7 SATA port 2/3 are not support in HM55 .
SATA2TXP AF6 They are only in PM 55

SATA

SATA3RXN AH3
SATA3RXP AH1
SATA3TXN AF3
SATA3TXP AF1

ESATA

40

SATA4RXN AD9 SATA_RXN4 27
SATA4RXP AD8 SATA_RXP4 27
SATA4TXN AD6 SATA_TXN4 27
SATA4TXP AD5 SATA_TXP4 27

SATA5RXN AD3
SATA5RXP AD1
SATA5TXN AB3
SATA5TXP AB1

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

SATAICOMPO AF16
SATAICOMPI AF15 SATA_COMP R218 37.4/F_4 +1.05V_PCH
SATALED# T3 SATA_LED# SATA_LED# 29
Y9 SATA_DET0#
V1 SATA_DET1#
(+3V) SATA0GP / GPIO21
(+3V_S5) SATA1GP / GPIO19

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

+3.3V_RUN R411 10K/J_4 SATA_LED#
R237 10K/J_4 SATA_DET0#
R405 10K/J_4 SATA_DET1#

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

R245 1 2 *1K_NC PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

iTPM ENABLE/DISABLE

+3.3V_RUN R208 *1K_NC/ SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

For AUDIO

25,31 ACZ_RST#_AUDIO R229 33/J_4 ACZ_RST#
31 ACZ_SDOUT_AUDIO R235 33/J_4 ACZ_SDOUT
C404 *10P/50V_4_NC/COG
31 ACZ_SYNC_AUDIO R234 33/J_4 ACZ_SYNC
C399 *10P/50V_4_NC/COG
31 ACZ_BITCLK_AUDIO R231 33/J_4 ACZ_BITCLK
C389 10P/50V_4/COG
77

+3.3V_RUN R412 *1K/F_4_NC ACZ_SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

RTC

1mA

+RTC_CELL
R443 20K/F_4 C582 1U/6.3V/X5R RTC_RST#
R428 20K/F_4 C583 1U/6.3V/X5R SRTC_RST#
R427 1M/J_4 SM_INTRUDER#

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U21D

Ibex-M 4 OF 10

LVDS--A

T48 L_BKLTEN
T47 L_VDD_EN
Y48 L_BKLTCTL
AB48 L_DDC_CLK
Y45 L_DDC_DATA
AB46 L_CTRL_CLK
V48 L_CTRL_DATA
T29 PAD AP39 LVD_IBG
T28 PAD AP41 LVD_VBG
T26 PAD AT43 LVD_VREFH
T27 PAD AT42 LVD_VREFL

AV53 LVDSA_CLK#
AV51 LVDSA_CLK
BB47 LVDSA_DATA#0
BA52 LVDSA_DATA#1
AY48 LVDSA_DATA#2
AV47 LVDSA_DATA#3
BB48 LVDSA_DATA0
BA50 LVDSA_DATA1
AY49 LVDSA_DATA2
AV48 LVDSA_DATA3

LVDS--B

AP48 LVDSB_CLK#
AP47 LVDSB_CLK
AY53 LVDSB_DATA#0
AT49 LVDSB_DATA#1
AU52 LVDSB_DATA#2
AT53 LVDSB_DATA#3
AY51 LVDSB_DATA0
AT48 LVDSB_DATA1
AU50 LVDSB_DATA2
AT51 LVDSB_DATA3

CRT

AA52 CRT_BLUE
AB53 CRT_GREEN
AD53 CRT_RED
V51 CRT_DDC_CLK
V53 CRT_DDC_DATA
Y53 CRT_HSYNC
Y51 CRT_VSYNC
R221 1K/F_4 DAC_IREF AD48 DAC_IREF
AB51 CRT_IRTN

SDVO

SDVO_TVCLKINN BJ46
SDVO_TVCLKINP BG46
SDVO_STALLN BJ48
SDVO_STALLP BG48
SDVO_INTN BF45
SDVO_INTP BH45
SDVO_CTRLCLK T51
SDVO_CTRLDATA T53

Digital Display Interface

DISPLAY PORT B

DDPB_AUXN BG44
DDPB_AUXP BJ44
DDPB_HPD AU38
DDPB_0N BD42
DDPB_0P BC42
DDPB_1N BJ42
DDPB_1P BG42
DDPB_2N BB40
DDPB_2P BA40
DDPB_3N AW38
DDPB_3P BA38

DISPLAY PORT C

DDPC_CTRLCLK Y49
DDPC_CTRLDATA AB49
DDPC_AUXN BE44
DDPC_AUXP BD44
DDPC_HPD AV40
DDPC_0N BE40
DDPC_0P BD40
DDPC_1N BE41
DDPC_1P BH41
DDPC_2N BD38
DDPC_2P BC38
DDPC_3N BB36
DDPC_3P BA36

DISPLAY PORT D

DDPD_CTRLCLK U50
DDPD_CTRLDATA U52
DDPD_AUXN BC46
DDPD_AUXP BD46
DDPD_HPD AT38
DDPD_0N BJ40
DDPD_0P BG40
DDPD_1N BJ38
DDPD_1P BG38
DDPD_2N BF37
DDPD_2P BH37
DDPD_3N BE36
DDPD_3P BD36

ibexPeak-M_Rev1_0

UMA 0.5%
DIS 1%

+3.3V_SUS **Res. of TDI near PCH**

R416 *200_NC
R418 *200_NC
R420 *200_NC
R422 20K/F_4_NC
R417 *100_NC
R419 *100_NC
R421 *100_NC
R423 *10K_NC

PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

R415 51/J_4 PCH_JTAG_TCK_BUF

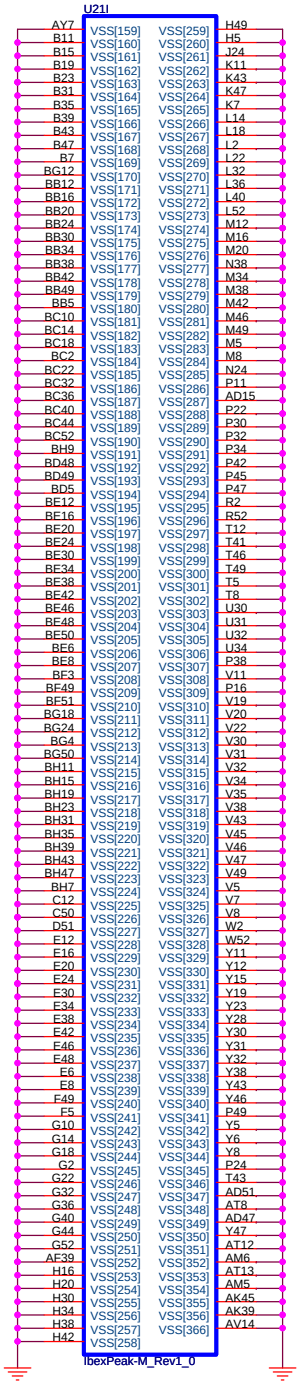
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

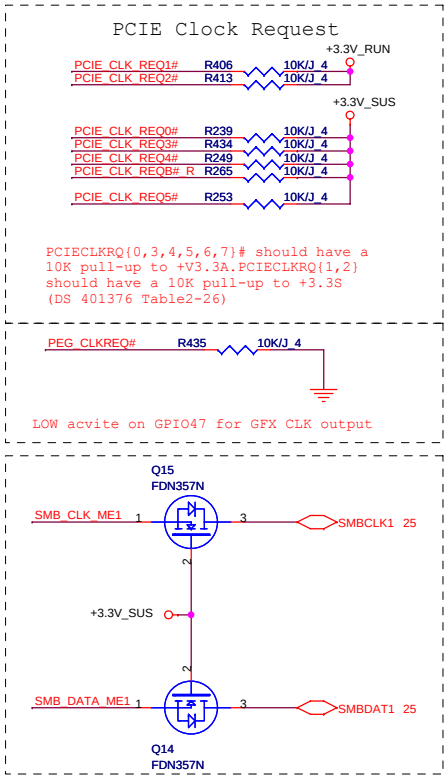
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A

Date: Wednesday, February 10, 2010 Sheet 7 of 46

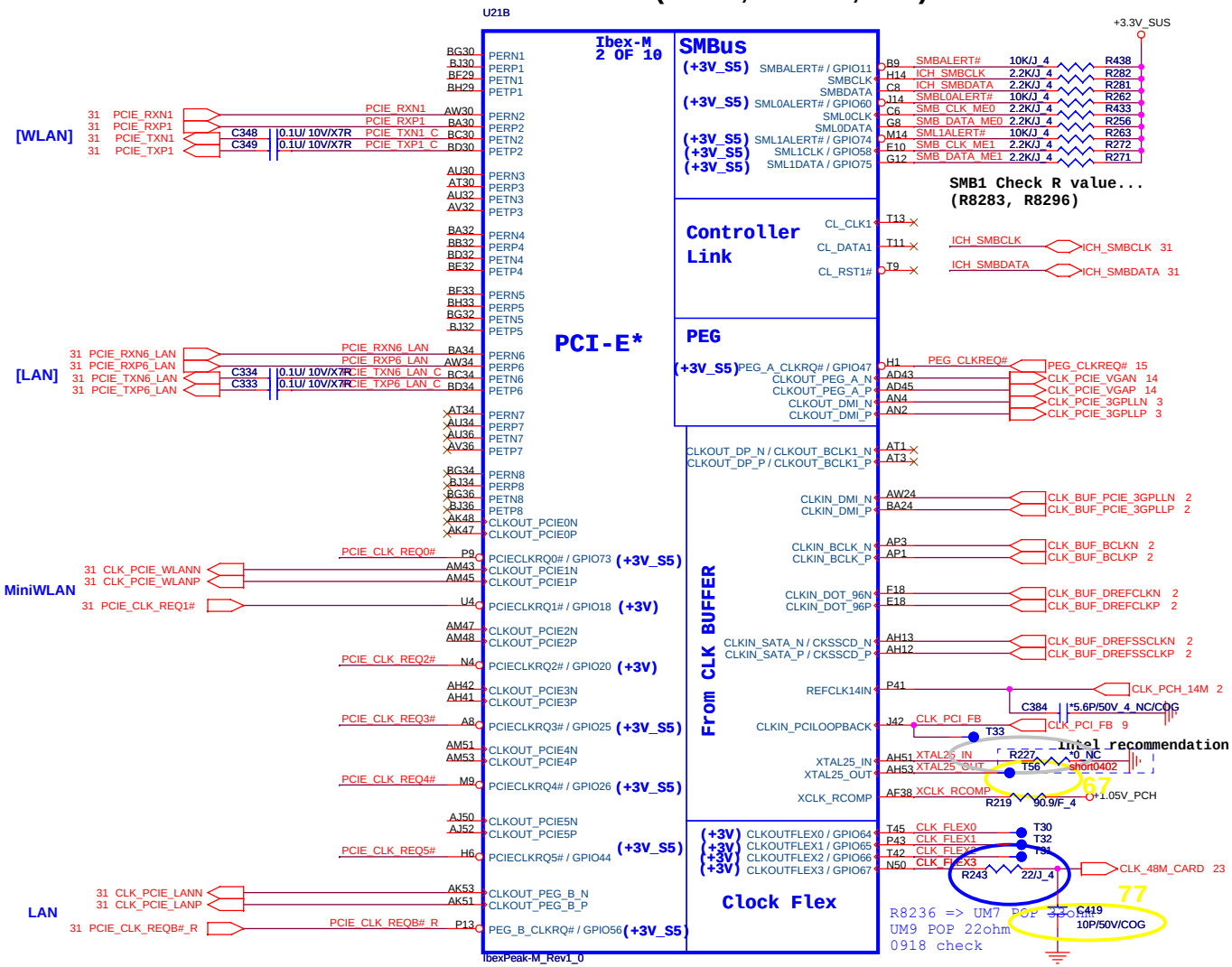
IBEX PEAK-M (GND)





IBEX PEAK-M (PCI-E,SMBUS,CLK)

08

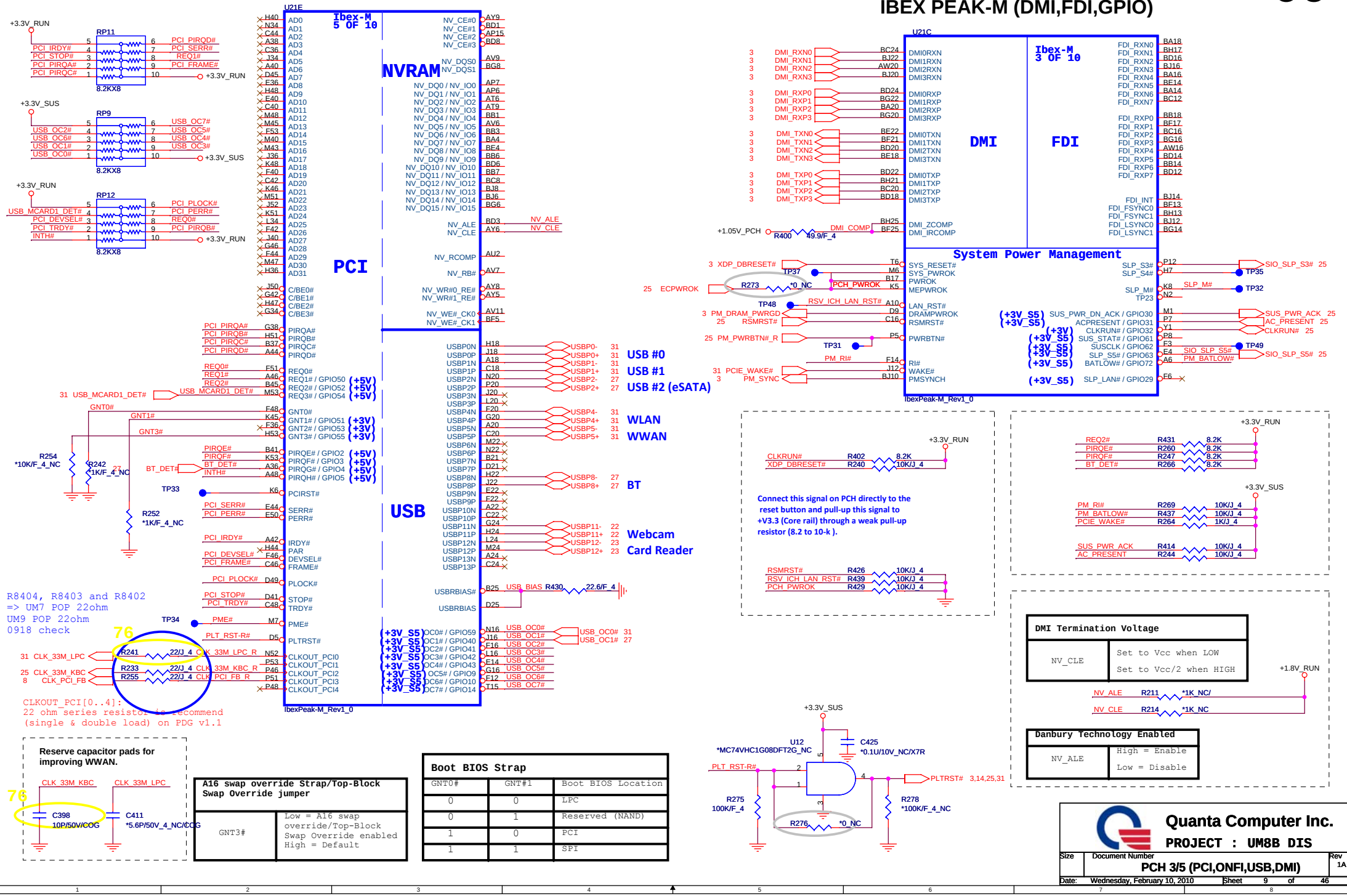


Quanta Computer Inc.	PROJECT : UM8B DIS	
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev 1A
Date: Wednesday, February 10, 2010	Sheet 8 of 46	

IBEX PEAK-M (PCI,USB,NVRAM)

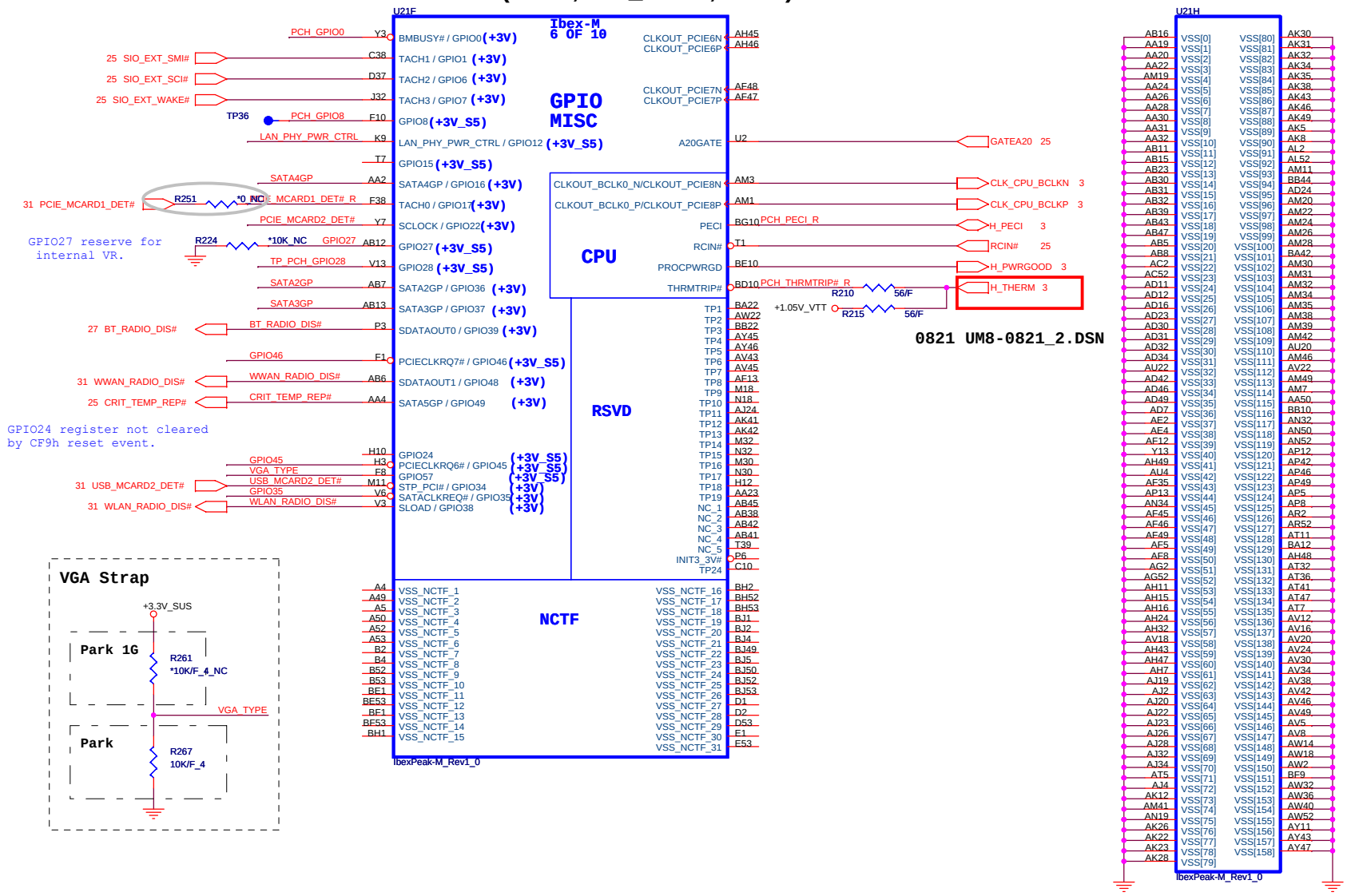
IBEX PEAK-M (DMI,FDI,GPIO)

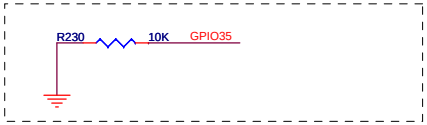
09

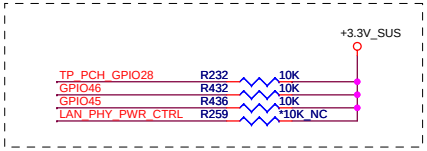


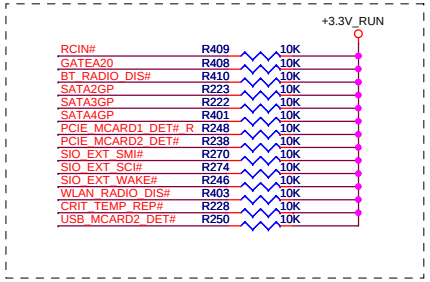
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

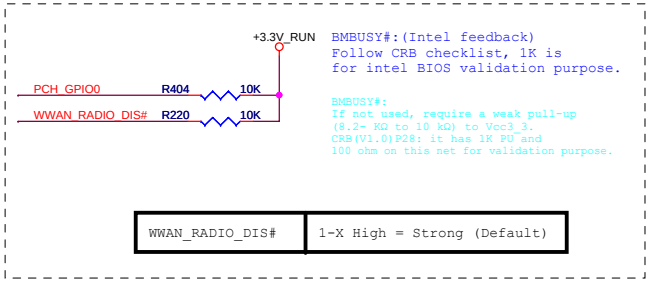
IBEX PEAK-M (GND)









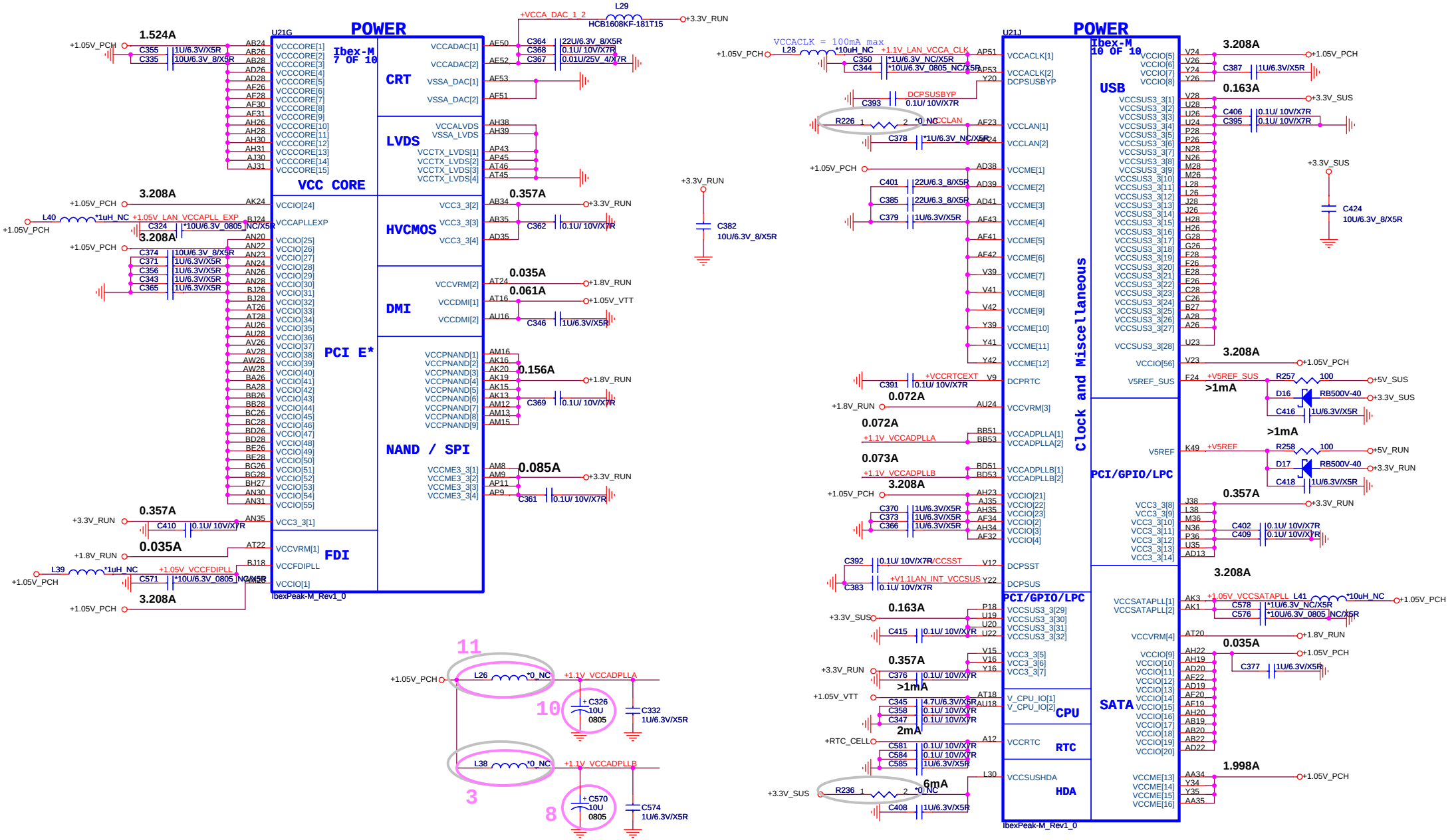


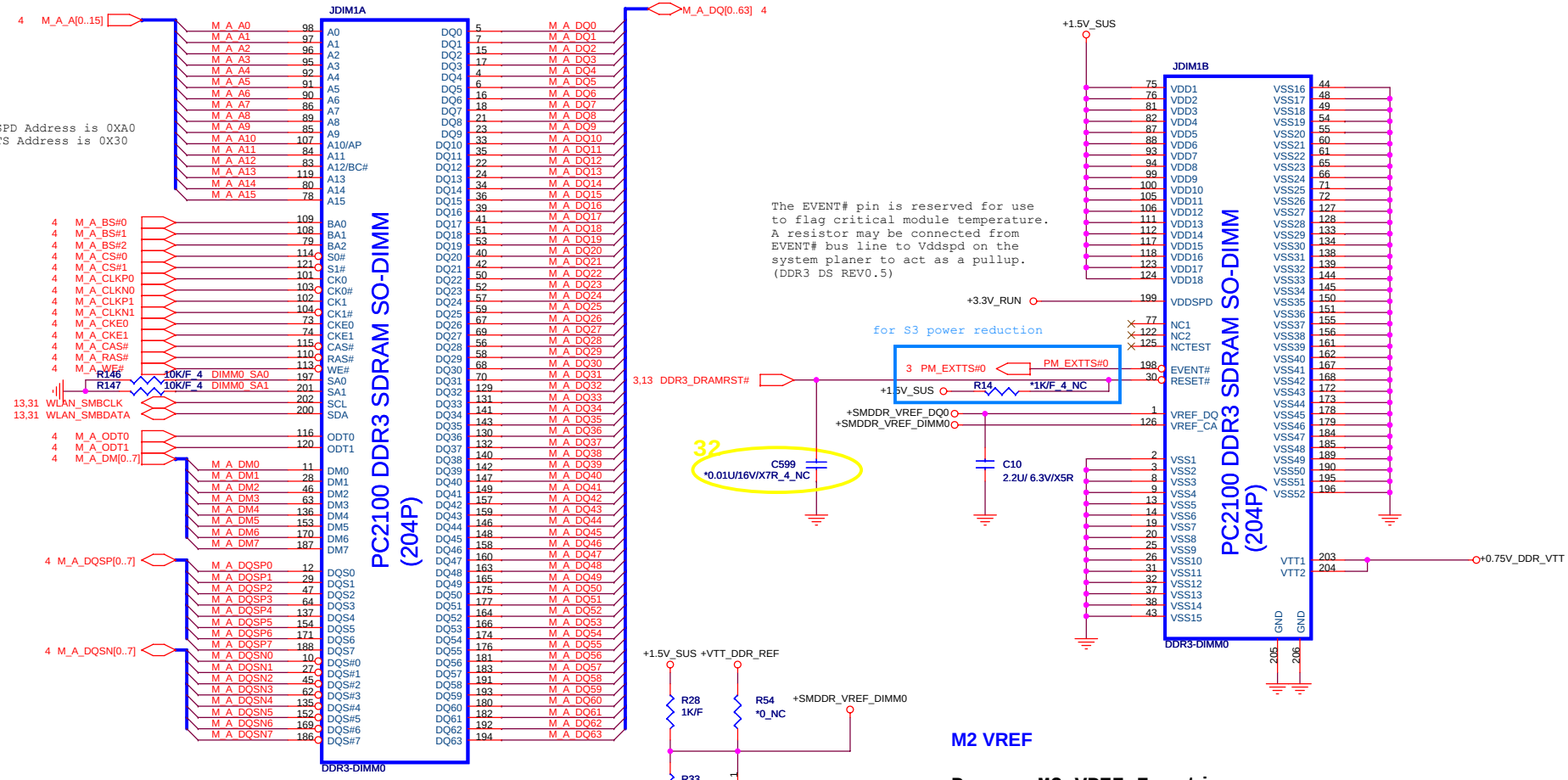
Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A
Date: Wednesday, February 10, 2010	Sheet 10 of 46	

Cap quantities follow UM3





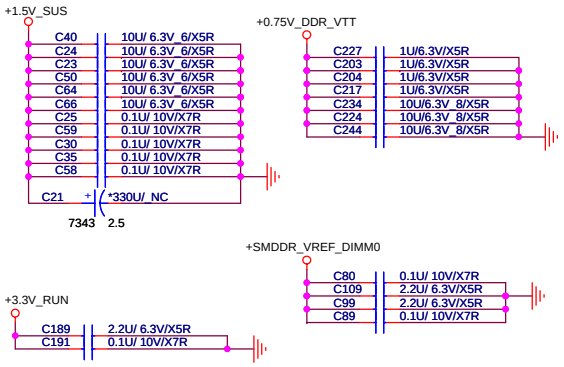
M2 VREF

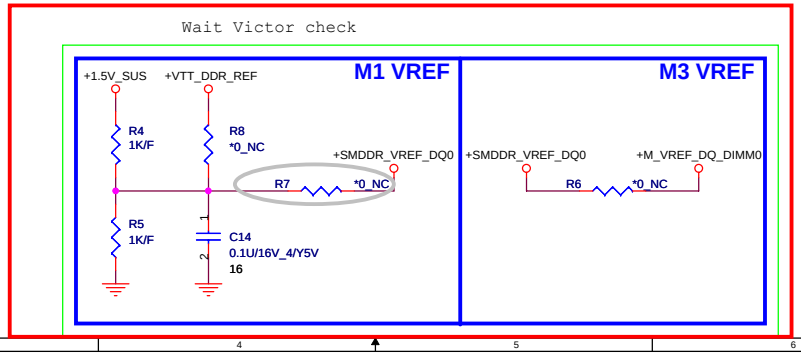
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

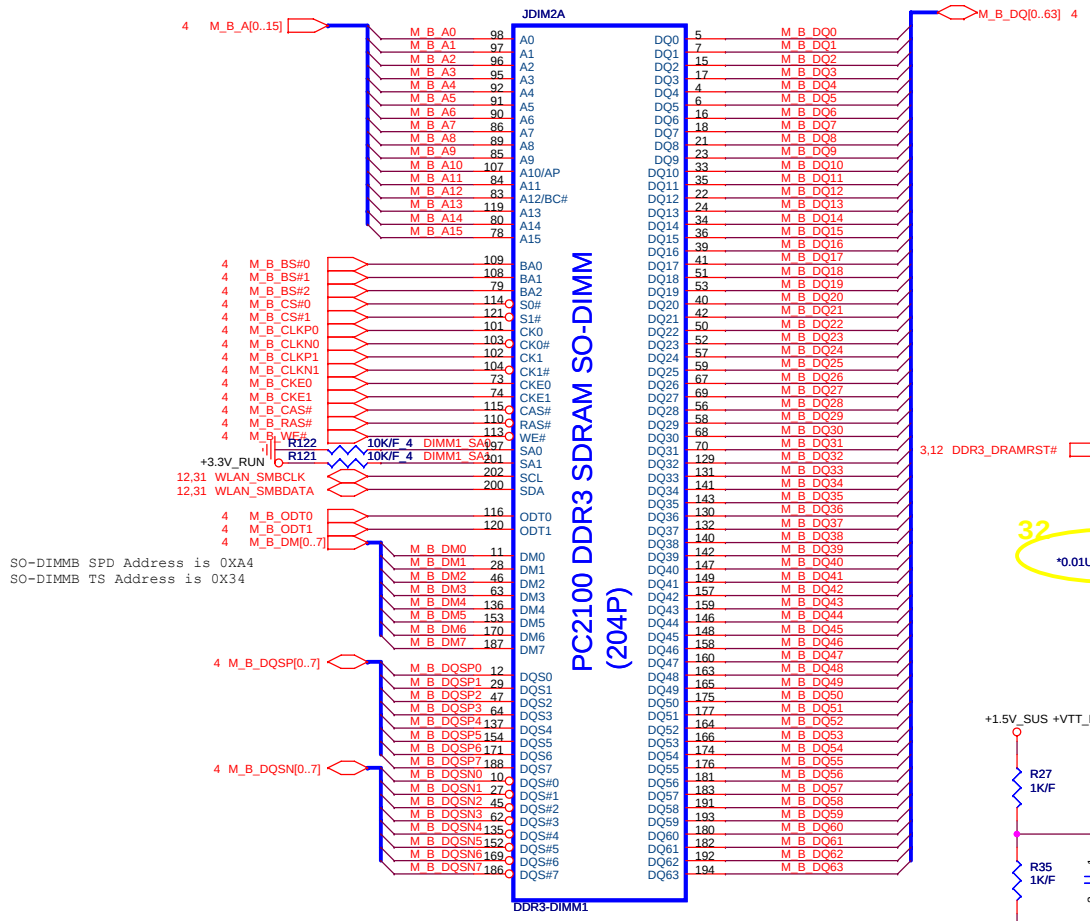
Place these Caps near So-Dimm0.

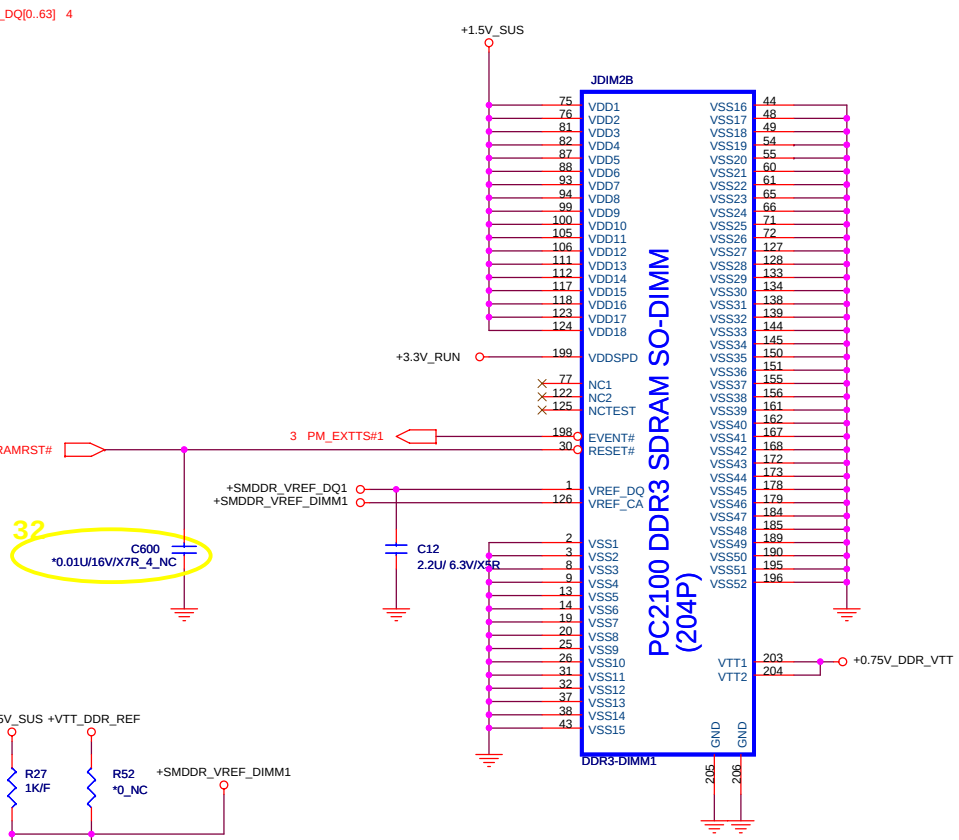
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

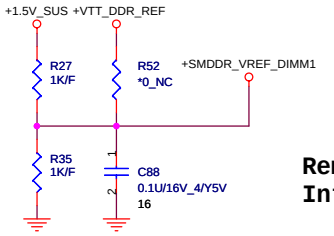




Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: DDR3 DIMM-0	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 12 of 46	



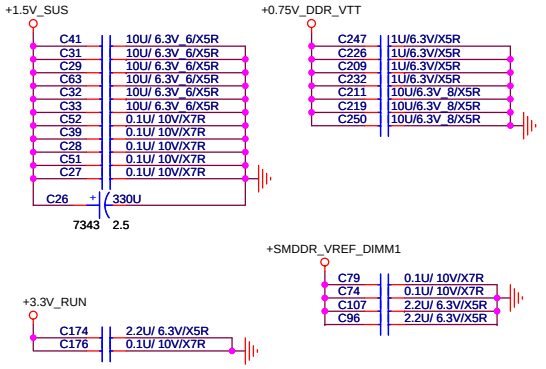




Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

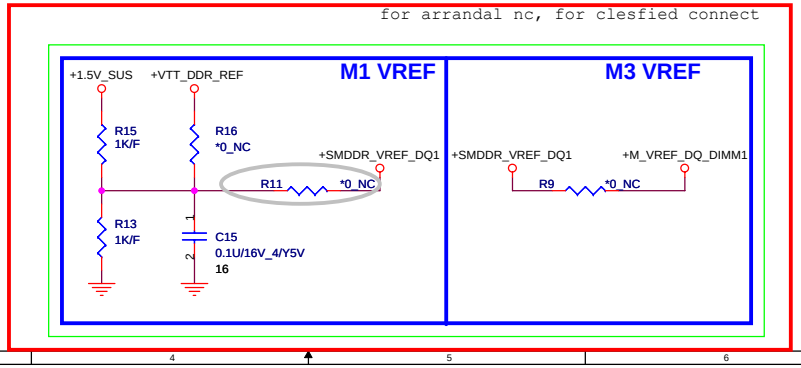
M3 => support for Clarksfield processor

Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



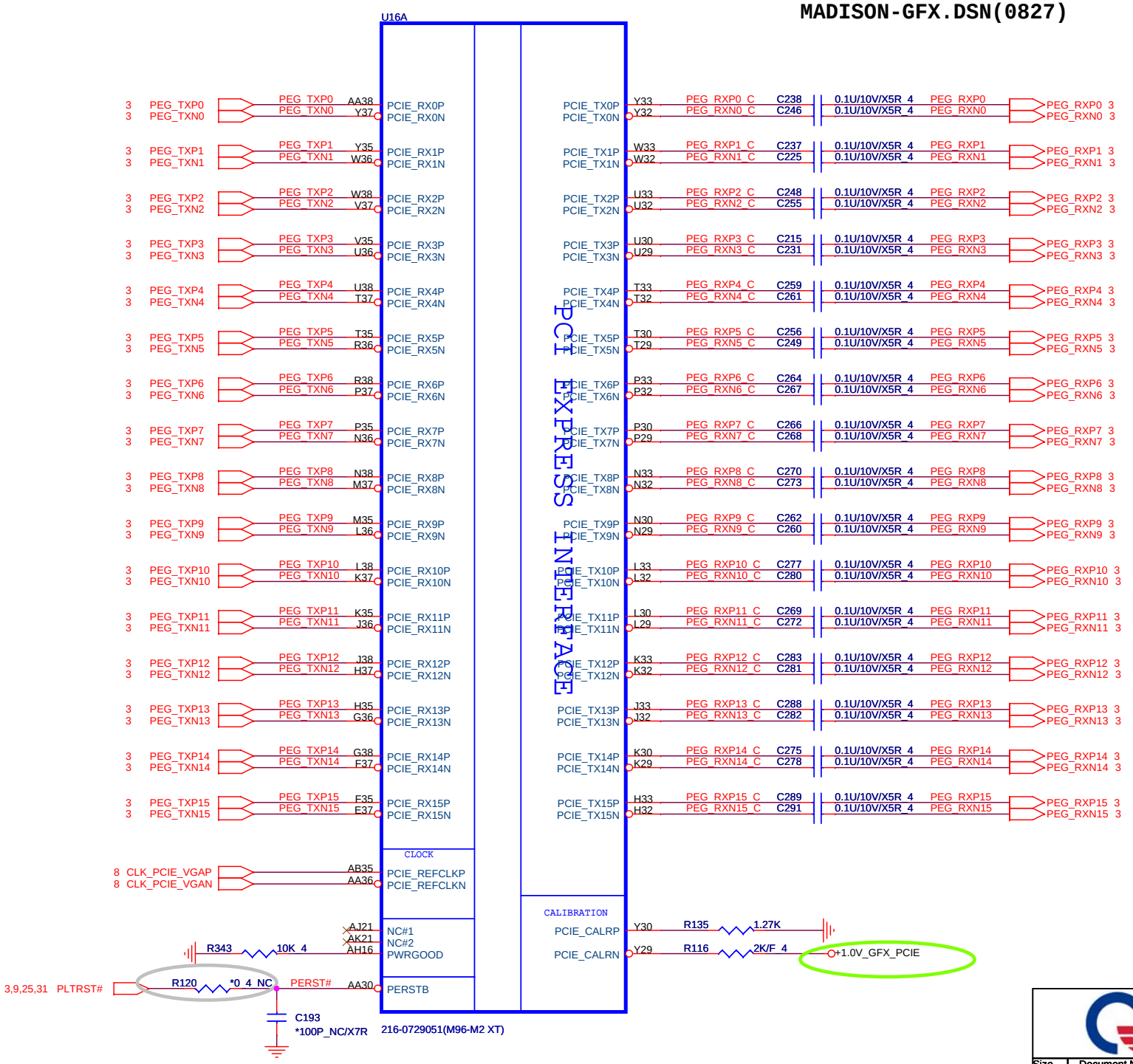
Wait Victor check

for arrandal nc, for clesfied connect



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date: Wednesday, February 10, 2010	Sheet 13 of 46	



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: Madison PCIE I/F	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 14 of 46	

Memory Straps		R342 RAM_TYPE_CFG3	R340 RAM_TYPE_CFG2	R341 RAM_TYPE_CFG1	R339 RAM_TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
800 MHz 1Gb(128M*16) Hynix_Orion die	H5TQ2G63BFR-12C	0	0	1	0
800 MHz 1Gb(128M*16) Samsung_E die	K4W2G1646b-HC12	0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

(GPIO_19_CTF)
Critical temperature fault (active high)
CTF will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power.

!!! NC when PARK-M2

Park and Madison

GPU Power-on sequence

1 => +3V_D
2 => +1.5V_GPU = +1.5V_RUN
3 => +VGPU_CORE
4 => +VGPU_IO
5 => +1V = +1.0V_GFX_PCIE
6 => +1.8V_GPU = +1.8V_RUN_GFX
7 => dGPU_PWROK

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	VGAVSYNC2	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0
BIOS_ROM_EN (Internal pull down)	GPIO_22_ROMCSB	1 = Enable external BIOS ROM device 0 = Disable external BIOS ROM device	0

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

For Park,Madison production version ASIC is need removed workaround.

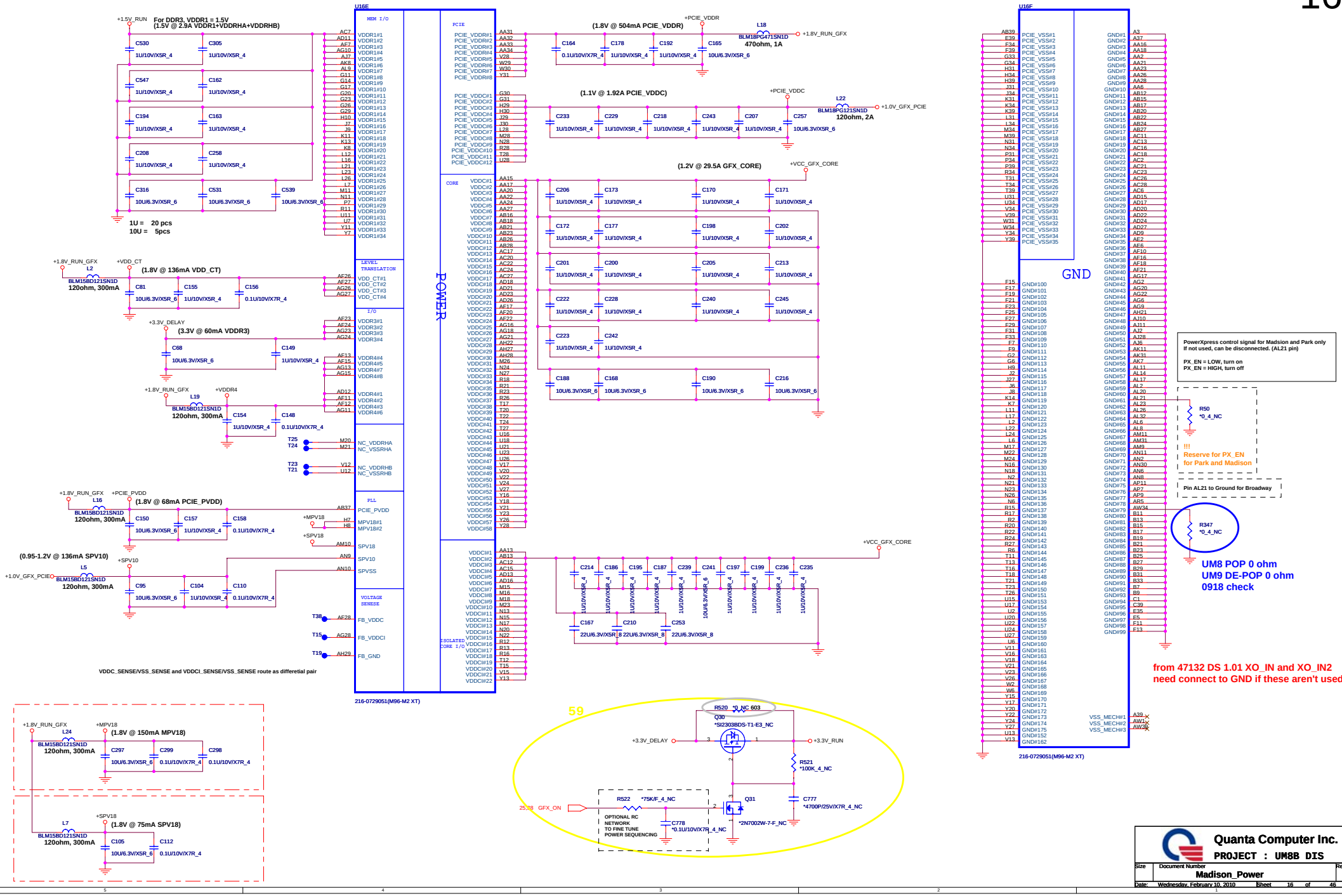
Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

Solve Intermittent System Boot-up Hangs

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

216-0729051(M96-M2 XT)



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_Power	1A

Date: Wednesday, February 10, 2010 Sheet 16 of 46

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

DPC & DPD aren't used.

U16H

DP C/D POWER | DP A/B POWER | DP E/F POWER | DP PLL POWER

+1.8V_RUN_GFX
+1.0V_GFX_PCIE
+DPA_VDD18
+DPA_VDD10
+DPB_VDD18
+DPE_VDD18
+DPE_VDD10
+DPA_PVDD

(1V @ 200mA DPA_VDD10)
(1.8V @ 20 mA DPA_PVDD)
(1.8V @ 400mA DPE_VDD18; 200mA for DPE/DPF respectively)
(1.8V @ 40mA DPE_PVDD; 20mA for DPE/DPF respectively)
(1.1V @ 200mA DPE_VDD10; 100mA for DPE/DPF respectively)
(1.8V @ 110mA DPA_VDD18)

DPE & DPF for LVDS
DPA for HDMI

UM8 POP 0 ohm
UM9 DE-POP 0 ohm
0918 check

from 47132 DS 1.01 XO_IN and XO_IN2
need connect to GND if these aren't used

216-0729051(M96-M2 XT)

U16G

LVDS CONTROL
LVTMDP

VARY_BL
DIGON
BIA_PWM
ENVDD

TXCLK_UP_DPF3P
TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P
TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P
TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P
TXOUT_U2N_DPF0N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP_DPE3P
TXCLK_LN_DPE3N
TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N
TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N
TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N
TXOUT_L3P
TXOUT_L3N

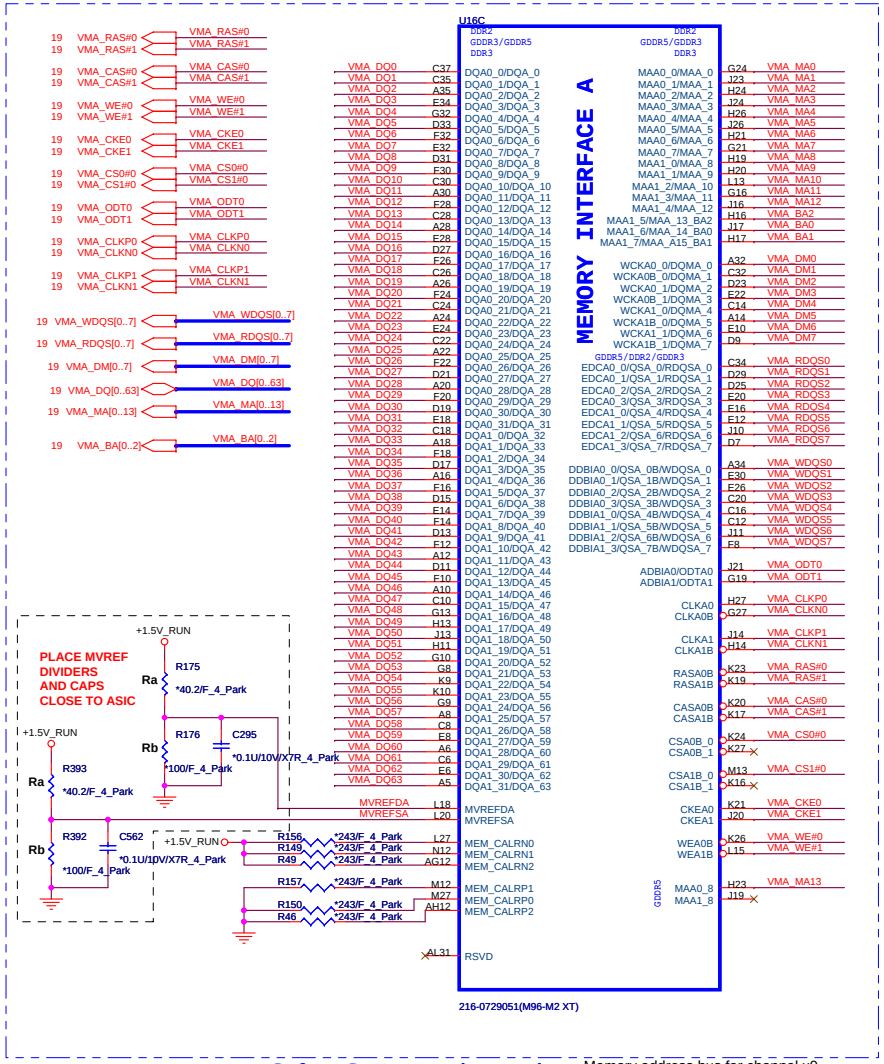
LCD_ACLK+
LCD_ACLK-
LCD_A0+
LCD_A0-
LCD_A1+
LCD_A1-
LCD_A2+
LCD_A2-

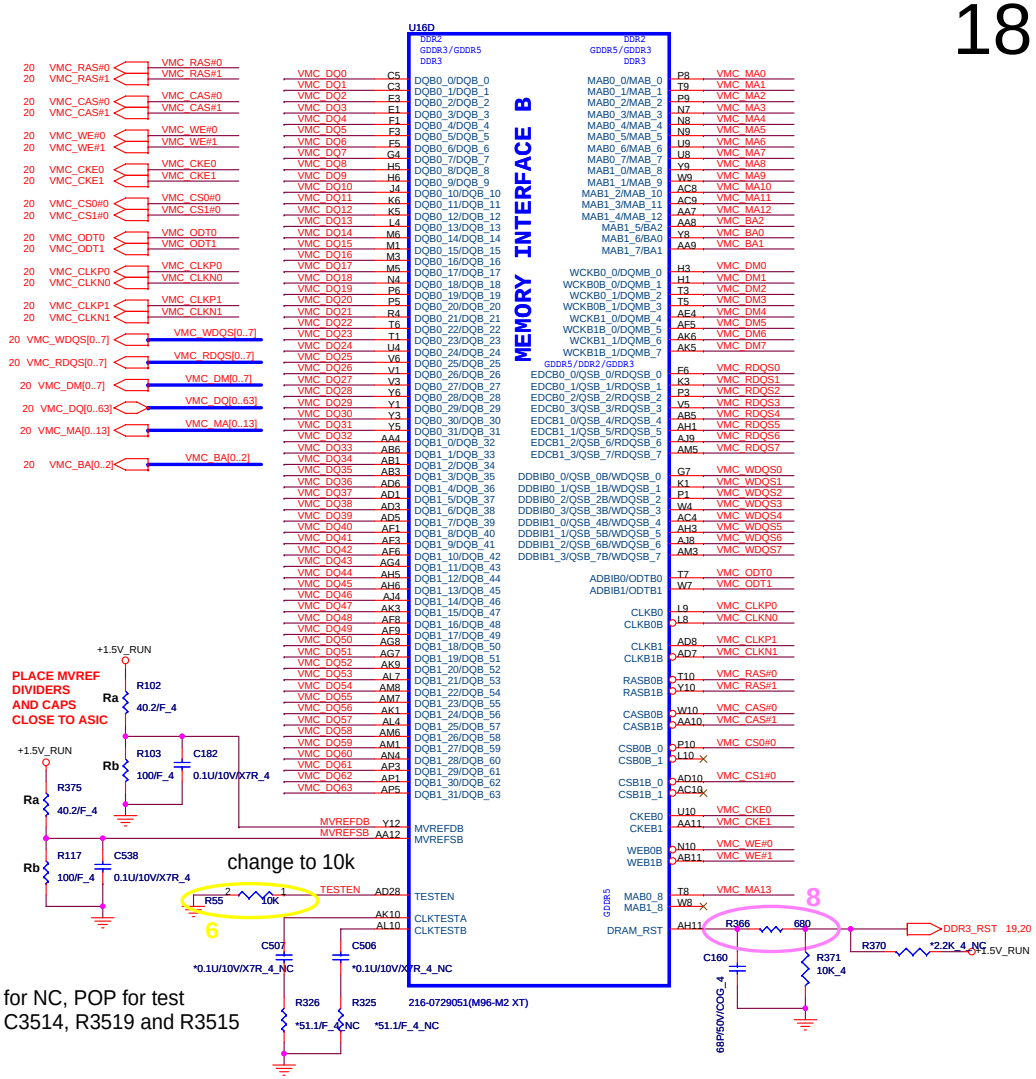
PAD T37
PAD T20
PAD T36
PAD T35

216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_DP_POWER	1A
Date: Wednesday, February 10, 2010	Sheet 17 of 46	





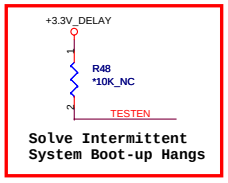
Normal for NC, POP for test
C3513, C3514, R3519 and R3515

NC for GFX Park portion

For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

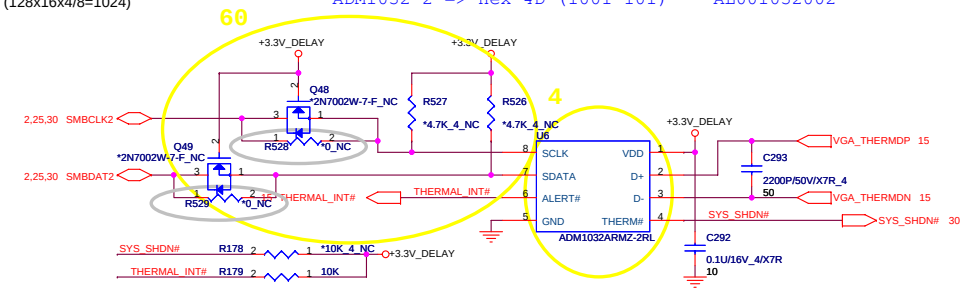


DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

Memory address bus for channel x0. Provides multiplexed row and column addresses. For 128-Mbit x16 DDR3 support, MAx13 is supported on MAx0_8. (128x16x4/8=1024)

ADM1032-1 => Hex 4C (1001 100) AL001032001
ADM1032-2 => Hex 4D (1001 101) AL001032002

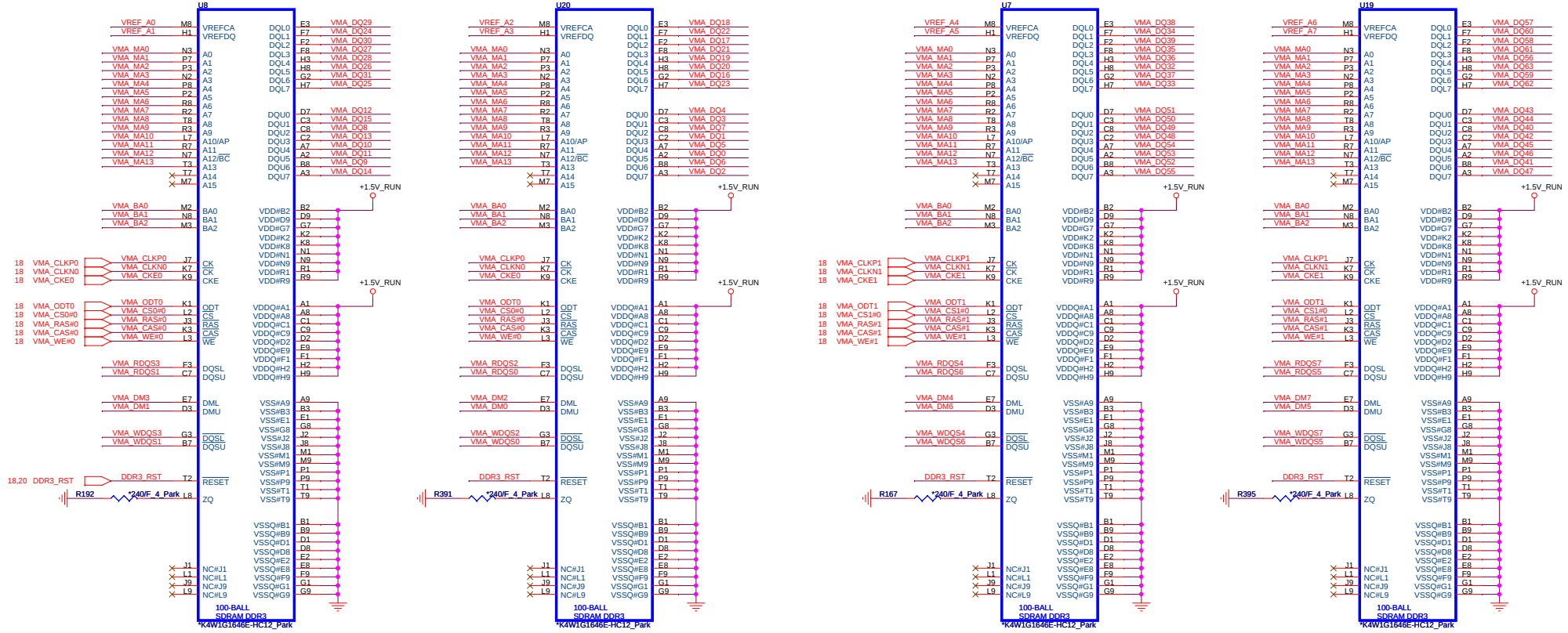


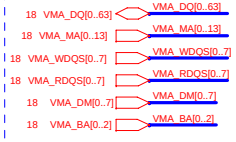
Designator	For M97-M2	For Madison
R272	10K	10K
R271	0R/Short	680R
R273	NC	NC
C408	2.2nF	68pF

Quanta Computer Inc.	PROJECT : UM8B DIS	
Size	Document Number: Madison_MEMORY/THERM	Rev 1A
Date: Wednesday, February 10, 2010	Sheet 18 of 46	

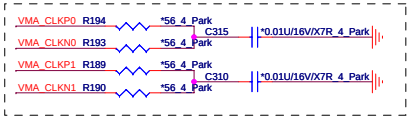
CHECK PN

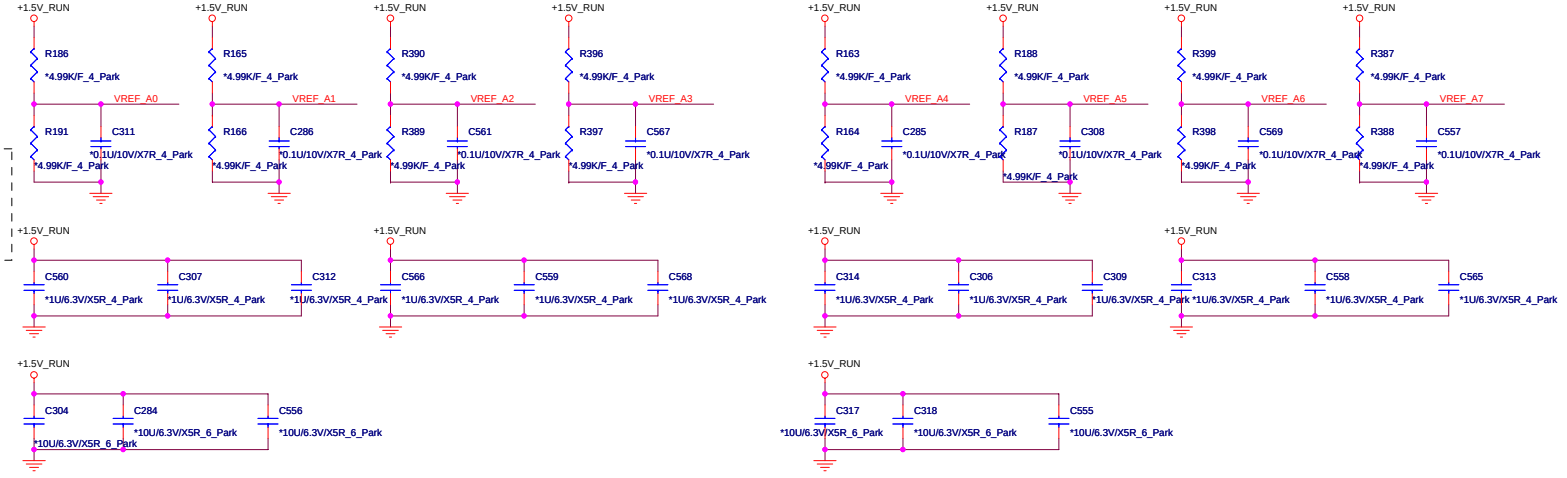
DDR3 64MX16, CH A : 512MB





Placement has to be close to VRAM





NC for GFX Park portion

Samsung: AKD5LGGT505

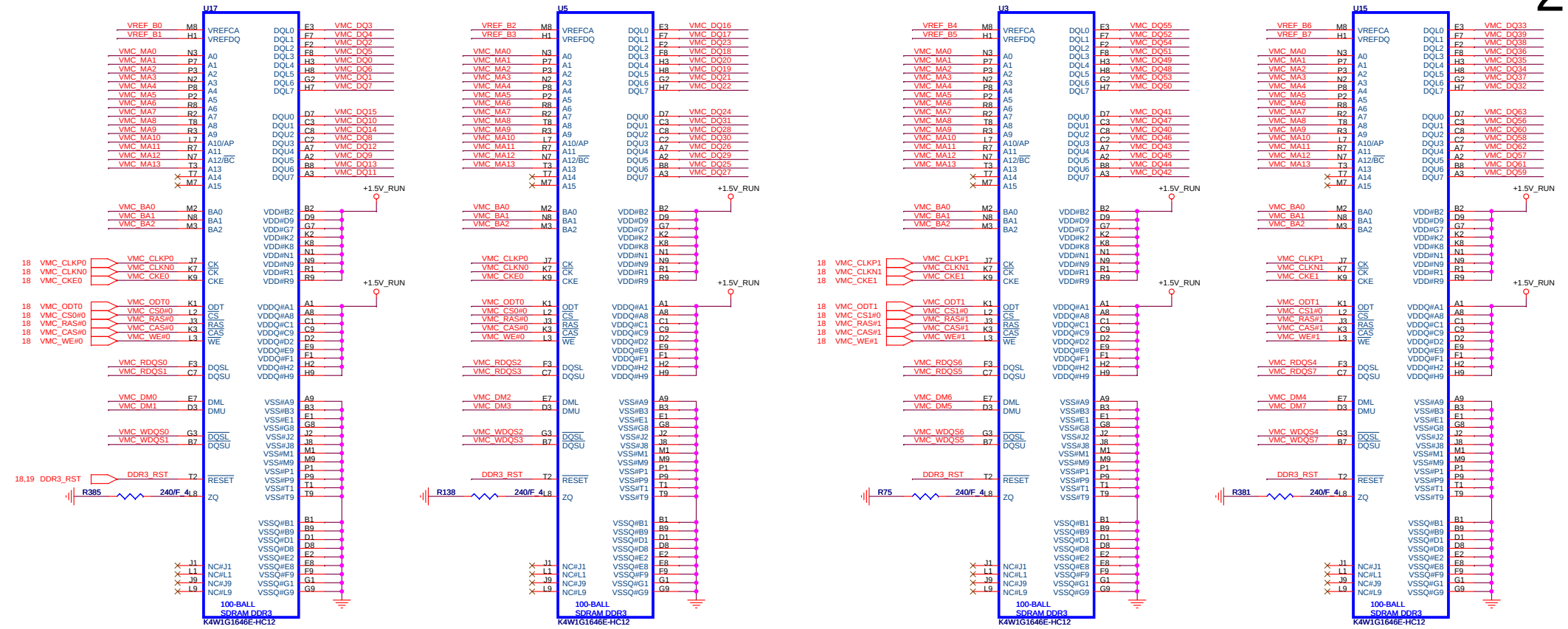
Hynix: AKD5LZGTW03

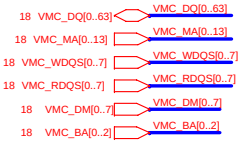
Quanta Computer Inc.

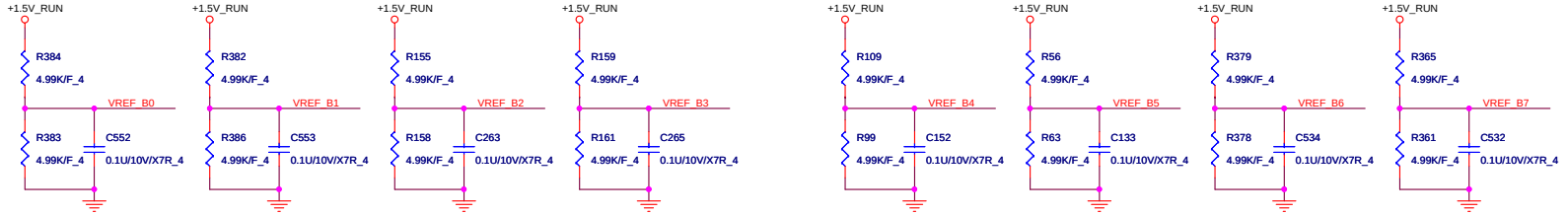
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_DDR3_A_512M	1A
Date: Wednesday, February 10, 2010	Sheet 19 of 46	

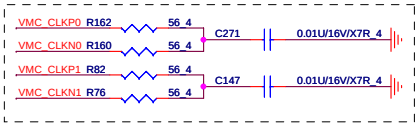
DDR3 64MX16, CH B : 512MB

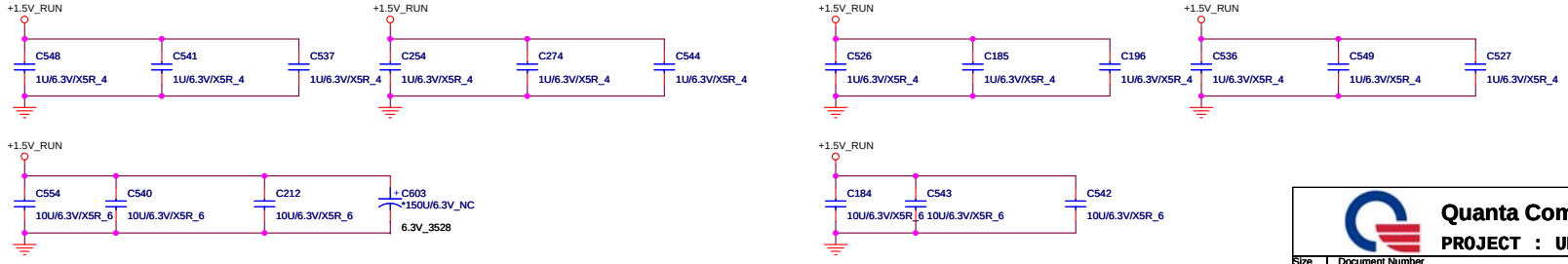






Placement has to be close to VRAM

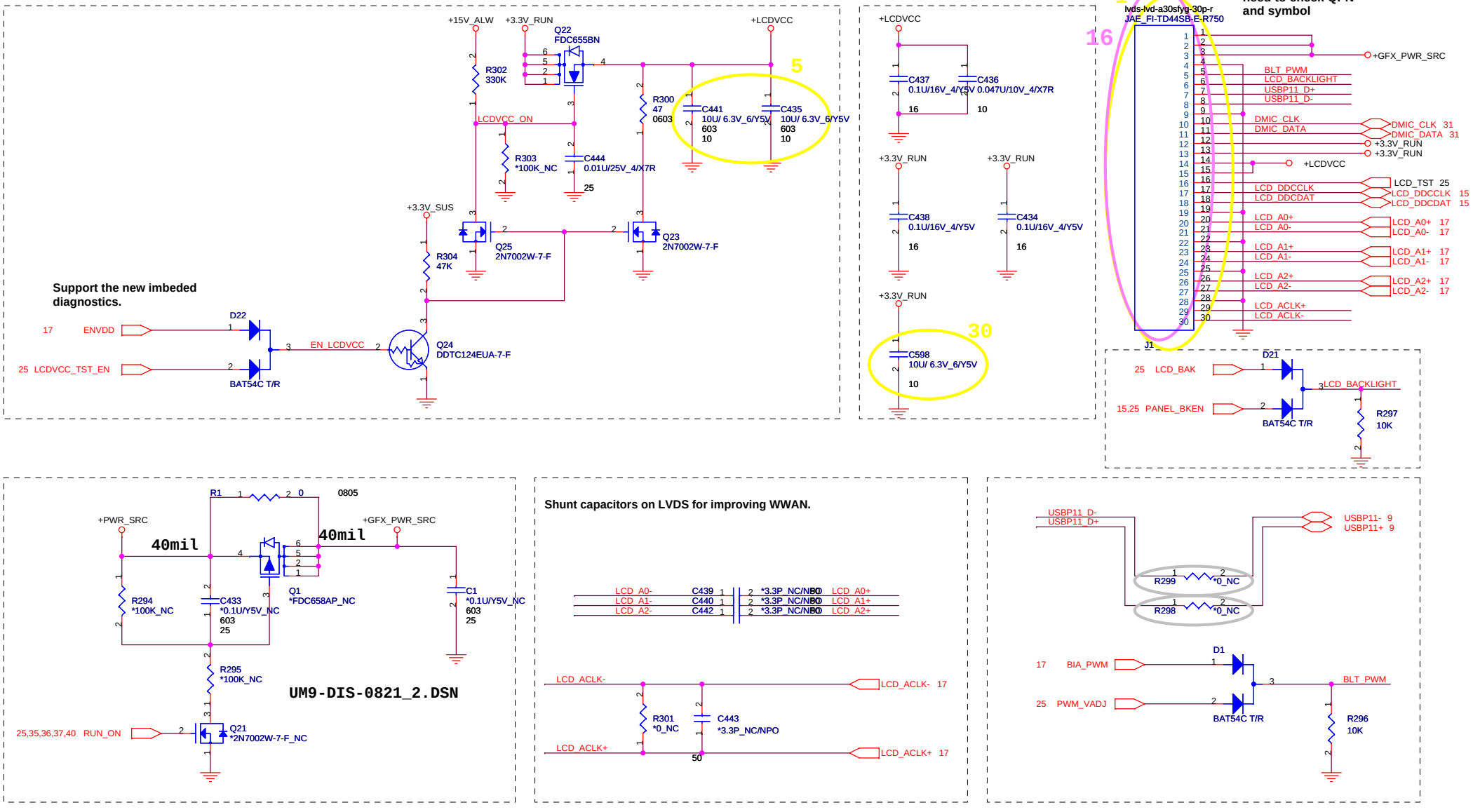




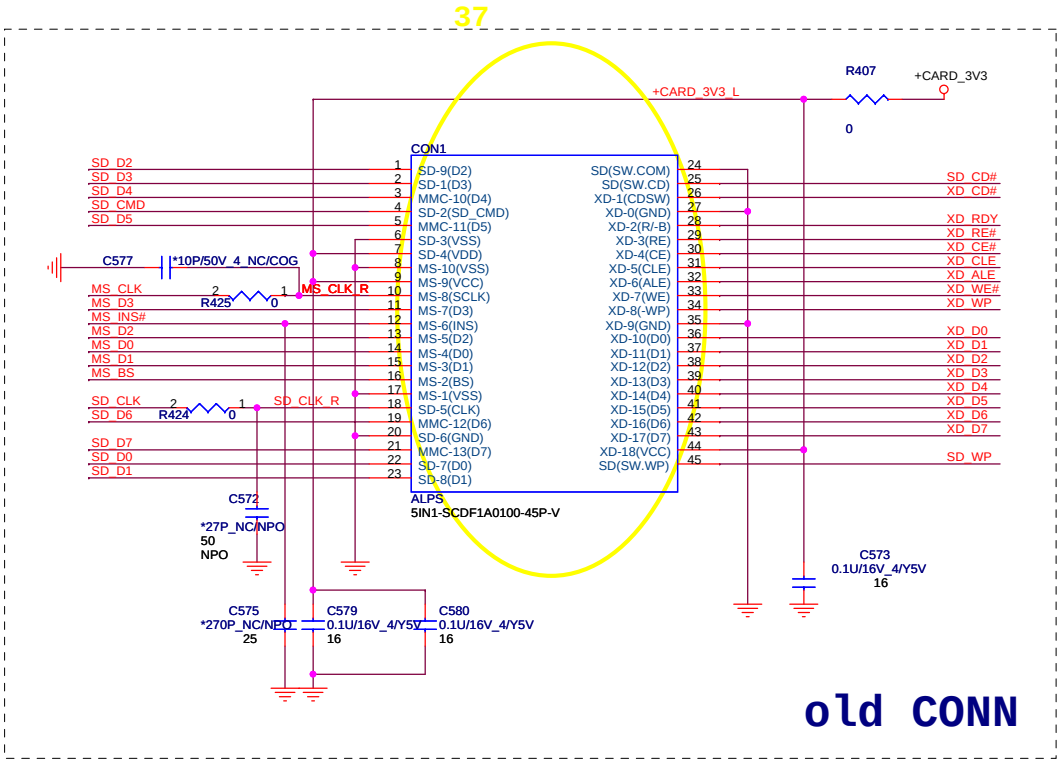
Quanta Computer Inc.

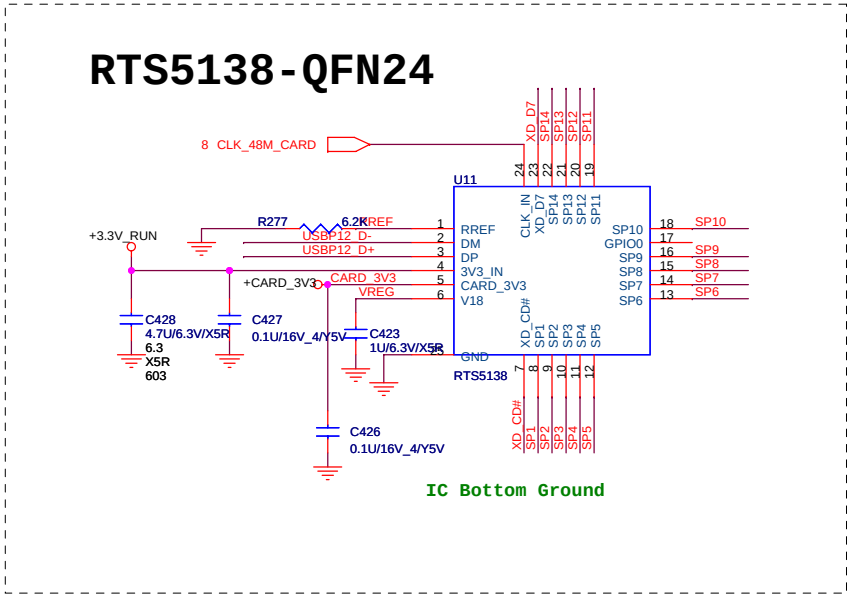
PROJECT : UM8B DIS

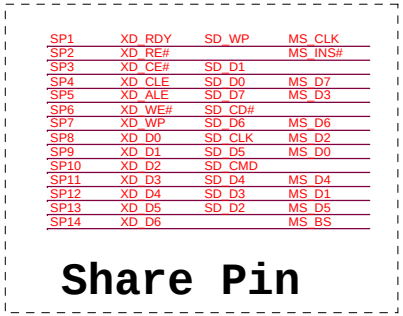
Size	Document Number	Rev
	Madison_DDR3_B_512M	1A
Date: Wednesday, February 10, 2010	Sheet 20 of 46	

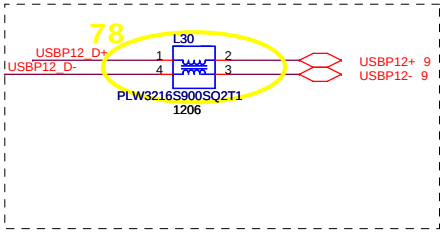


Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: LCD CONN	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 22 of 46	





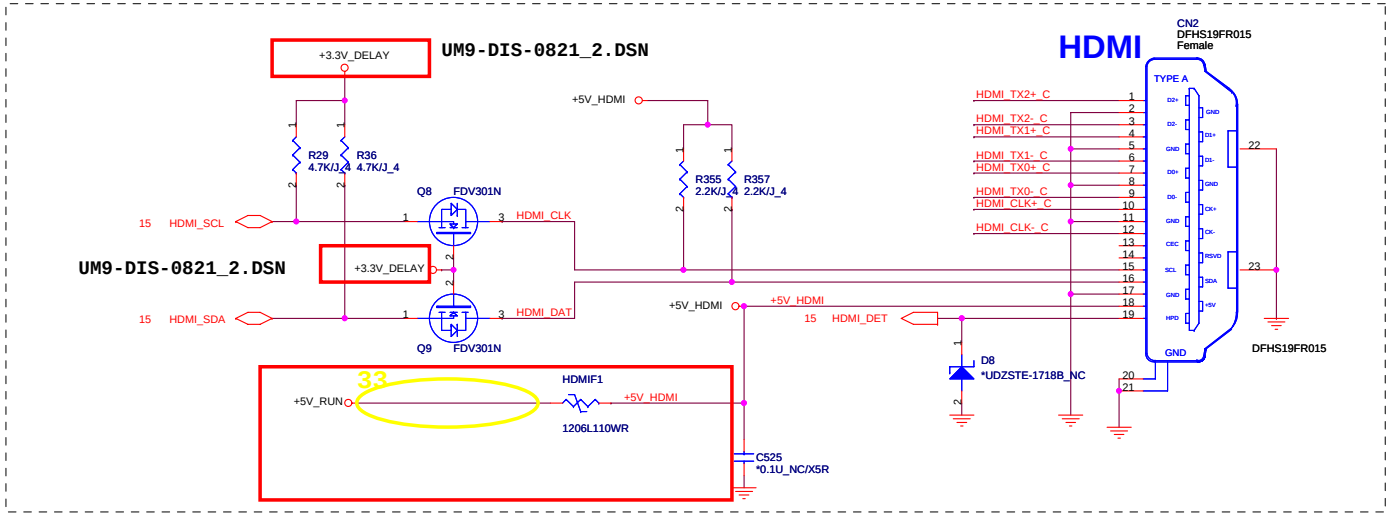


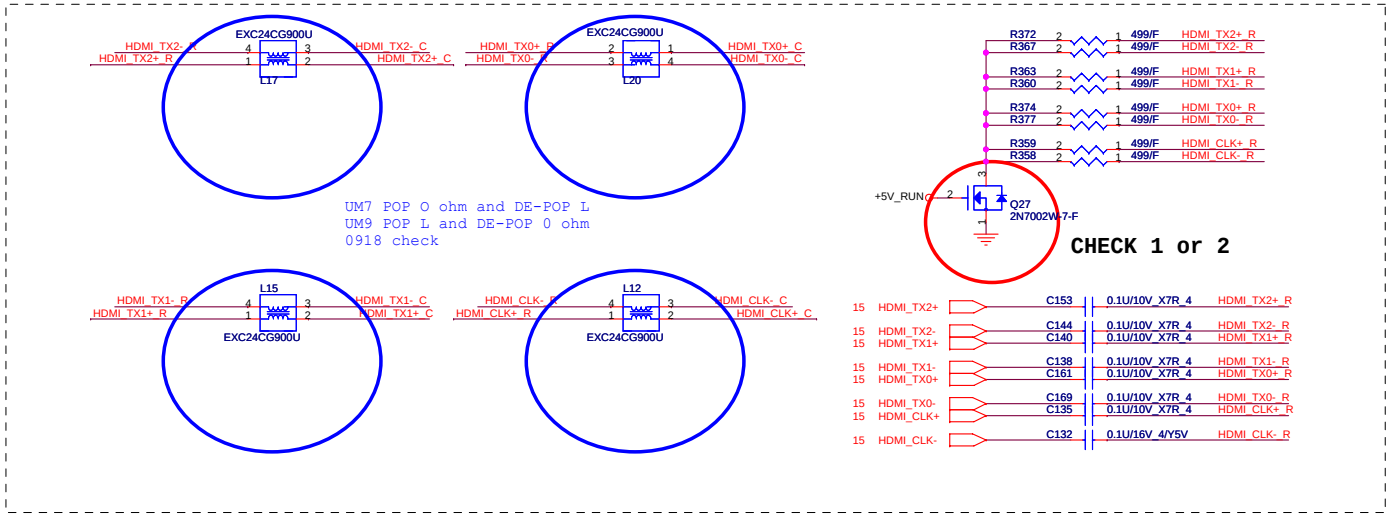


Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Card Reader(RST5138)	1A
Date: Wednesday, February 10, 2010	Sheet 23 of 46	





Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	HDMI	1A

Date: Wednesday, February 10, 2010 Sheet 24 of 46

UM3

ITE8502E LQFP-128L

U4

KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO

ITE8502E lqfp128-16x16-4

Place these caps close to ITE8502.

Charge and BAT
PCH
LAN, Clock Thermal IC

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Check

UM7 POP 2.2k
UM9 POP 10k
0918 check

UM7 DE-POP
UM9 POP
0918 check

Board ID Straps

Park 1G
Discrete
Park
UMA

VGA_TYPE
VGA_IDENTIFY

BID1	USB_RIGHT_EN#	UM8(UMA)	UM8C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13"	0	0
14"	1	0
17"	0	1

32KHz Clock.

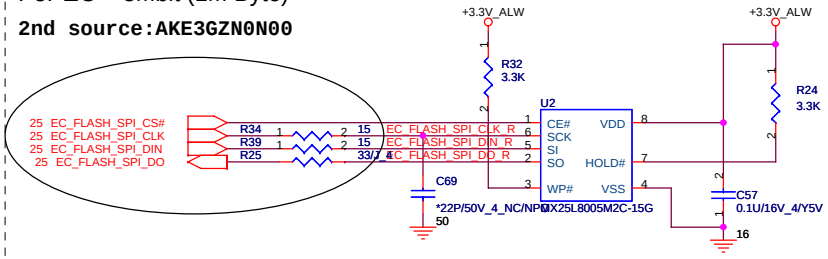
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	SIO ITE8502	1A

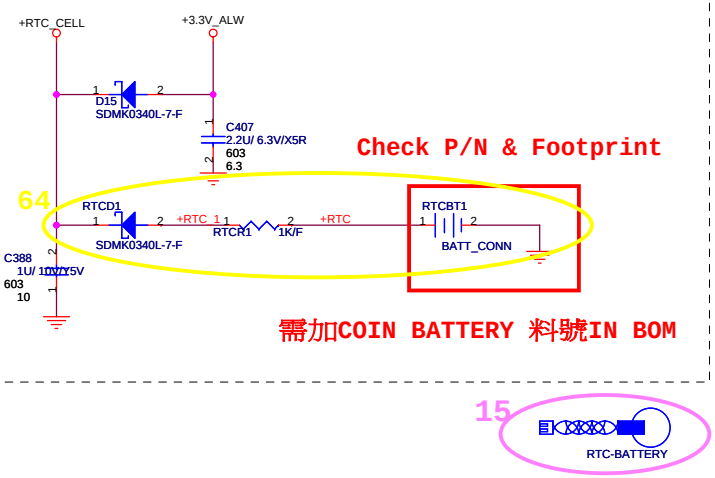
Date: Wednesday, February 10, 2010 Sheet 25 of 46

For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



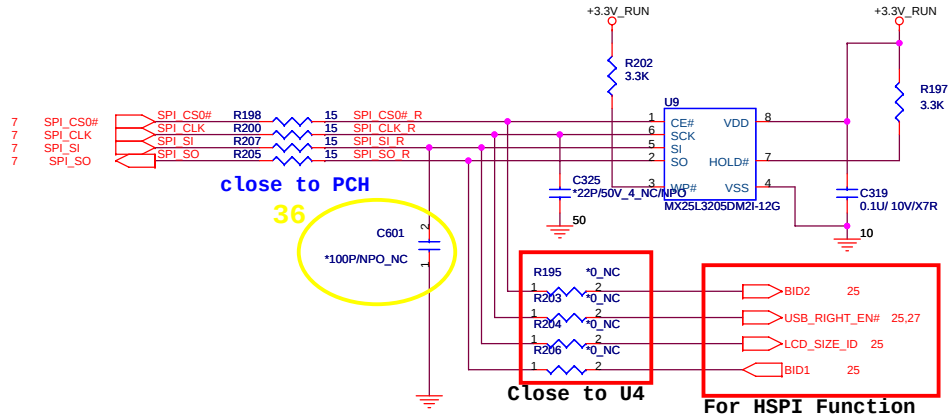
RTC BATTERY



For PCH

32Mbit (4M Byte)

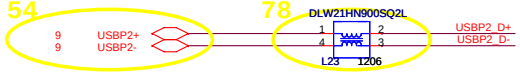
2nd source:AKE39ZP0N00



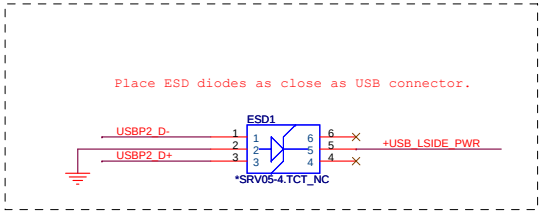
Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: FLASH/RTC	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 26 of 46	

eSATA and USB To DB

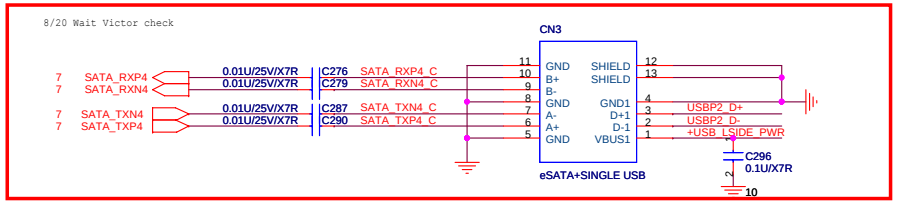
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

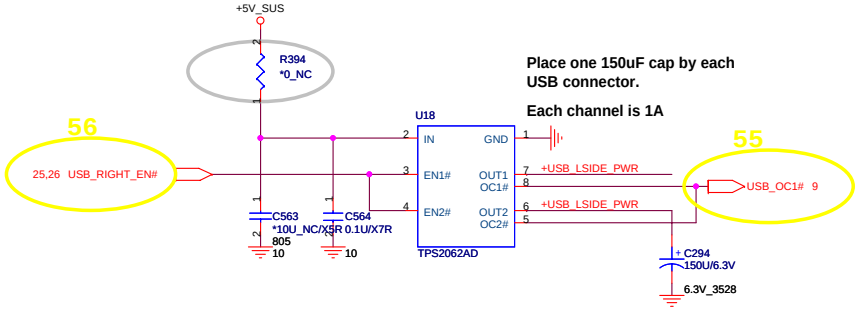


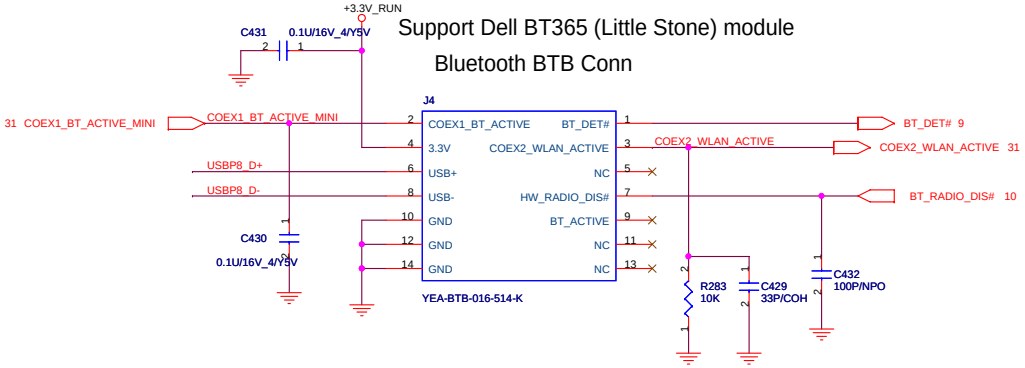
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

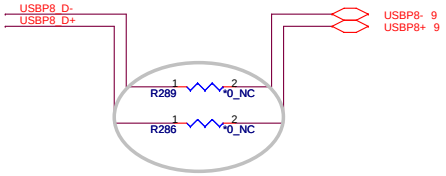


USB and eSATA Conn.









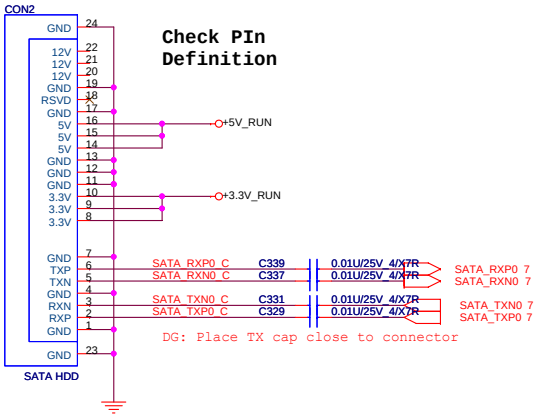
Quanta Computer Inc.

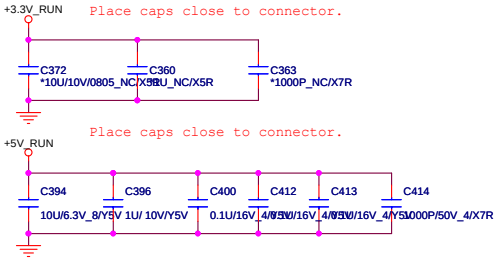
PROJECT : UM8B DIS

Size	Document Number	Rev
	eSATA & Right USB & BT	1A

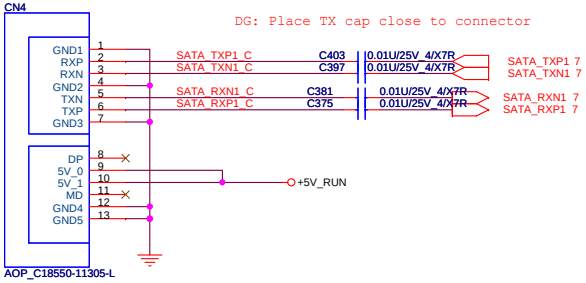
Date: Wednesday, February 10, 2010 Sheet 27 of 46

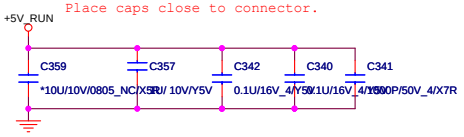
SATA Connector.

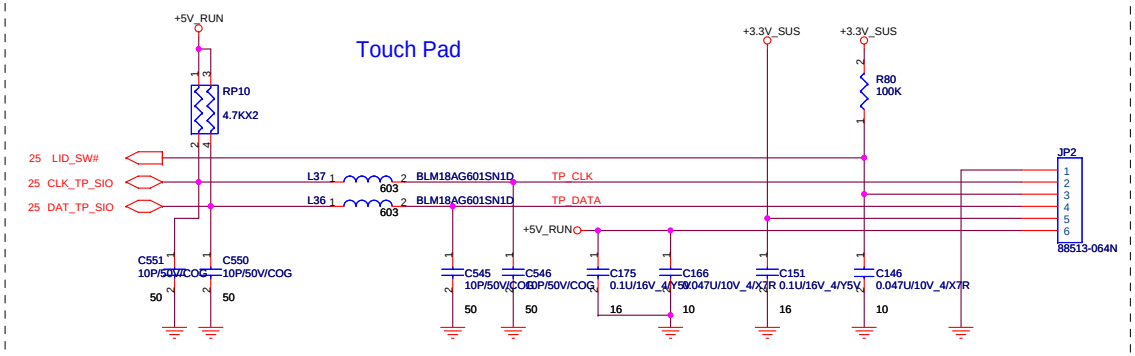




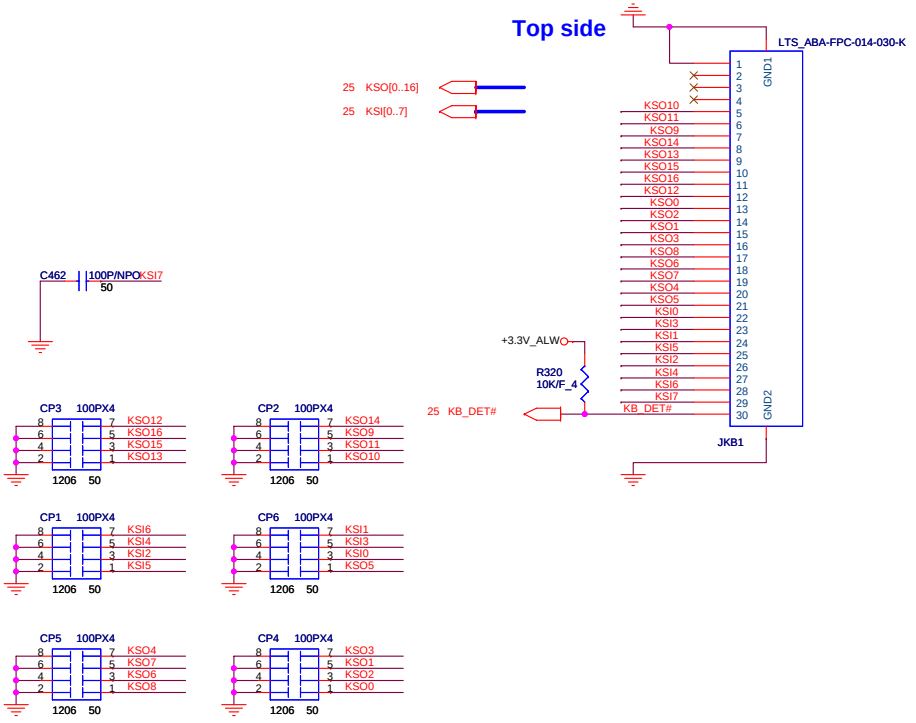
ODD Connector







KEYBOARD CONNECTOR

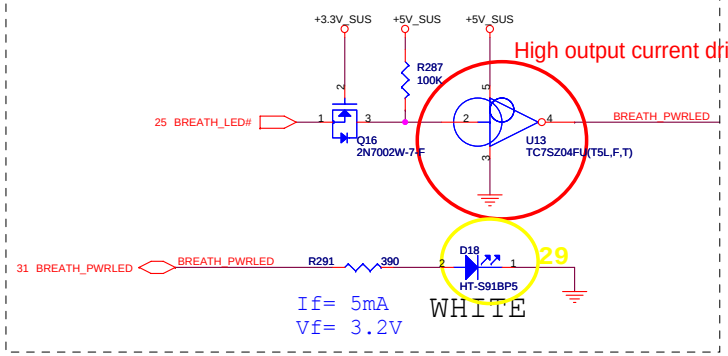


100P CAPS CLOSE TO JKB1

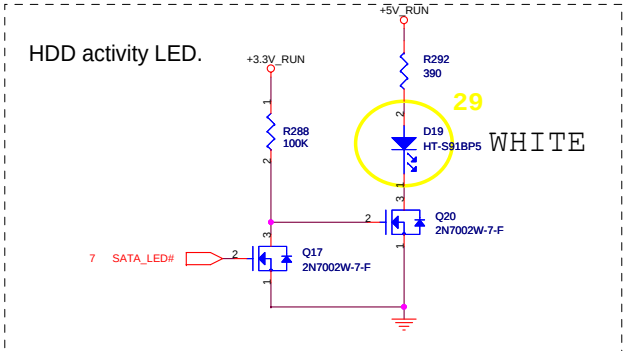
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	SATA (HDD&ODD) & TP & KB	1A
Date: Wednesday, February 10, 2010	Sheet 28 of 46	

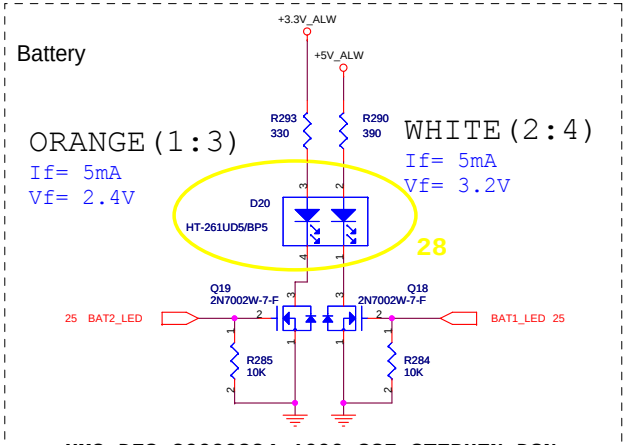
Power



HDD activity LED.



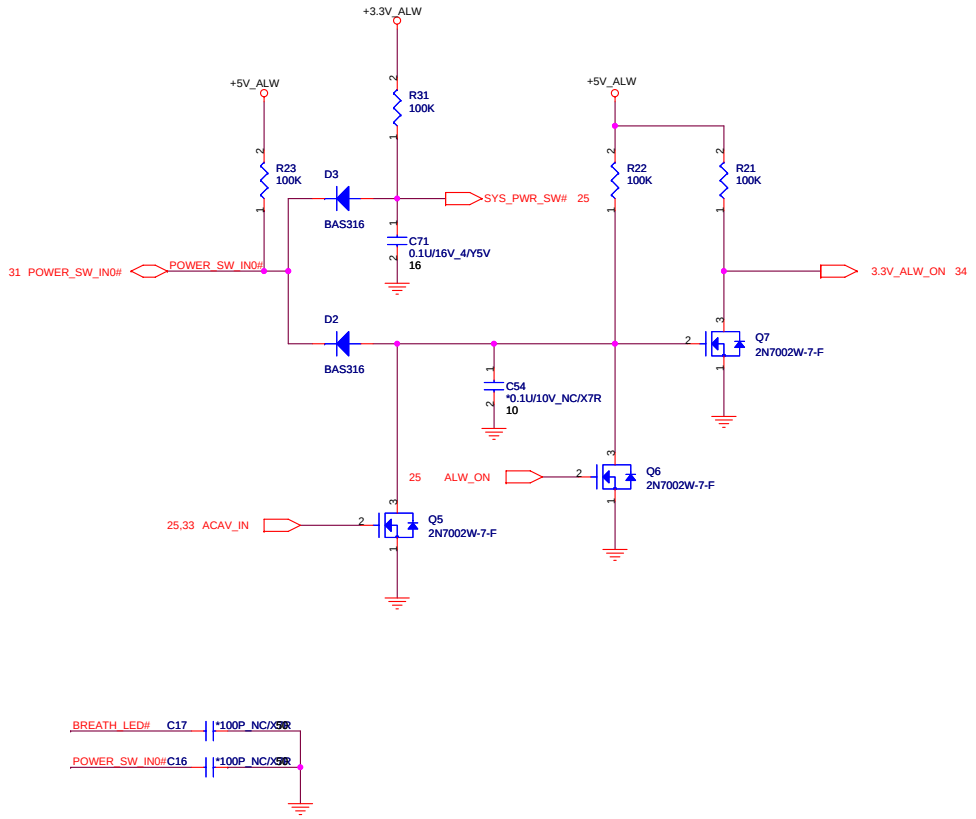
Battery



UM3_DIS_20090824_1000_SSI_STEPHEN.DSN

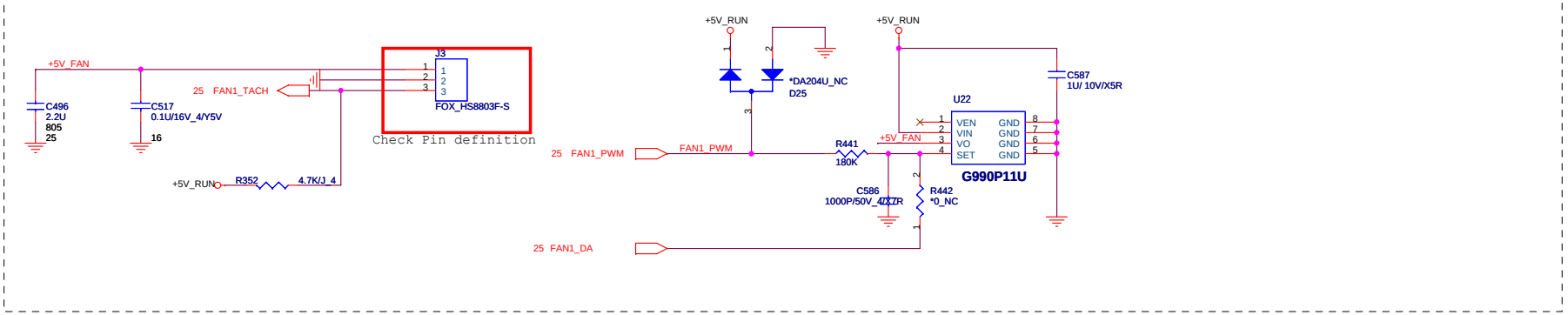
check outpout current for 3 LED

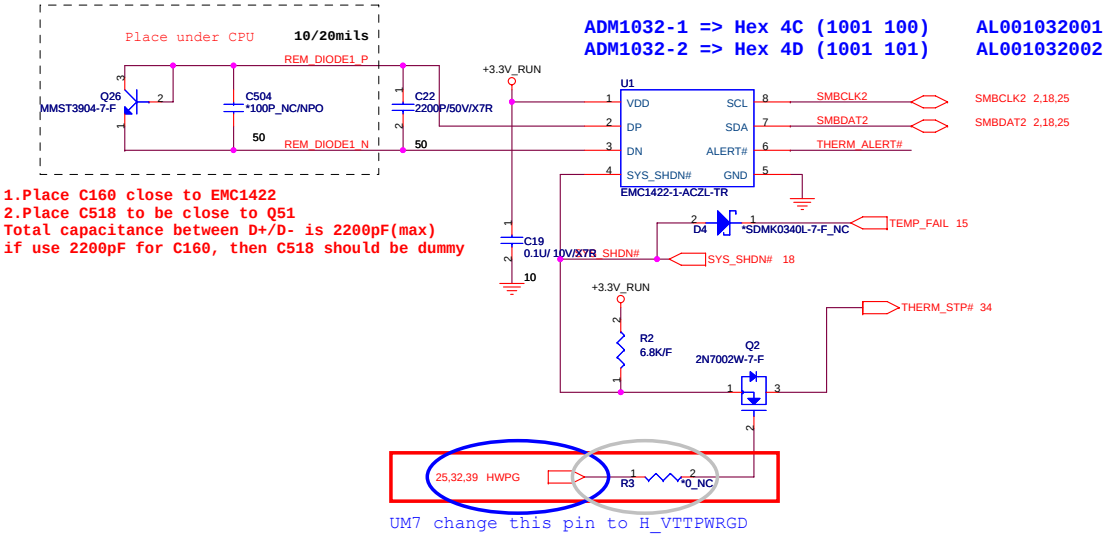
3VALW ON POWER LOGIC

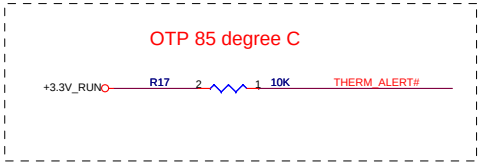


Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: SWITCH, LED	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 29 of 46	

FAN CONTROL



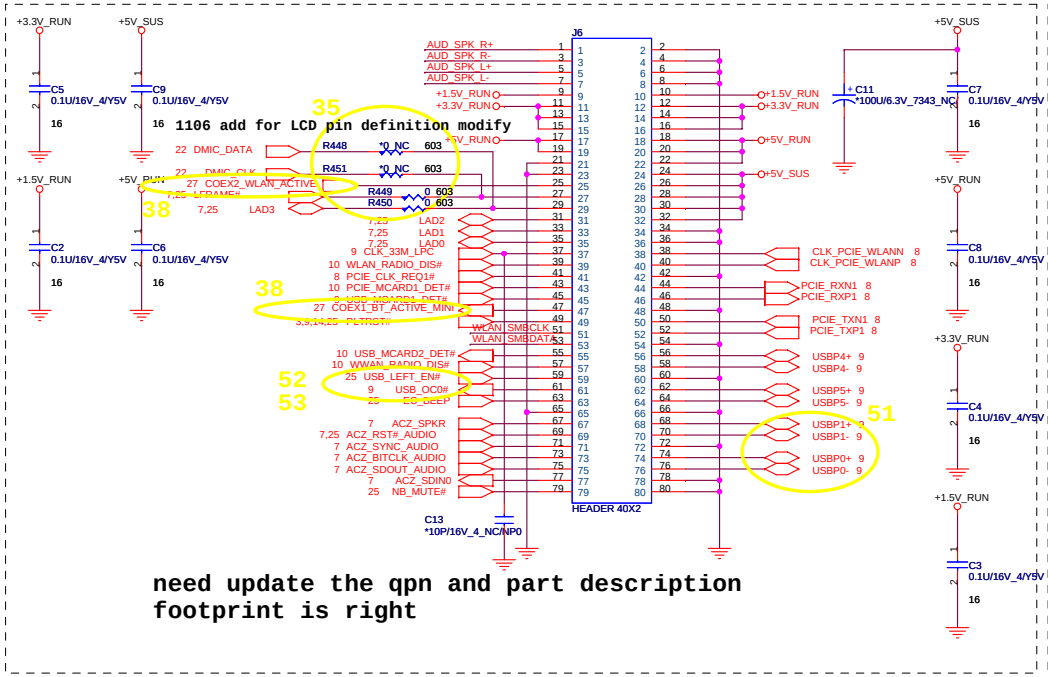




SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

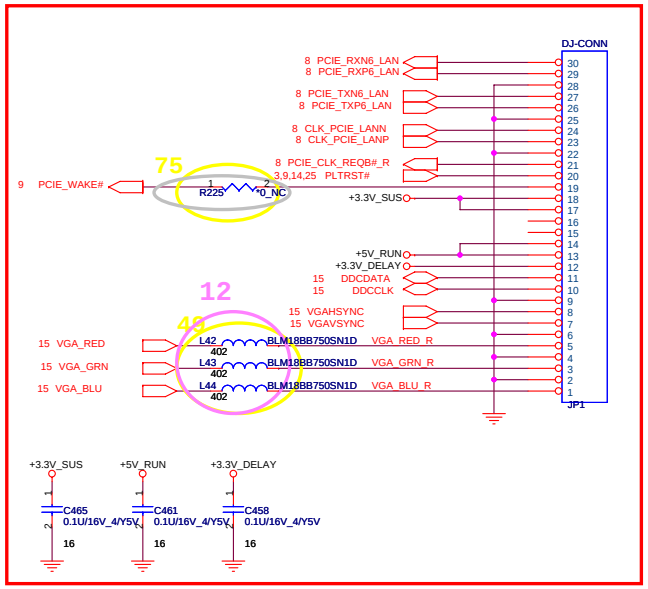
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	FAN & THERMAL	1A
Date: Wednesday, February 10, 2010	Sheet 30 of 46	

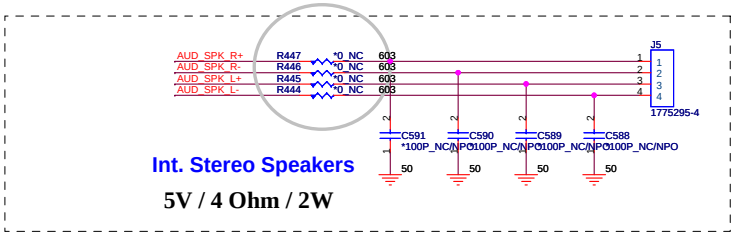


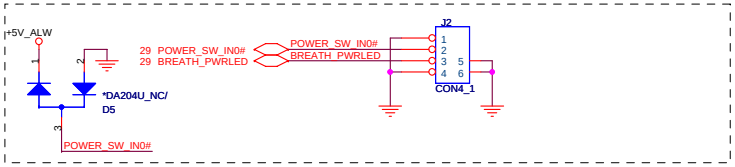
need update the qpn and part description
footprint is right

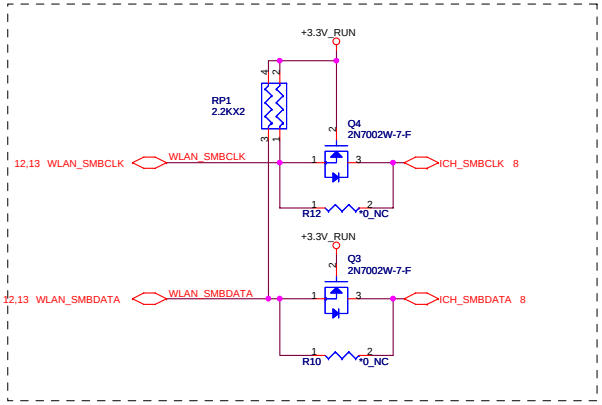
Check P/N and footprint



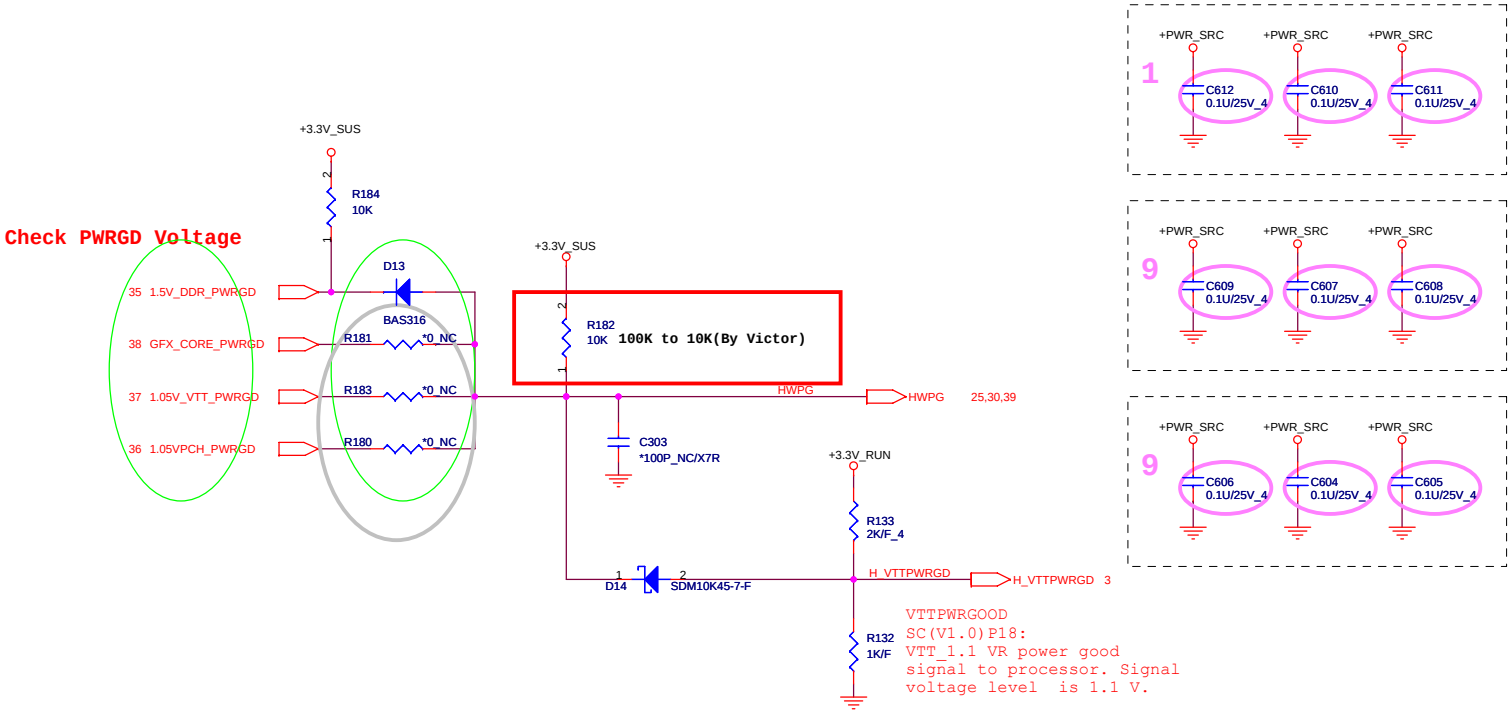
To CRT board



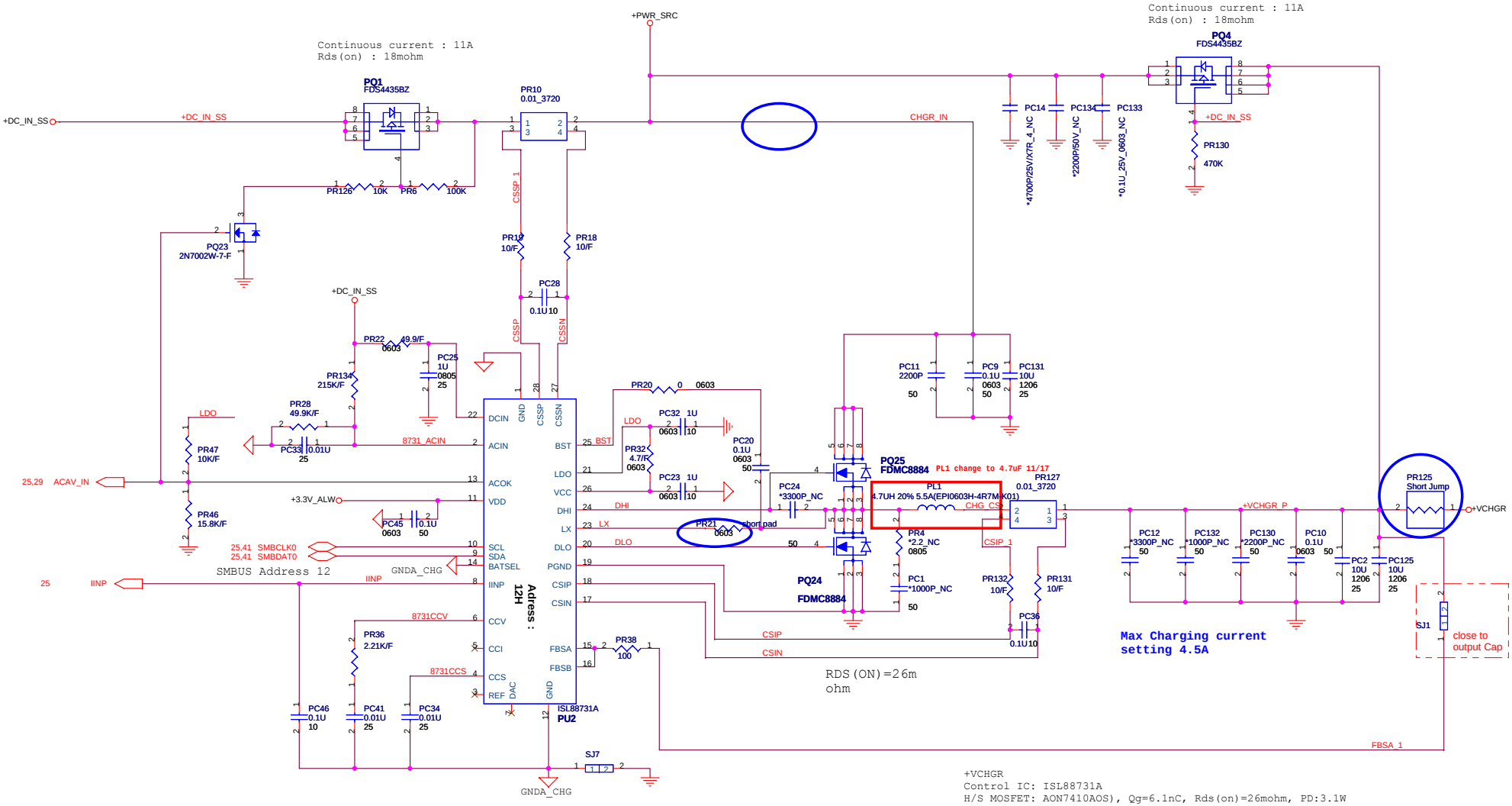




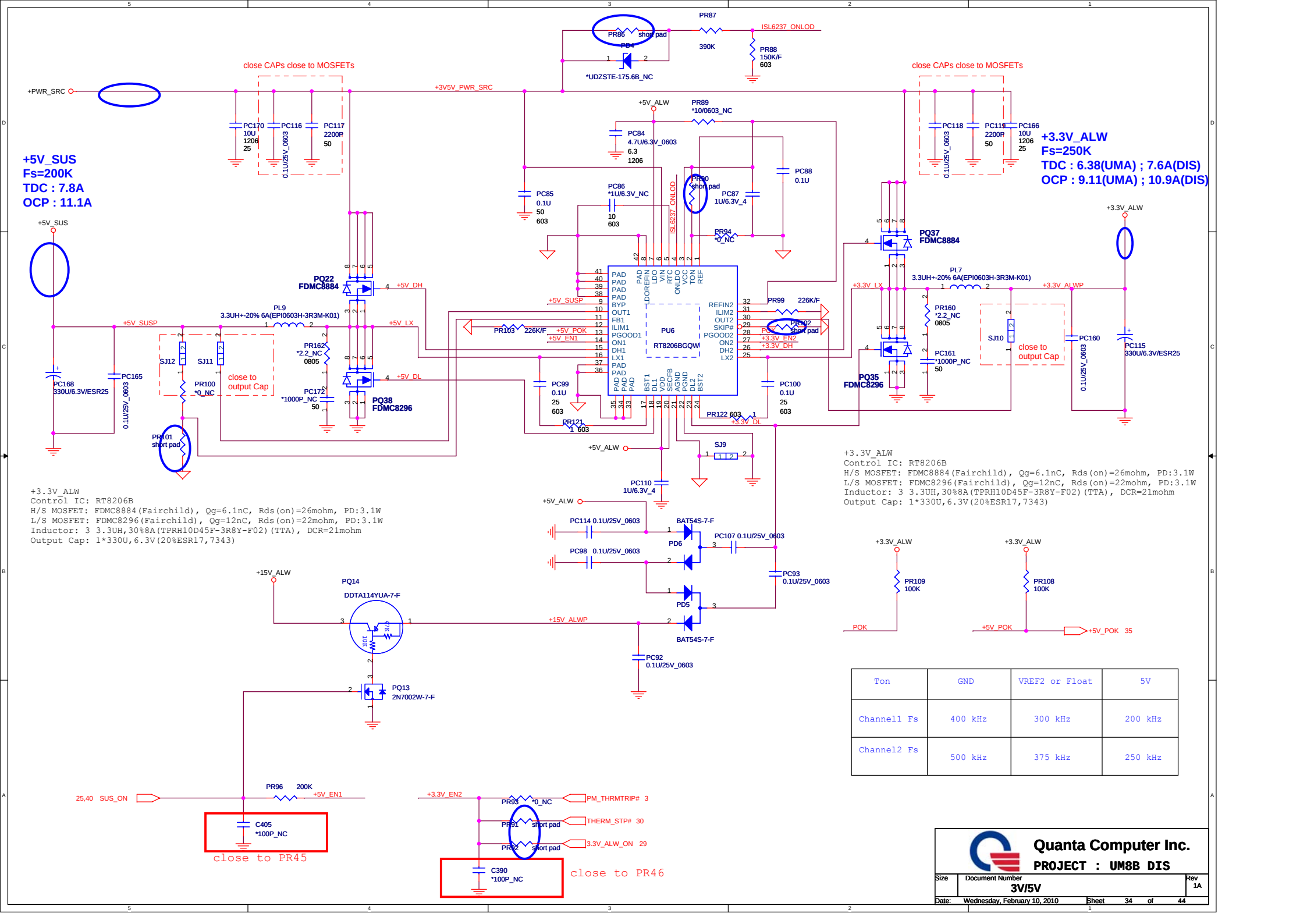
Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: BTB CONN & Audio conn	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 31 of 46	



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: System Reset Circuit	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 32 of 46	

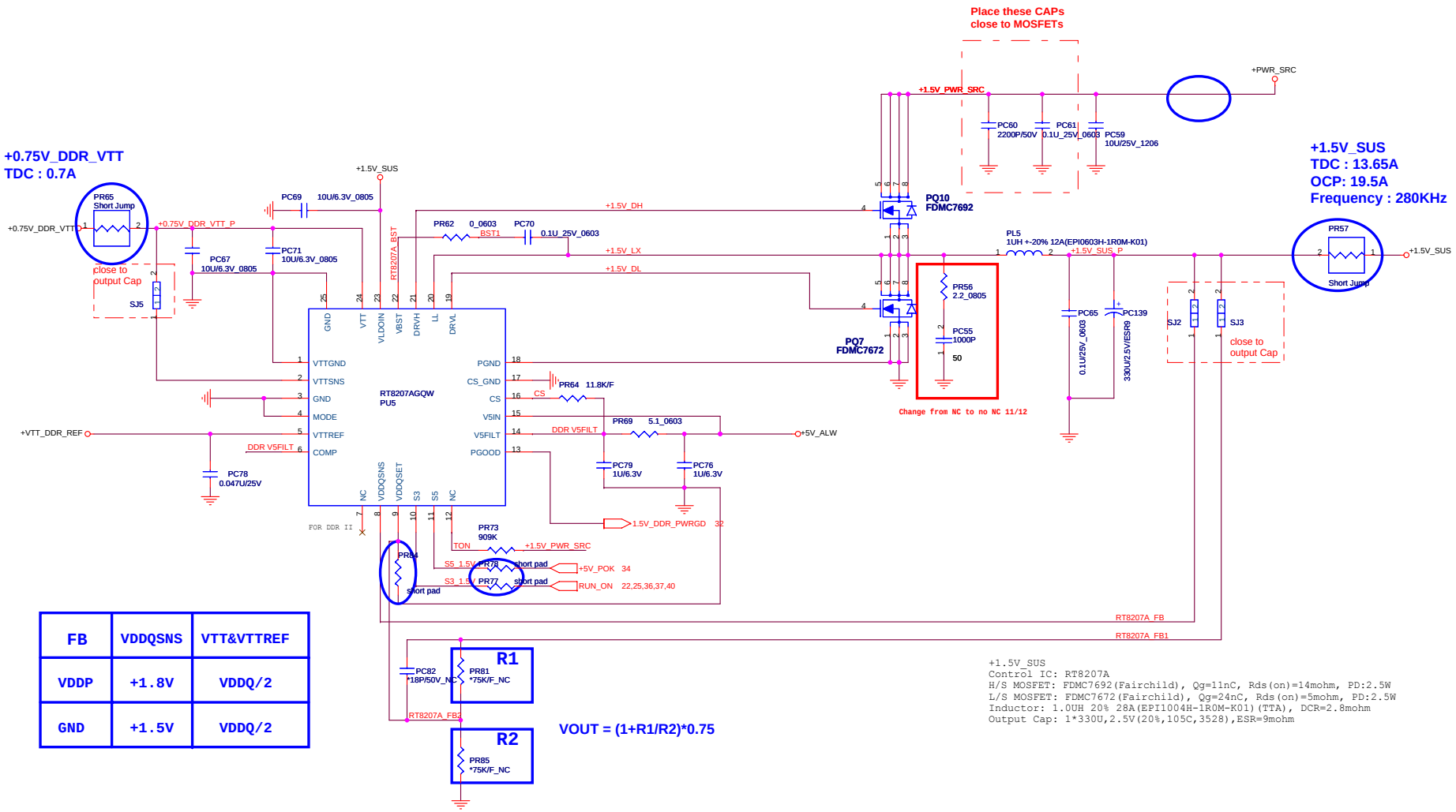


Quanta Computer Inc.			
PROJECT : UM8B DIS			
Size	Document Number		Rev
	Charger		1A
Date: Wednesday, February 10, 2010	Sheet 33 of 44		



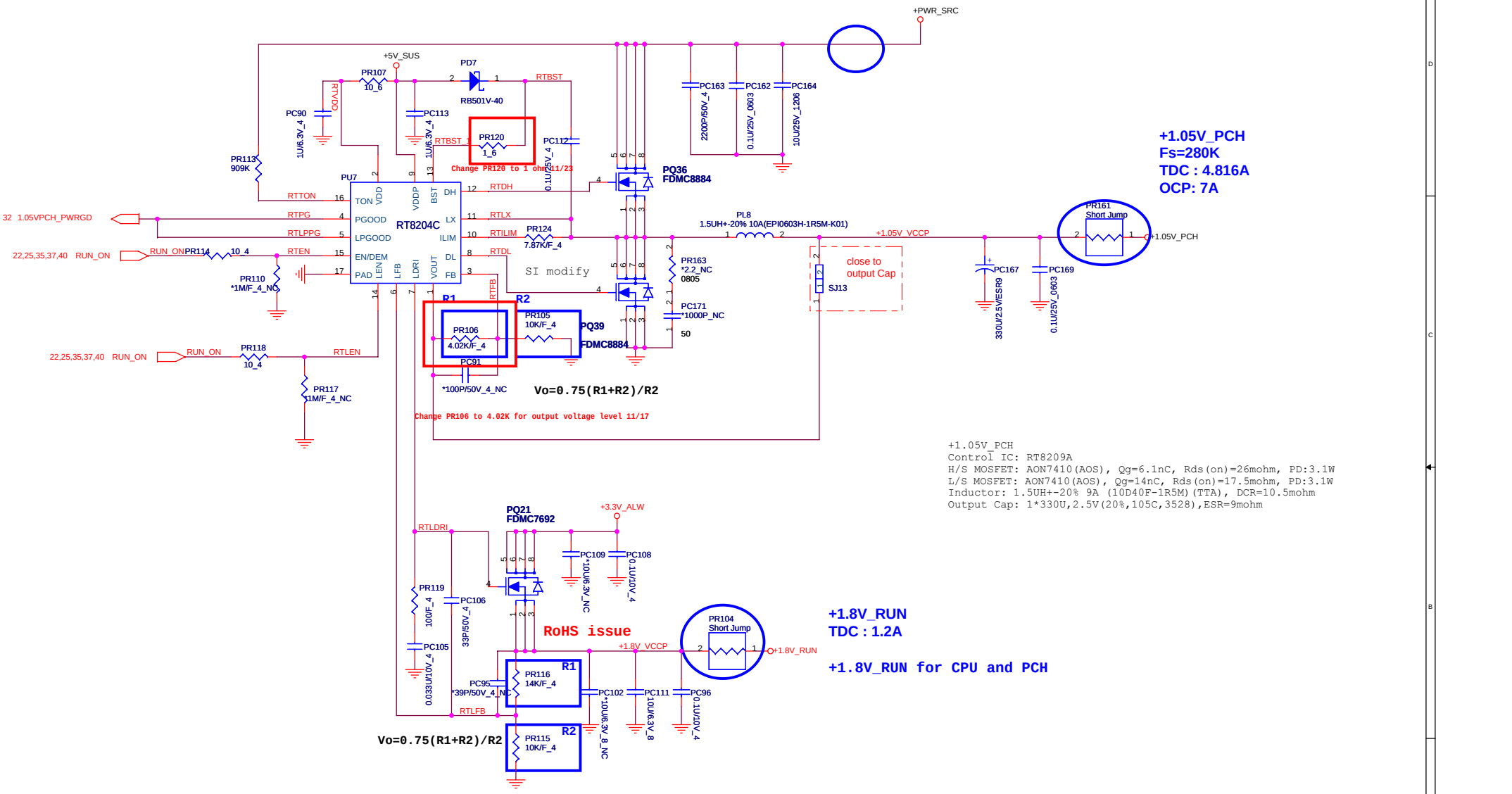
Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: 3V/5V	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 34 of 44	

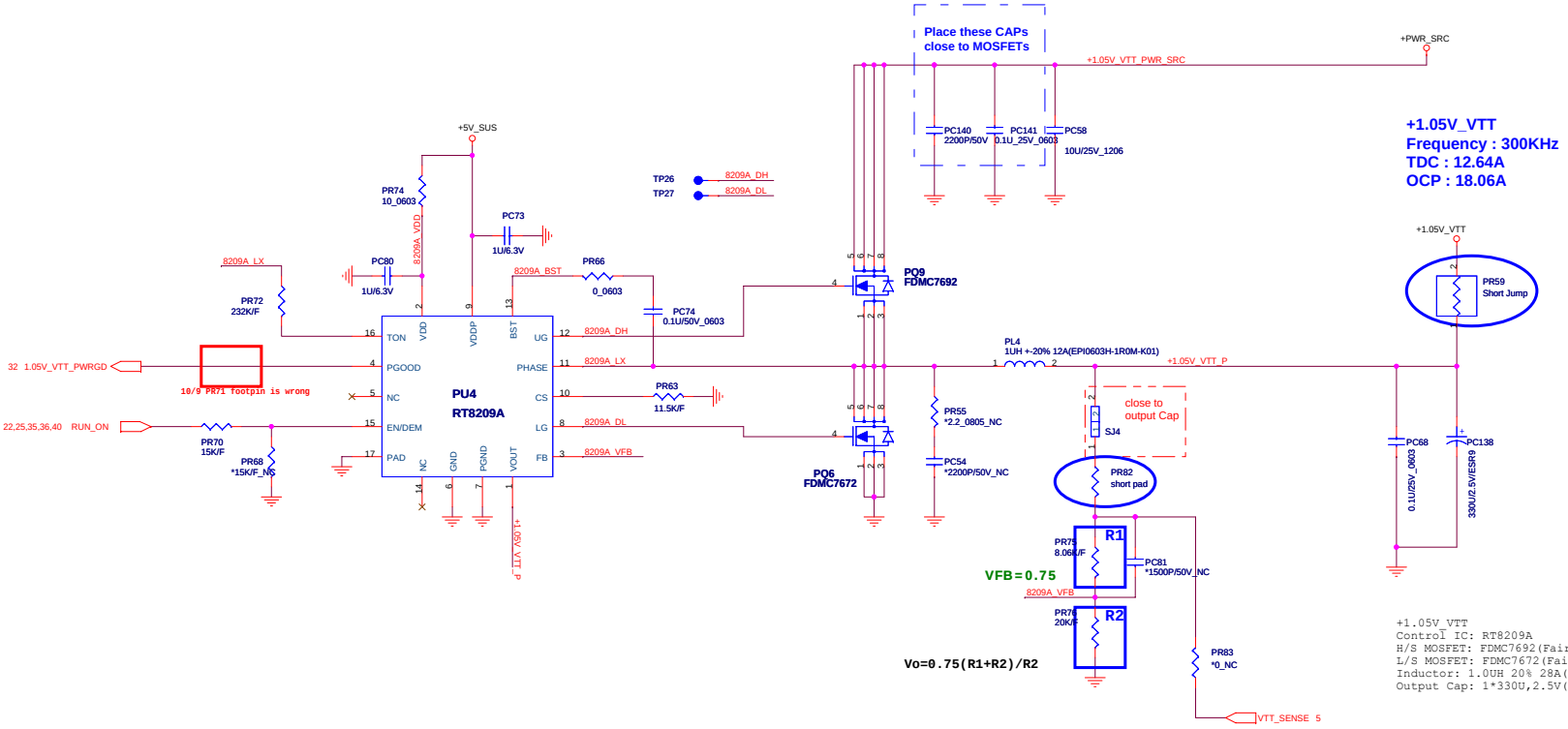


FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

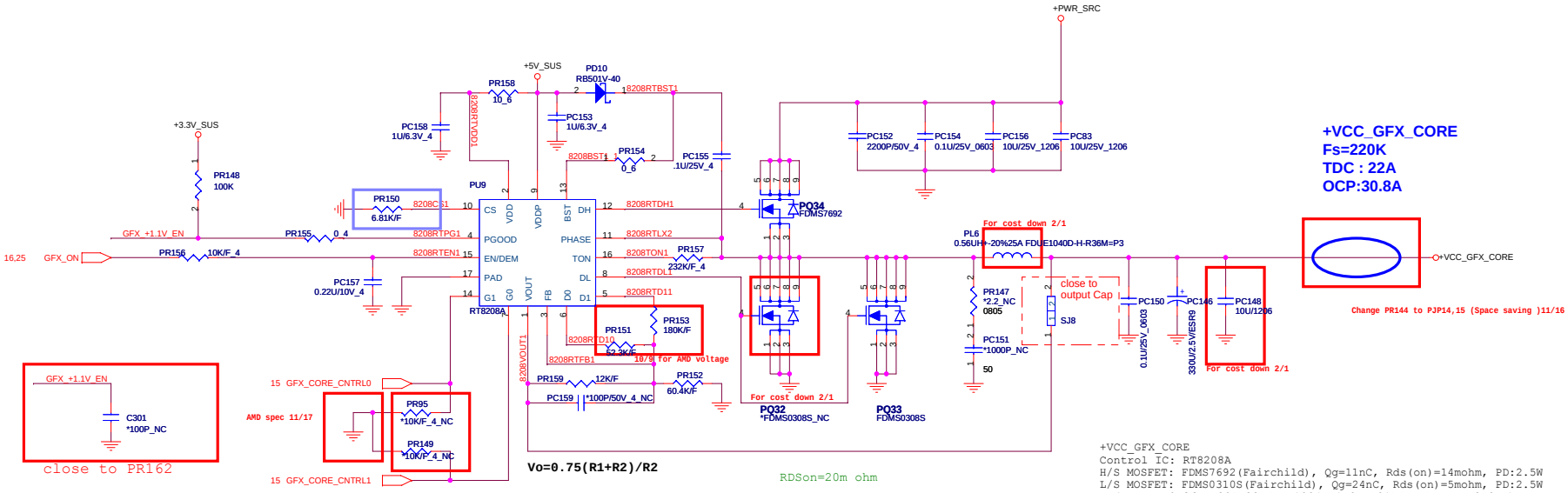
Quanta Computer Inc.	PROJECT : UM8B DIS	
Size	Document Number: 1.5V_DDR/0.75V	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 35 of 44	



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: 1.05V_PCH	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 36 of 44	



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: 1.05V_VTT	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 37 of 44	



+VCC_GFX_CORE
Fs=220K
TDC : 22A
OCP:30.8A

+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 2*330U,2.5V(20%,105C,3528),ESR=9mohm

+VCC_GFX_CORE_M92

For M96-LP:

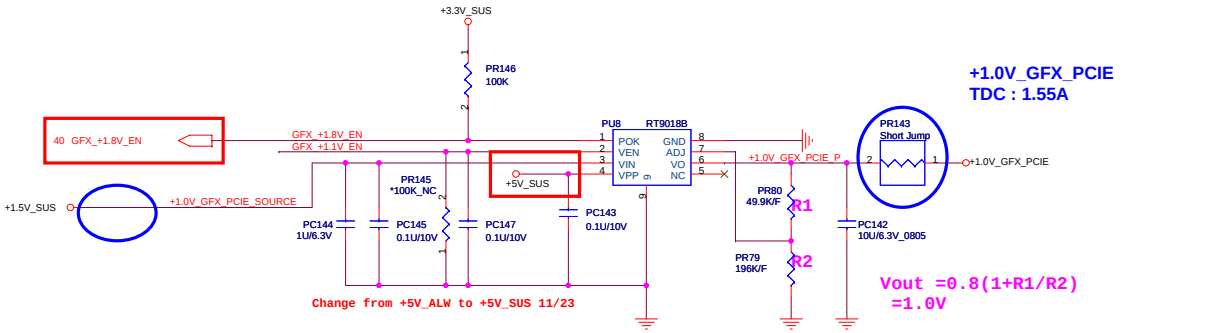
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.0V
HIGH	HIGH	1.05V(N/A)

For Park-XT:

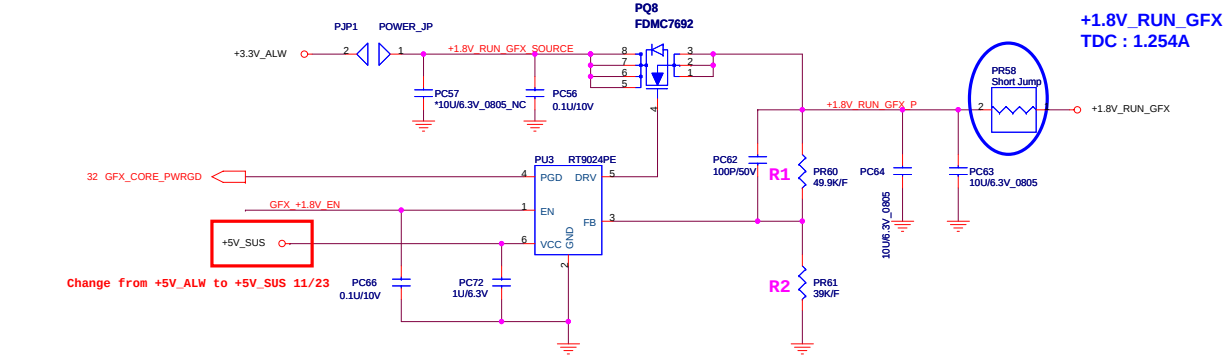
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V

Chagne List:

For Park-XT:	For M96-LP:
PR151:52.3K	PR151:90.9K
PN:CS35232FB10	PN:CS39092FB11
PR79:196K	PR79:133K
PN:CS41962FB01	PN:CS41332FB06



+1.0V_GFX_PCIE
TDC : 1.55A

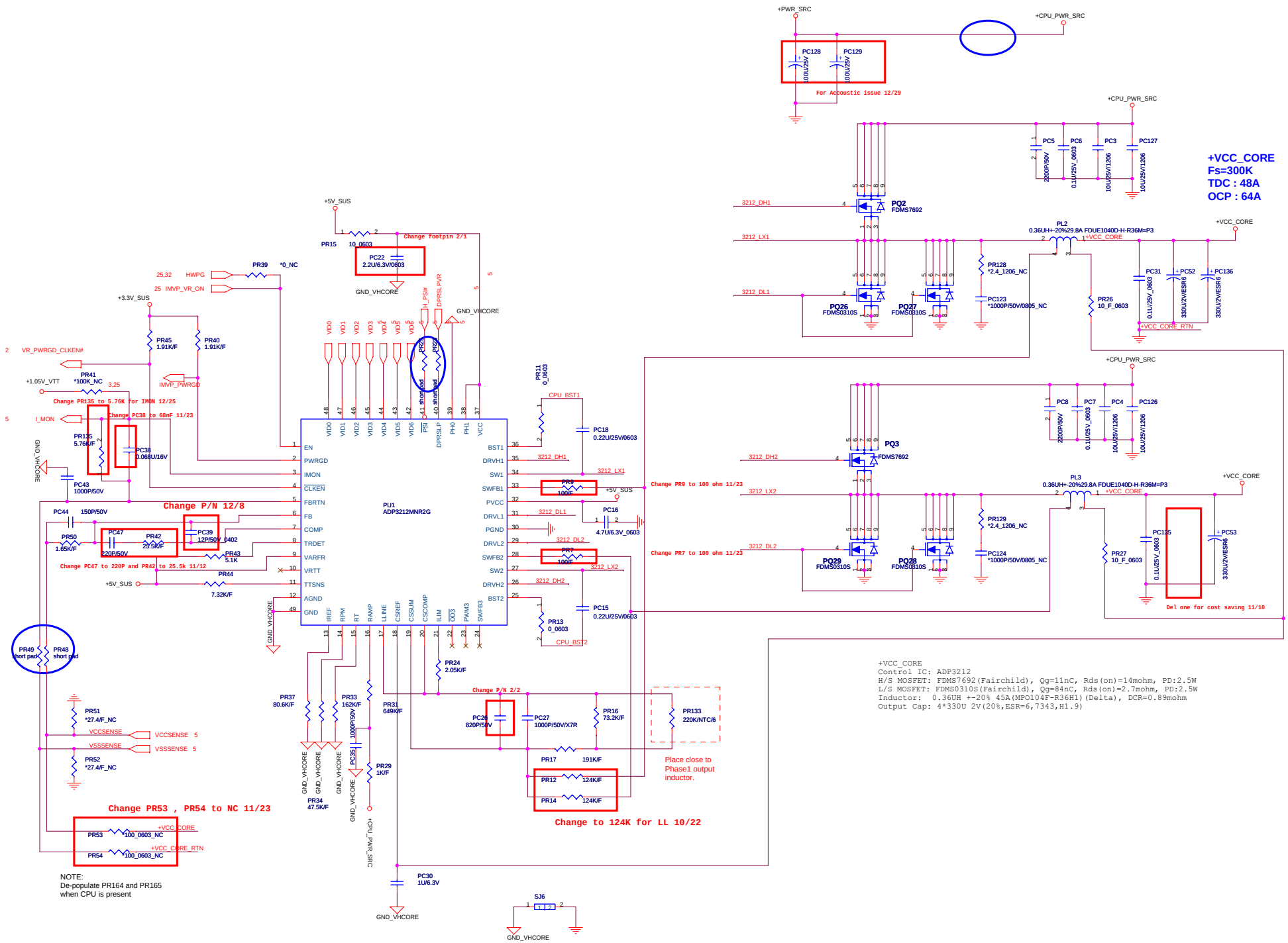


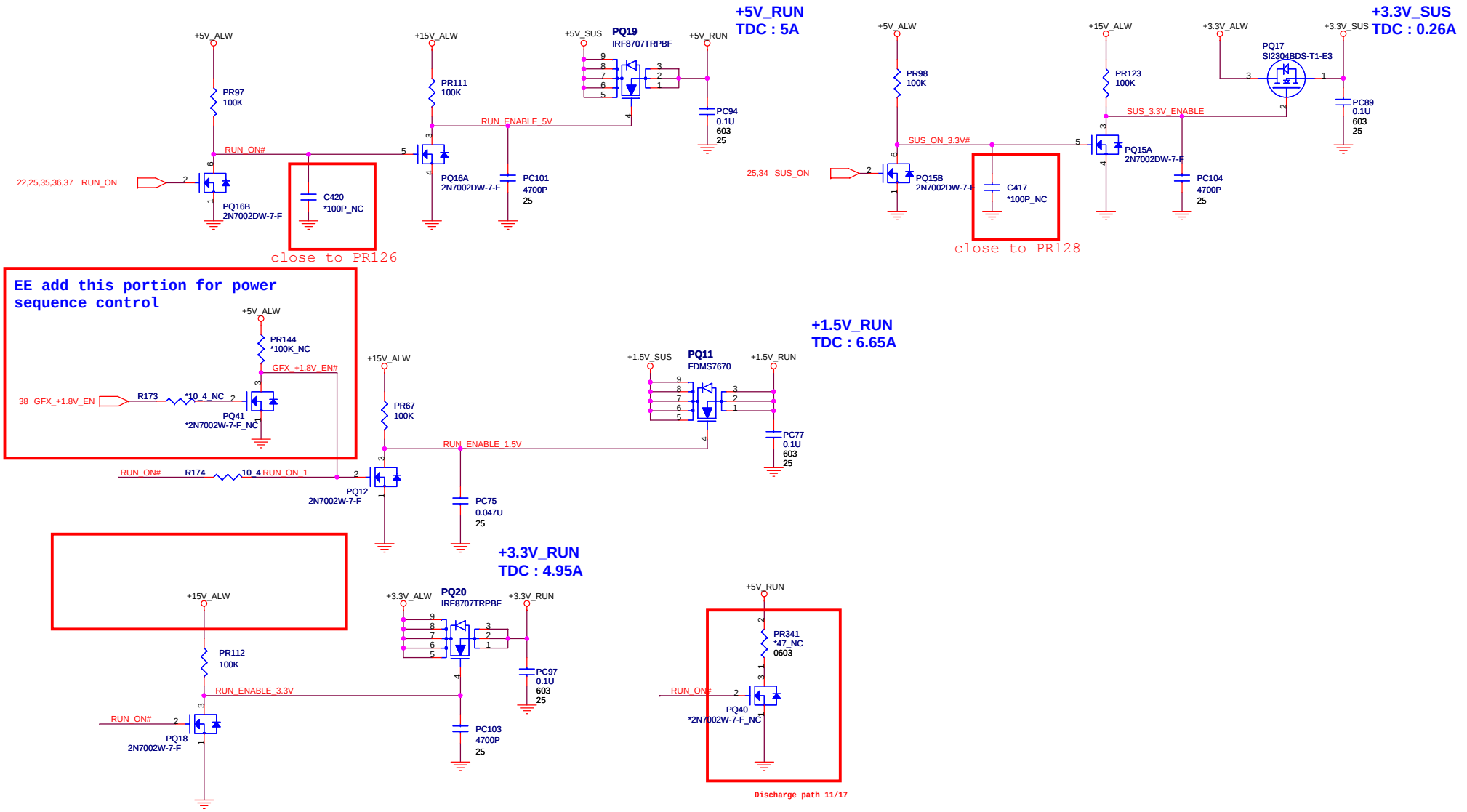
+1.8V_RUN_GFX
TDC : 1.254A

Quanta Computer Inc.
PROJECT : UM8B DIS

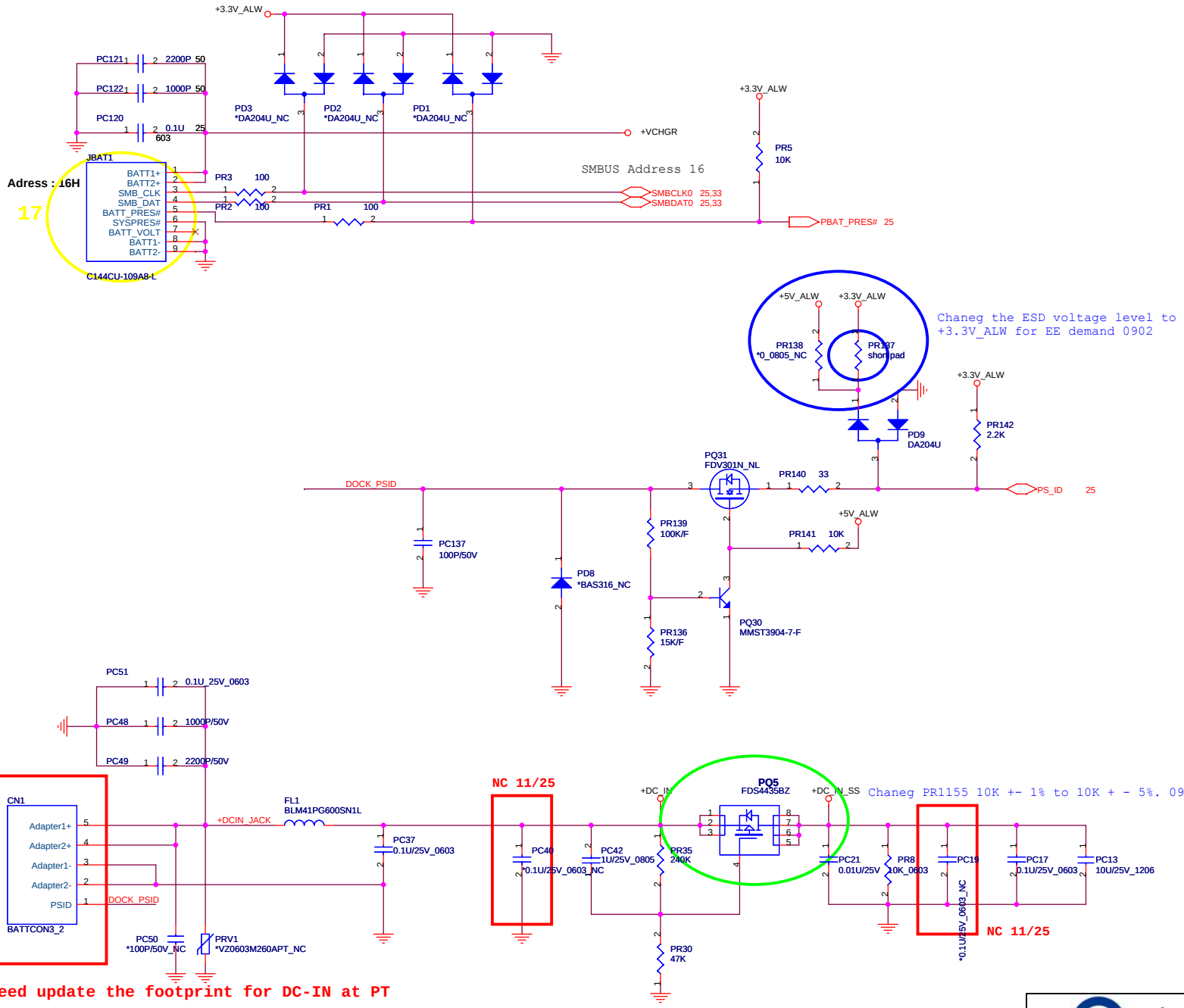
Size	Document Number	Rev
	VGA power	1A

Date: Wednesday, February 10, 2010 Sheet 38 of 44


+VCC_CORE
Fs=300K
TDC : 48A
OCP : 64A
PU1
ADP3212MNR2G
PQ2
FDMS7692
PQ3
FDMS7692
PQ26
FDMS0310S
PQ27
FDMS0310S
PQ29
FDMS0310S
PQ28
FDMS0310S
PL2
0.36UH+-20%29.8A FDUE1040D-H-R36M=P3
PL3
0.36UH+-20%29.8A FDUE1040D-H-R36M=P3
Change P/N 12/8
Change PC47 to 220P and PR42 to 25.5k 11/12
Change PR53 , PR54 to NC 11/23
Change to 124K for LL 10/22
Change P/N 2/2
Change PR9 to 100 ohm 11/23
Change PR7 to 100 ohm 11/23
Change PR135 to 5.76K for IMON 12/25
Change PC38 to 68nF 11/23
Change footpin 2/1
For Accoustic issue 12/29
Del one for cost saving 11/10
Place close to Phase1 output inductor.
+VCC_CORE
Control IC: ADP3212
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=84nC, Rds(on)=2.7mohm, PD:2.5W
Inductor: 0.36UH +-20% 45A(MPO104F-R36H1)(Delta), DCR=0.89mohm
Output Cap: 4*330U 2V(20%,ESR=6,7343,H1.9)
NOTE:
De-populate PR164 and PR165
when CPU is present
Quanta Computer Inc.
PROJECT : UM8B DIS
CPU_CORE
Wednesday, February 10, 2010
Sheet 39 of 44

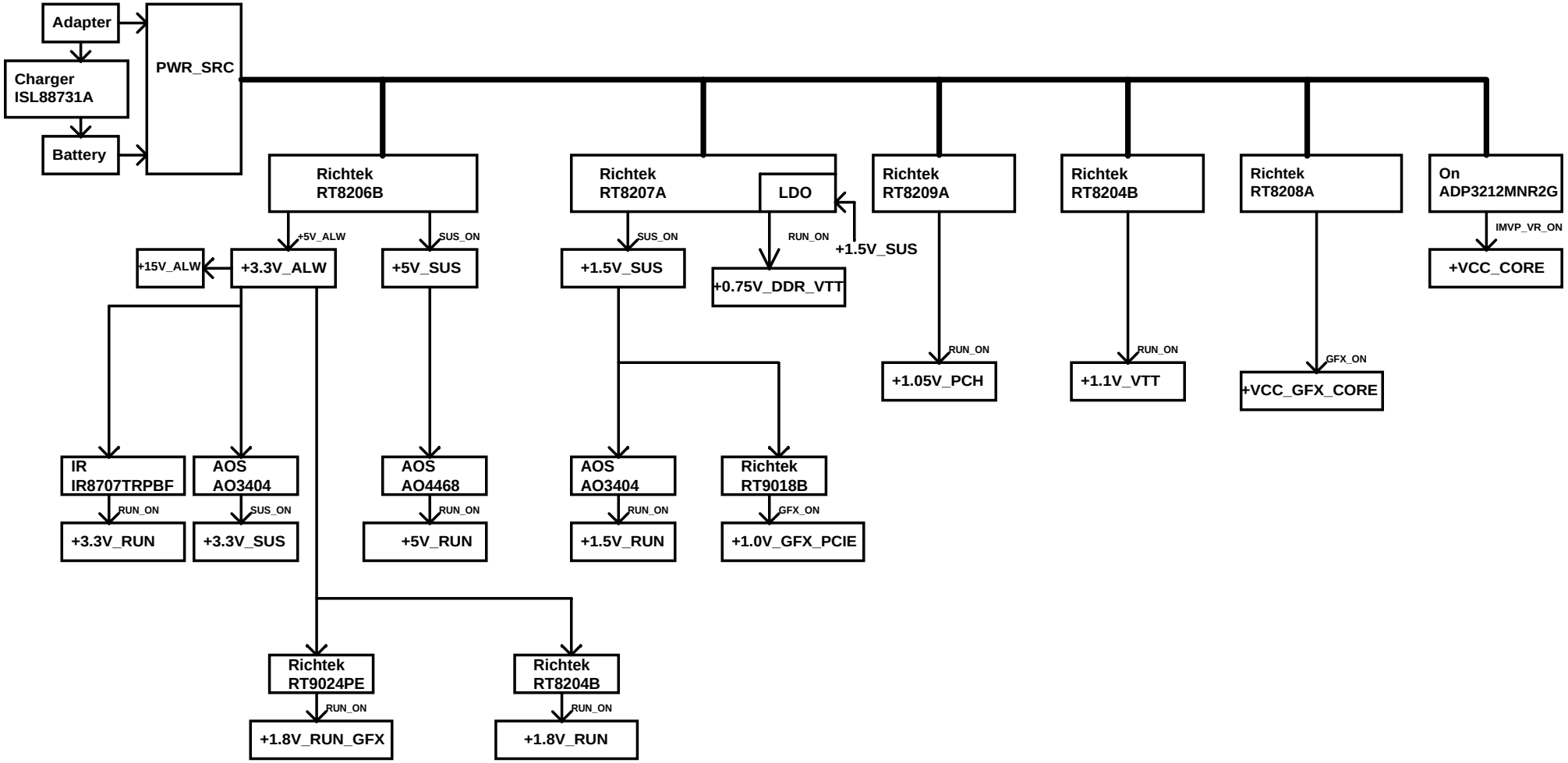


Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: Run Power Switch	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 40 of 44	



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: Batt & DC-IN	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 41 of 44	

VER : 1A

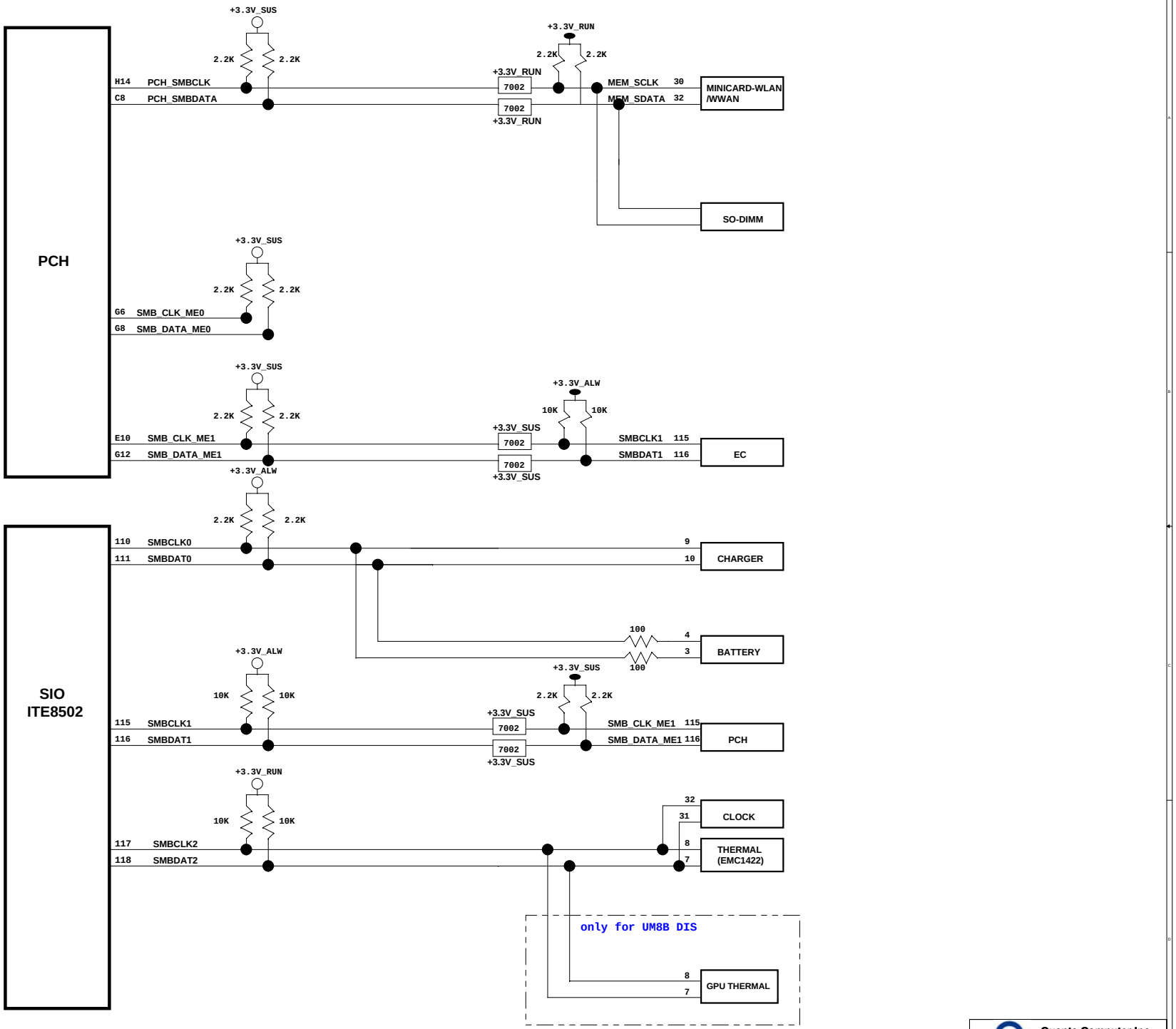


Quanta Computer Inc.

PROJECT : UM8B DIS

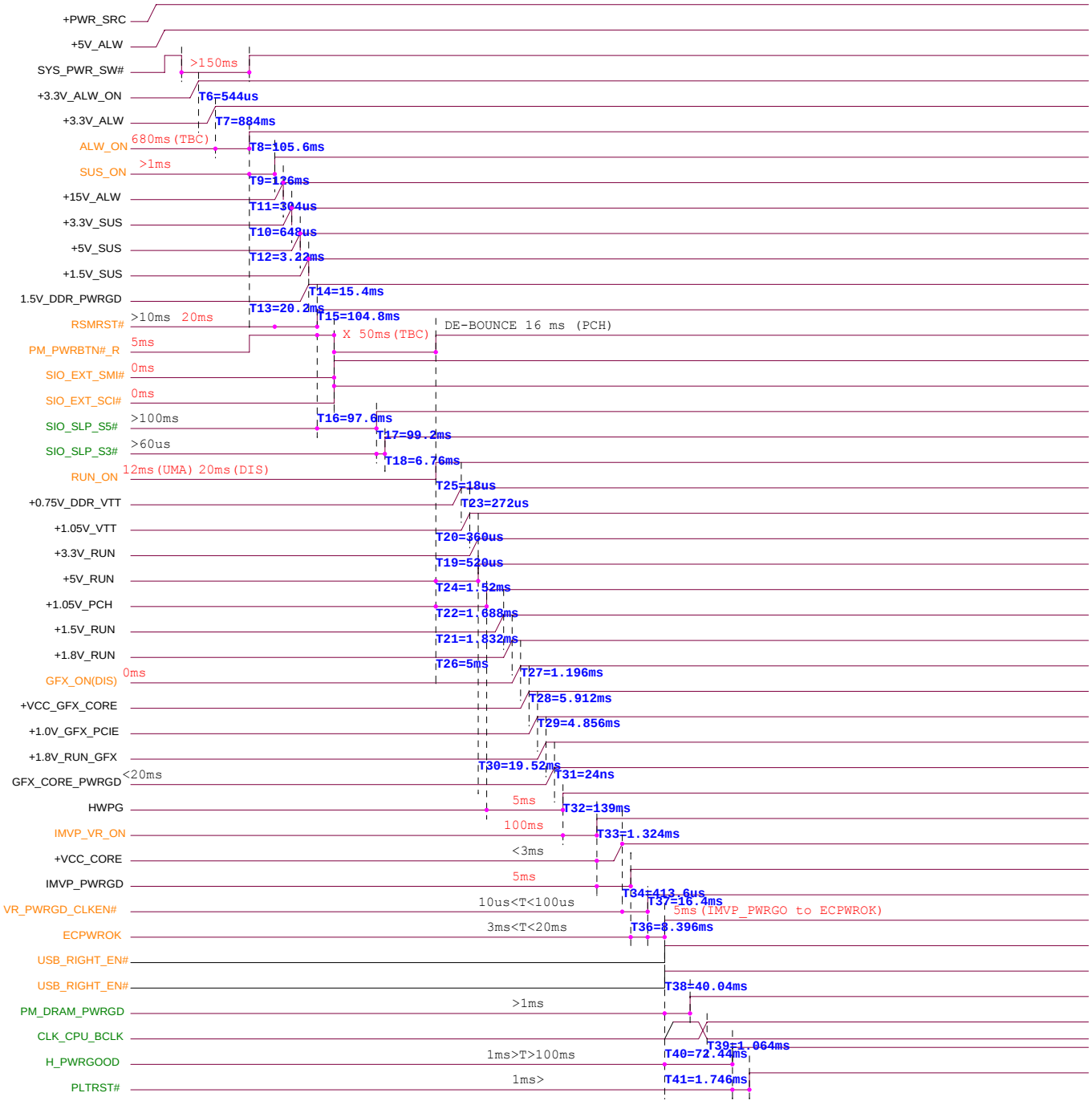
Size	Document Number	Rev
	Schematic Block Diagram1	1A

Date: Wednesday, February 10, 2010 Sheet 42 of 46



Quanta Computer Inc.
PROJECT : UM8B DIS
Size | Document Number: SMBUS BLOCK | Rev 1A
Date: Wednesday, February 10, 2010 | Sheet 43 of 46

UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



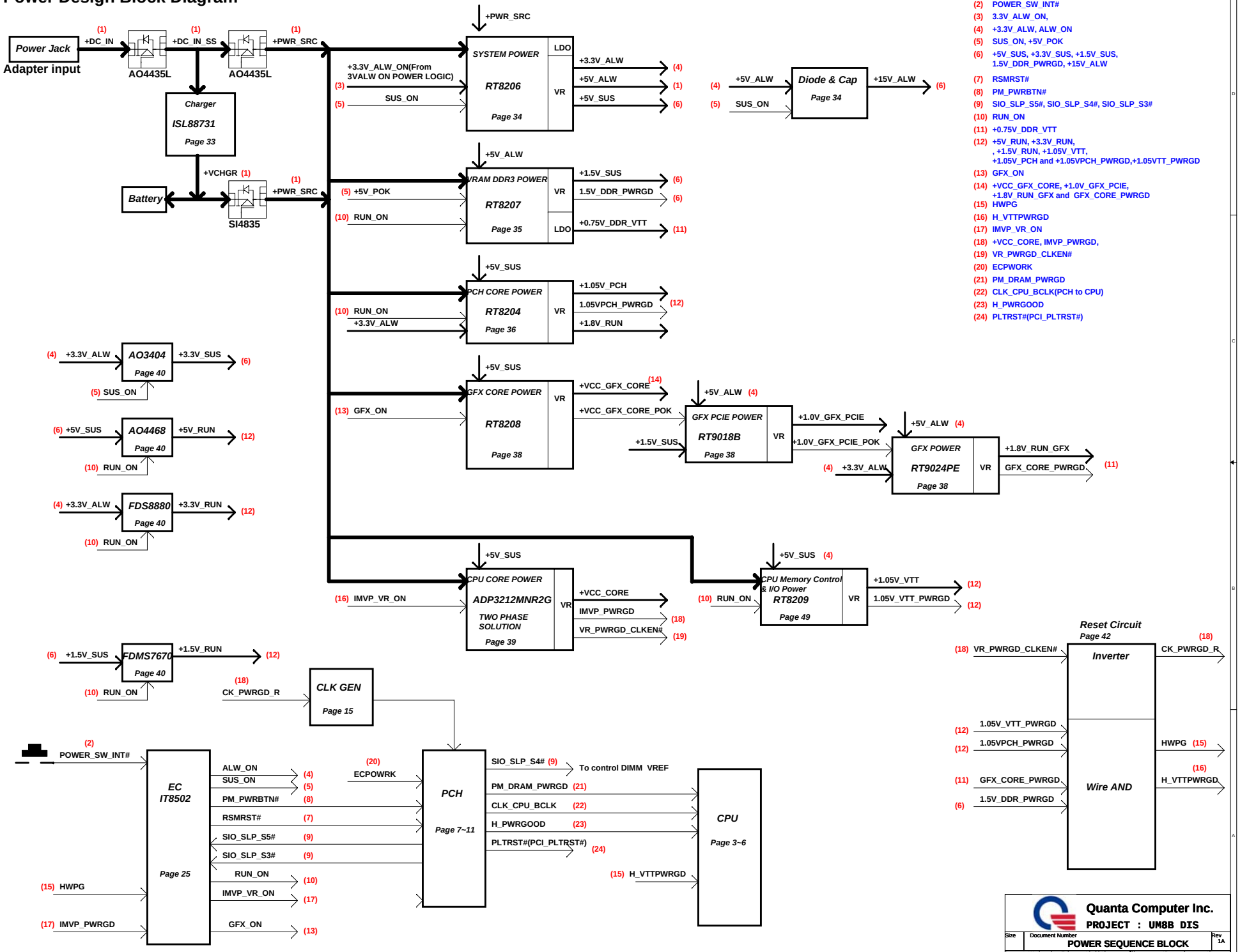
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	POWER SEQUENCE	1A

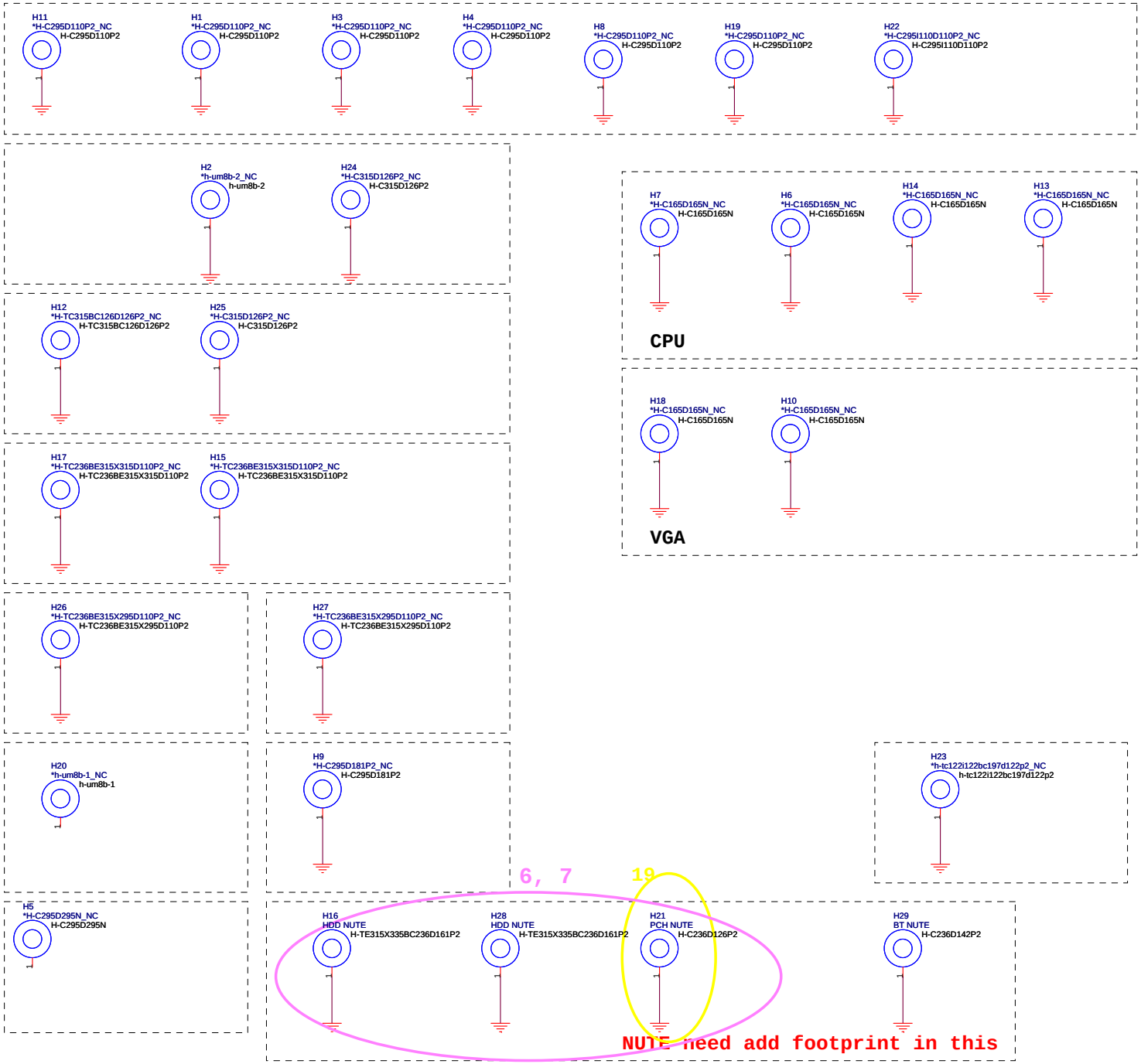
Date: Wednesday, February 10, 2010 Sheet 44 of 46

Power Design Block Diagram



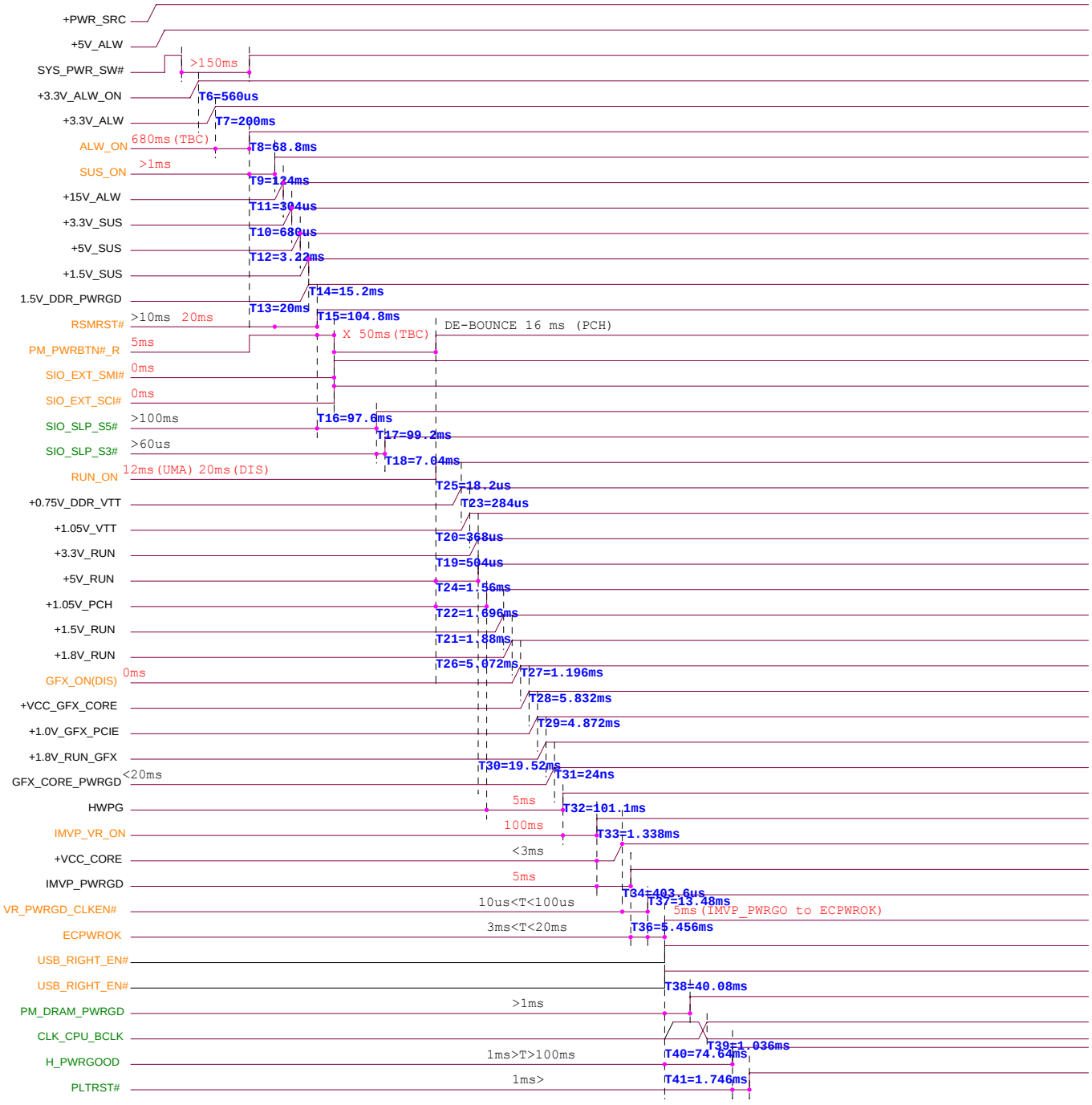
(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON, +5V_POK
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) RUN_ON
(11) +0.75V_DDR_VTT
(12) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(13) GFX_ON
(14) +VCC_GFX_CORE, +1.0V_GFX_PCIE, +1.8V_RUN_GFX and GFX_CORE_PWRGD
(15) HWPG
(16) H_VTTPWRGD
(17) IMVP_VR_ON
(18) +VCC_CORE, IMVP_PWRGD,
(19) VR_PWRGD_CLKEN#
(20) ECPOWRK
(21) PM_DRAM_PWRGD
(22) CLK_CPU_BCLK(PCH to CPU)
(23) H_PWRGOOD
(24) PLTRST#(PCI_PLTRST#)

Quanta Computer Inc.			
PROJECT : UM8B DIS			
Size	Document Number		Rev
	POWER SEQUENCE BLOCK		1A
Date: Wednesday, February 10, 2010	Sheet 45 of 46		



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: PAD&SCREW	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 46 of 46	

UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	POWER SEQUENCE	1A

Date: Wednesday, February 10, 2010 Sheet 47 of 46