

# Compal Confidential

Model Name : ZIUS6/S7

File Name : LA-A321PR01

BOM P/N:4319OP38L5x -- ZIUS7  
4319OP38L0x -- ZIUS6

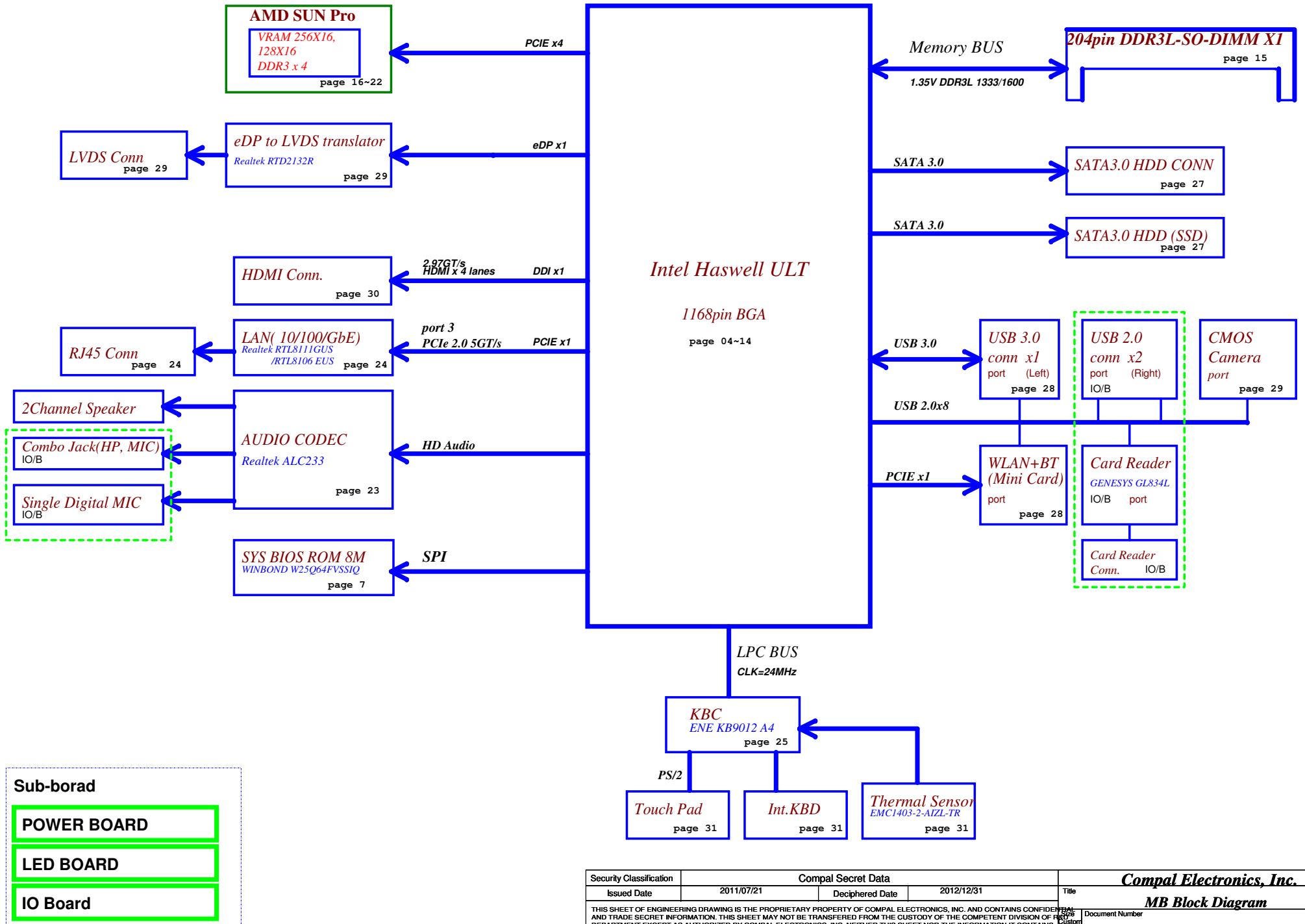
# Compal Confidential

## ZIUS6/S7 M/B Schematics Document

Intel SharyBay ULT Processor + AMD SUN Pro

2013-03-14  
[www.rosefix.com](http://www.rosefix.com)  
REV: 0.2

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### Voltage Rails

power plane	State	B+	+5VALW	+3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS  +VGA_CORE (PX) +0.95VS_VGA (PX) +3.3VS_VGA (PX) +1.8VS_VGA (PX) +1.5VS_VGA (PX)
S0		○	○	○	○	○
S3		○	○	○	○	✗
S5 S4/AC		○	○	✗	✗	✗
S5 S4/ Battery only		✗	✗	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	✗

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
CPU OPTION	CPU1@
INTEL UMA	UMA@
AMD SUN Pro	PX@
VRAM Option	S1G@ M1G@ H1G@ S2G@ M2G@
LAN RTL8111GUS	8111@ SWR@
LAN RTL8106EUS	8106@ SWR@
USB3.0	USB3@
EMI PART	EMI@
ESD PART	ESD@

### BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.2
3	0.1
4	
5	
6	
7	

### EC SM Bus1 address

Device	Address
Smart Battery Charger	

### EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2-AIZL-TR	1001_101xb
Panel - eDP to LVDS translator	
SharkBay ULT	
AMD SUN Pro	

### CPU SM Bus address

Device	Address
DDR DIMM0	0XA0
WALN	
Touch Pad	

### CPU SML0 Bus address

Device	Address

### USB 2.0 Port Table

Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	USB 2.0 Port (I/O Board)
3	Card Reader
4	Touch Screen (reserve)
5	Camera
6	Mini Card (WLAN/BT)
7	

### USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

### PCIe Port Table

Port	Lane	
1		
2		LAN
3		WLAN
4		
5	0	GPU
	1	
	2	
6	0	
	1	
	2	
	3	

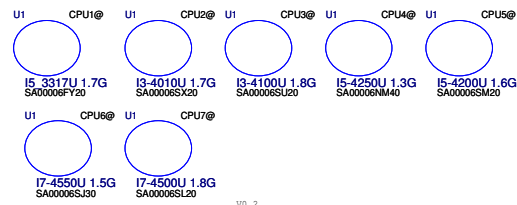
### SATA Port Table

Port	
3	
2	
1	mSATA SSD
0	HDD

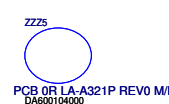
### SMBUS Control Table

	HOST	VGA	BATT	KB9012	SODIMM	WLAN	PANEL sensor ADM1032	Thermal sensor EMC1403	VGA sensor ADM1032	CPU Sensor	Touch Pad	Security ROM	NFC
EC_SMB_CK1	KB9012	X	V	X	X	X	X	X	X	X	X	X	X
EC_SMB_DA1	+3VLP		+3VLP										
EC_SMB_CK2	KB9012	V	X	X	X	X	V	V	V	V	X	X	X
EC_SMB_DA2	+3VS	+3VS					+3VS	+3VS	+3VS	+3VALW			
SMBCLK	CPU	X	X	X	X	X	X	X	X	X	+3VS	+3VS	+3VS
SMBDATA	+3VALW												
SML0CLK	CPU	X	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW												
SML1CLK	KB9012	X	X	V	X	X	X	X	X	V	X	X	X
SML1DATA	+3VS			+3VS						+3VALW			

### CPU part



### PCB part



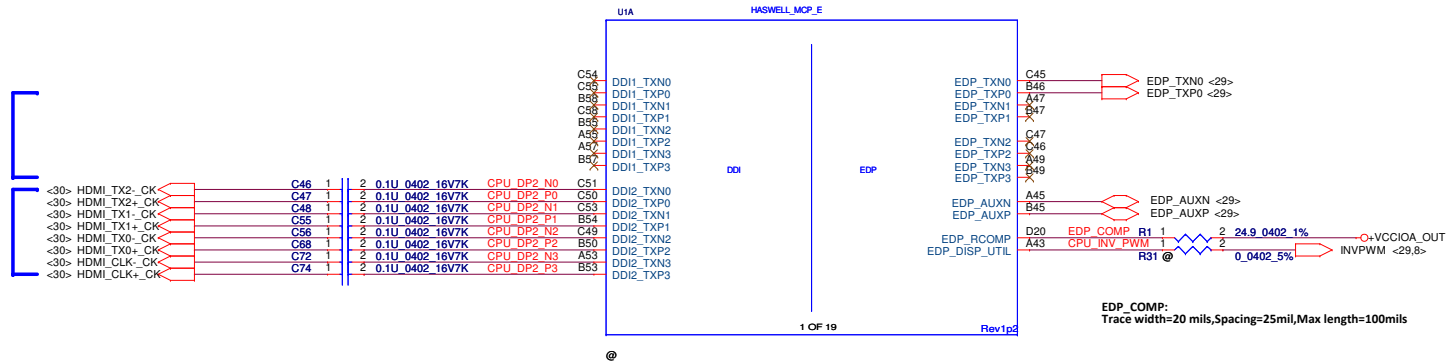
### VRAM



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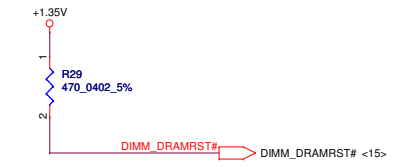
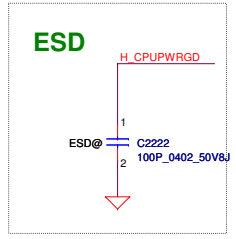
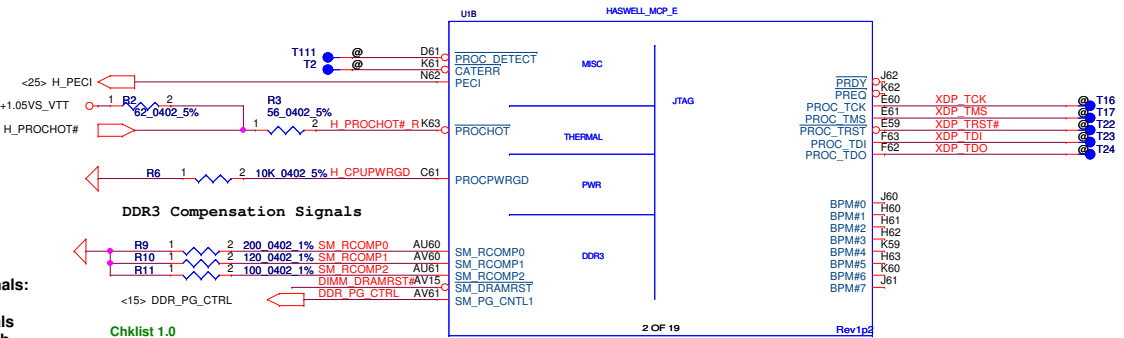
CRT

HDMI

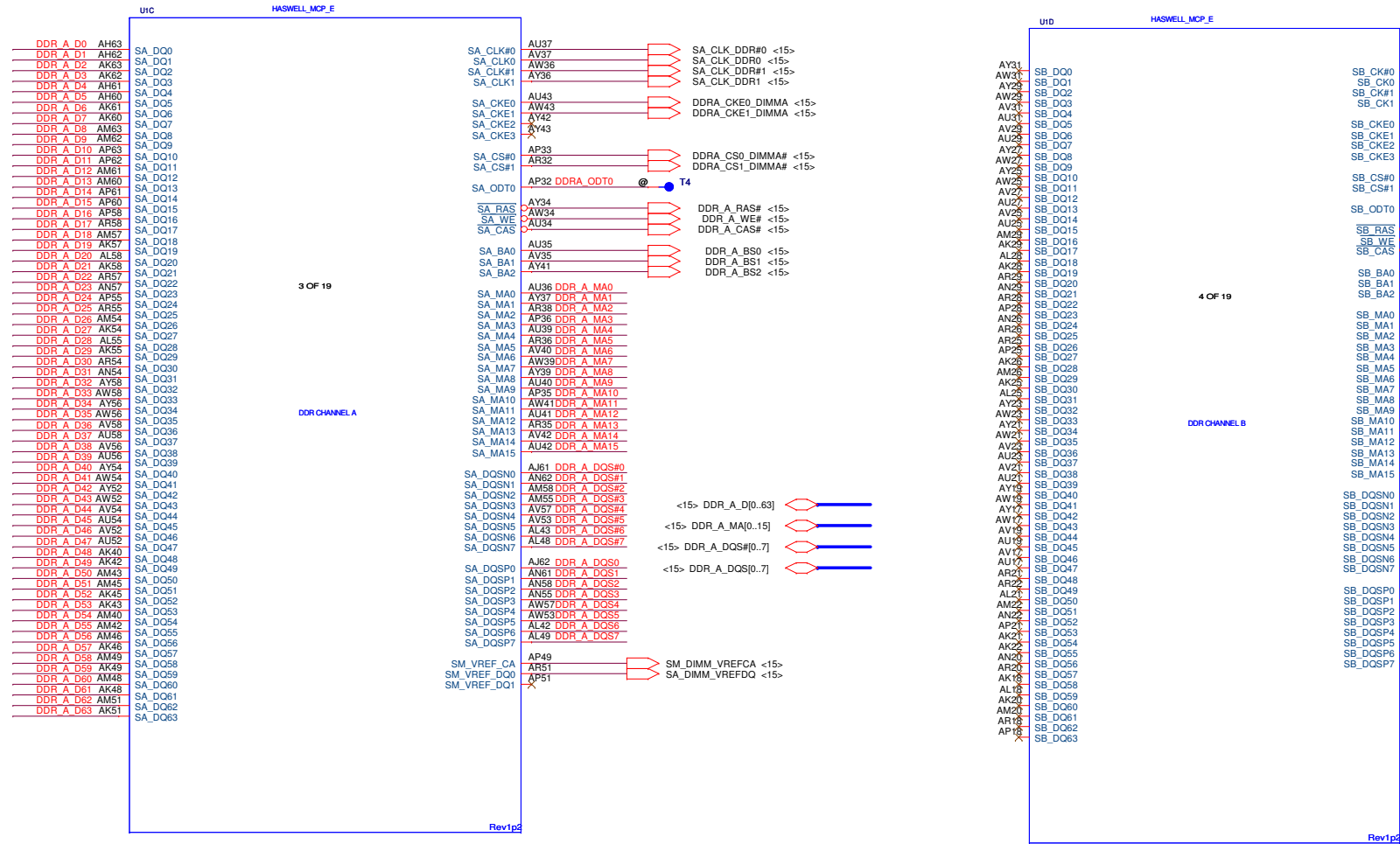


**DDR3 Compensation Signals:**  
20mils to comp signals  
25mils to non-comp signals  
500mil for Max trace length

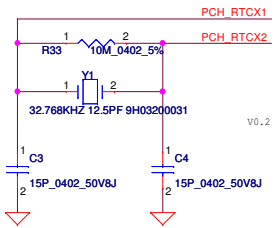
Chklist 1.0  
SM\_RCAMP1 -->120 ohm 1%



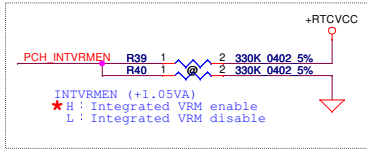
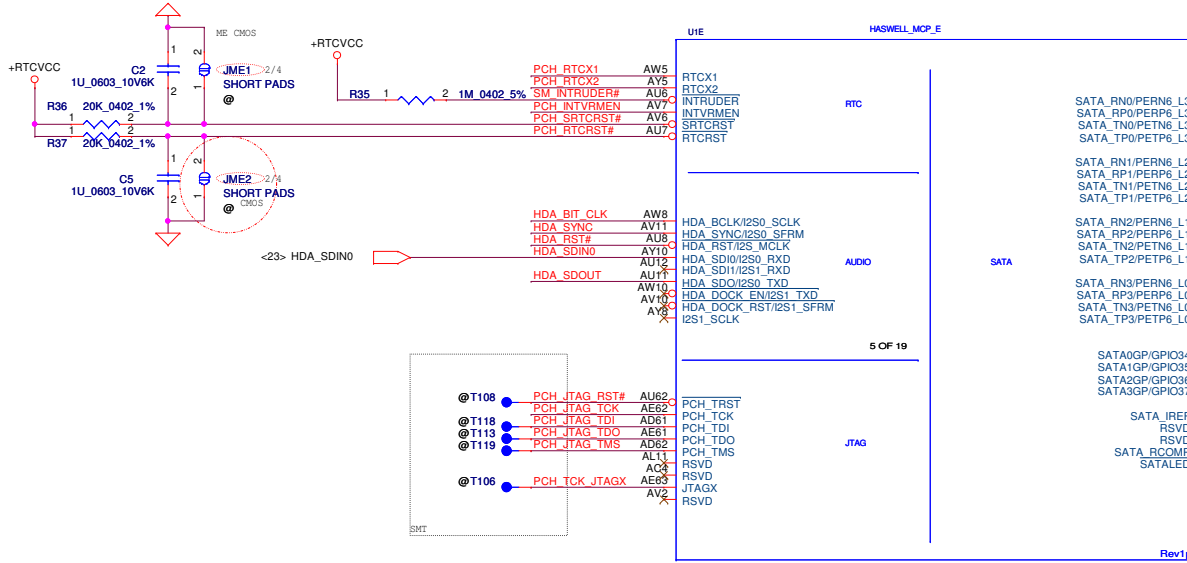
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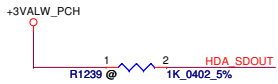
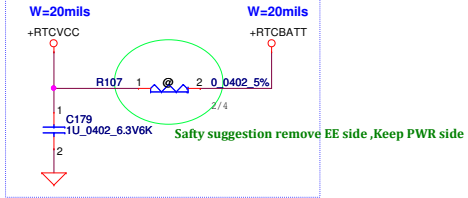
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JME2 Short PAD placement to Bottom side.

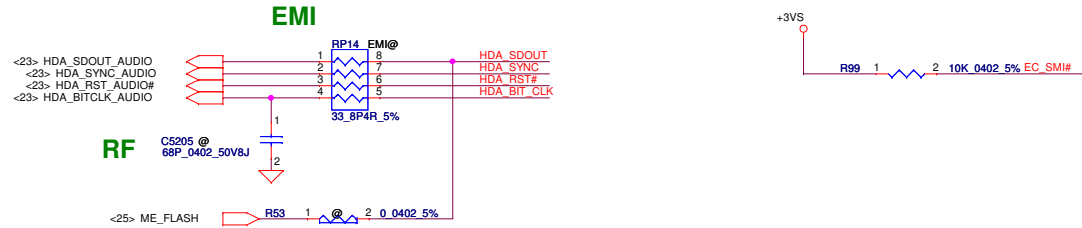
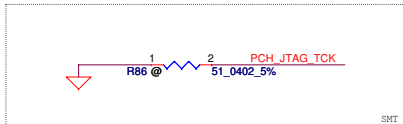


### RTC Battery



HDA\_SDOUT  
ME debug mode, this signal has a weak internal PD  
\* Low = Disabled (Default)  
High = Enabled [Flash Descriptor Security Override]

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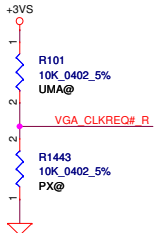
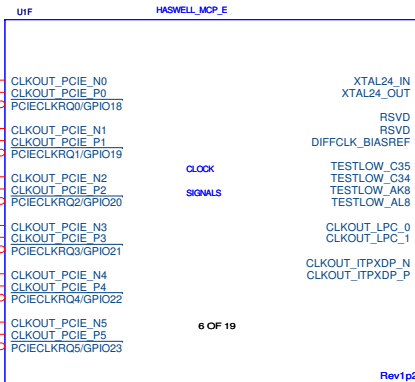


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GLAN

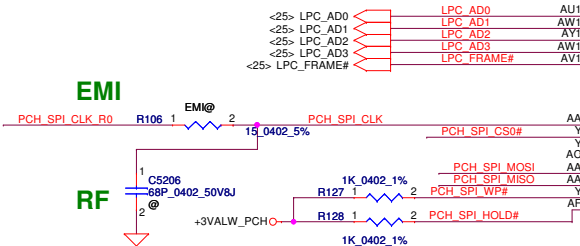
WLAN

dGPU

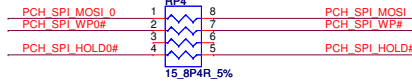


EMI

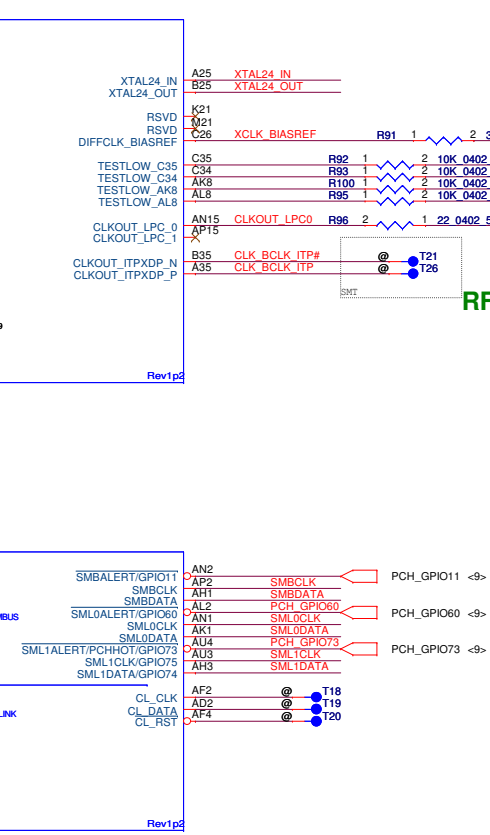
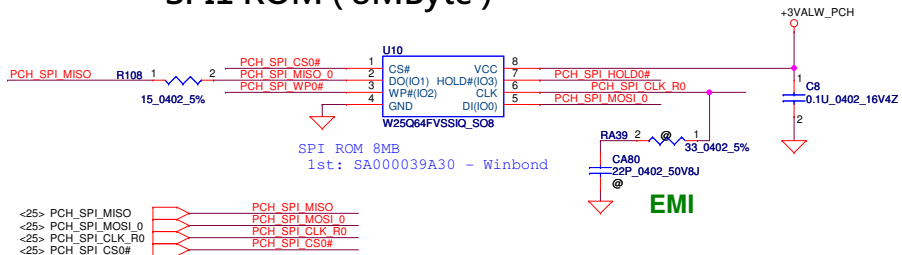
RF



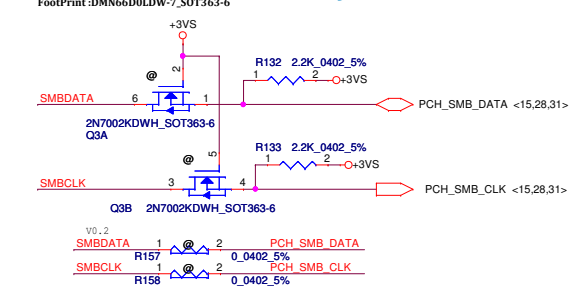
**CHKLIST1.0**  
 2 SPI Device = 33 ohm  
 1 SPI Device = 15 ohm



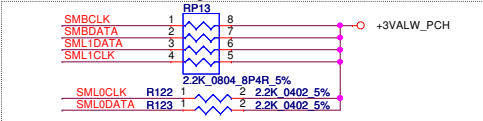
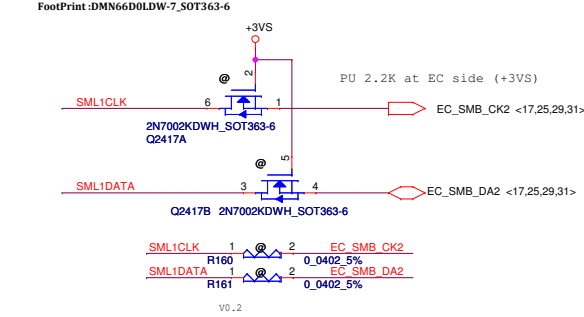
SPI1 ROM ( 8MByte )



SMBus :SPD/PCIe/Security/TP



SML1 Bus :EC/Sensors



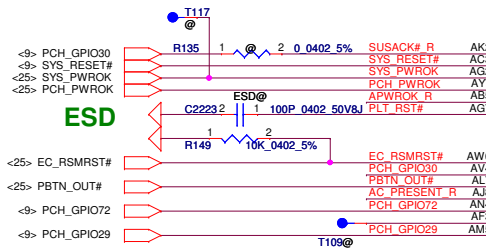
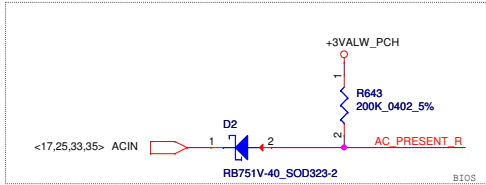
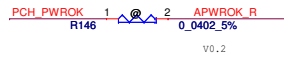
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Note: SUSACK# and SUSWRN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit

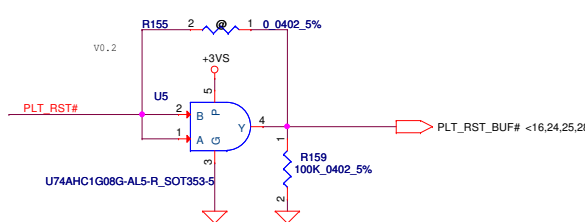
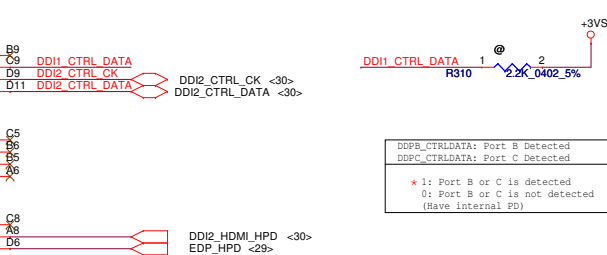
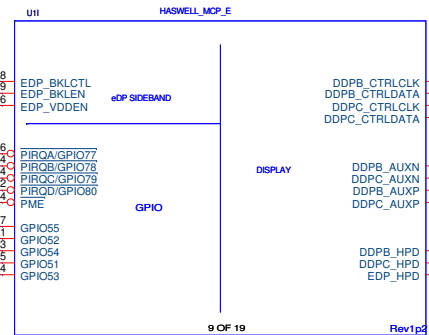
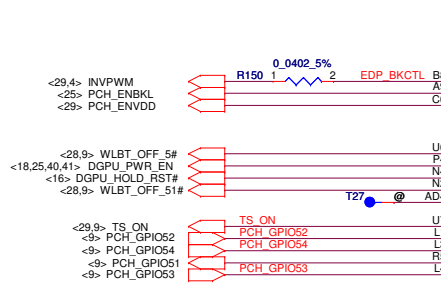
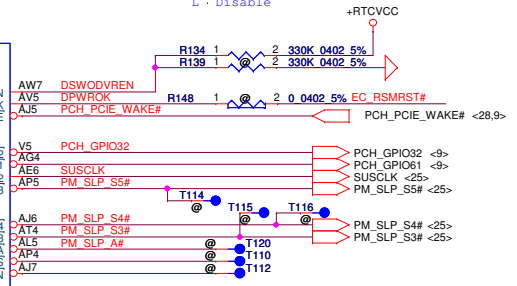
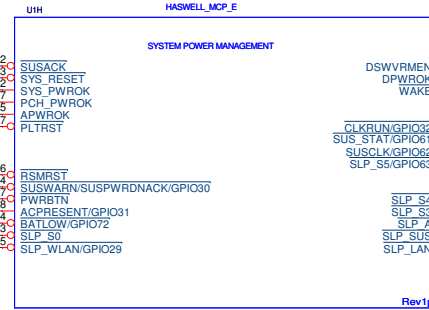
CAN be NC ,if not support Deep Sx

DPWROK: Tired togher with RSMRST# that do not support Deep Sx

DSWODVREN - On Die DSW VR Enable  
 \* H : Enable (DEFAULT)  
 L : Disable

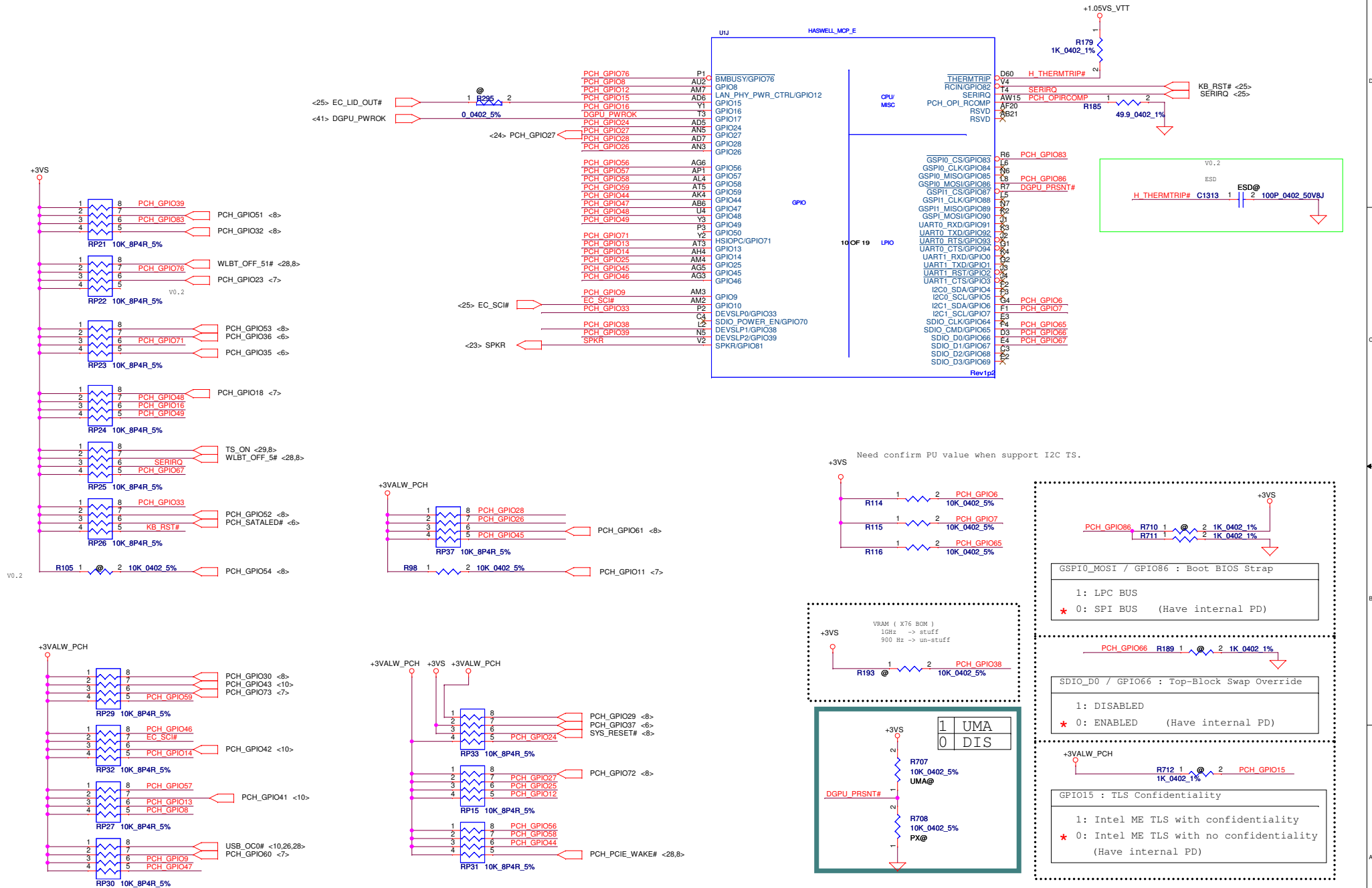


PCH\_BATLOW# Need pull high to VCCDSW3\_3 (If no deep Sx , connect to VCCSUS3\_3)



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D

C

B

A

D

C

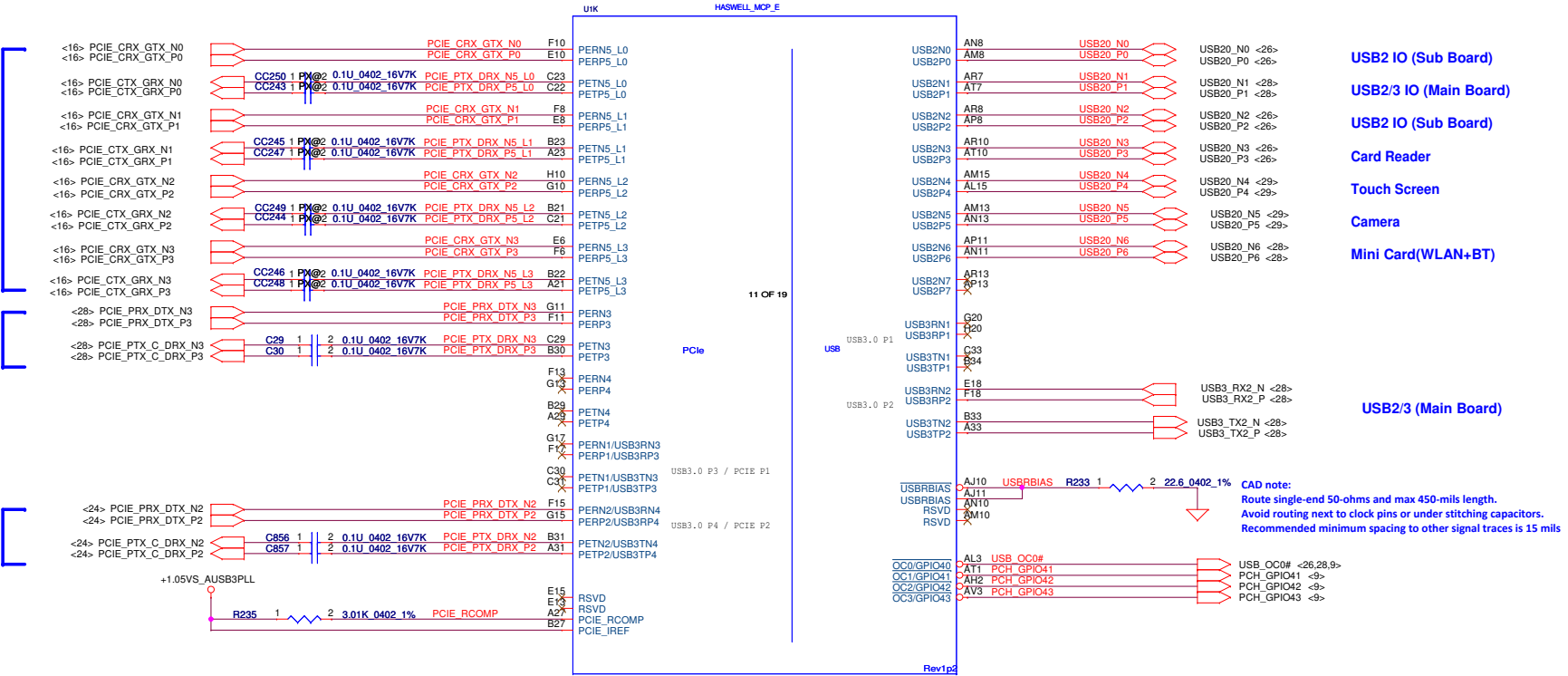
B

A

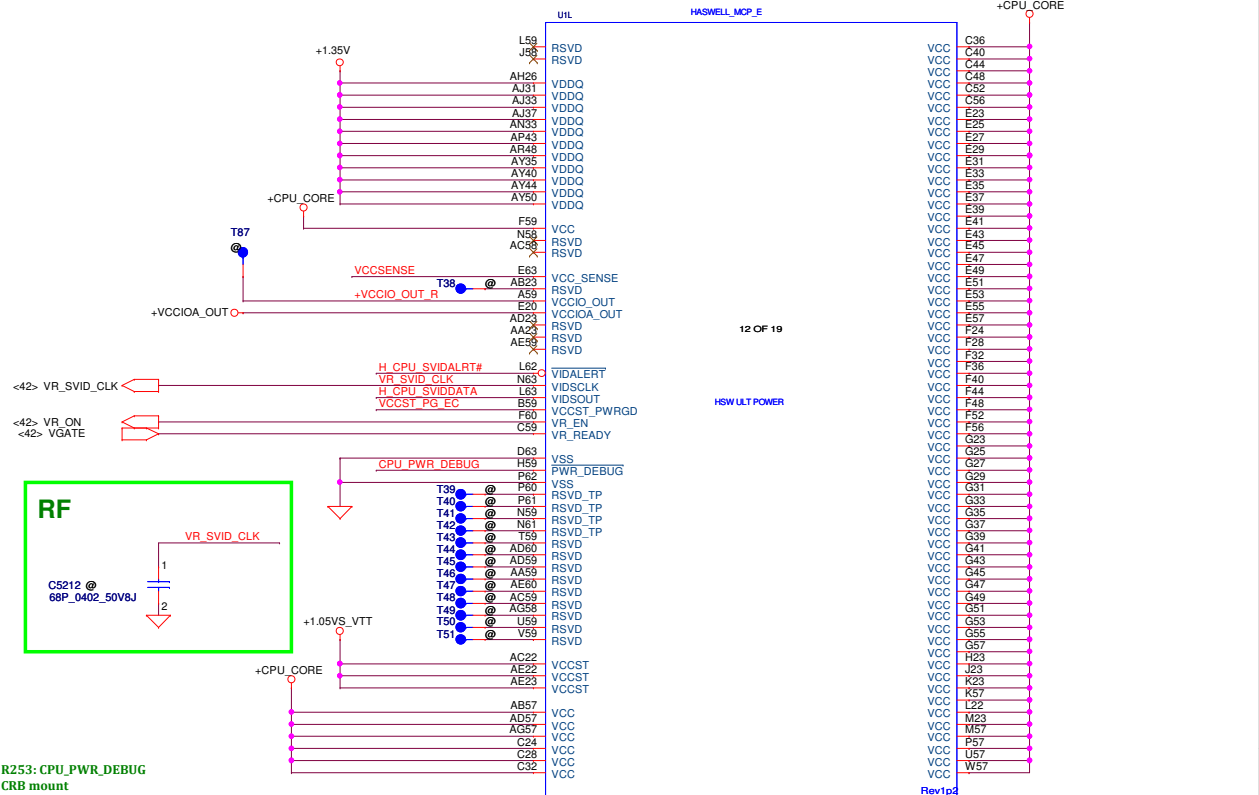
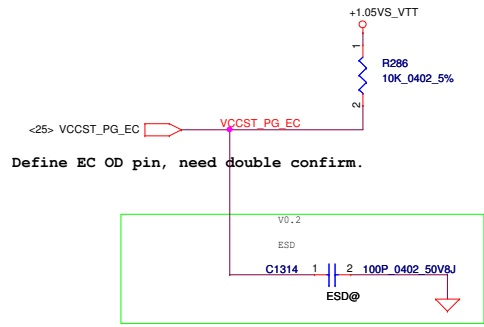
dGPU

WLAN

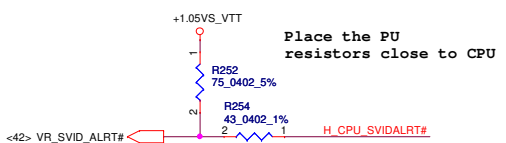
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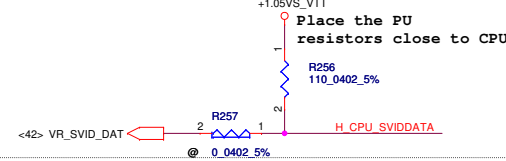
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**SVID ALERT**

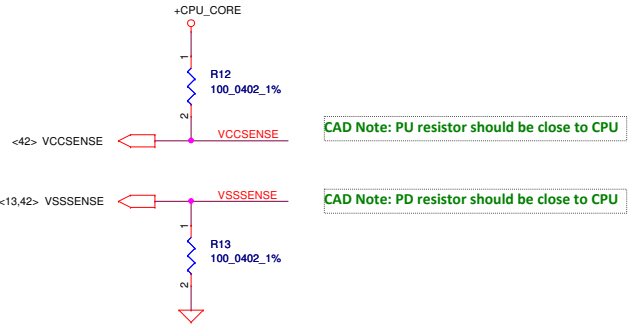
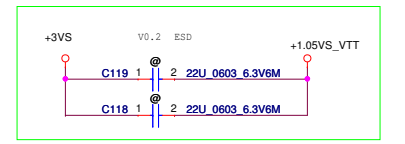
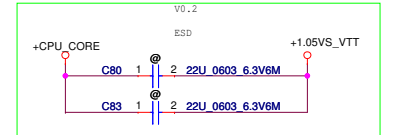
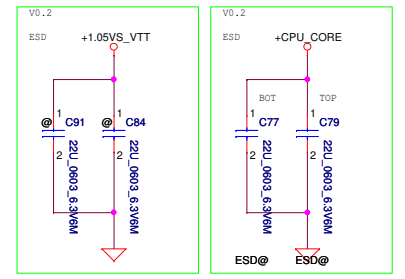
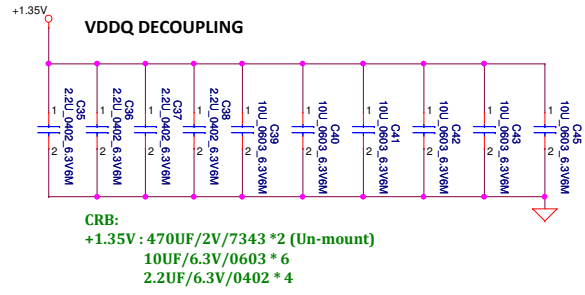


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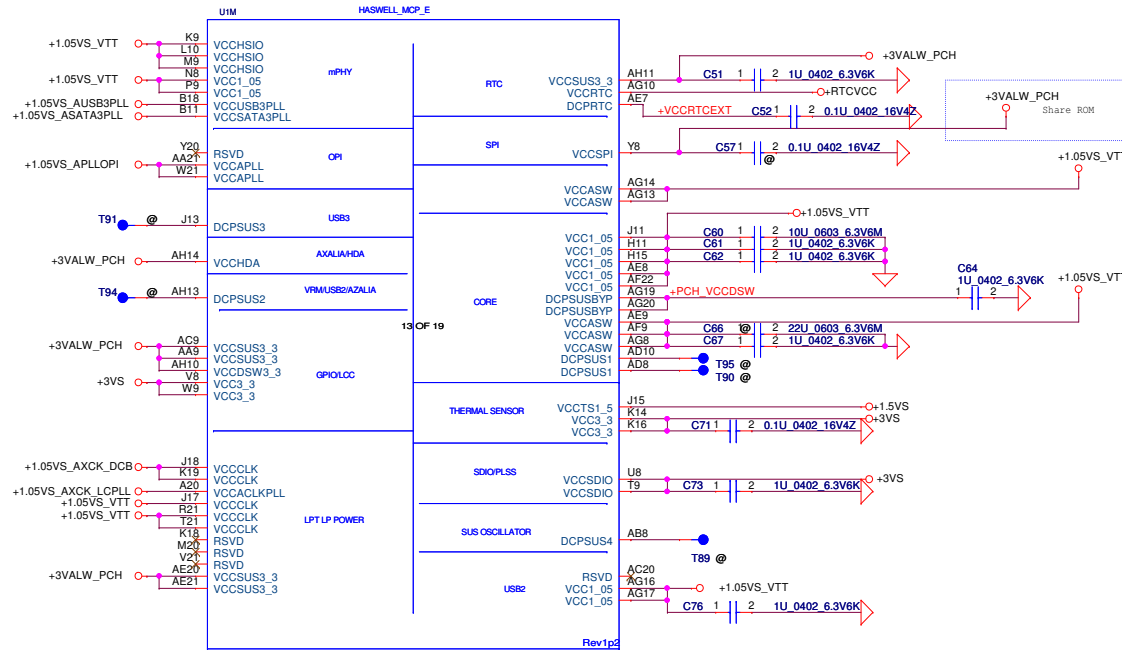
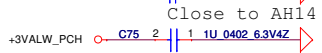
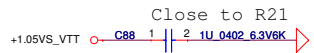
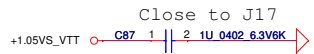
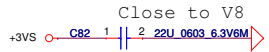
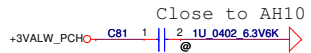
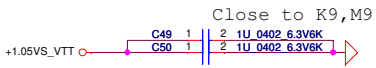
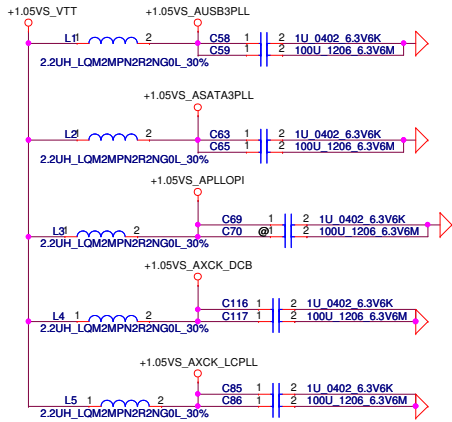
R256:  
CRB r0.7 changed from 130 Ohms to 110 Ohms

R253: CPU\_PWR\_DEBUG  
CRB mount  
Check list, XDP use only



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Check Power Source Close to N8  
 +1.05VS\_VTT C53 @ 2 1U 0402 6.3V6K

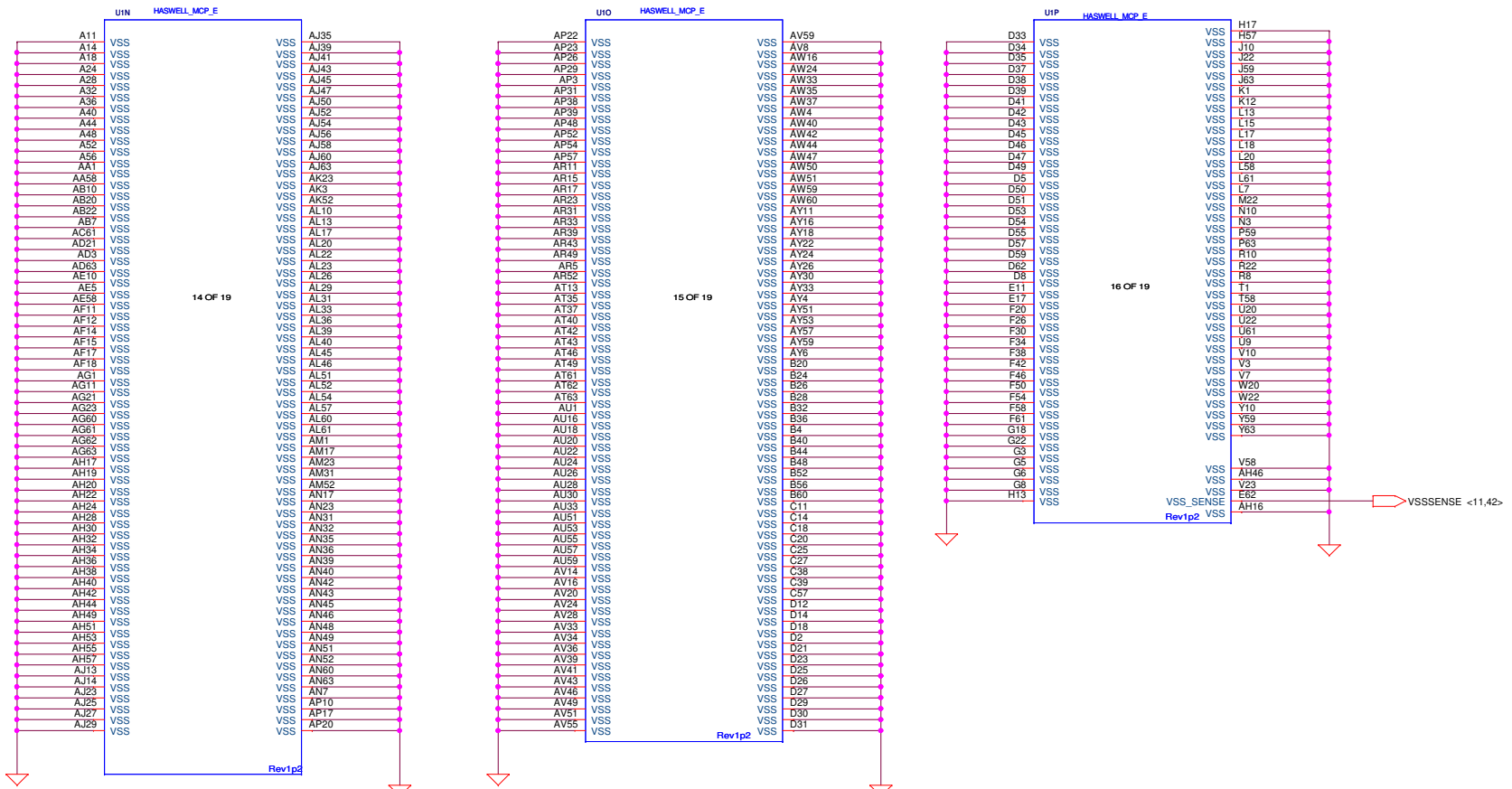


18mA

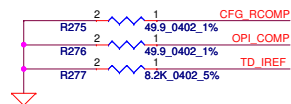
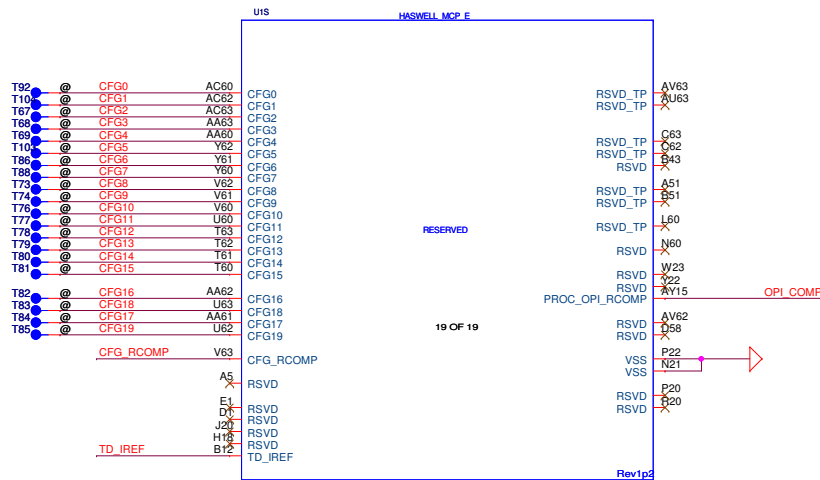
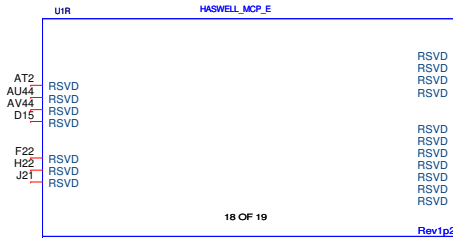
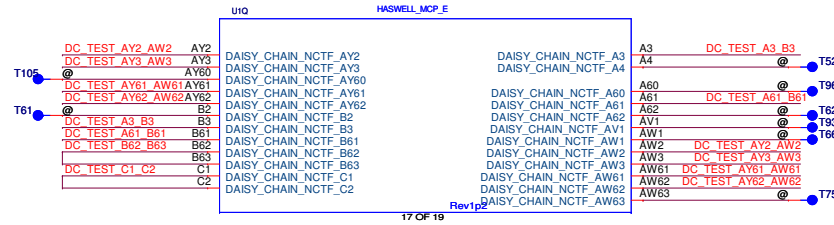
658mA

+RTCVCC  
 1U\_0402\_6.3V6K  
 C54

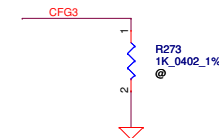
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/12/13	Deciphered Date	2012/12/13	Title <b>HSW MCP(9/11) Power</b>
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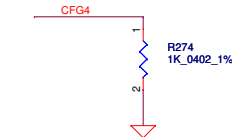
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Issued Date	2011/12/13	Deciphered Date	2012/12/13	Compal Electronics, Inc. <b>HSW MCP(10/11) GND</b>	
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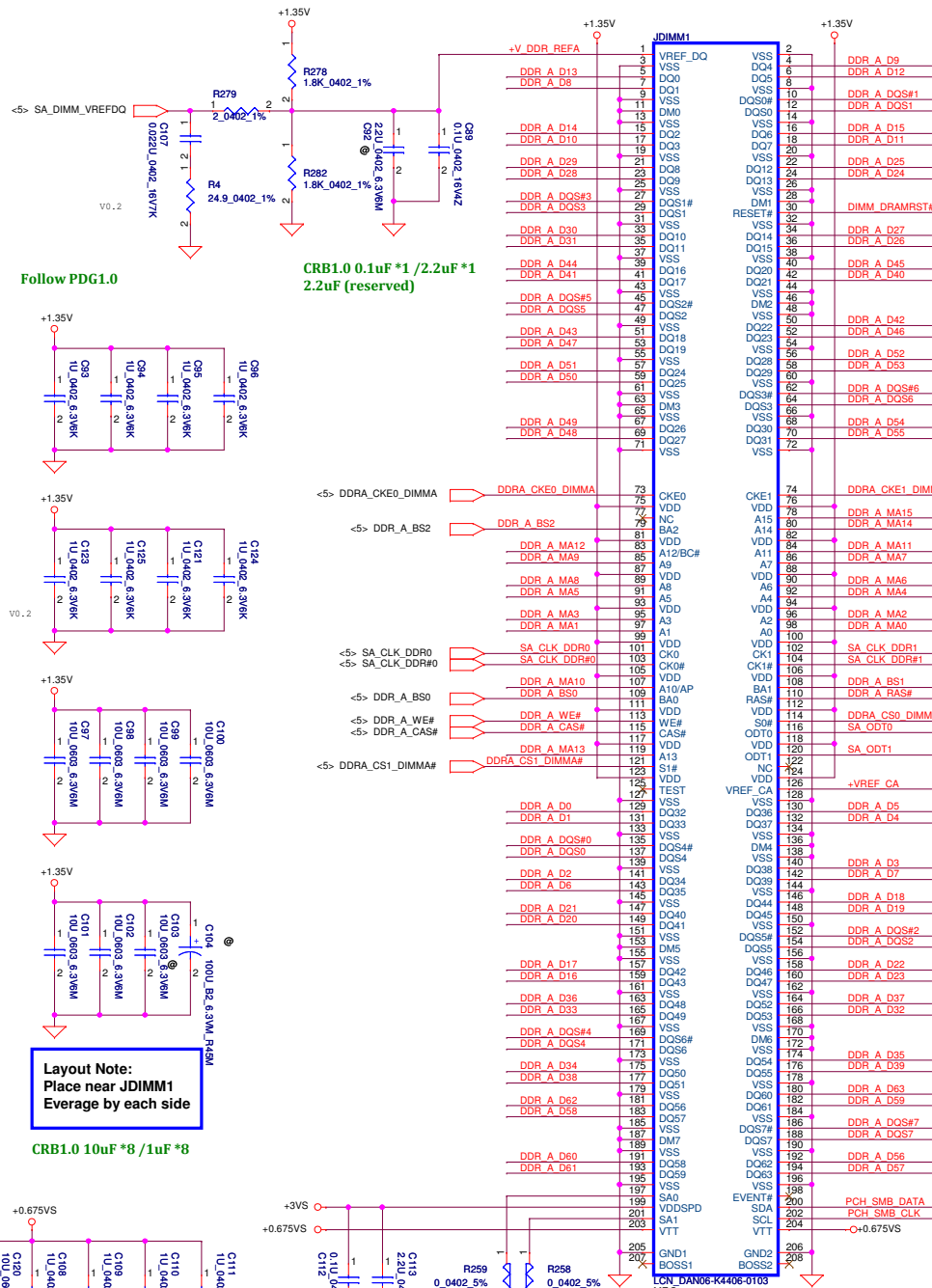
### CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



All VREF traces should have 10 mil trace width

Follow PDG1.0

CRB1.0 0.1uF \*1 / 2.2uF \*1  
2.2uF (reserved)

CRB1.0 0.1uF \*1 / 2.2uF \*1  
2.2uF (reserved)

Layout Note:  
Place near JDIMM1  
Everage by each side

CRB1.0 10uF \*8 / 1uF \*8

Layout Note:  
Place near JDIMM1.203,204

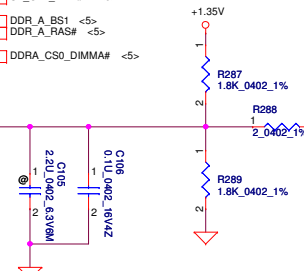
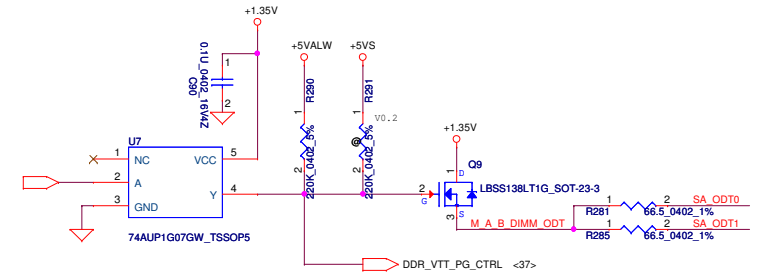
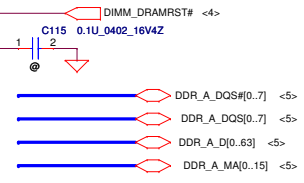
CRB1.0 10uF \*1 / 1uF \*4

CHANNEL A /TYPE :Reverse / H:4mm

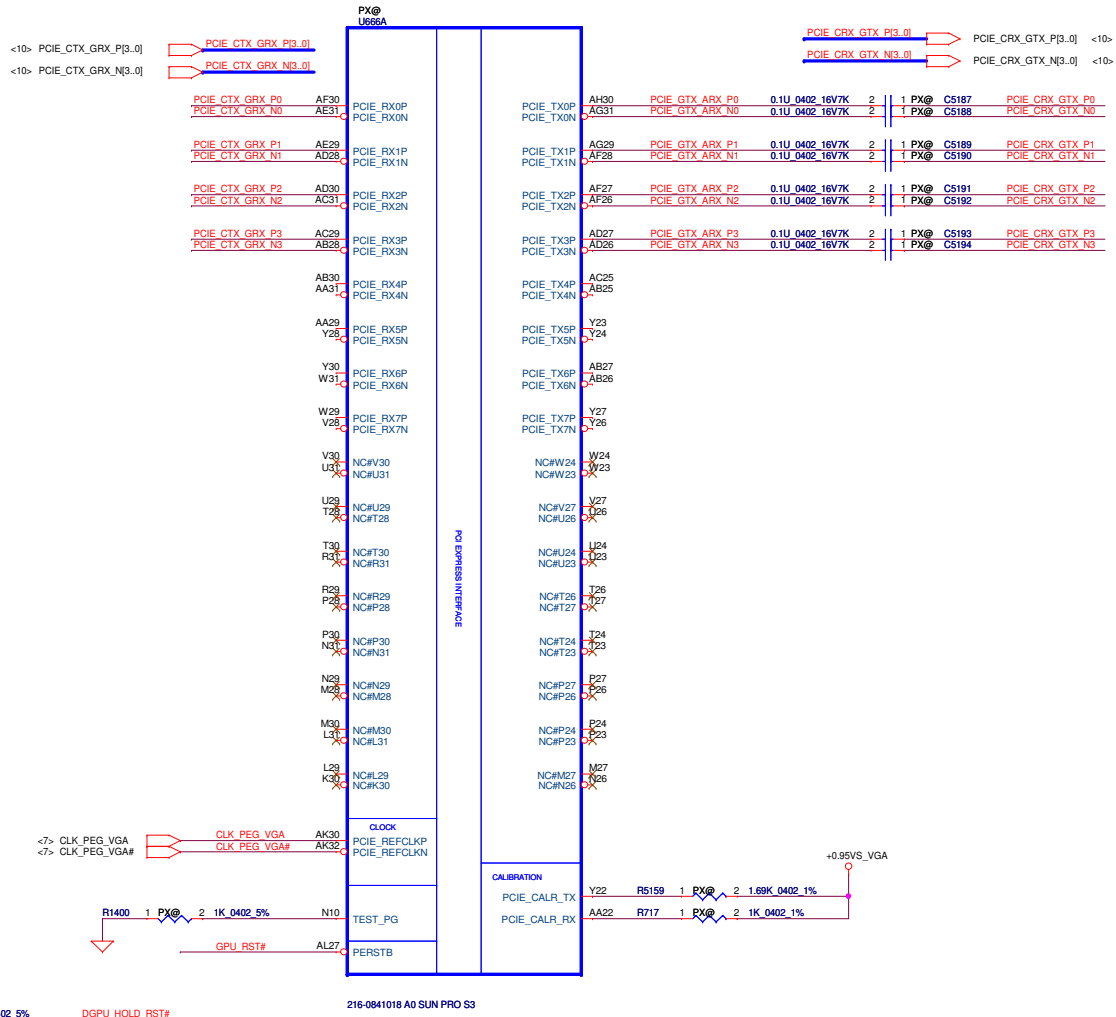
CHA SPD ADDRESS IS 0xA0

CHA TS ADDRESS IS 0x30

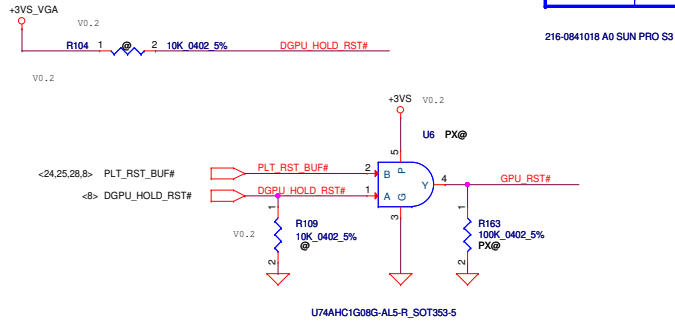
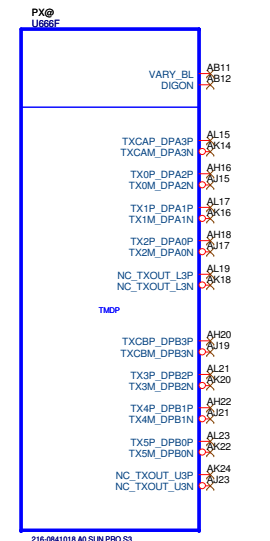
PN:SP0700LT00



Security Classification	Compal Secret Data		Title <b>DDRIII DIMMA</b>
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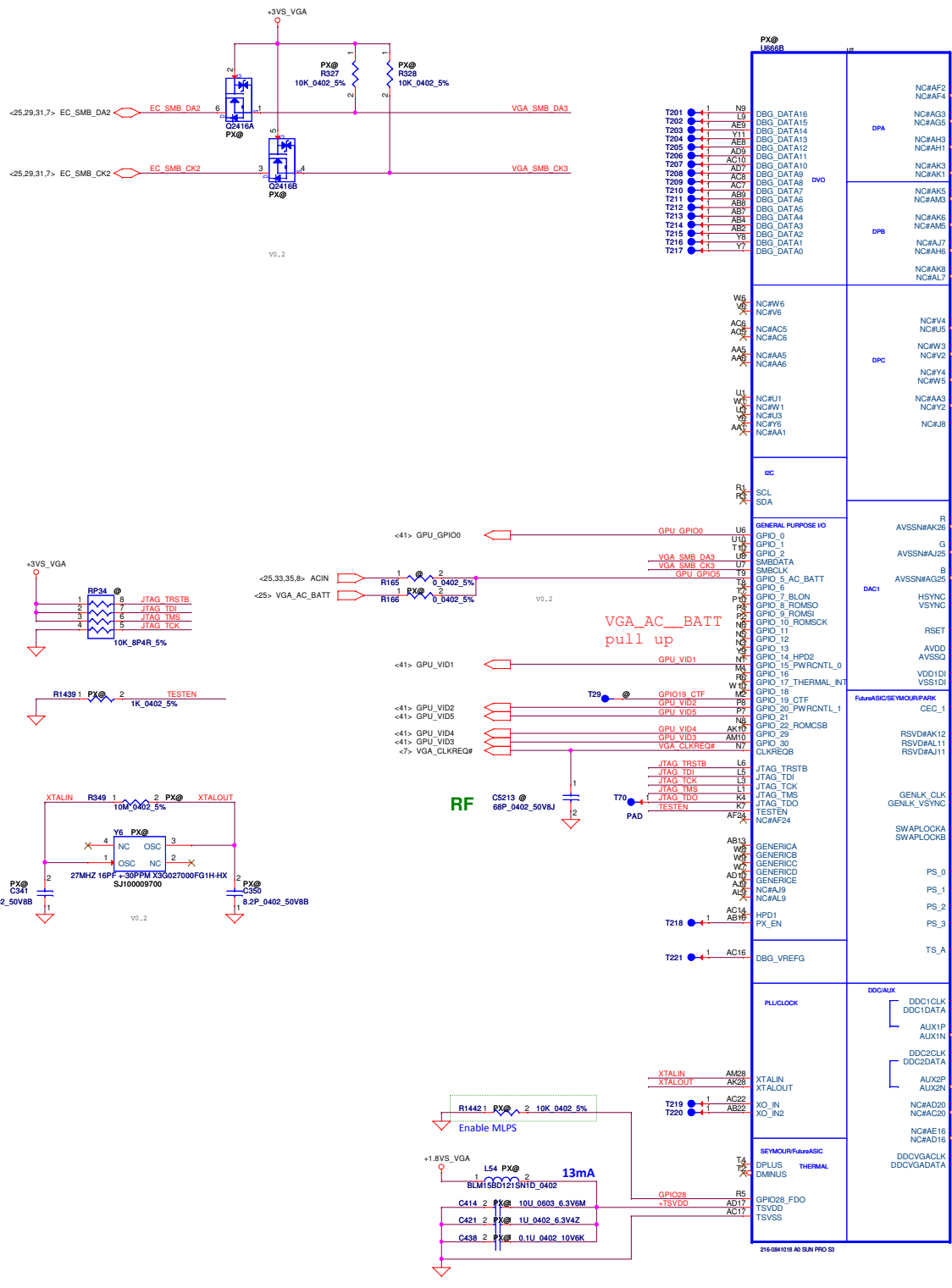


No Use GPU Display Port output



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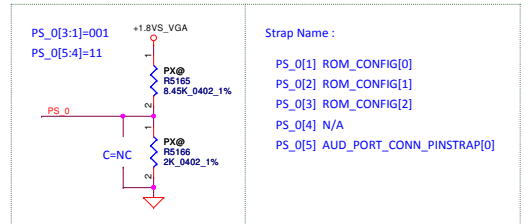


**Resistor Divider Lookup Table**

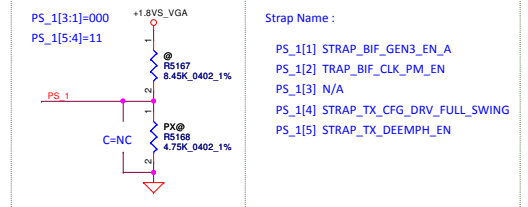
R_ru (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

**Capacitor Divider Lookup Table**

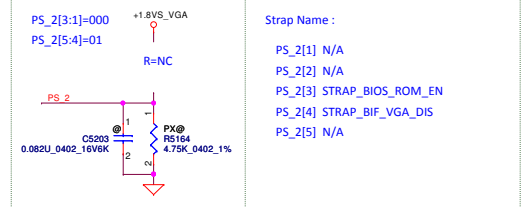
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



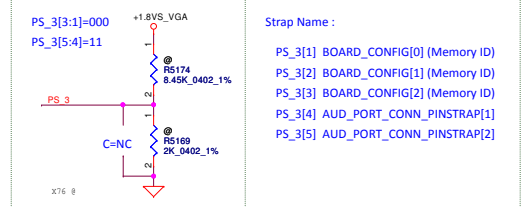
- Strap Name :
- PS\_0[1] ROM\_CONFIG[0]
  - PS\_0[2] ROM\_CONFIG[1]
  - PS\_0[3] ROM\_CONFIG[2]
  - PS\_0[4] N/A
  - PS\_0[5] AUD\_099K\_CONN\_PINSTRAP[0]



- Strap Name :
- PS\_1[1] STRAP\_BIF\_GEN3\_EN\_A
  - PS\_1[2] TRAP\_BIF\_CLK\_PM\_EN
  - PS\_1[3] N/A
  - PS\_1[4] STRAP\_TX\_CFG\_DRV\_FULL\_SWING
  - PS\_1[5] STRAP\_TX\_DEEMPH\_EN



- Strap Name :
- PS\_2[1] N/A
  - PS\_2[2] N/A
  - PS\_2[3] STRAP\_BIOS\_ROM\_EN
  - PS\_2[4] STRAP\_BIF\_VGA\_DIS
  - PS\_2[5] N/A

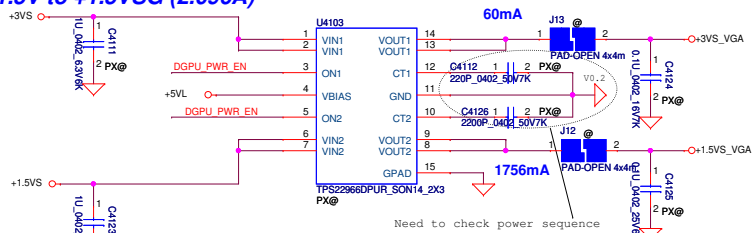


- Strap Name :
- PS\_3[1] BOARD\_CONFIG[0] (Memory ID)
  - PS\_3[2] BOARD\_CONFIG[1] (Memory ID)
  - PS\_3[3] BOARD\_CONFIG[2] (Memory ID)
  - PS\_3[4] AUD\_PORT\_CONN\_PINSTRAP[1]
  - PS\_3[5] AUD\_PORT\_CONN\_PINSTRAP[2]

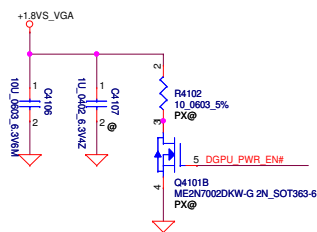
Memory ID	Memory Type	Configuration	Size
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB
011	SA000068R10	Samsung K4W4G1646B-HC11	2GB
100	SA000065D20	Micron MT41K256M16HA-107G:E	2GB

(default)

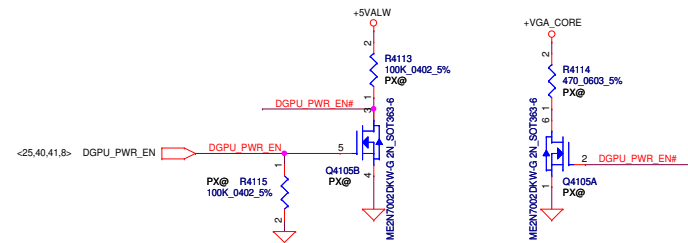
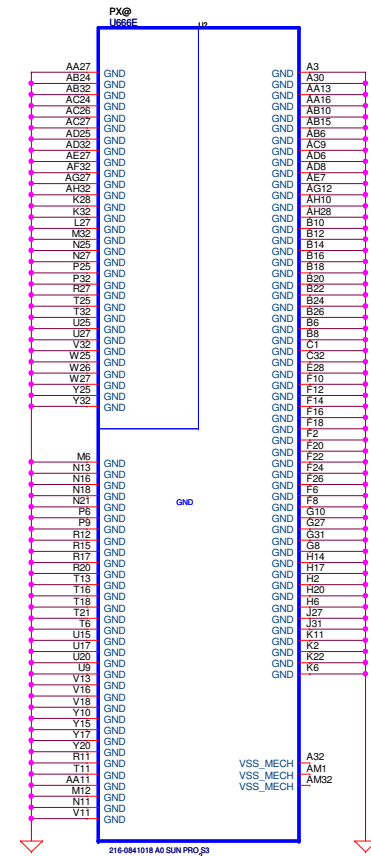
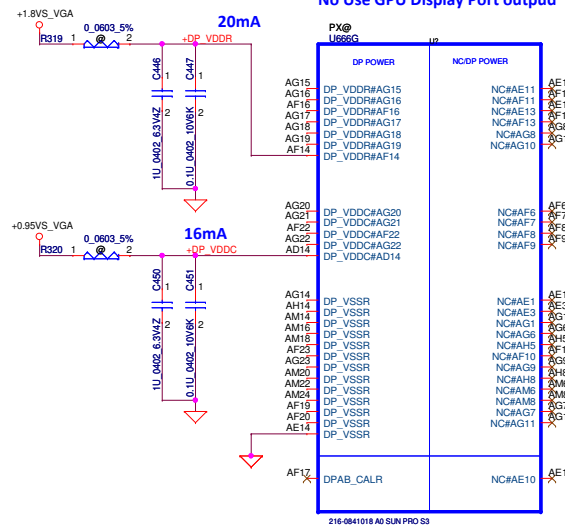
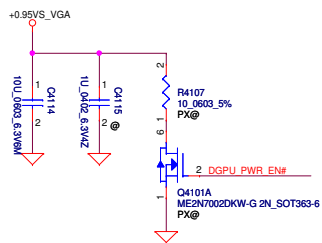
**+3VS to +3VSG (60mA)**  
**+1.5V to +1.5VSG (2.096A)**



**+1.8VALW to +1.8VSG (818mA)**



**+0.95VALW to +0.95VSG (4.016A)**



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<b>+VGA_CORE</b>	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

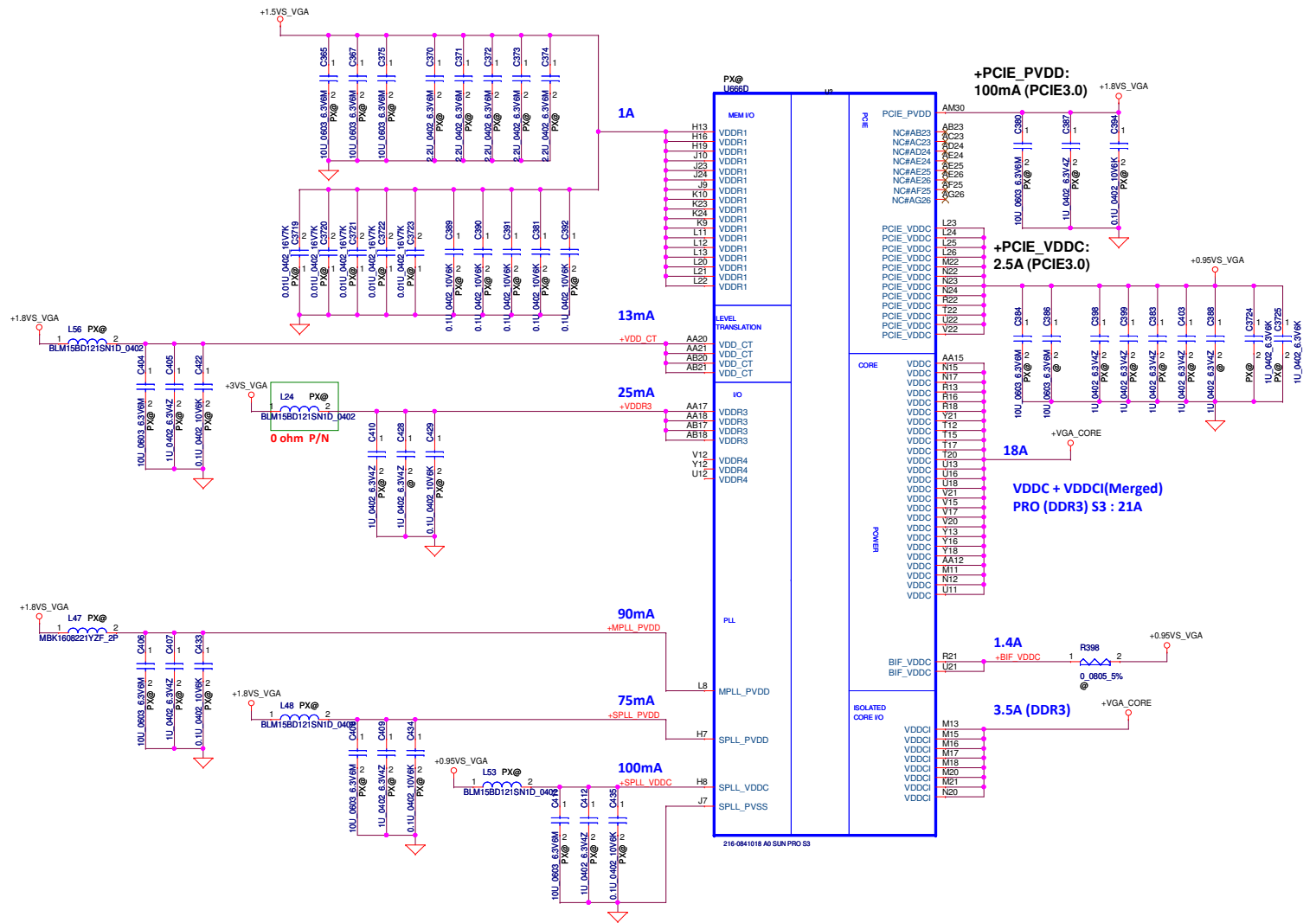
<b>+0.95VS_VGA</b>	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

<b>+1.5VS_VGA</b>	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

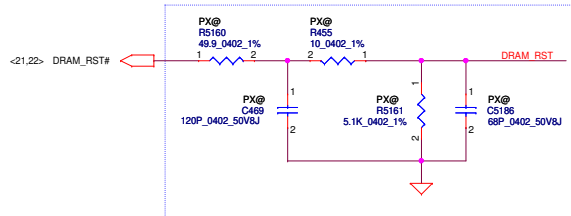
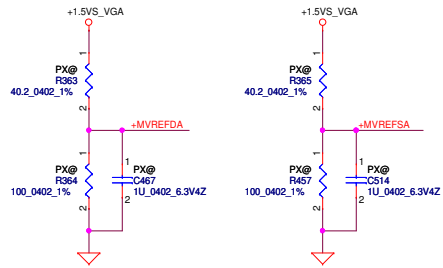
<b>+1.8VS_VGA</b>	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1

VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

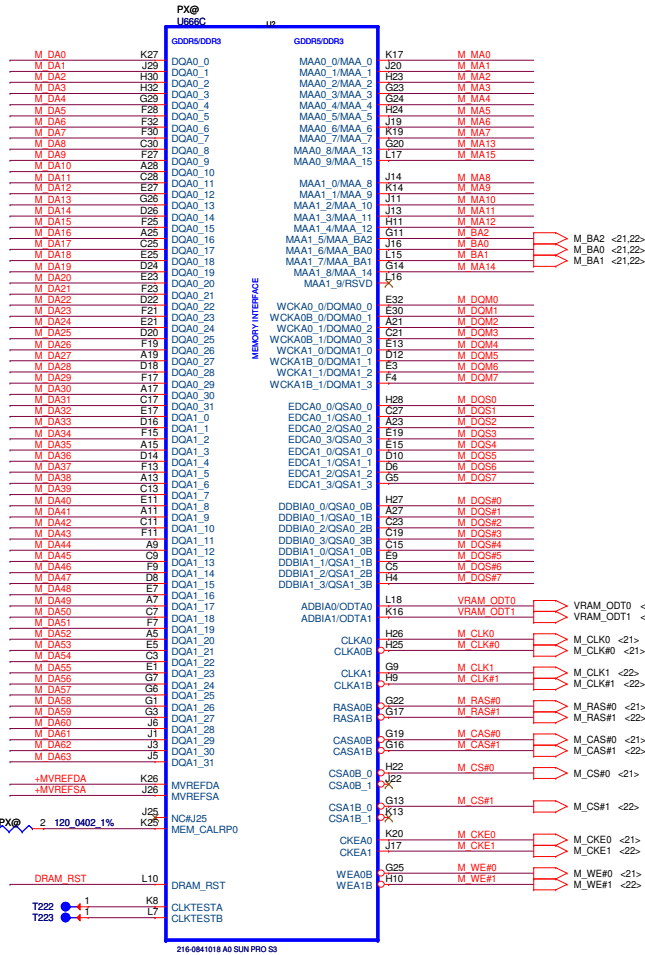
<b>+3VS_VGA</b>	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)



- <21,22> M\_DA[63..0] M\_DA[63..0]
- <21,22> M\_MA[15..0] M\_MA[15..0]
- <21,22> M\_DQM[7..0] M\_DQM[7..0]
- <21,22> M\_DQS[7..0] M\_DQS[7..0]
- <21,22> M\_DQS# [7..0] M\_DQS# [7..0]



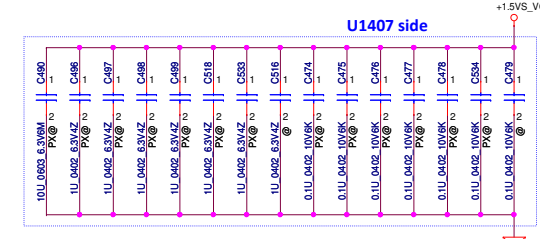
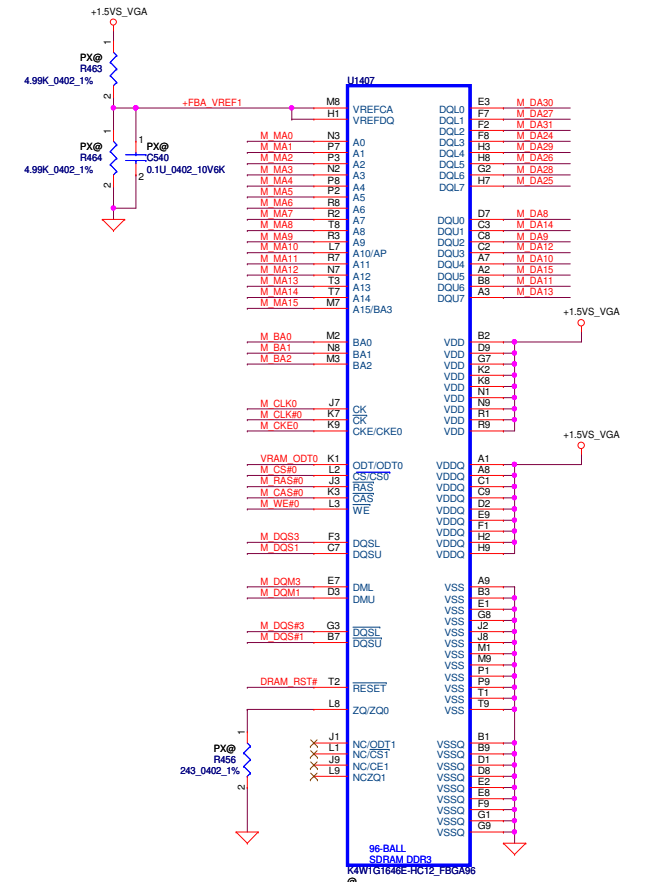
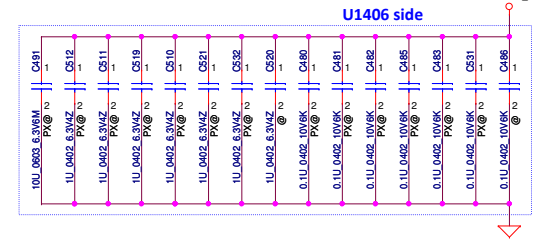
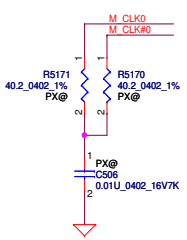
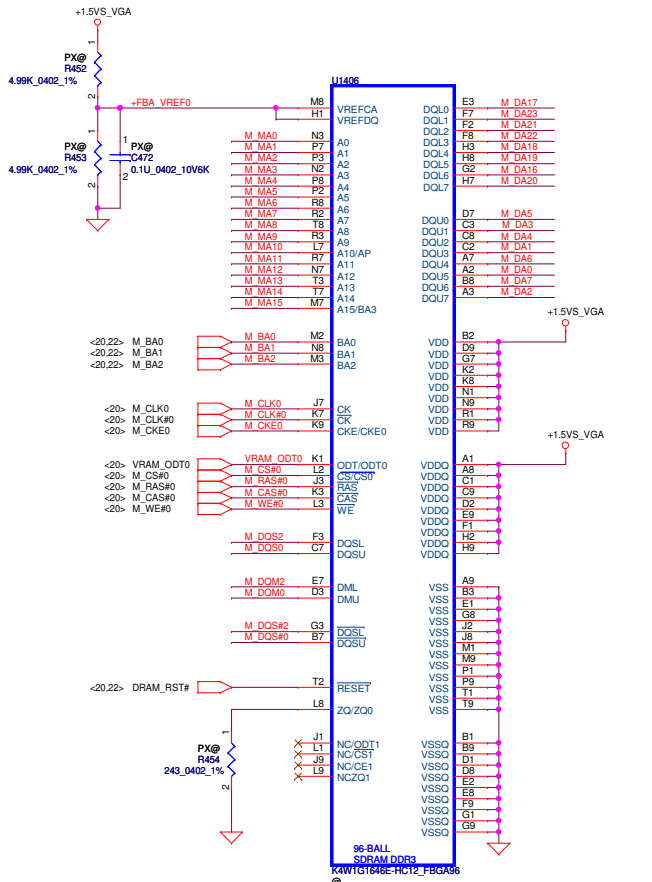
Place close to GPU (within 25mm)  
and place component close to each other



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# Memory Partition A - Lower 32 bits

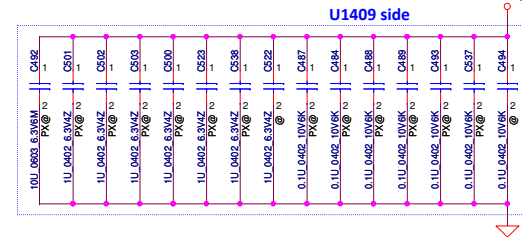
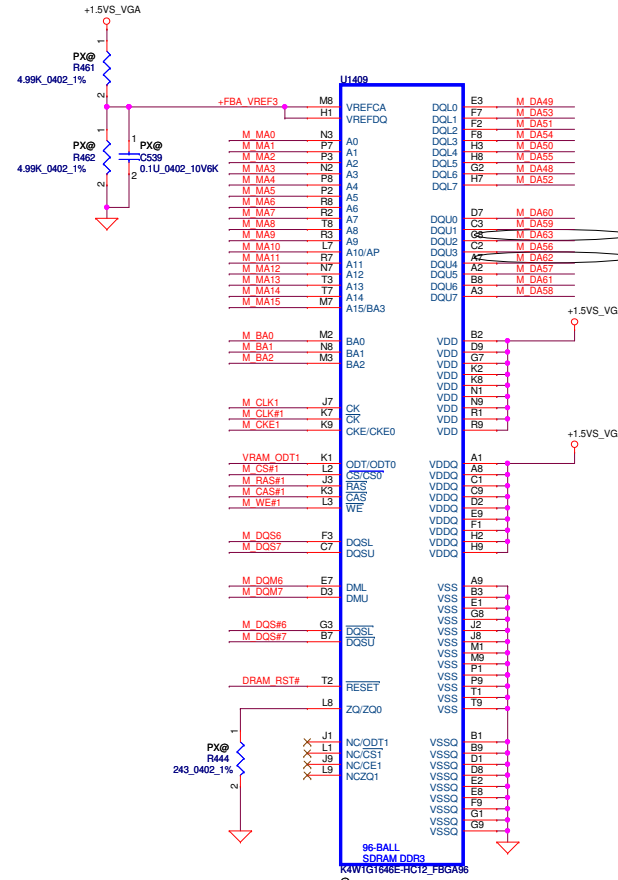
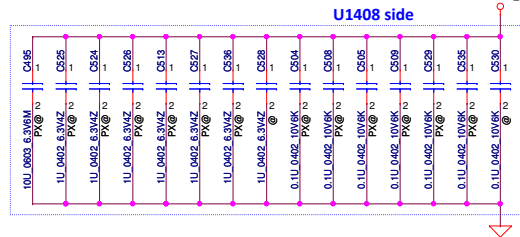
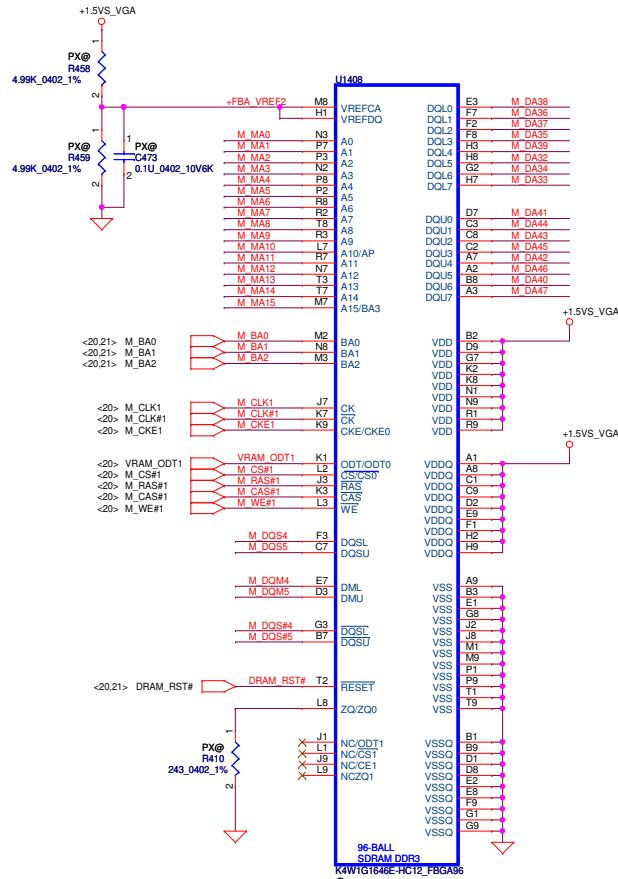
- <20,22> M\_DA[63..0]
- <20,22> M\_MA[15..0]
- <20,22> M\_DOM[7..0]
- <20,22> M\_DQS[7..0]
- <20,22> M\_DQS# [7..0]

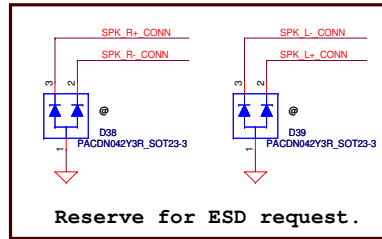
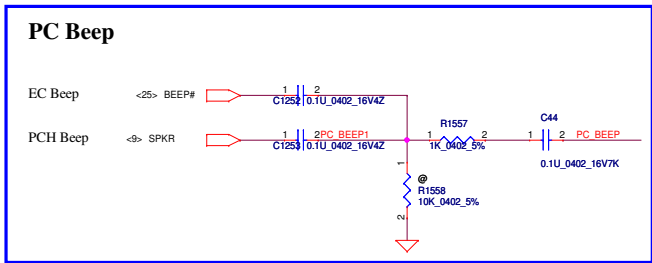
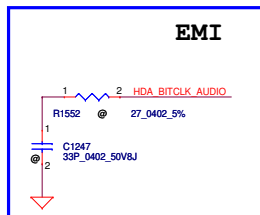
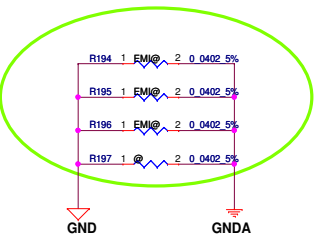
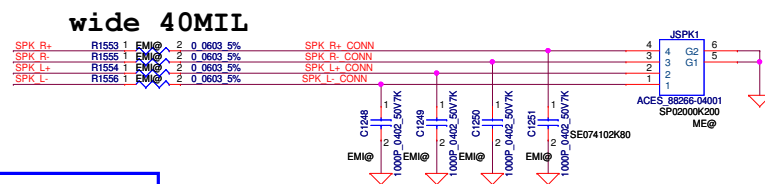
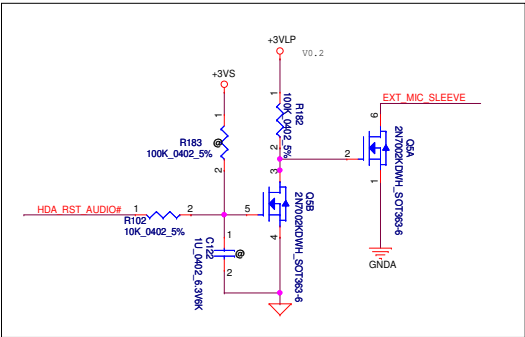
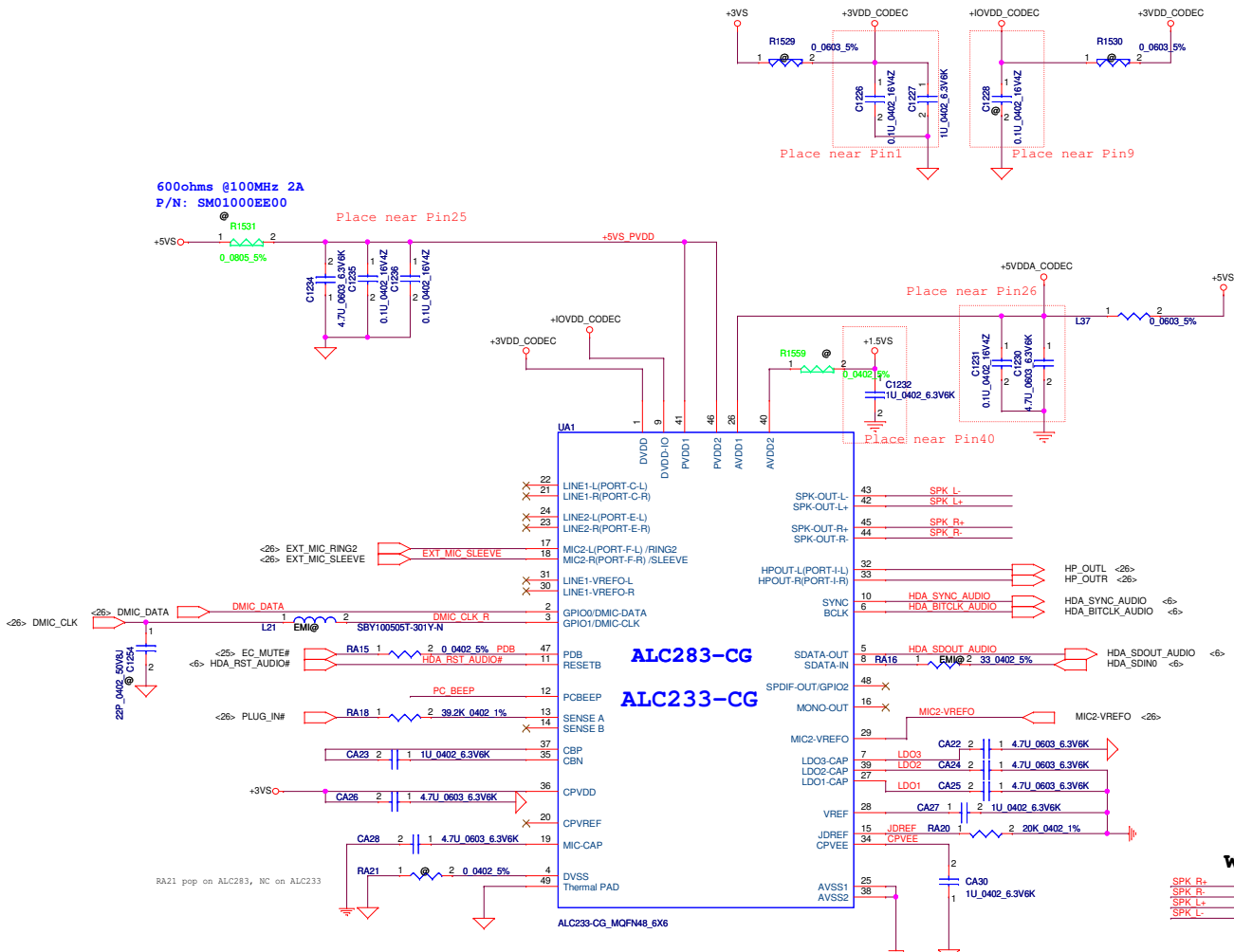


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# Memory Partition A - Upper 32 bits

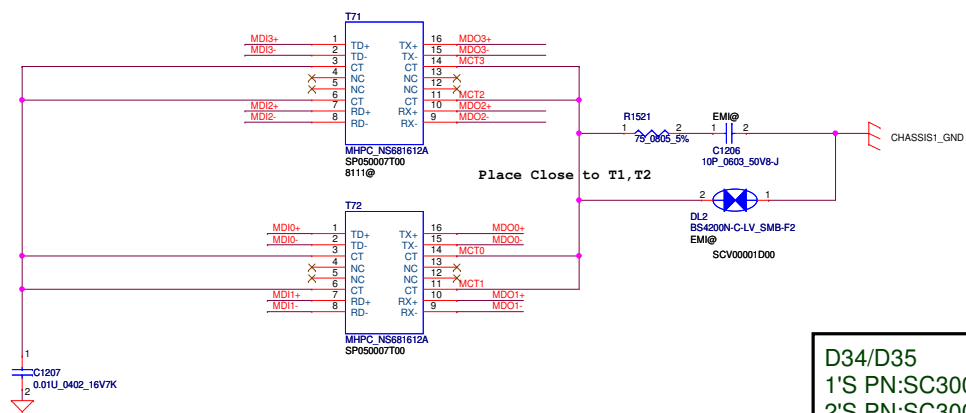
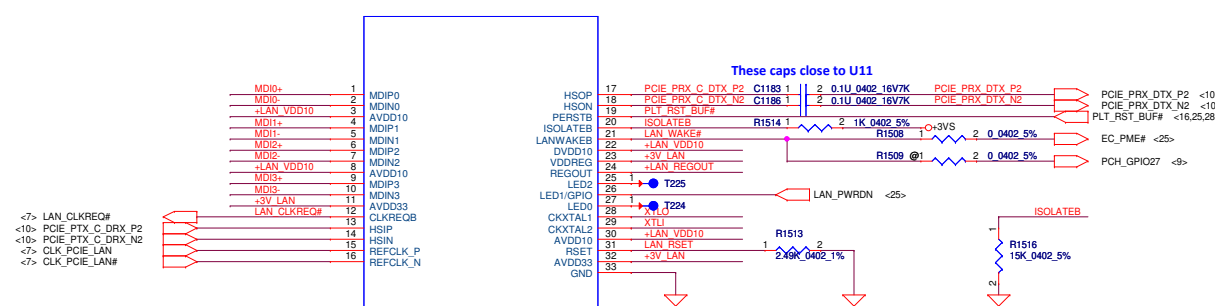
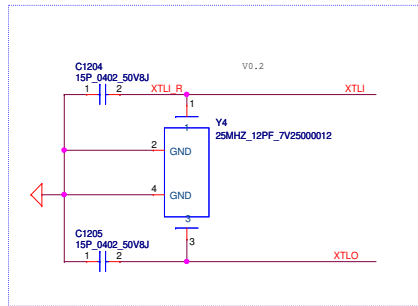
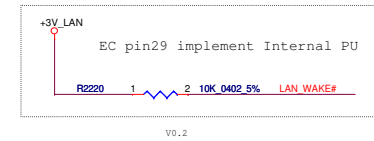
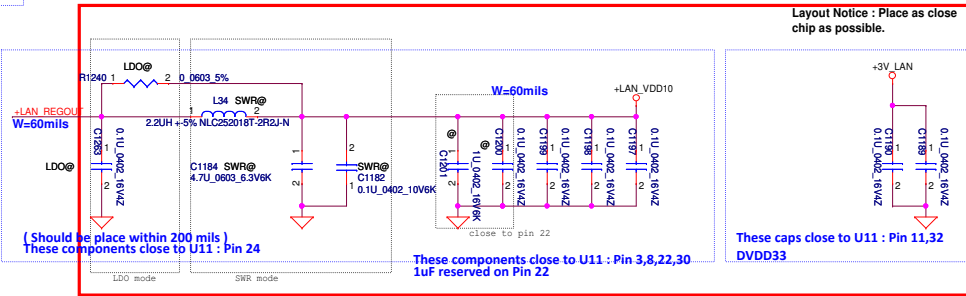
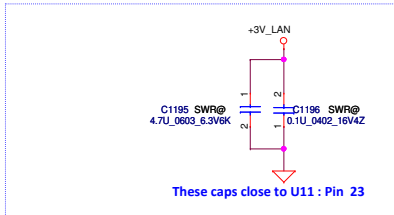
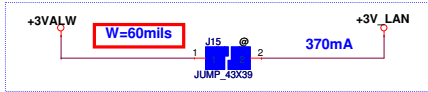
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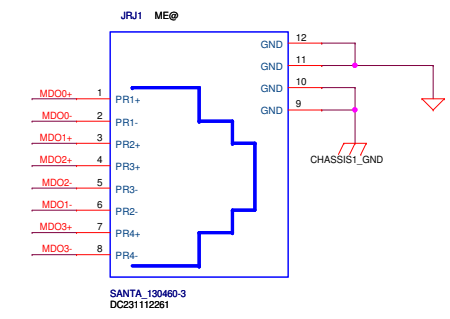
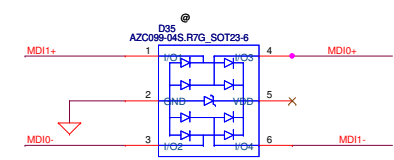
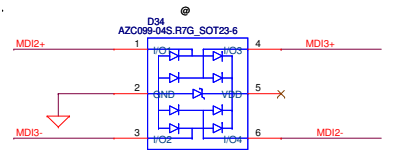


Security Classification	Compal Secret Data		Title	Hd Audio Codec ALC259Q-VC	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Size	Document Number
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+3\_LAN Rising time (10%~90%) >1mS and <100mS



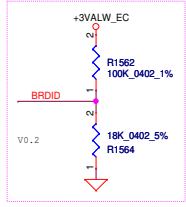
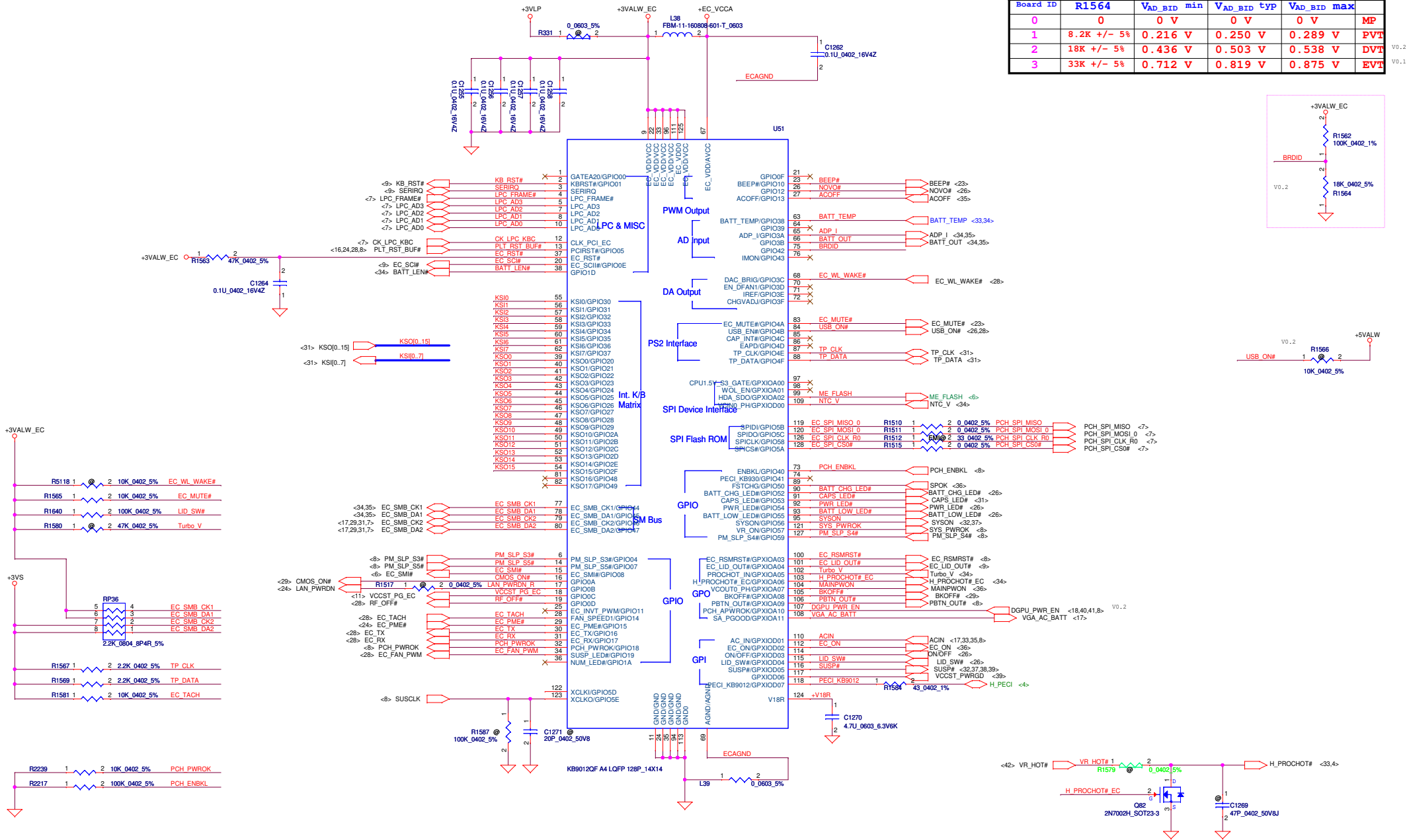
**D34/D35**  
1'S PN:SC30001G00  
2'S PN:SC30002E00



Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	LAN-RTL8111GUS/8106EUS
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				Document Number LA-A321P02
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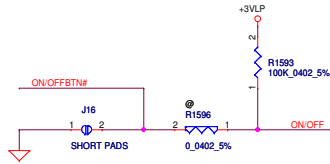
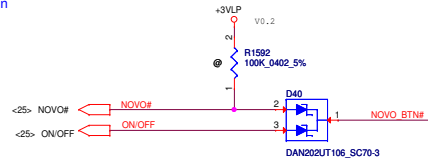
Vcc	3.3V +/- 5%				
R1562	100K +/- 5%				
Board ID	R1564	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT



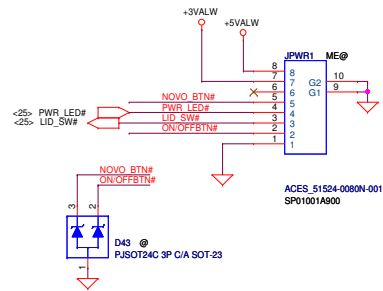
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Issued Date		Deciphered Date		Date	
2011/06/15		2012/07/11		Thursday, March 14, 2013	
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# I/O Board CONN.

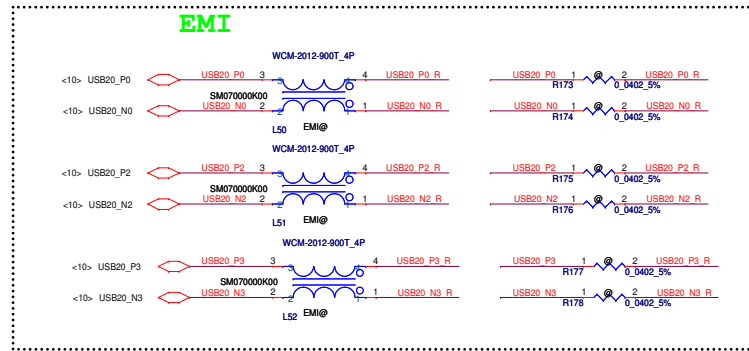
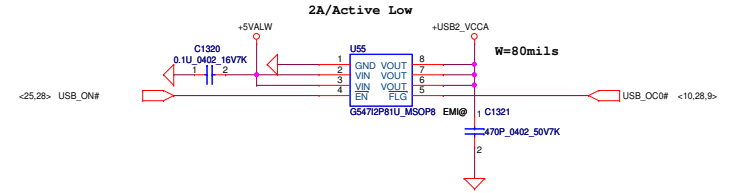
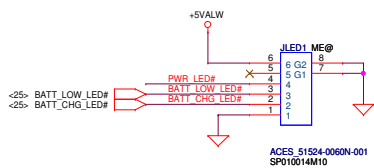
Connector: 0.3A / pin



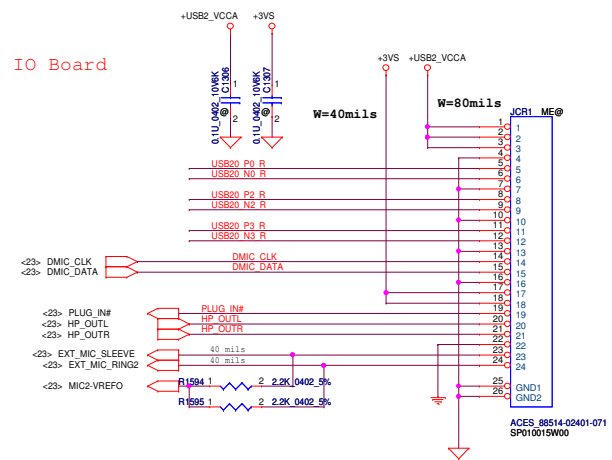
## Power Board



## LED Board

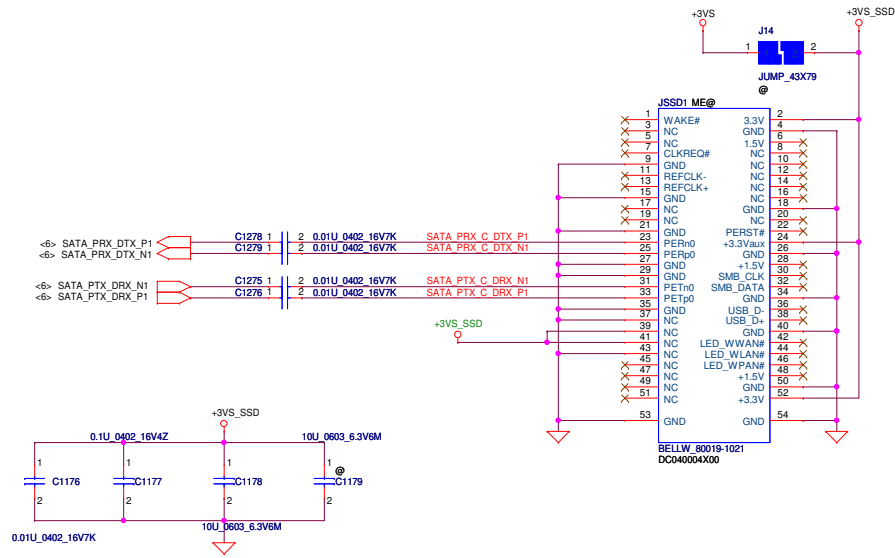


## IO Board

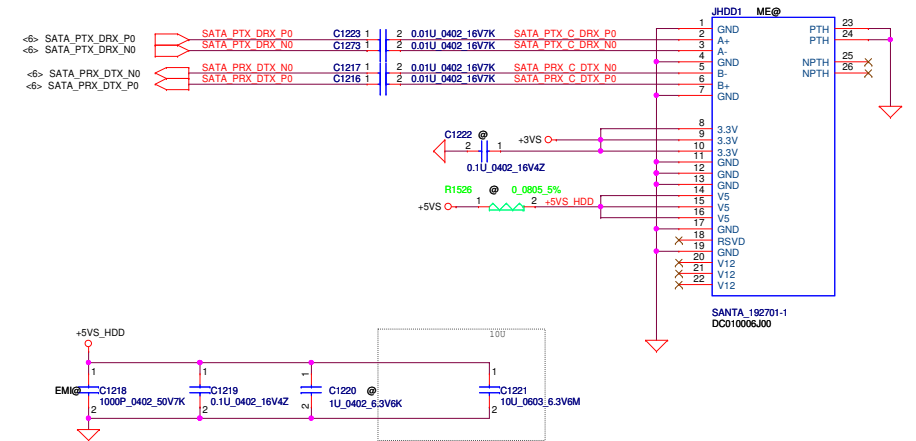


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# msATA CONN.

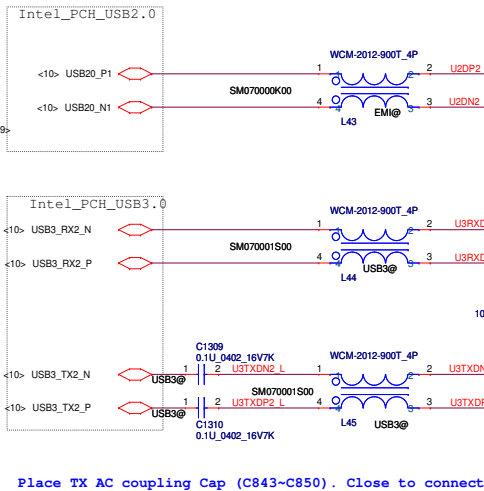
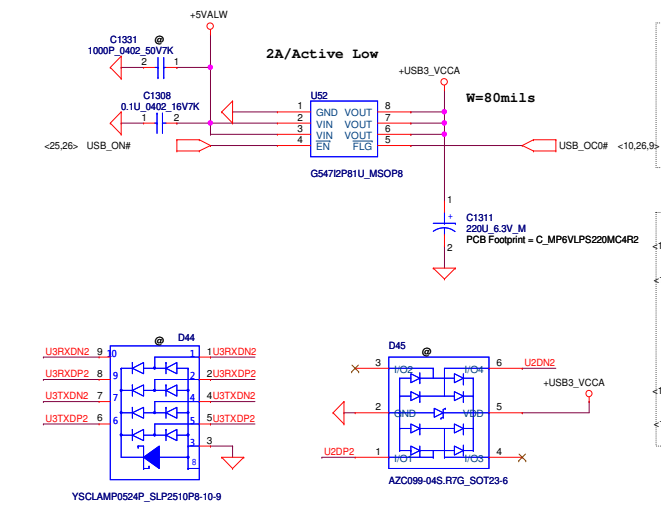


# SATA HDD CONN.

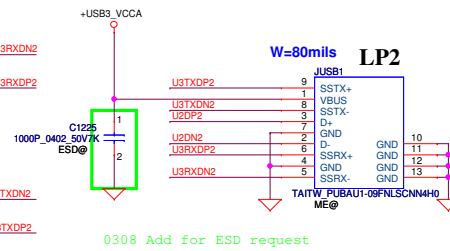


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	<b>HDD/ODD/IBT Connector</b>	
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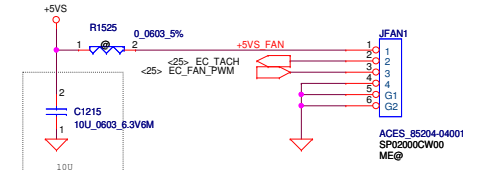
# USB 3.0 Charger & Conn.



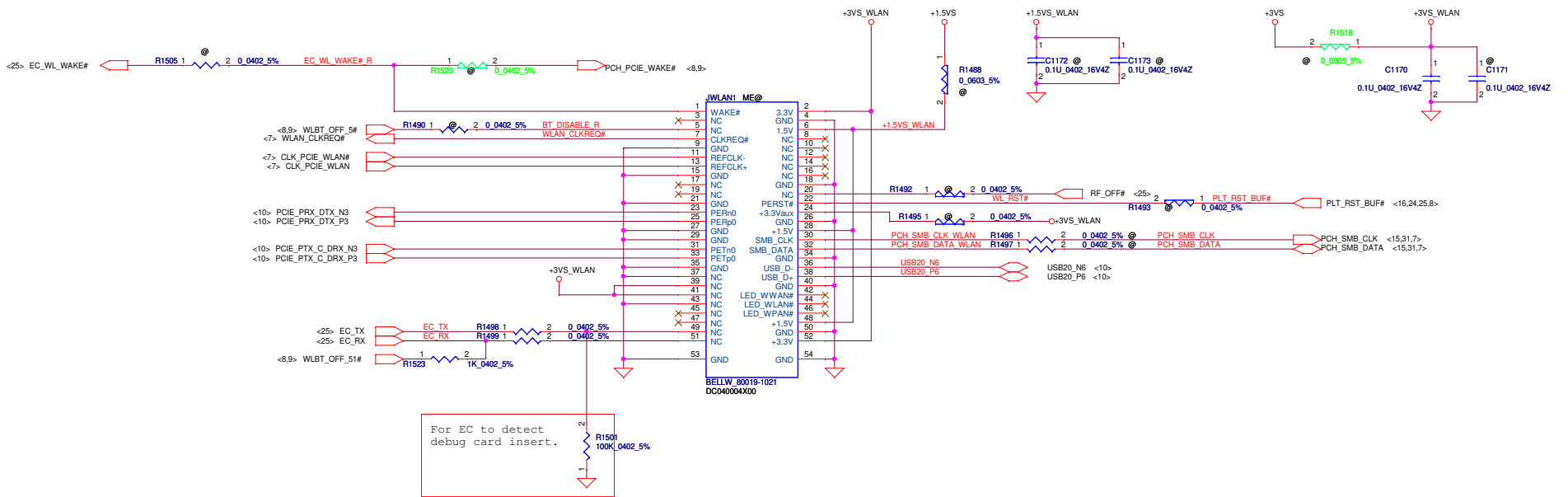
# FAN CONN.



# FAN1 Conn



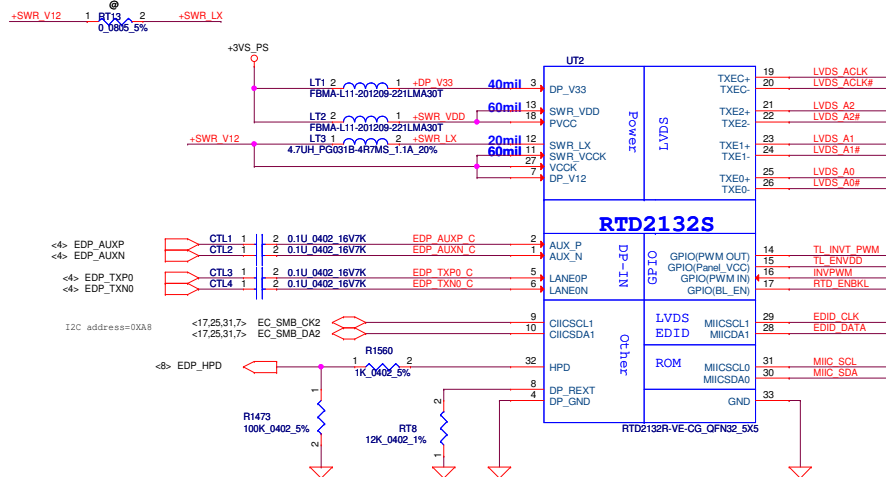
# Mini-Express Card for WLAN(Half)



Note: The real behavior of BT\_DISABLE are  
BT\_DISABLE=LOW, BT=OFF  
BT\_DISABLE=HIGH, BT=ON

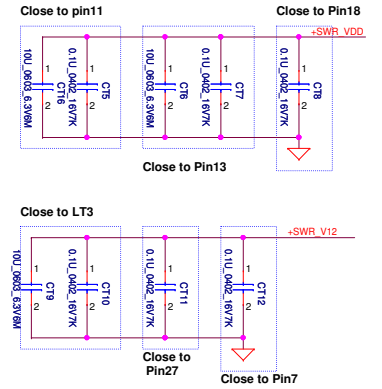
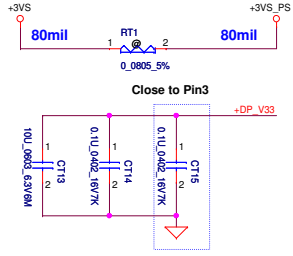
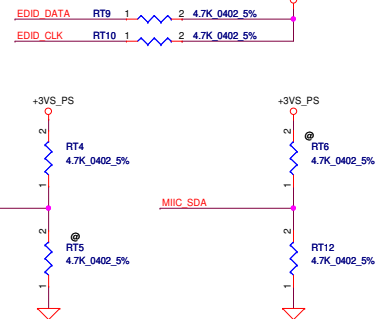
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RTD2132R LDO MODE

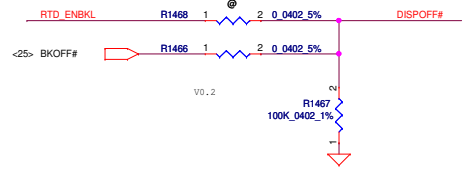
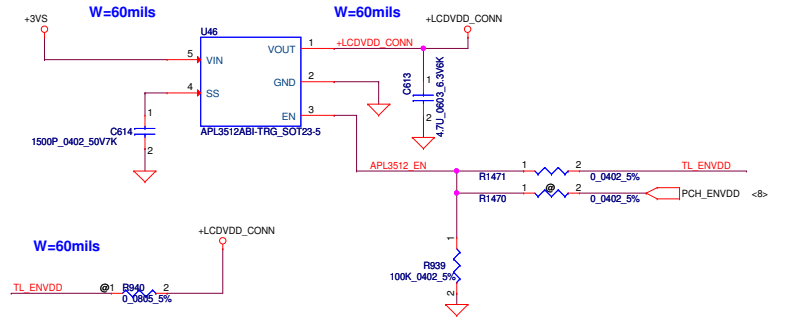


MIIC_SCL \ MIIC_SDA	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

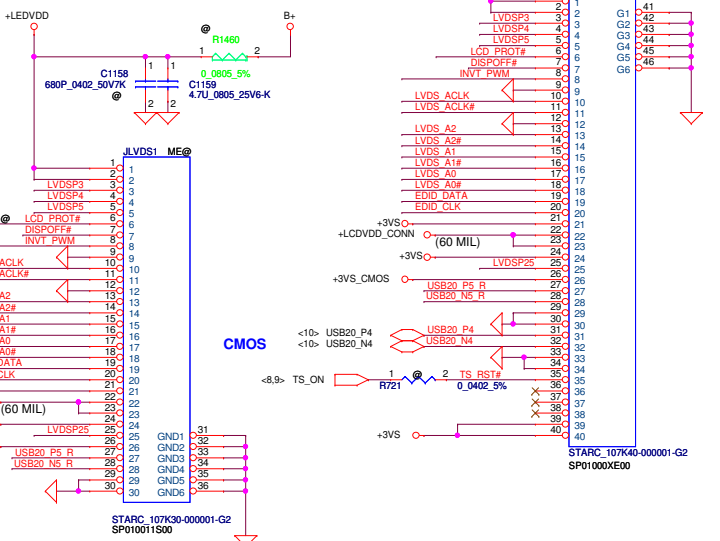
TL\_ENVDD need 60 mil if use for LVDS power on R version



LCD POWER CIRCUIT

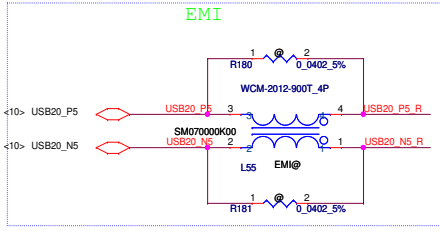
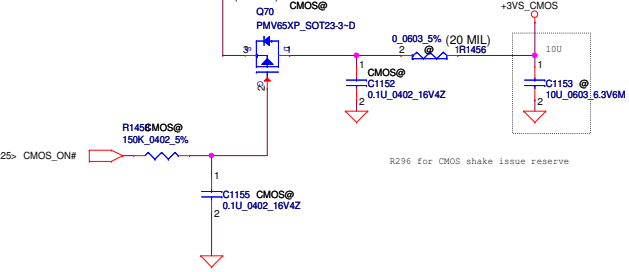


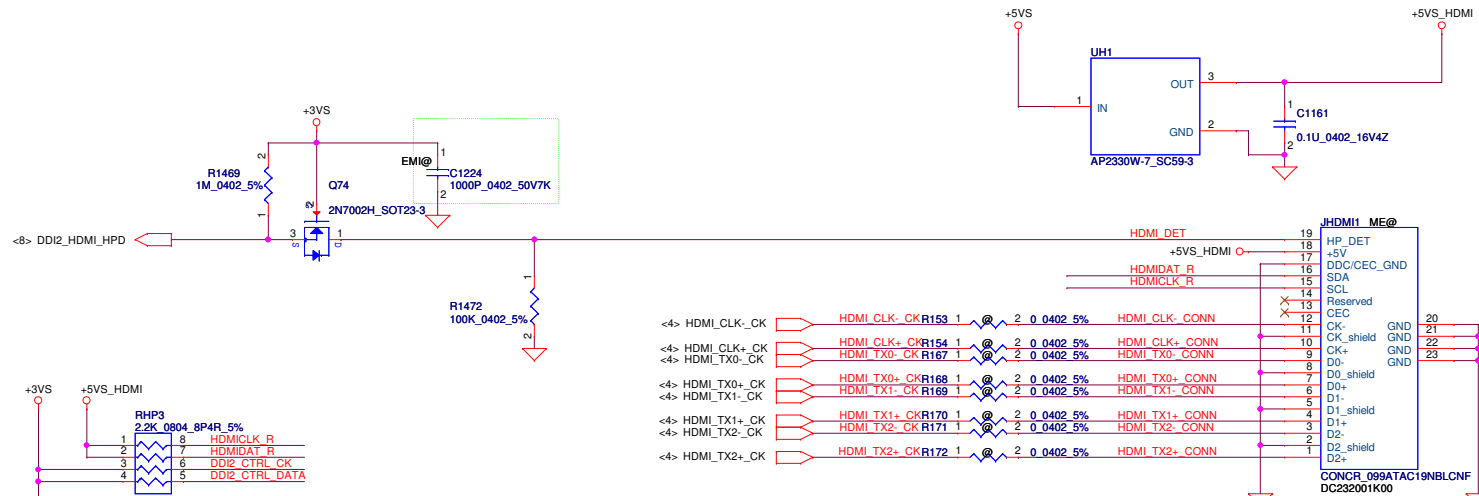
VGA LCD/PANEL BD. Conn.



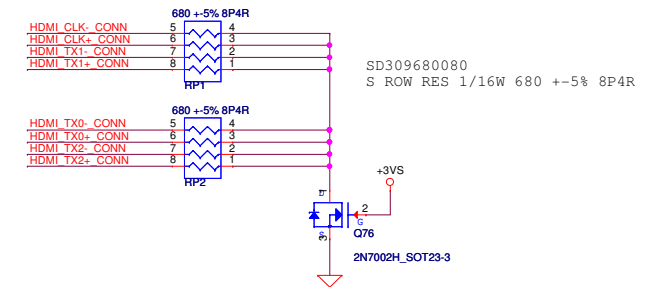
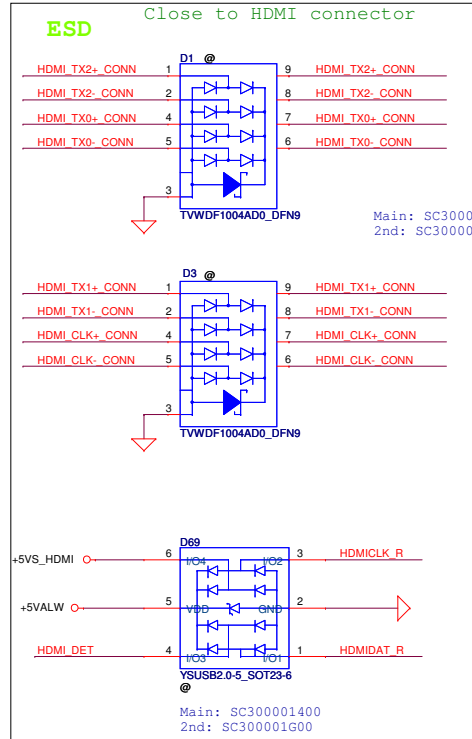
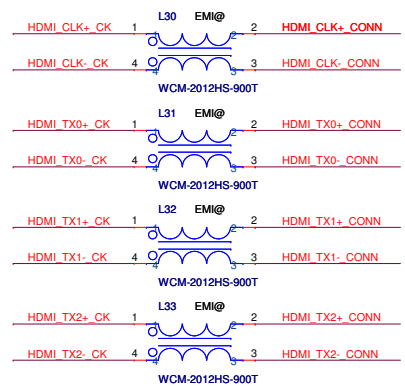
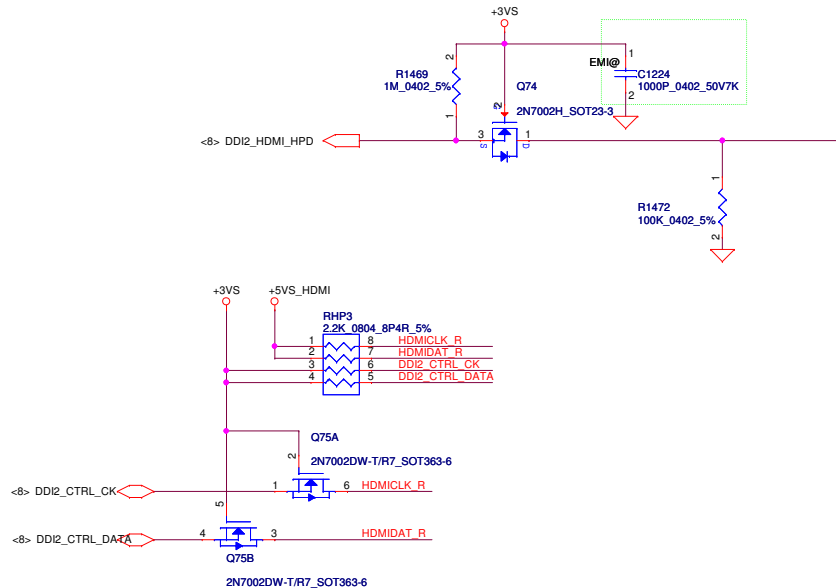
RTD2132R Internal load switch for +LCD\_VCC

CMOS Camera

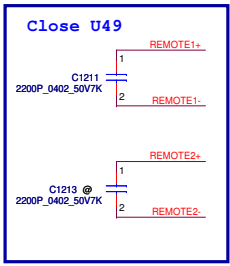




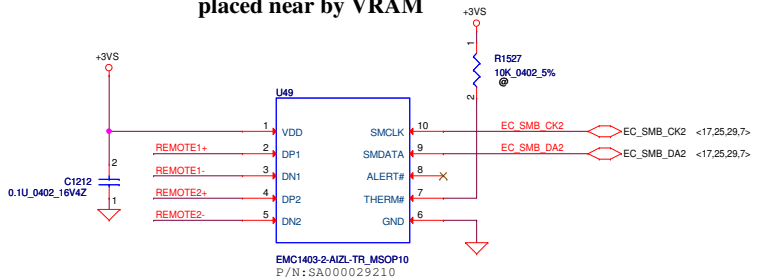
Change Symbol to main source 02/24



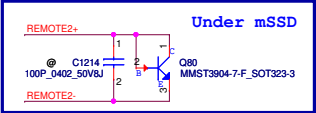
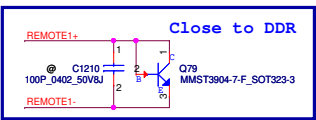
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				<b>HDMI CONN</b>
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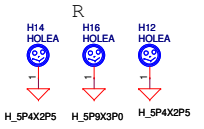
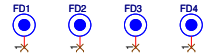
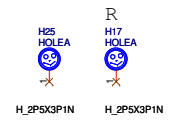
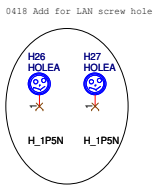
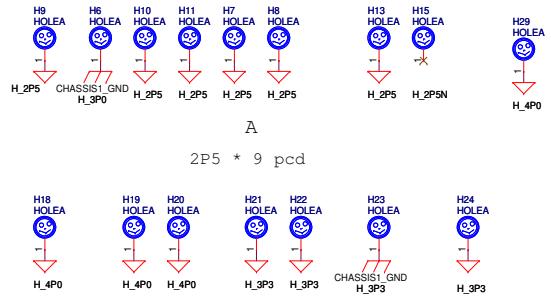
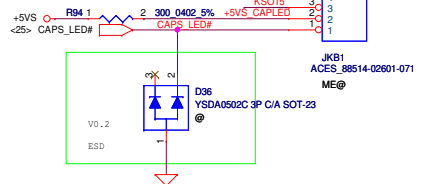
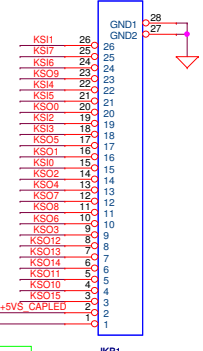
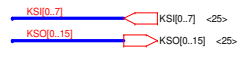
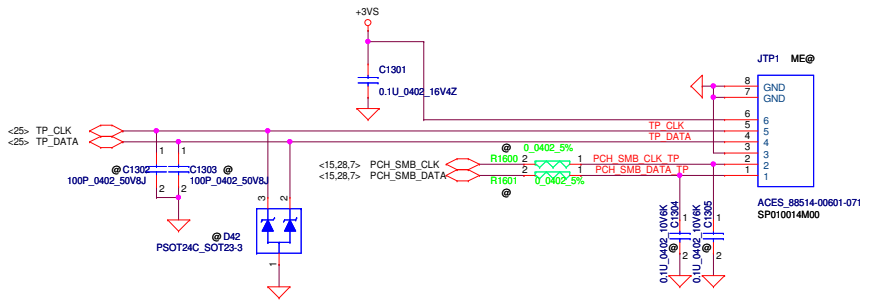
**SMSC thermal sensor placed near by VRAM**



Address 1001\_101xb P/N:SA000029210 F75303M P/N:SA000046C00



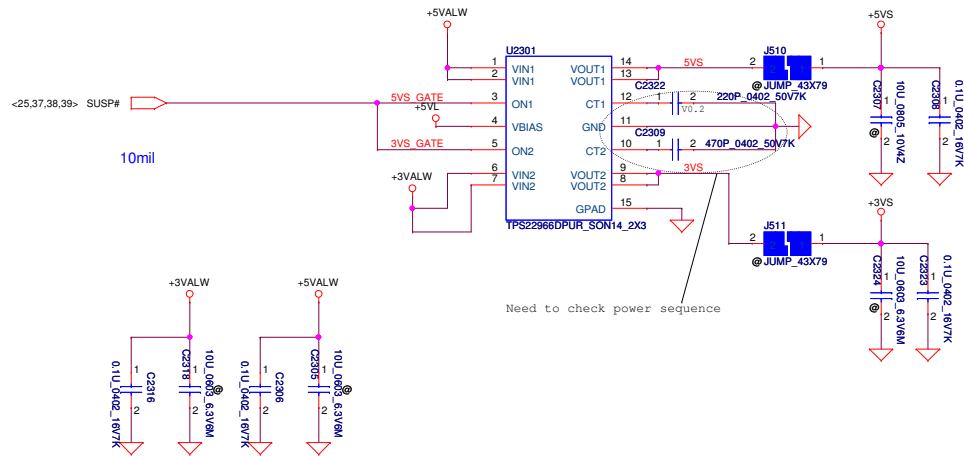
REMOTE1, 2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



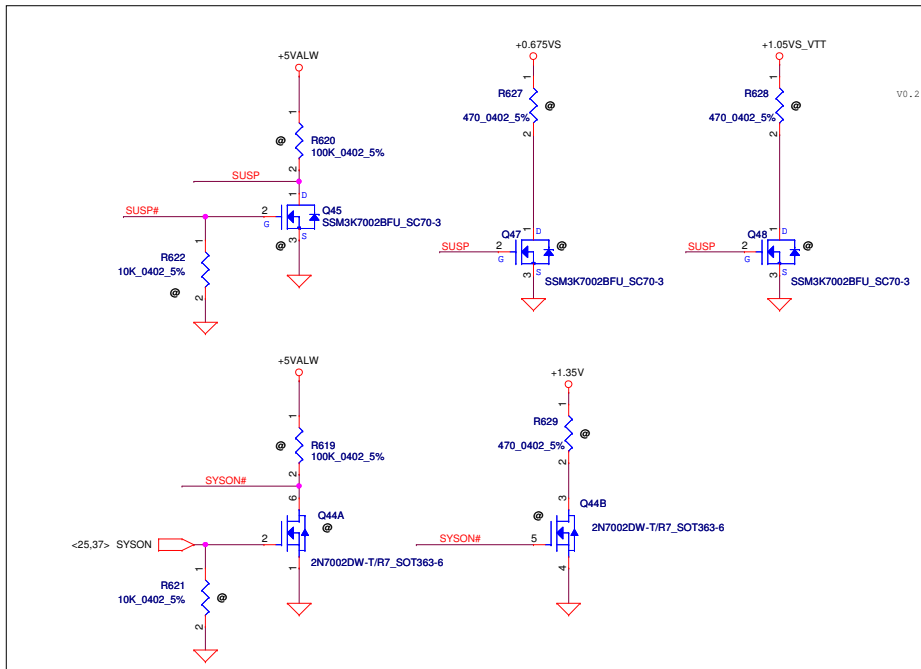
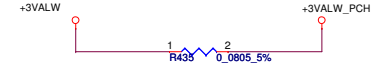
M/B 橢圓孔 M/B KB 橢圓孔

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Size Custom	Document Number	Date: Tuesday, March 19, 2013		Rev 0.2
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**+5VALW TO +5VS**  
**+3VALW TO +3VS**

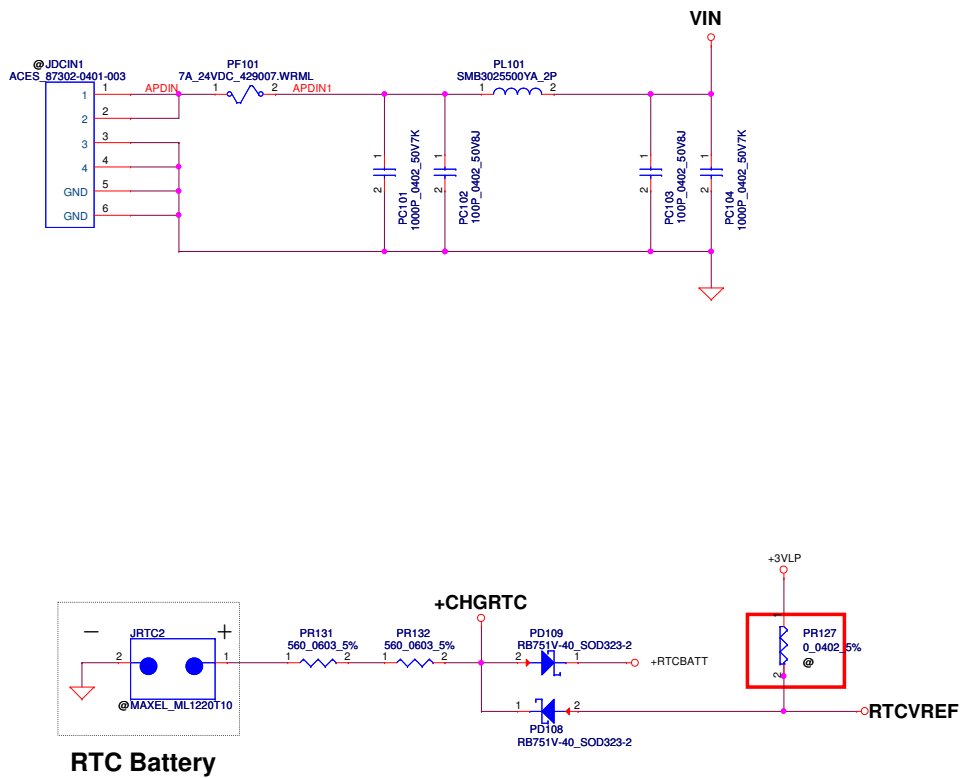


**+3VALW TO +3VALW(PCH AUX Power)**  
**+5VALW TO +5VALW(PCH AUX Power)**

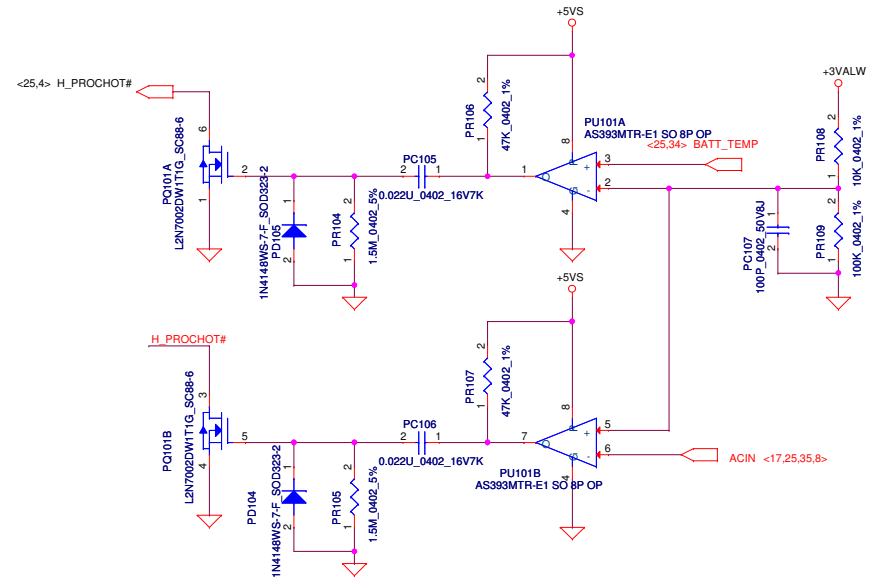


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	DC Interface	
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				Custom	LA-A321PR02
				Date:	Thursday, March 14, 2013
				Sheet	32 of 46



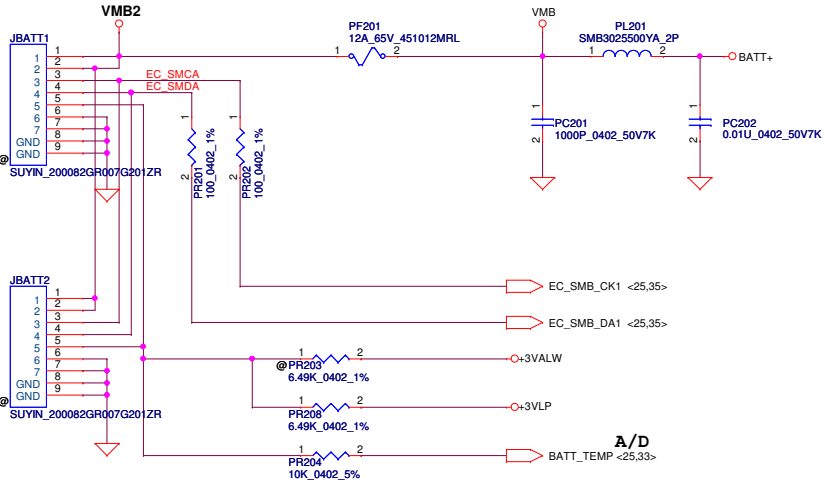


RTC Battery



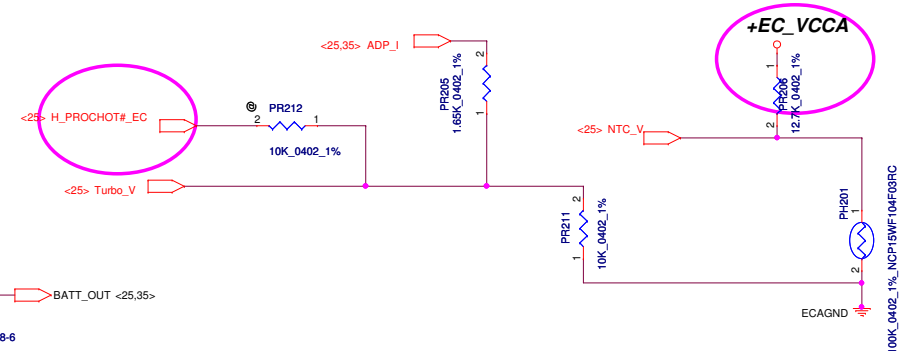
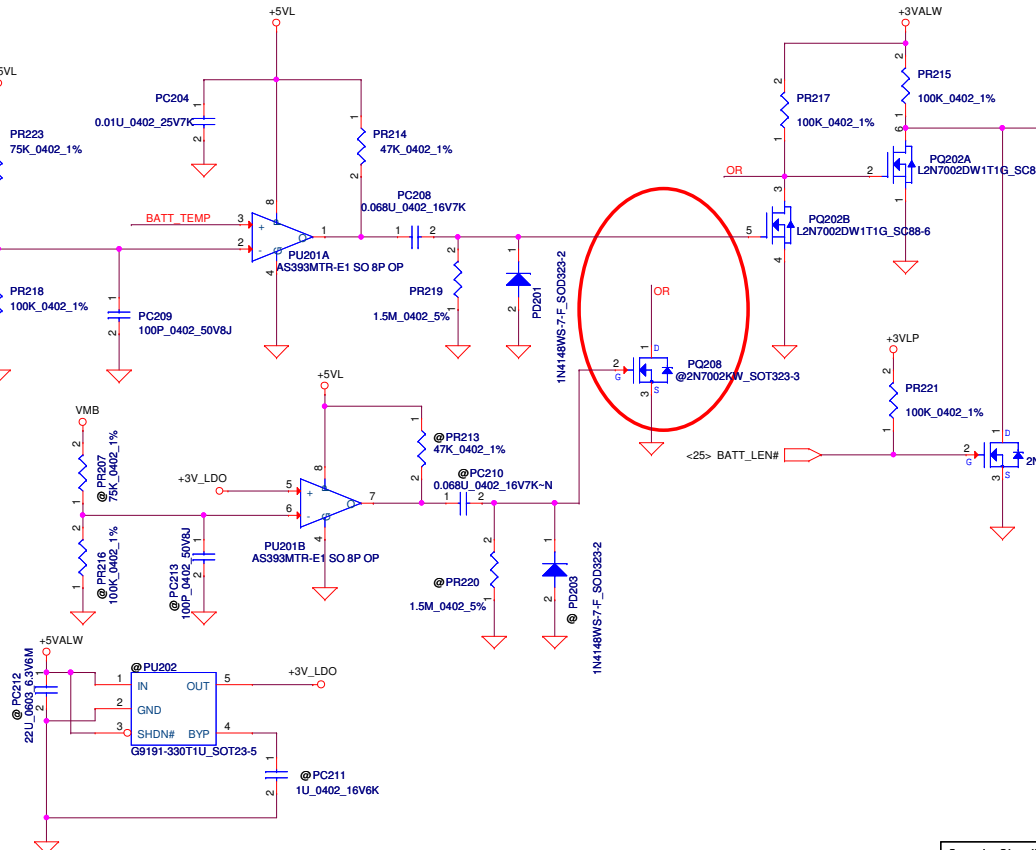
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**JBATT1 Just for 13.3"**  
**JBATT2 Just for 14"**

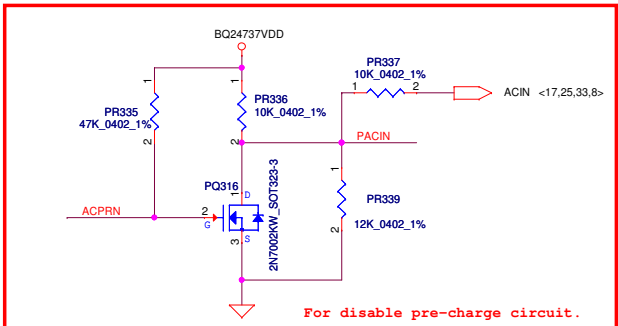
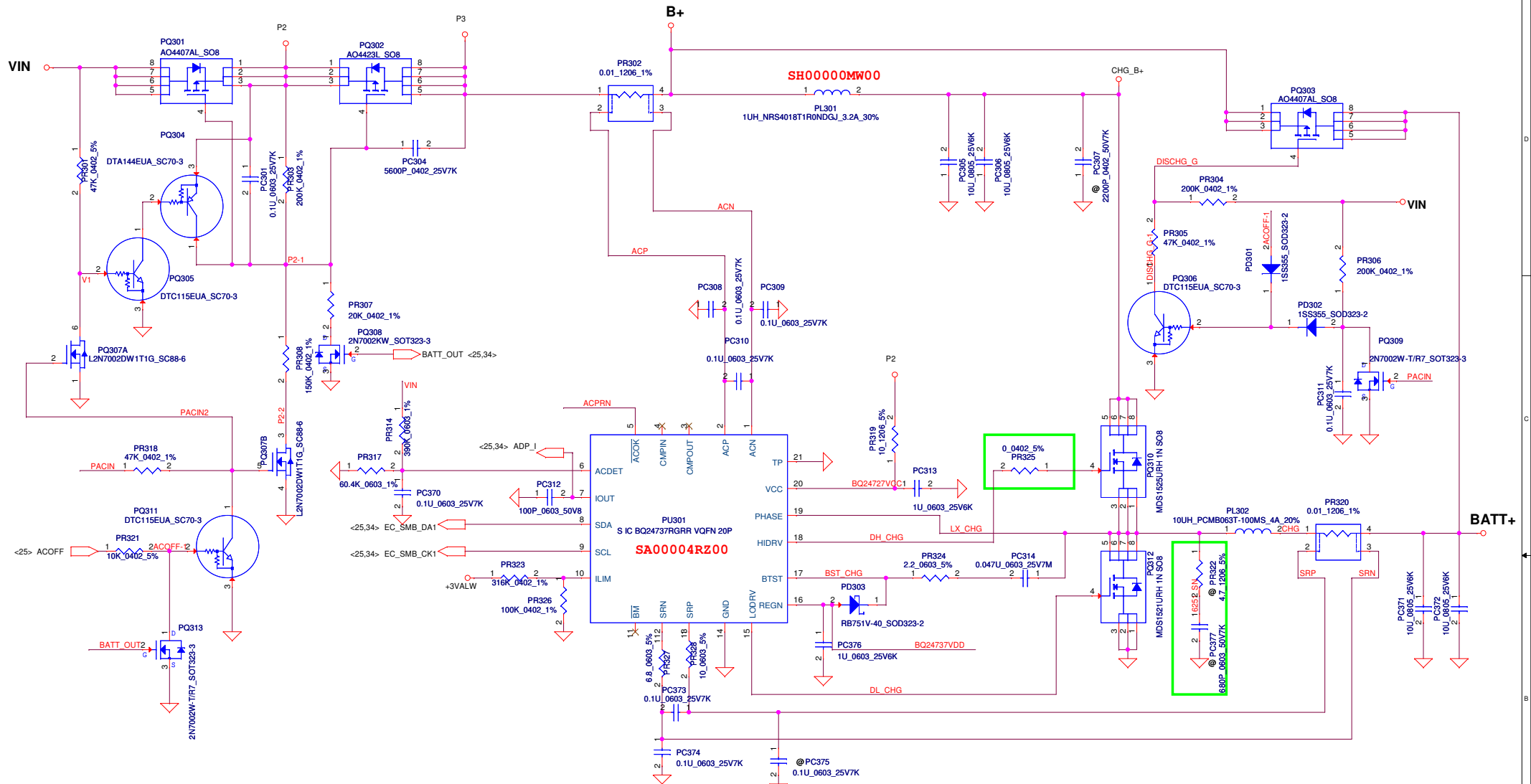


**PH1 under CPU bottom side :**  
**CPU thermal protection at 93 +3 degree C**  
**Recovery at 56 +3 degree C**

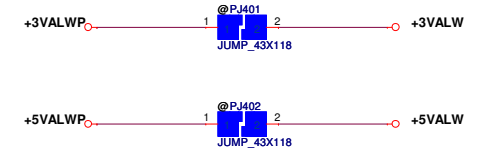
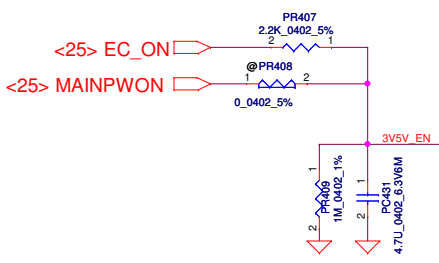
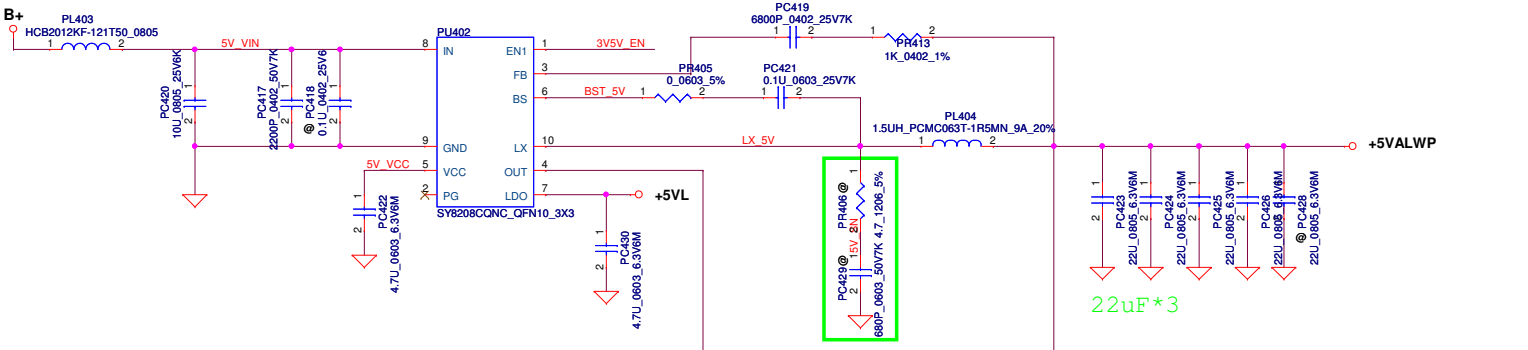
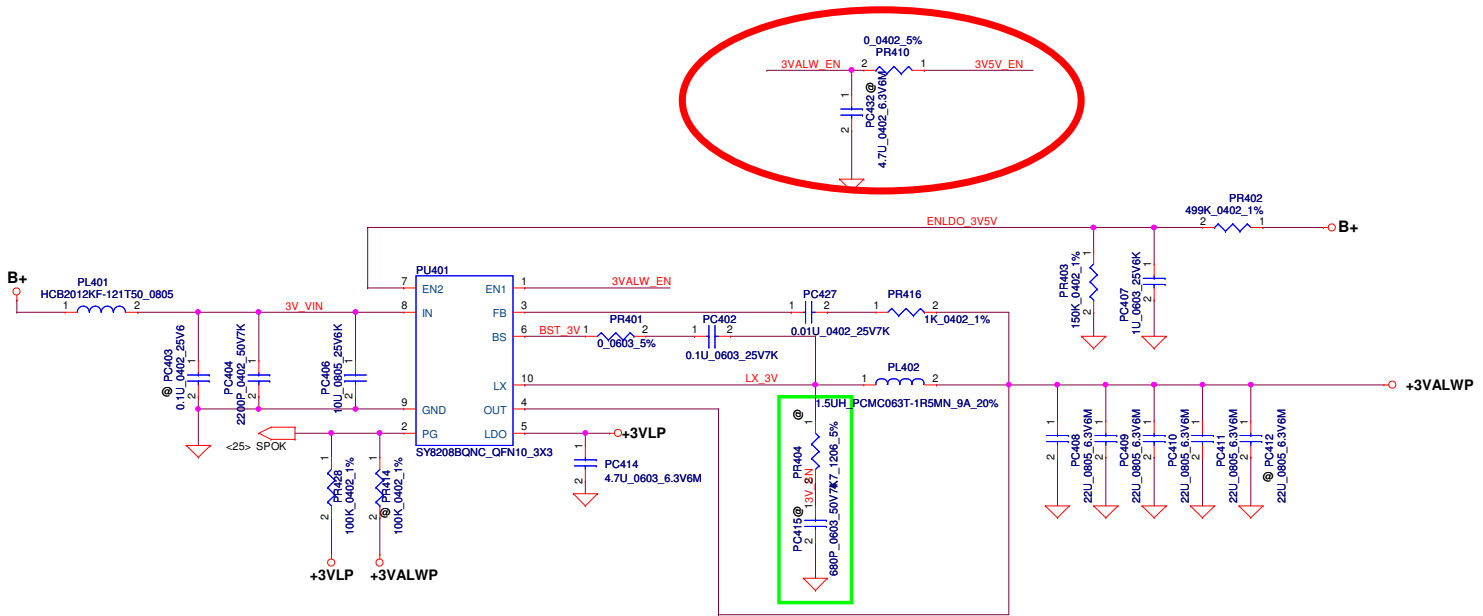
**65W(UMA) : PR205=1.65K(SD034165180)**



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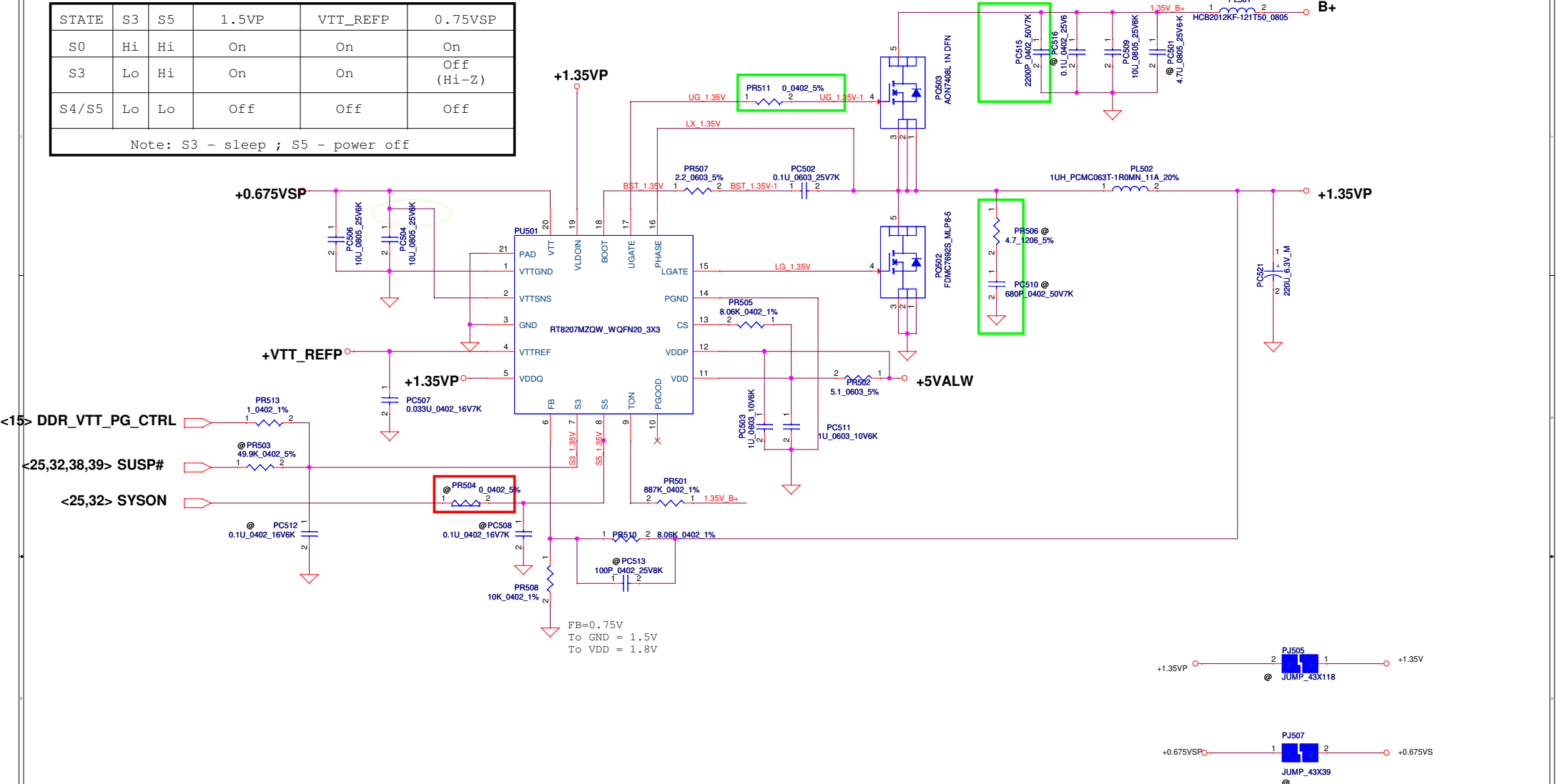
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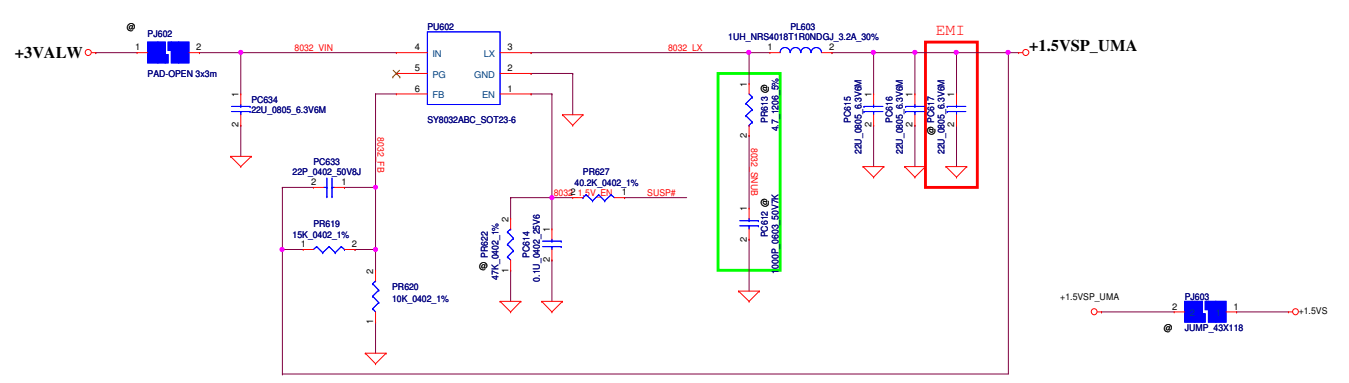
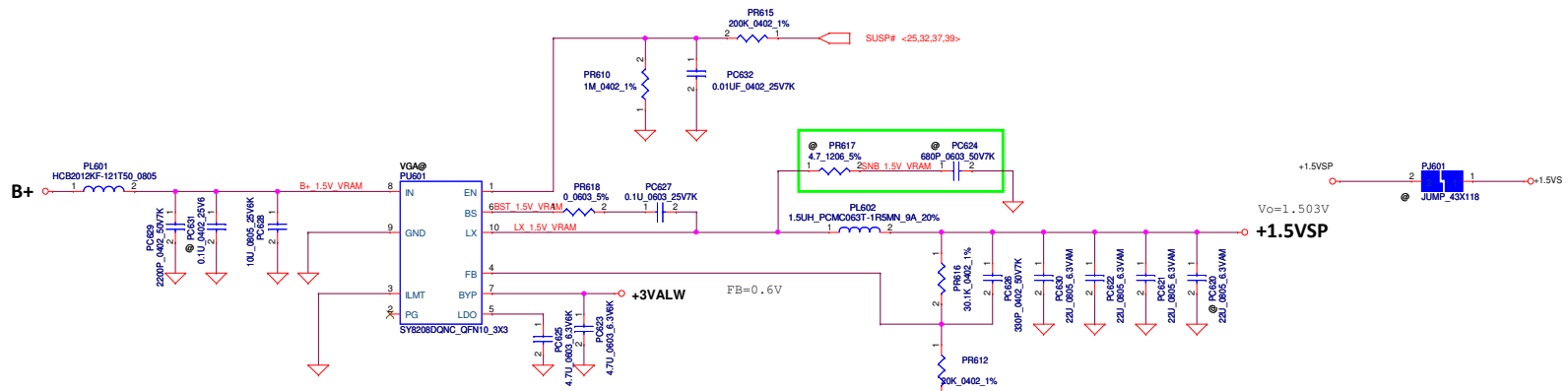


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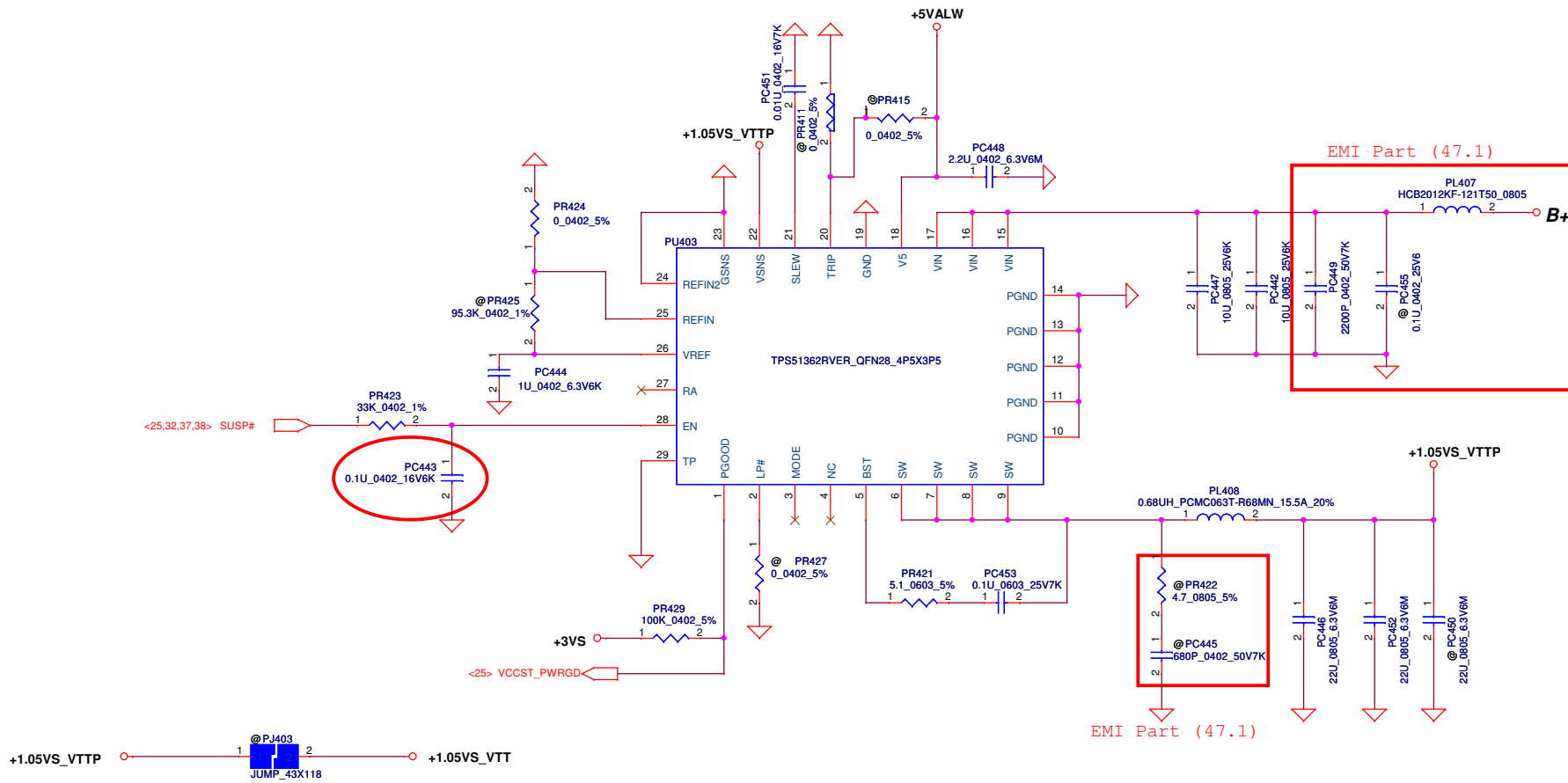
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



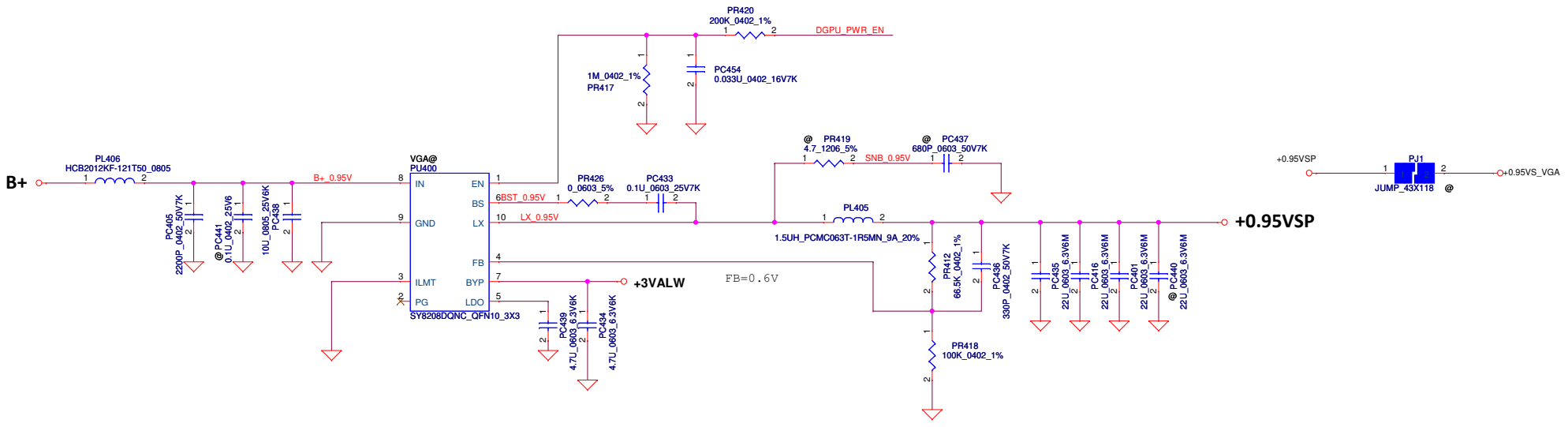
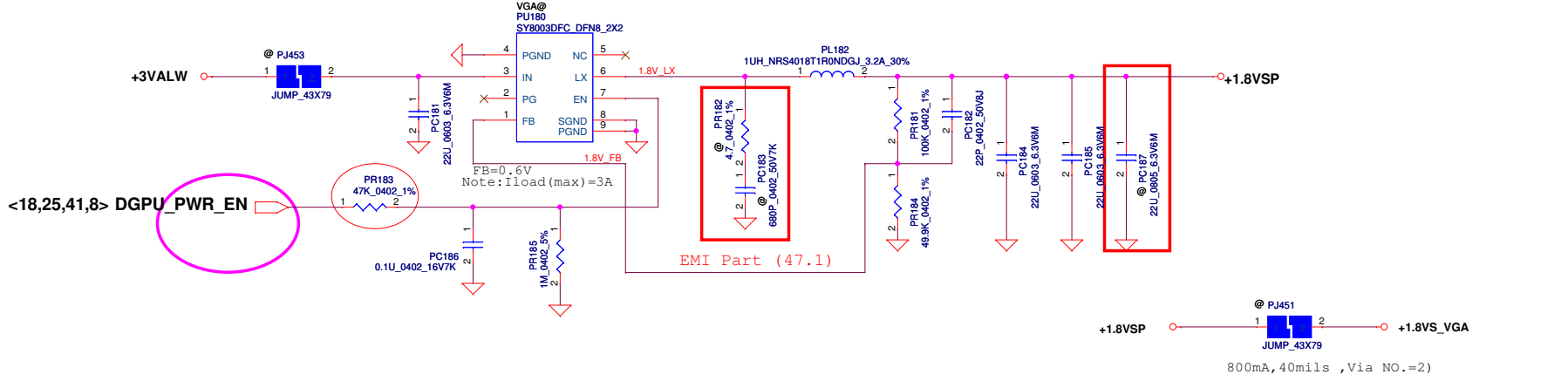


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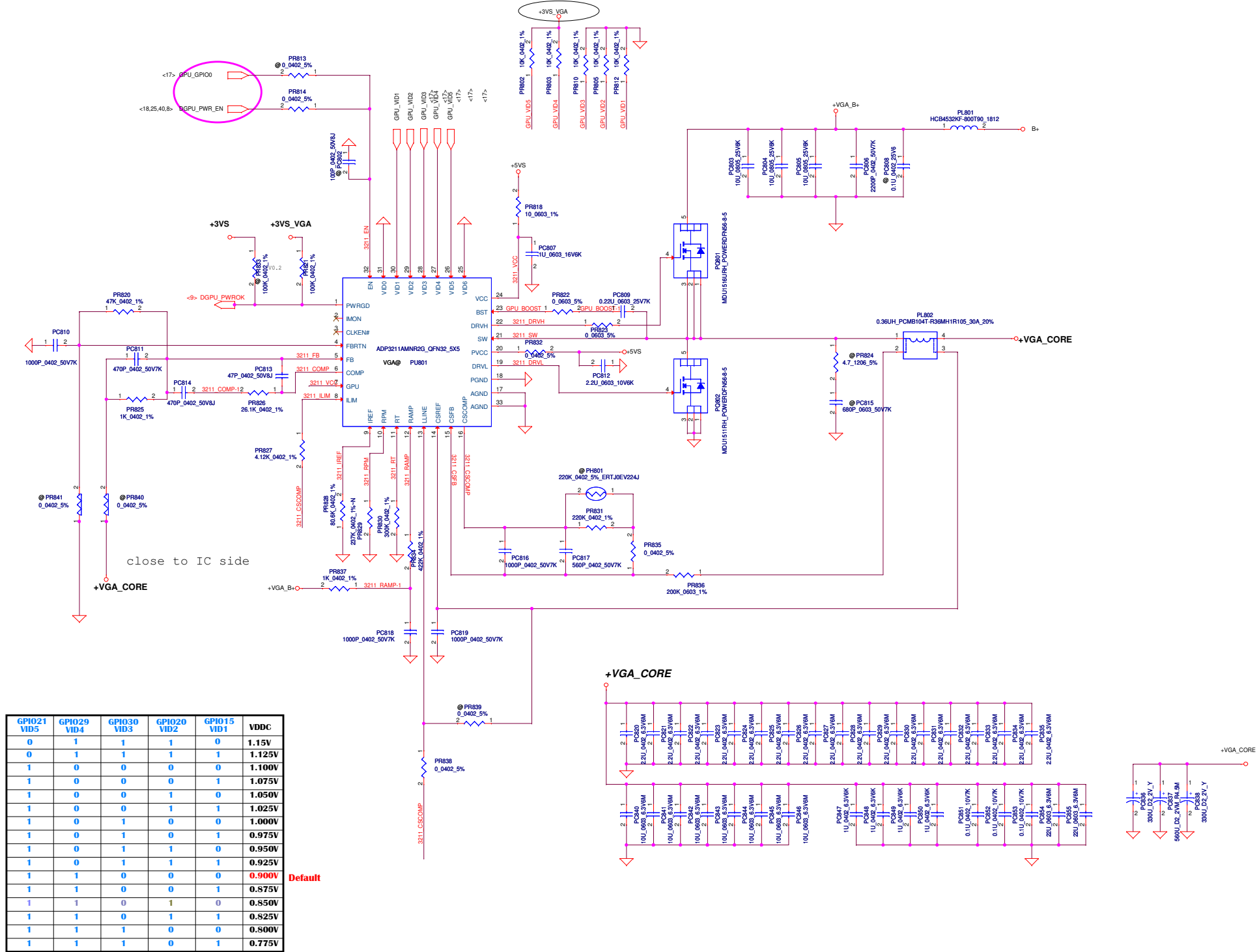
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1.8V controller (35.15), Support component (35.16)



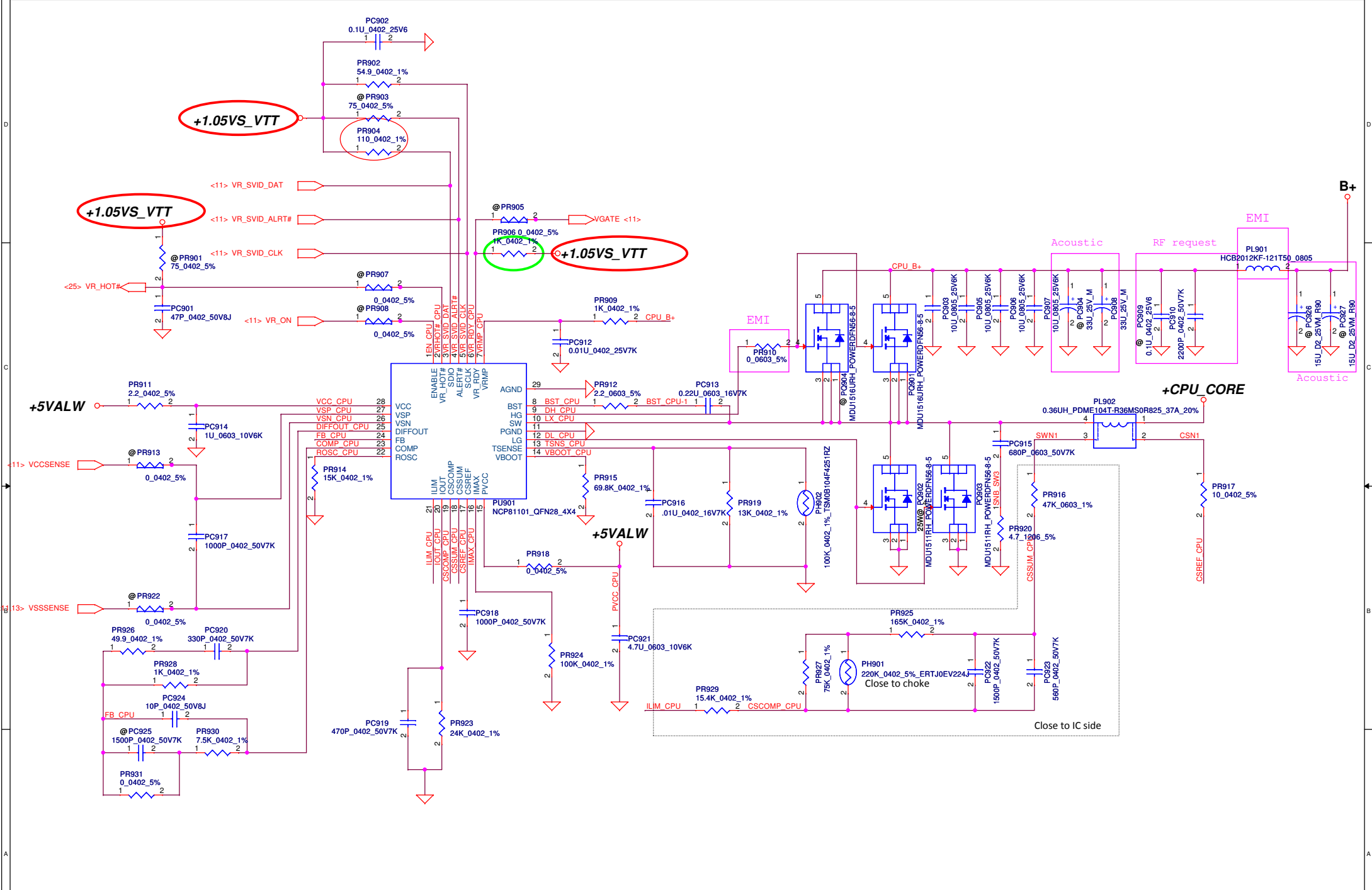
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GPIO21 VID5	GPIO29 VID4	GPIO30 VID3	GPIO20 VID2	GPIO15 VID1	VDDC
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	1	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	1	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

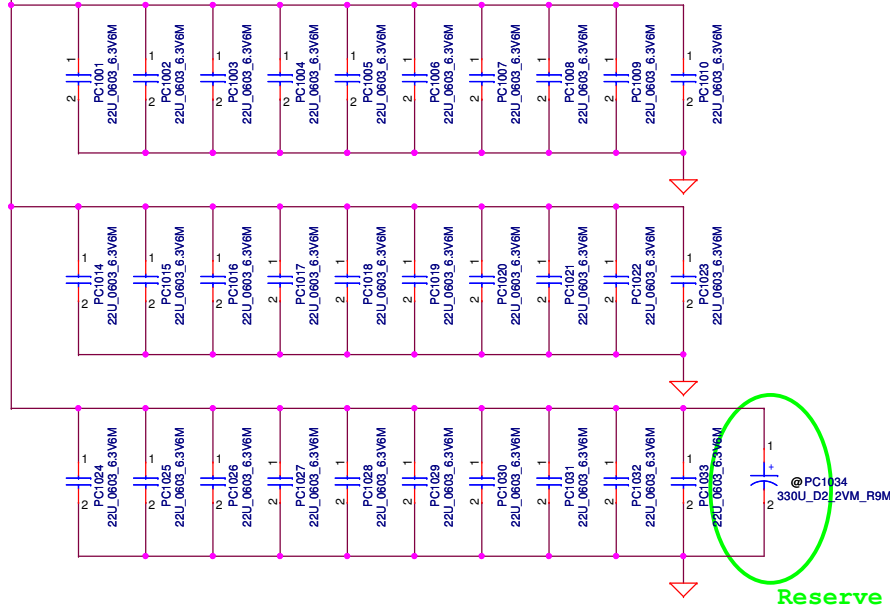


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+CPU\_CORE

30 X 22u/0805

RF request



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	<b>LA-A321PR02</b>	0.2		
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Version change list (P.I.R. List)

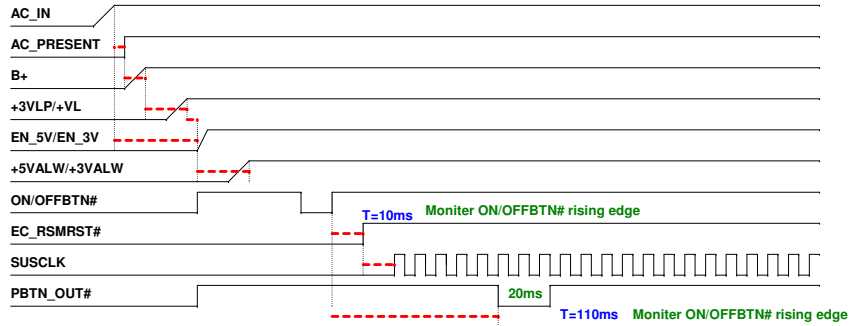
Item	Modify List	PG#	Reason for change	Date	Phase
1	For HW sequence	44	ADD PR821 100K ohm pull high +VS_VGA	3/11	SDV
2	For HW sequence	37	Remove PC512 0.1U_0402	3/11	SDV
3	For HW sequence	39	Change PC443 to 0.1U_0402	3/11	SDV
4	For HW sequence	40	Change PC186 to 0.1uf	2/7	SDV
5	For HW sequence	40	Change PC454 to 0.033uf	2/7	SDV
6	For HW sequence	40	Change PR183 to 47K ohm	2/7	SDV
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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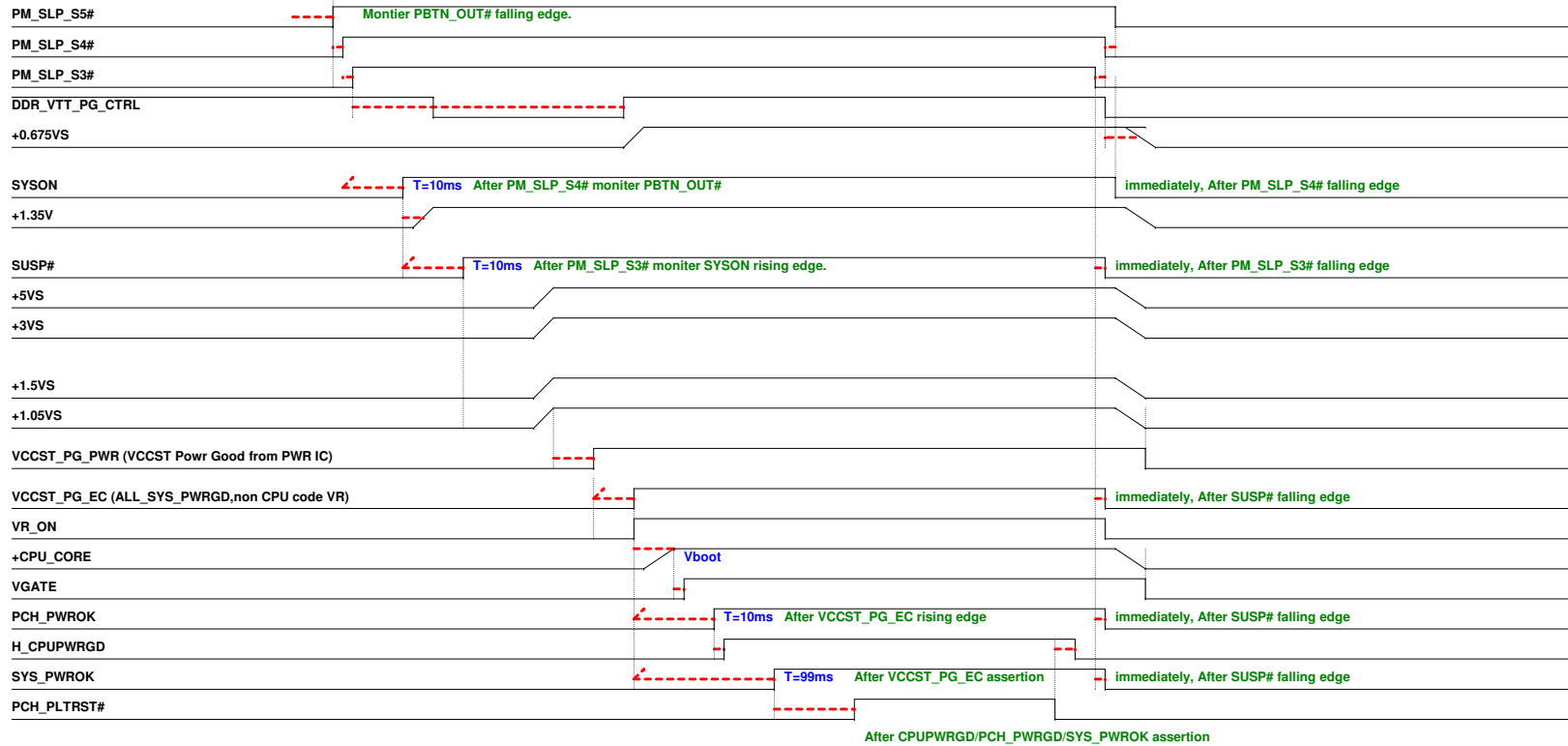
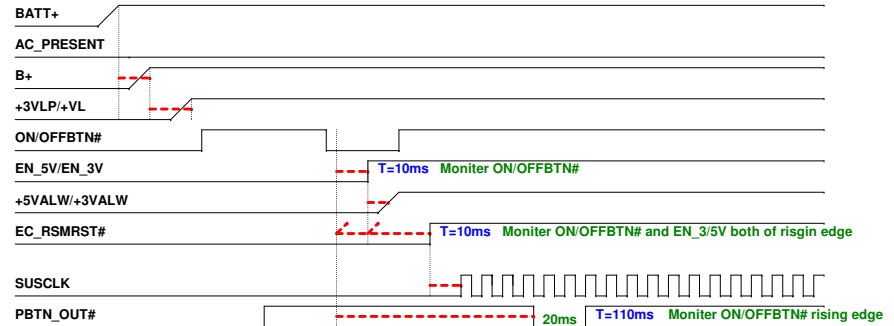
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13					
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