Multi-Channel PMIC with I2C Interface for OLED Panels

General Description

The RT6940 includes one SVDD Boost converter, one VGH boost converter, one Async-Buck converter, one Sync-Buck converter and one VGL negative inverting converter. This device is suitable for OLED TV panels. Many functions can be programmable by I2C interface including Buck VCCO/VCCT converters voltage, SVDD converter voltage, VGH voltage, VGL voltage, VPRED OP-Amplifier, BDP Comparator, BDP start/end delay time, switching frequency, and integrated multiple-time programmable (MTP) non-volatile memory.

The RT6940 also integrates complete protection functions including, OVP, UVP, OCP, and OT protection. The device is used for OLED in the WQFN-56L 7x7 package.

Applications

- OLED Panels

Ordering Information

RT6940□□

- Package Type
  QW : WQFN-56L 7x7 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT6940GQW : Product Number

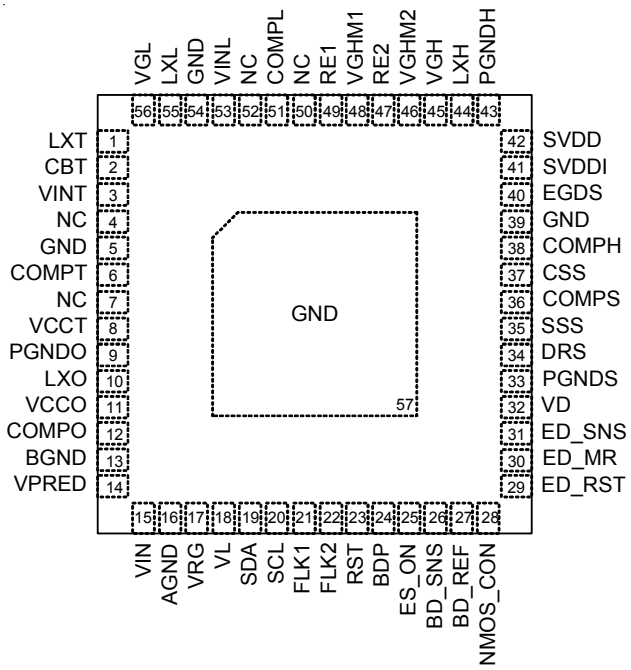
YMDNN : Date Code

Features

- **9.6V to 15.4V Input Voltage Range**
- **SVDD Boost Converter**
  - **15V to 20V, Programmable Output**
  - **Adjustable Switching Frequency from 500kHz to 900kHz**
  - **0.2V/0.4V Over-Current Protection**
- **VCCT3.3 Async-Buck Converter**
  - **3V to 3.6V, Programmable Output**
  - **Adjustable Switching Frequency from SVDD Frequency x 1 to SVDD Frequency x 2**
  - **2A Over-Current Protection**
- **VCCO1.8 Sync-Buck Converter**
  - **1.5V to 2.8V, Programmable Output**
  - **Adjustable Switching Frequency from SVDD Frequency x 1 to SVDD Frequency x 2**
  - **1.5A Over-Current Protection**
- **VGH Boost Converter**
  - **22V to 32V, Programmable Output**
  - **Adjustable Switching Frequency from SVDD Frequency x 1 to SVDD Frequency x 2**
  - **1.5A Over-Current Protection**
- **VGL Negative Inverting Converter**
  - **-4V to -13V, Programmable Output**
  - **Adjustable Switching Frequency from SVDD Frequency x 1 to SVDD Frequency x 2**
  - **1.5A Over-Current Protection**
- **Programmable VGH BDP Current from 600mA to 1050mA**
- **Programmable VGL BDP Current from 450mA to 900mA**
- **Programmable BDP Start/End Delay Time**
- **Adjustable VPRED from 3V to 6.5V**
- **Programmable Delay Time of T1,T3,T4 and T6**
- **Integrated MTP Memory**
- **I²C-Compatible Interface for Register Control**
- **Under-Voltage Protection**
- **Over-Temperature Protection**

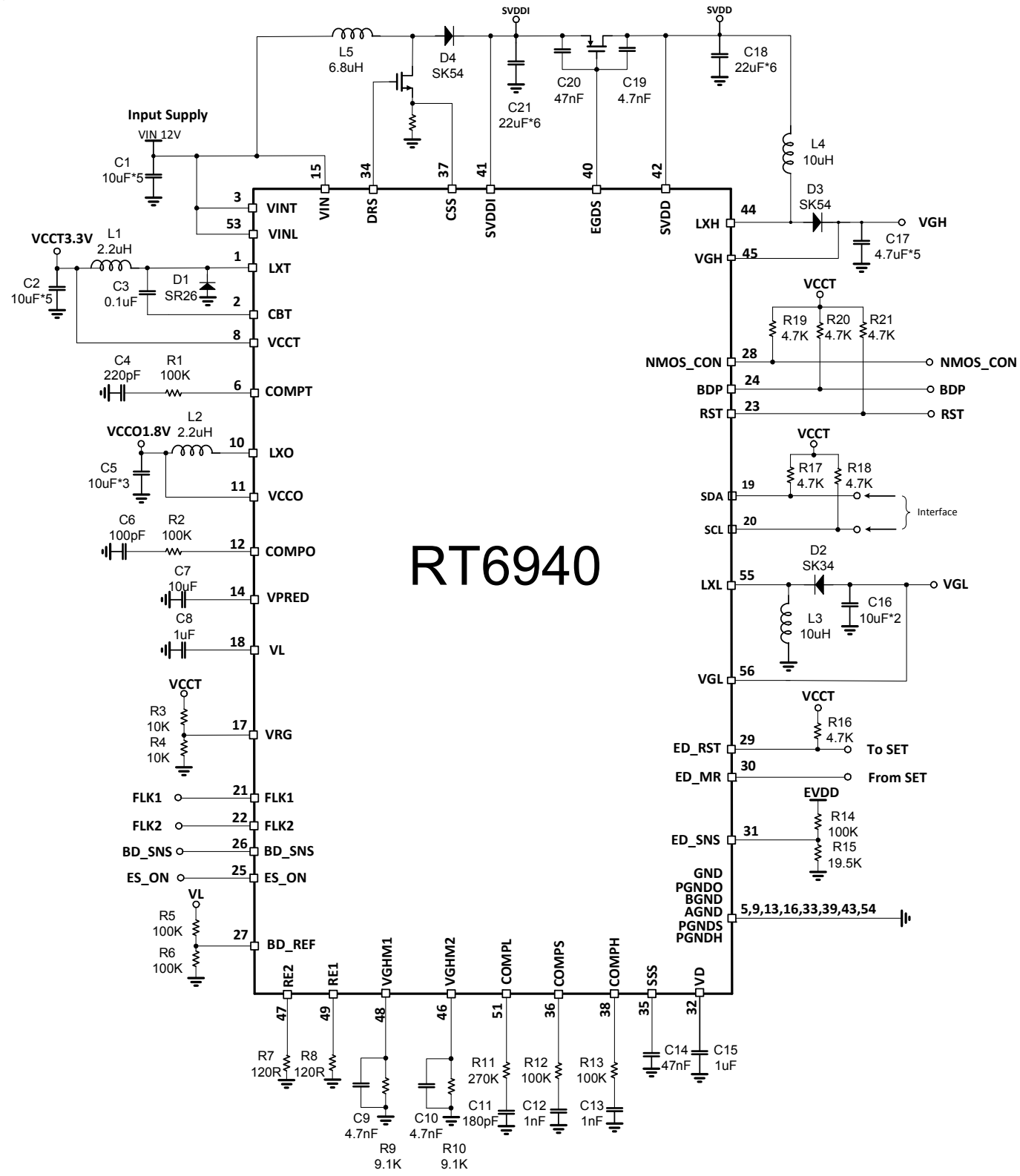
Pin Configuration

(TOP VIEW)

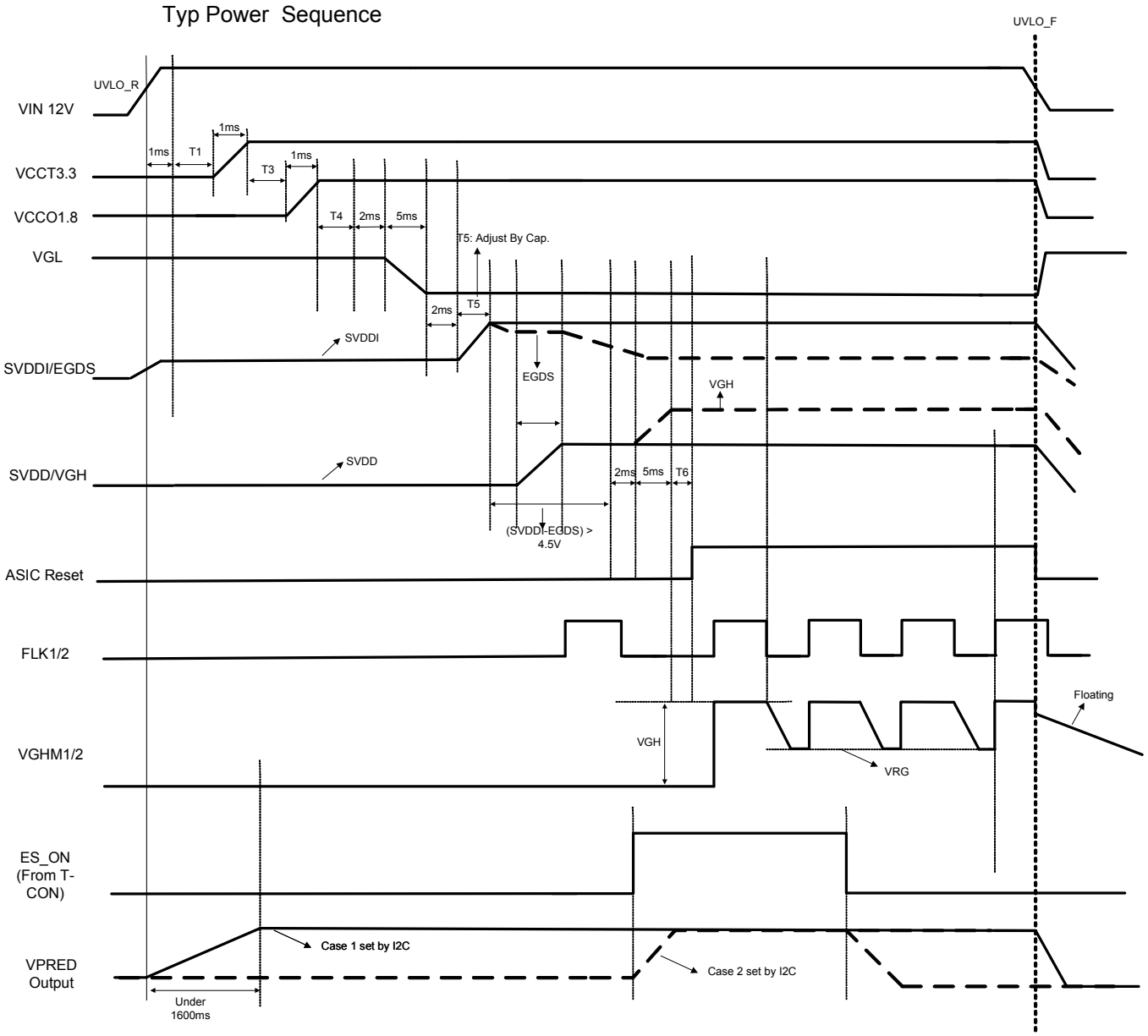


WQFN-56L 7x7

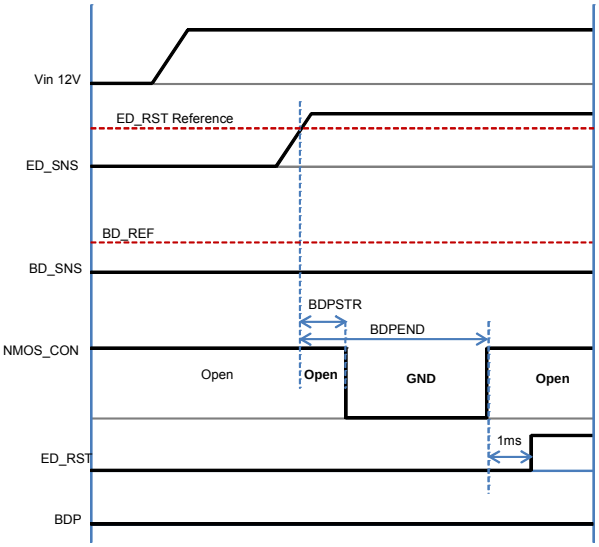
Typical Application Circuit



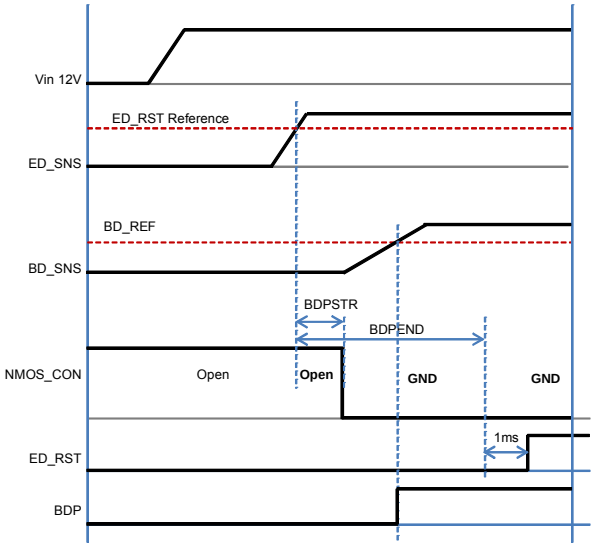
Timing Diagram



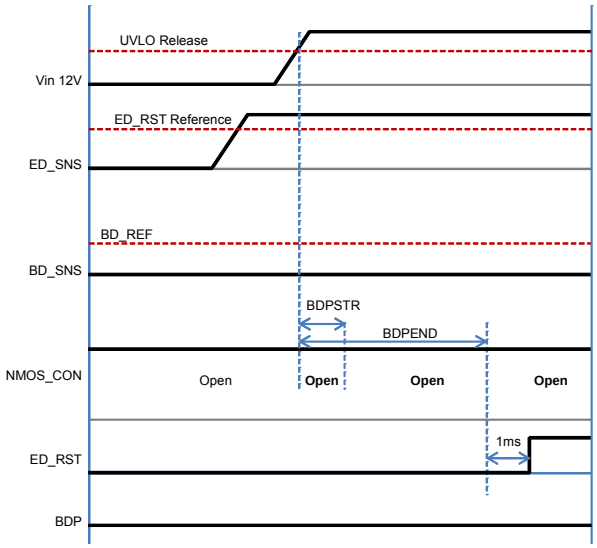
■ Power ON BDP Sequence @ On, normal case



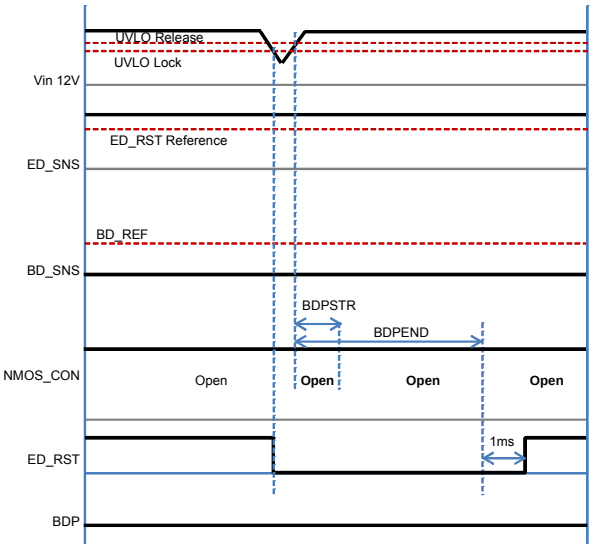
■ Power ON BDP Sequence @ On, BDP Detect case



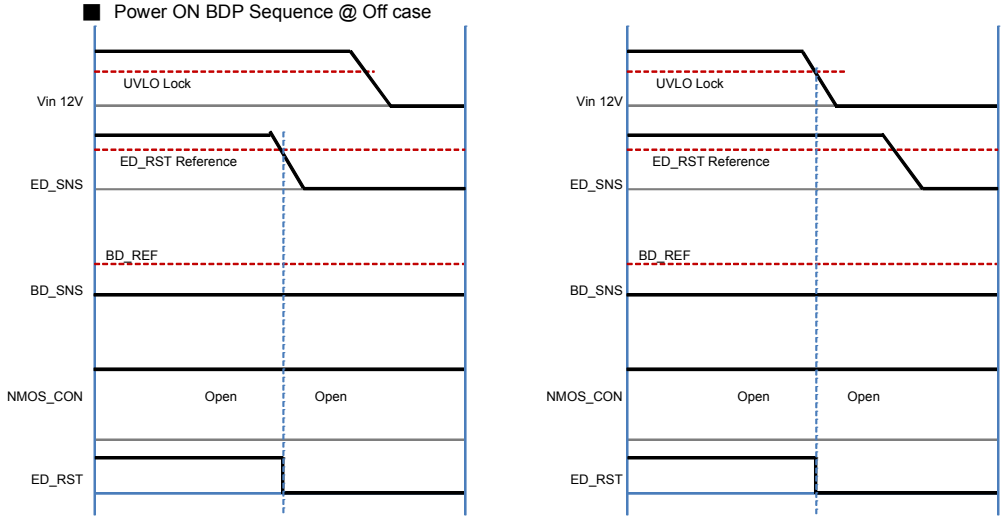
■ Power ON BDP Sequence @ Vin12V, EVDD 24V Sequence reverse



■ Power ON BDP Sequence @ Vin12V DIP



■ Power ON BDP Sequence @ Off case

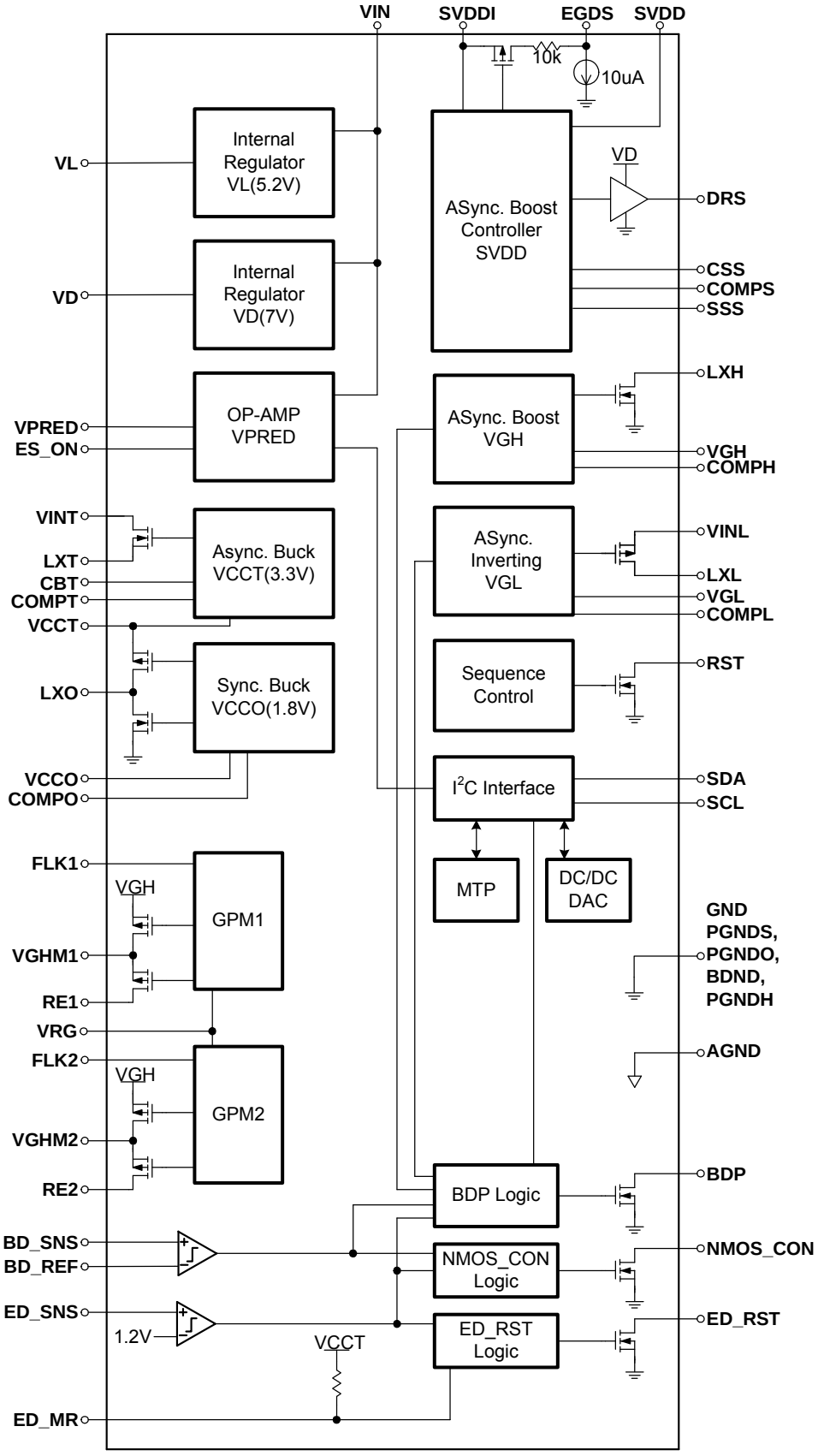


Functional Pin Description

Pin No	Pin Name	Pin Function
1	LXT	VCCT3.3 buck converter switching node.
2	CBT	VCCT3.3 buck converter bootstrap pin.
3	VINT	VCCT3.3 buck converter supply power.
4, 7, 50, 52	NC	No internal connection.
5	GND	Common ground.
6	COMPT1	VCCT3.3 buck converter compensation pin.
8	VCCT	VCCT3.3 buck converter output sensing and VCCO1.8 supply power.
9	PGNDO	VCCO1.8 buck converter power ground.
10	LXO	VCCO1.8 buck converter switching node.
11	VCCO	VCCO1.8 buck converter output sensing.
12	COMPO	VCCO1.8 buck converter compensation pin.
13	BGND	VPRED OP-AMP ground.
14	VPRED	VPRED OP-AMP output.
15	VIN	IC & VPRED OP-AMP supply power.
16	AGND	Analog ground.
17	VRG	GPM1/2 level setting pin DC level.
18	VL	Internal regulator output.
19	SDA	I2C data I/O.
20	SCL	I2C clock input.
21	FLK1	GPM1 control signal.
22	FLK2	GPM2 control signal.
23	RST	ASIC reset signal.
24	BDP	BDP output.
25	ES_ON	VPRED OP-AMP EN input.
26	BD_SNS	BDP sensing input.
27	BD_REF	BDP reference input.
28	NMOS_CON	NMOS control output.
29	ED_RST	EVDD reset output.
30	ED_MR	EVDD masking input.
31	ED_SNS	EVDD sensing input.
32	VD	Internal regulator output for SVDD external FET driver power.
33	PGNDS	SVDD MAIN FET power ground.
34	DRS	SVDD MAIN FET control pin.
35	SSS	SVDD soft-start control pin.

Pin No	Pin Name	Pin Function
36	COMPS	SVDD compensation pin.
37	CSS	SVDD MAIN FET current sensing pin.
38	COMPH	VGH boost converter compensation pin.
39	GND	Common ground.
40	EGDS	SVDD ISO FET control pin.
41	SVDDI	SVDD ISO FET input.
42	SVDD	SVDD ISO FET output sensing.
43	PGNDH	VGH Boost converter power ground.
44	LXH	VGH Boost converter switching node.
45	VGH	VGH Boost converter output sensing and GPM1,2 supply power.
46	VGHM2	GPM2 output.
47	RE2	GPM2 slope control pin.
48	VGHM1	GPM1 output.
49	RE1	GPM1 slope control pin.
51	COMPL	VGL compensation pin.
53	VINL	VGL inverting converter supply power.
54	GND	Common ground.
55	LXL	VGL inverting converter switching node.
56	VGL	VGL inverting converter output sensing.
57 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN, VINT, VINL, LXT to GND ---------- –0.3V to 19.5V
- VPRED to GND ---------- –0.3V to 16.5V
- SVDDI, SVDD, EGDS to GND ---------- –0.3V to 21V
- SVDDI to SVDD ---------- –0.3V to 18V
- CBT to GND ---------- –0.3V to (LXT+7V)
- VL, VCCT, VCCO, LXO, COMPT, COMPO, COMPS, COMPH, COMPL, SSS, VRG, BD_SNS, BD_REF, ED_SNS, ED_RST, ED_MR, SDA, SCL, FLK1, FLK2, RST, BDP, ES_ON, NMOS_CON to GND ---------- –0.3V to 6V
- VD, DRS, CSS to GND ---------- –0.3V to 7V
- VGH, LXH, VGHM1, RE1, VGHM2, RE2 to GND ---------- –0.3V to 36V
- VGL to GND ---------- –16V to +0.3V
- LXL to VINL ---------- –36V to +0.3V
- PGNDO, BGND, PGNDS, PGNDH, AGND to GND ---------- –0.3V to +0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-56L 7x7 ---------- 3.7W
- Package Thermal Resistance (Note 2)
  WQFN-56L 7x7, θ_{JA} ---------- 27°C/W
  WQFN-56L 7x7, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 9.6V to 15.4V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, GND = PGND = 0V, VCCT = 3.3V, VCCO = 1.8V, SVDD = 16.8V, VGH = 26V, VGL = –8V, VPRED = 6.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
Supply Voltage	V_{IN}		9.6	12	15.4	V
VIN Under Voltage Rising	V_{UVLO}	VIN rising	8.5	9	9.5	V
VIN Under Voltage Falling		VIN falling	7.5	8	8.5	V
VIN Over Voltage Protection	V_{IN_OVP}	VIN rising, hysteresis = 1.5V	18	18.5	19.5	V
IIN Quiescent Current	I_{QVIN}	V_{IN} = 12V, all converters switching and no loading	10	15	20	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VL Output Voltage	V_L		–5%	5.2	5%	V
VD Output Voltage	V_D		–5%	7	5%	V
Fault Detection						
Fault Trigger Duration			40	50	60	ms
Thermal Shutdown	OT	Temperature rising	--	150	--	°C
Thermal Shutdown Hysteresis	OT_Hys		--	30	--	°C
Open Drain Output (RST, BDP, ED_RST, NMOS_CON)						
RST, BDP, ED_RST Output Low Voltage		Open drain (3.3V I/F), sink 10mA	--	--	0.4	V
NMOS_CON Output Low Voltage		Open drain (3.3V I/F), sink 15mA	--	--	0.2	V
Power on RST Delay Time	t_{DLY6}	After VGH 100%. 2 bits. 4 steps.	1	--	7	ms
Logic Input (SDA, SCL, FLK1, FLK2, ES_ON, ED_MR)						
High-level Input Voltage	V_{IH}		1.3	--	--	V
Low-level Input Voltage	V_{IL}		--	--	0.8	V
Input Leakage Current		Except ED_MR (There is internal pull high resistor on ED_MR). SDA, SCL, FLK1, FLK2, ES_ON 0V or 3.3V	–2	0.01	2	µA
Input Capacitance		SDA, SCL	--	5	--	pF
SDA Output Low Voltage	V_{ACK}	I_{SDA} = 6mA	--	--	0.45	V
I^2C Timing Characteristics						
SCL Frequency	f_{SCL}		1	--	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3	--	--	µs
Hold Time (Repeated) START Condition	t_{HD_STA}		0.6	--	--	µs
SCL Pulse-Width Low	t_{LOW}		1.3	--	--	µs
SCL Pulse-Width High	t_{HIGH}		0.6	--	--	µs
Setup Time for a Repeated START Condition	t_{SU_STA}		0.6	--	--	µs
Data Hold Time	t_{HD_DAT}		0	--	800	ns
Data Setup Time	t_{SU_DAT}		100	--	--	ns
SDA and SCL Receiving Rising Time	t_R		20 + 0.1CB	--	300	ns
SDA and SCL Receiving Falling Time	t_F		20 + 0.1CB	--	300	ns
SDA Transmitting Fall Time	t_{FF}		20 + 0.1CB	--	250	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup Time for STOP Condition	t_{SU_STO}		0.6	--	--	μs
Bus Capacitance	CB		--	--	400	pF
Pulse width of Suppressed Spike	t_{SP}		--	85	--	ns
Internal Oscillator						
SVDD Switching Frequency	f_{OSC1}	2bits, 3 steps. 500kHz / 700kHz / 900kHz	−15%	700	15%	kHz
VGH Switching Frequency	f_{OSC2}	2bits, 4 steps. f_{OSC1} x 1 / f_{OSC1} x 1.33 / f_{OSC1} x 1.66/ f_{OSC1} x 2	−15%	f_{OSC1} x 1.33	15%	kHz
VGL Switching Frequency	f_{OSC3}	2bits, 4 steps. f_{OSC1} x 1 / f_{OSC1} x 1.33 / f_{OSC1} x 1.66/ f_{OSC1} x 2	−15%	f_{OSC1} x 1.33	15%	kHz
VCCT Switching Frequency	f_{OSC4}	1bits, 2 steps. f_{OSC1} x 1 / f_{OSC1} x 2	−15%	f_{OSC1} x 1	15%	kHz
VCCO Switching Frequency	f_{OSC5}	1bits, 2 steps. f_{OSC1} x 1 / f_{OSC1} x 2	−15%	f_{OSC1} x 2	15%	kHz
SVDD Boost Converter (SVDD)						
Output Voltage Range	V_{S_SVDD}	6 bits, 51 steps. SVDD > VIN + 2.5V	15	--	20	V
Output Regulation	S_{VDD}	No load, ±2% error, default output	−2	--	2	%
Output Resolution	Re_{so_SVDD}	6 bits, 51 steps. SVDD > VIN + 2.5V	--	0.1	--	V
Maximum Duty Cycle	D_{MAX_SVDD}		81	90	99	%
Load Regulation		0 < I_{LOAD} <1.5A	−1	--	1	%
Line Regulation		V_{IN} = 9.6V to 15.4V, I_{LOAD} = 1.5A	--	--	0.4	%/V
Short Circuit Protection	V_{SCP_SVDD}	SVDDI falling. After 10us, IC restarts. If IC restarts 3 times, IC shutdown.	15	20	25	%
Fault Trip Level	V_{FT_SVDD}	SVDD falling. After 50ms, IC shutdown.	60	65	75	%
Over-Voltage Protection	V_{OVP_SVDD}	SVDDI rising, hysteresis = 0.5V	20.5	21	22.5	V
SVDD–GND Discharging Resistance	R_{SVDD}	V_{IN} = 5V	--	4.7	--	kΩ
Soft-Start Charge Current	I_{SSS}		−20%	9.5	20%	μA
Soft-Start Period	t_{SS_SVDD}	SSS charges external capacitor 47nF from 0V to reference of SVDD.	0.5	5	20	ms
Power on SVDD Delay time		After VGL 100%	0.5	2	8	ms
External N-MOSFET Gate Driver (DRS of SVDD)						
DRS High Voltage	D_{RS_OH}		4	7	9	V
DRS Low Voltage	D_{RS_OL}		--	--	0.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
External NMOS Switch Current Limit	V_{CSS_OCP}	1 bit, 2 steps. 0.2V/0.4V	–20%	0.2	20%	V
DRS to VD High-Side On-Resistance	R_{DSON_DRSH}		1	3	7	Ω
DRS to GND Low-Side On-Resistance	R_{DSON_DRSL}		1	3	7	Ω
External Isolation P-MOSFET Switch (EGDS of SVDD)						
EGDS Output High Voltage			--	SVDDI	--	V
EGDS Output Low Voltage			--	SVDDI – 5.8	--	V
EGDS Gate Pull High Resistor			--	12	--	kΩ
EGDS Gate Sink Current	I_{EGDS_SINK}		4	10	20	μA
EGDS Soft Start time	t_{SS_EXTGD}	When external isolation MOSFET Cgs = 47nF	--	20	--	ms
VGH Boost Converter (VGH)						
Output Voltage Range	V_{S_VGH}	5 bits, 21 steps.	22	--	32	V
Output Regulation	V_{GH}	No load, ±3% error, default output	–3	--	3	%
Output Resolution	Reso_VGH	5 bits, 21 steps.	--	0.5	--	V
Maximum Duty Cycle	D_{MAX_VGH}		81	90	99	%
Minimum On-Time	t_{MOT_VGH}		10	100	160	ns
Load Regulation		$0 < I_{LOAD} < 0.1A$.	–1	--	1	%
Line Regulation		SVDD = 15V to 20V (I_{LOAD} = 0.1A)	--	--	0.4	%/V
LXH Current Limit			1.5	2	--	A
LXH Current Limit for BDP		Based on SVDD = 16V, V_{GH} = 27V, inductor = 10uH, F_{OSC2} = 1.4MHz, I_{LOAD} = 200mA / 300mA / 400mA / 500mA, BDP can be set I_{LXH} to detect 600mA / 750mA / 900mA / 1050mA	600	--	1050	mA
LXH Current Limit for BDP Resolution		2bits, 4 steps	--	150	--	mA
Short Circuit Protection	VS_{CP_VGH}	VGH falling. After 10μs, IC restarts. If IC restarts 3 times, IC shutdown.	15	20	25	%
Fault Trip Level	VF_{T_VGH}	VGH falling. After 50ms, IC shutdown.	60	65	70	%
Over-Voltage Protection	V_{OVP_VGH}	VGH rising, hysteresis = 1.5V	34	35	36	V
LXH On-Resistance	R_{DSON_LXH}	I_{LXH} = 100mA	300	500	700	mΩ
LXH Leakage Current	I_{LK_LXH}	V_{LXH} = 32V	--	--	10	μA
VGH–GND Discharging Resistance	R_{VGH}	V_{IN} = 5V	3	4.7	6	kΩ
Soft-Start Period	t_{SS_VGH}	From SVDD to VGH	2	5	8	ms
Power on VGH Delay time		After (SVDDI – EGDS) > 4.5V	0.5	2	7	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ASync. Inverting Converter (VGL)						
Output Voltage Range	V_{S_VGL}	5 bits, 19 steps	–13	--	-4	V
Output Regulation	V_{GL}	No load, ±3% error, default output	–3	--	3	%
Output Resolution	Reso_VGL	5 bits, 19 steps	--	0.5	--	V
Maximum Duty Cycle	D_{MAX_VGL}		81	90	99	%
Load Regulation		1mA < I_{LOAD} < 0.1A	–1	--	1	%
Line Regulation		V_{INL} = 9.6V to 15.4V , I_{LOAD} = 0.1A	–1	--	1	%
LXL Positive Current Limit			1.5	2	--	A
LXL Positive Current Limit for BDP		Based on V_{INL} = 12V, V_{GL} = -6V, inductor = 10uH, F_{OSC3} = 1.4MHz, I_{LOAD} = 200mA / 300mA / 400mA / 500mA, BDP can be set I_{LXL} to detect 450mA / 600mA / 750mA / 900mA	450	--	900	mA
LXL Positive Current Limit for BDP Resolution		2bits, 4 steps	--	150	--	mA
Short Circuit Protection	V_{SCP_VGL}	VGL rising. After 10us, IC restarts. If IC restarts 3 times, IC shutdown.	–1.6	–1.3	–1	V
Fault Trip Level	V_{FT_VGL}	VGL rising. After 50ms, IC shutdown.	63	70	77	%
Over-Voltage Protection	V_{OVP_VGL}	VGL falling. Hysteresis = 0.5V	–16	–14	–13.5	V
LXL High Side On-Resistance	R_{DSON_LXH}	I_{LXL} = 100mA	300	550	800	mΩ
LXL Leakage current High	I_{LK_LXLH}	V_{INL} = 12V,V_{LXL} = VGL	--	--	10	μA
LXL Leakage current Low	I_{LK_LXLL}	V_{INL} = 12V,V_{LXL} = 12V	--	--	10	μA
VGL–GND Discharging Resistance	R_{VGL}	V_{IN} = 5V	3	4.7	6.5	kΩ
Soft-Start Period	t_{SS_VGL}		2	5	8	ms
Power on VGL Delay Time	t_{DLY4}	After VCCO 100%+2ms. 2 bits. 4 steps.	1	--	7	ms
ASync. Buck Converter (VCCT)						
Output Voltage Range	V_{S_VCCT}	3 bits, 7 steps	3	--	3.6	V
Output Regulation	V_{CCT}	No load, ±3% error, default output	–3	--	3	%
Output Resolution	Reso_VCCT	3 bits, 7 steps	--	0.1	--	V
Maximum Duty Cycle	D_{MAX_VCCT}		81	90	99	%
Load Regulation		0 < I_{LOAD} < 1A	–1	--	1	%
Line Regulation		V_{INT} = 9.6V to 15.4V , (I_{LOAD} = 0.4A)	–1	--	1	%
LXT Positive Current Limit			2	2.5	--	A
Short Circuit Protection	V_{SCP_VCCT}	VCCT falling. After 10μs, IC restarts. If IC restarts 3 times, IC shutdown.	15	20	25	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Fault Trip Level	V_{FT_VCCT}	VCCT falling. After 50ms, IC shutdown.	60	65	70	%
Over-Voltage Protection	V_{OVP_VCCT}	VCCT rising , hysteresis = 0.1 x VCCT	115	120	125	%
LXT High Side On-Resistance	R_{DSON_LXTH}	I_{LXT} = 100mA	100	150	200	mΩ
LXT Leakage current High	I_{LK_LXTH}	V_{INT} = 12V, V_{LXT} = GND (C_{BT} = LXT)	--	--	10	μA
LXT Leakage current Low	I_{LK_LXTL}	V_{LXT} = 12V (C_{BT} = LXT)	--	--	10	μA
VCCT–GND Discharging Resistance	R_{VCCT}	V_{IN} = 5V	1.5	2.5	3.5	kΩ
Soft-Start Period	t_{SS_VCCT}		0.3	1	3	ms
Power on VCCT Delay Time	t_{DLY1}	After VIN UVLO + 1ms. 2 bits. 4 steps.	1	--	7	ms
Sync. Buck Converter (VCCO)						
Output Voltage Range	V_{S_VCCO}	4 bits, 14 steps. While VCCO is set to 2.8V, VCCT must be set larger than 3.3V.	1.5	--	2.8	V
Output Regulation	V_{CCO}	No load, ±2% error, default output	–2	--	2	%
Output Resolution	Reso_VCCO	4 bits, 14 steps	--	0.1	--	V
Load Regulation		0 < I_{LOAD} < 0.5A	–1	--	1	%
Line Regulation		V_{CCT} = 3V to 3.6V , (I_{LOAD} = 0.4A)	–1	--	1	%
LXO Positive Current Limit			1.5	2	--	A
Short Circuit Protection	V_{SCP_VCCO}	VCCO falling. After 10μs, IC restarts. If IC restarts 3 times, IC shutdown.	15	20	25	%
Fault Trip Level	V_{FT_VCCO}	VCCO falling. After 50ms, IC shutdown.	55	65	75	%
Over-Voltage Protection	V_{OVP_VCCO}	VCCO rising , hysteresis = 0.1 x VCCO	110	120	130	%
LXO High Side On-Resistance	R_{DSON_LXOH}	I_{LXO} = 200mA	50	120	170	mΩ
LXO Low Side On-Resistance	R_{DSON_LXOL}	I_{LXO} = 200mA	50	120	170	mΩ
LXO Leakage current High	I_{LK_LXOH}	V_{INT} = 12V, V_{CCT} = 3.3V, V_{LXO} = GND	--	--	10	μA
LXO Leakage current Low	I_{LK_LXOL}	V_{INT} = 12V, V_{CCT} = 3.3V, V_{LXO} = 3.3V	--	--	10	μA
VCCO–GND Discharging Resistance	R_{VCCO}	V_{IN} = 5V	1.5	2.5	3.5	kΩ
Soft-Start Period	t_{SS_VCCO}		0.3	1	3	ms
Power on VCCO Delay Time	t_{DLY3}	After VCCT 100%. 2 bits. 4 steps.	1	--	7	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OP-Amp (VPRED)						
Output Voltage Range	V_{S_VPRED}	3 bits, 8 steps	3	--	6.5	V
Output Regulation	V_{PRED}	No load, +-2% error, default output	–2	--	2	%
Output Resolution	Reso_VPRED	3 bits, 8 steps	--	0.5	--	V
Short-Circuit Current	I_{VPRED_SC}		--	±300	--	mA
Short Circuit Protection	V_{SCP_VPRED}	VPRED falling. After 10μs, IC restarts. If IC restarts 3 times, IC shutdown.	15	20	25	%
Slew Rate	S_{R_VPRED}		--	30	--	V/us
Gate Pulse Modulation (GPM1, GPM2)						
Adjustable GPM Stop Voltage Level			--	10xVRG	--	V
VGH-GPMx On-Resistance	R_{DSON_GPMH}	V_{GH} = 27V/-20mA at F_{LKx} = High	1.5	2.5	3.75	Ω
GPMx-REx On-Resistance	R_{DSON_GPML}	V_{GH} = 27V/+20mA at F_{LKx} = Low	1.5	2.5	3.75	Ω
FLK Frequency			--	--	400	kHz
FLKx to GPMx Rising Propagation Delay	t_{PGPMLH}		--	100	200	ns
FLKx to GPMx Falling Propagation Delay	t_{PGPMHL}		--	100	450	ns
External REx-GND Resistance			80	--	--	Ω
EVDD Voltage Detector						
Reference Voltage of EVDD	V_{ED_REF}		–5%	1.2V	5%	V
EVDD Comparator Hysteresis		ED_SNS falling	--	100	--	mV
ED_MR Pull High Resistance	R_{ED_MR}	Pull high to VCCT	7	10	13	kΩ
BDP Comparator						
BDP_REF Range of BDP Comparator		BDP_REF	1	--	4	V
BDP Comparator Hysteresis		While BDP_REF = 2.5V, BDP_SNS falling hysteresis	30	100	250	mV

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

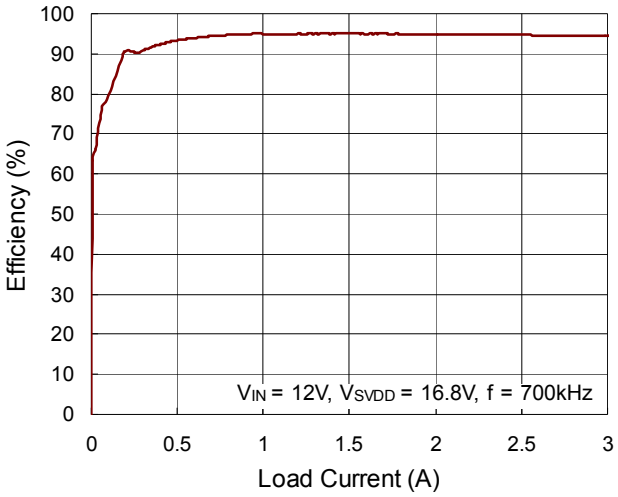
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

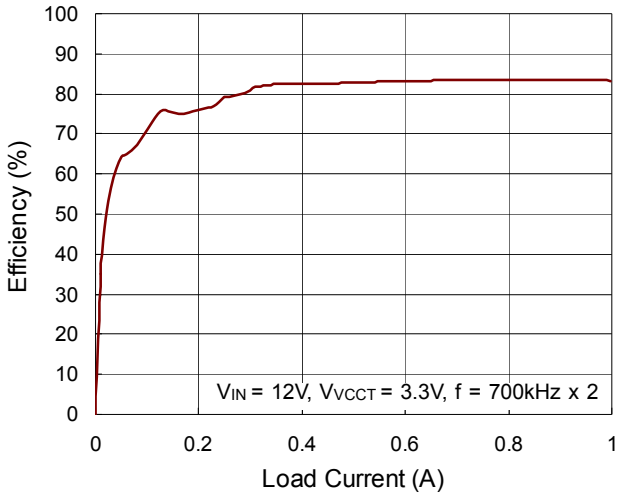
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

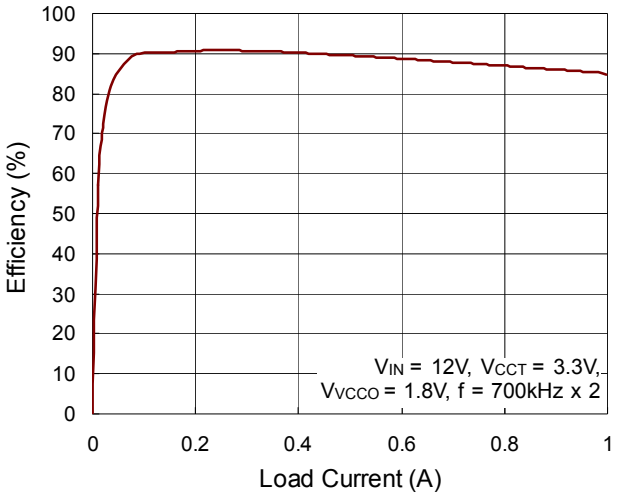
SVDD Efficiency vs. Load Current



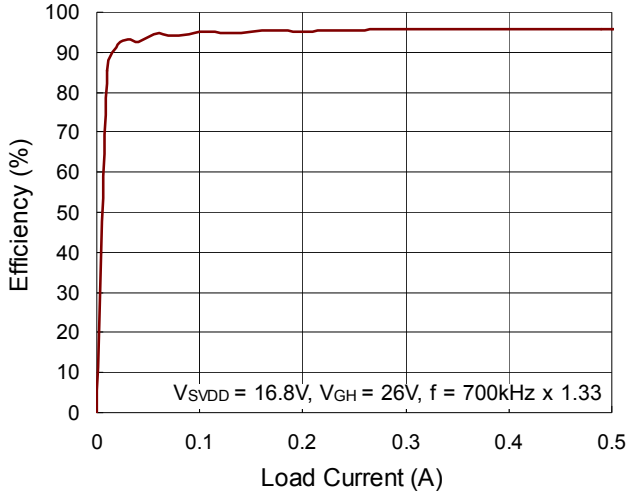
VCCT Efficiency vs. Load Current



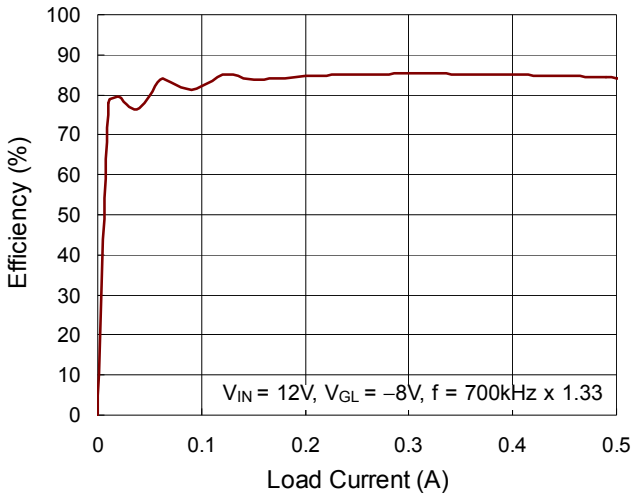
VCCO Efficiency vs. Load Current



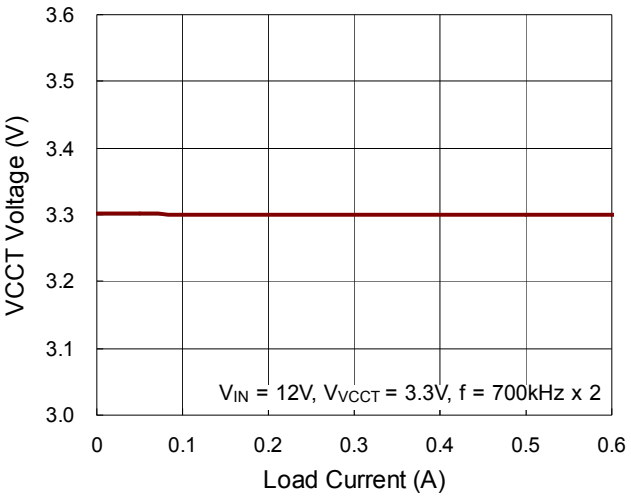
VGH Efficiency vs. Load Current



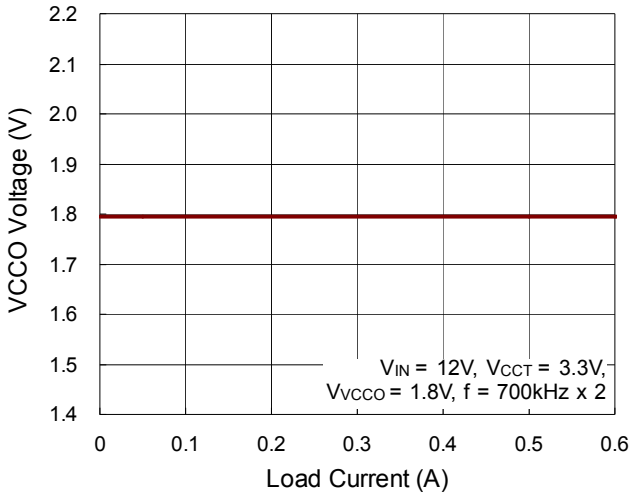
VGL Efficiency vs. Load Current



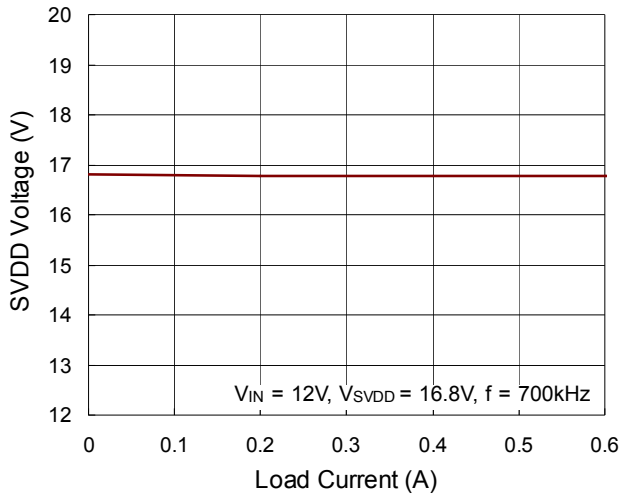
VCCT Voltage vs. Load Current



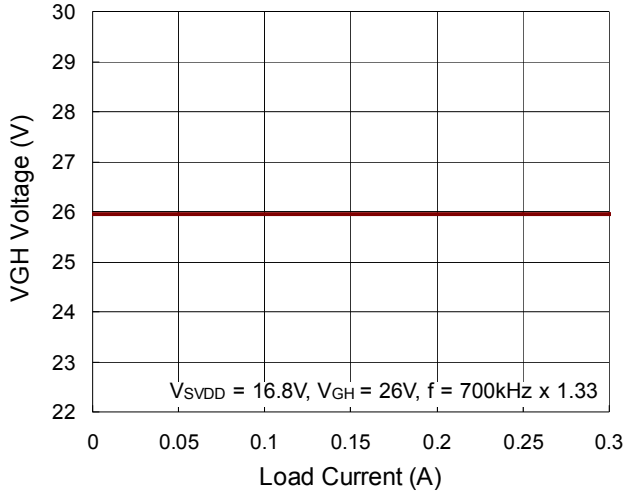
VCCO Voltage vs. Load Current



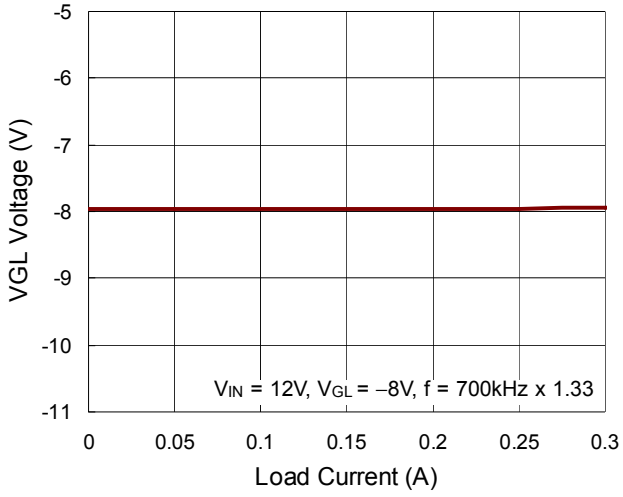
SVDD Voltage vs. Load Current



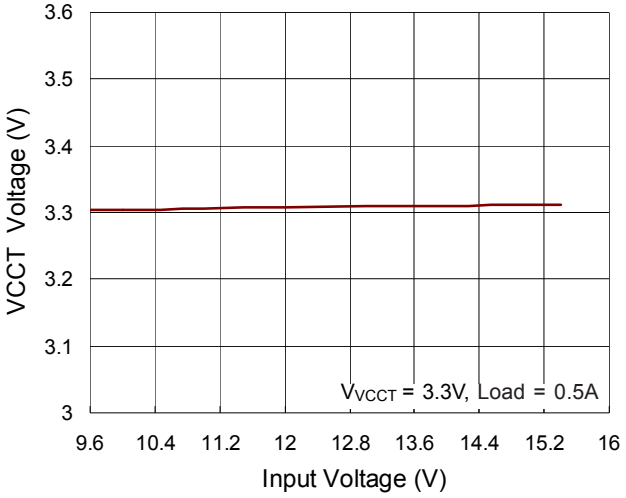
VGH Voltage vs. Load Current



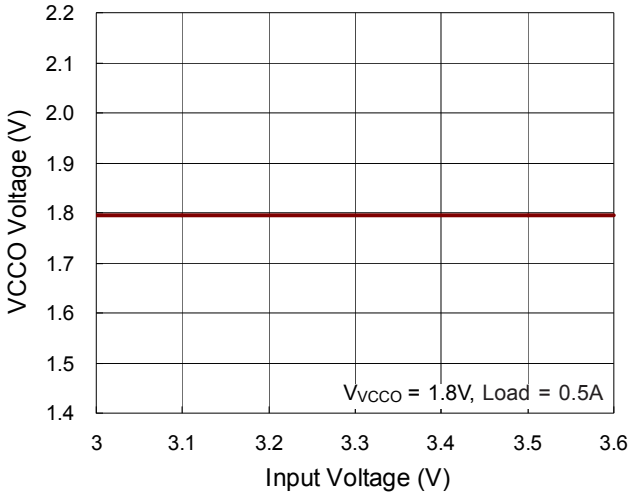
VGL Voltage vs. Load Current



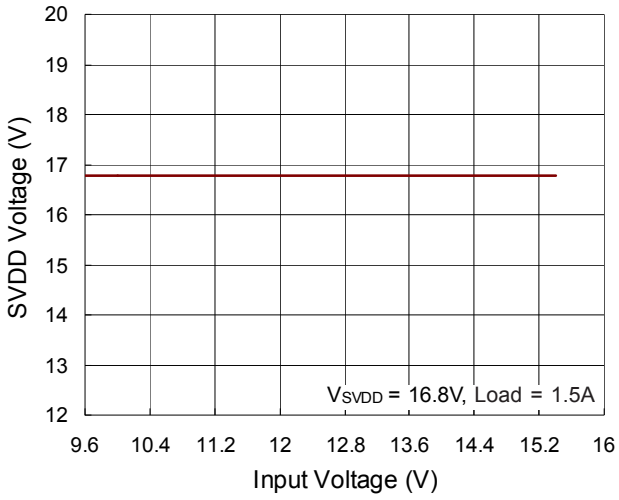
VCCT Voltage vs. Input Voltage



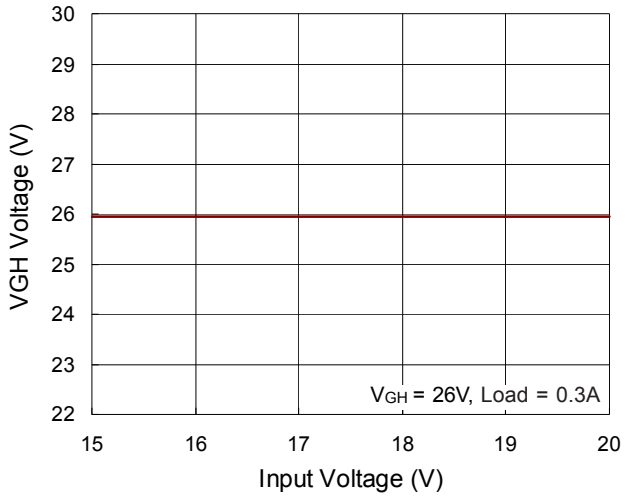
VCCO Voltage vs. Input Voltage



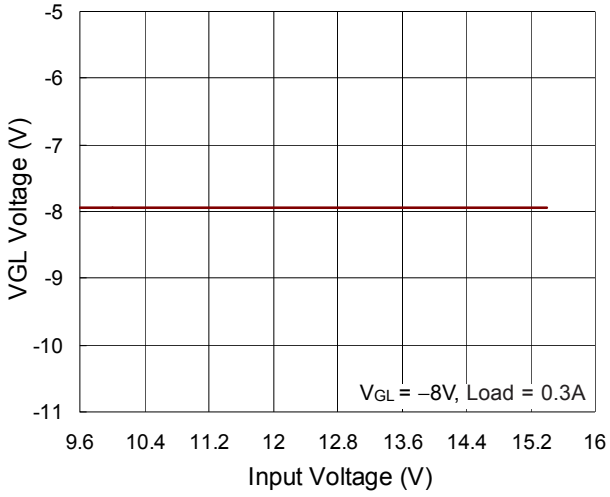
SVDD Voltage vs. Input Voltage



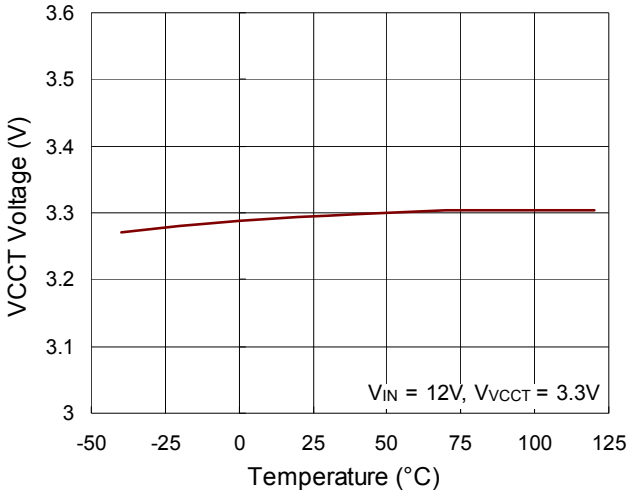
VGH Voltage vs. Input Voltage



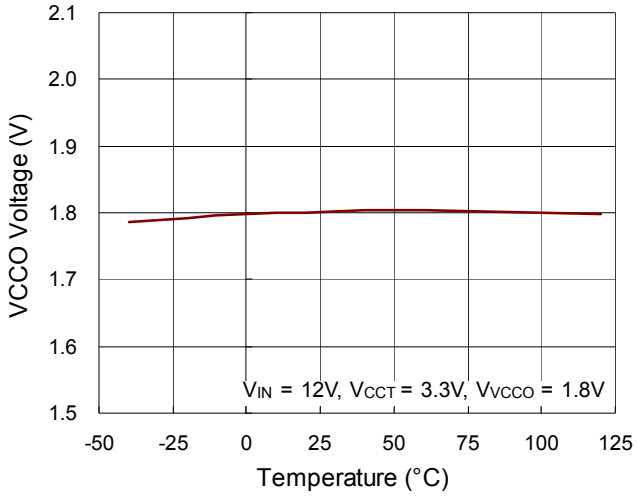
VGL Voltage vs. Input Voltage



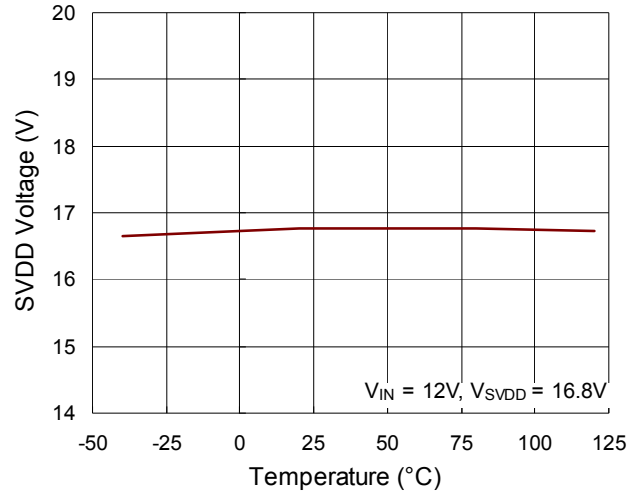
VCCT Voltage vs. Temperature



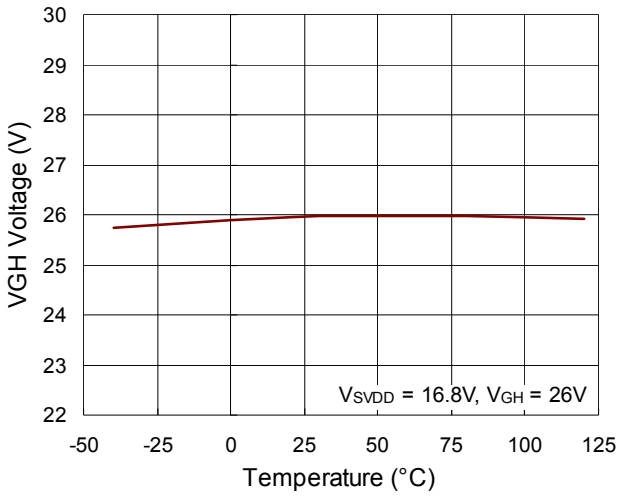
VCCO Voltage vs. Temperature



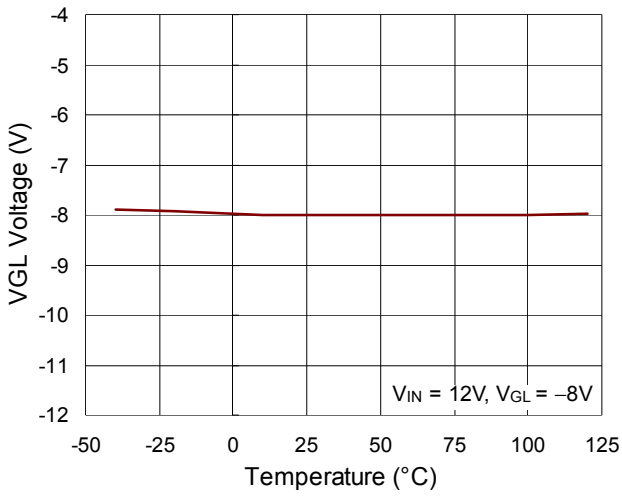
SVDD Voltage vs. Temperature



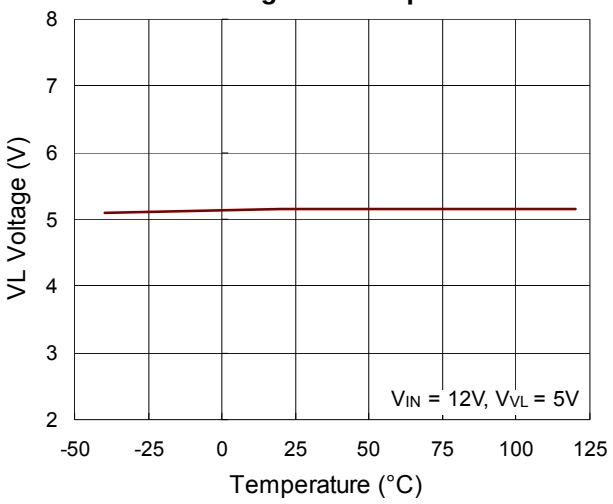
VGH Voltage vs. Temperature



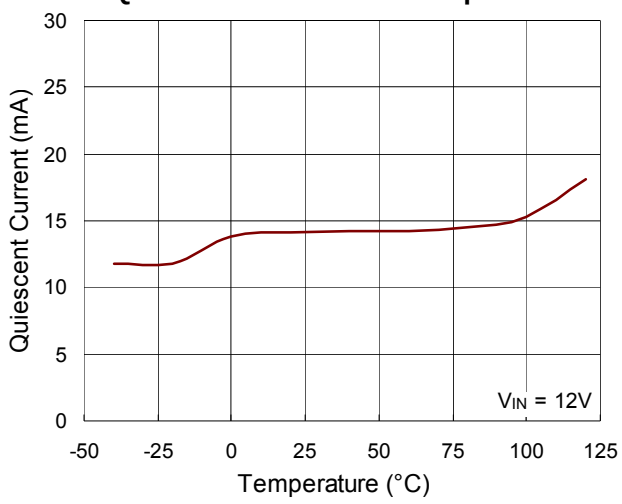
VGL Voltage vs. Temperature



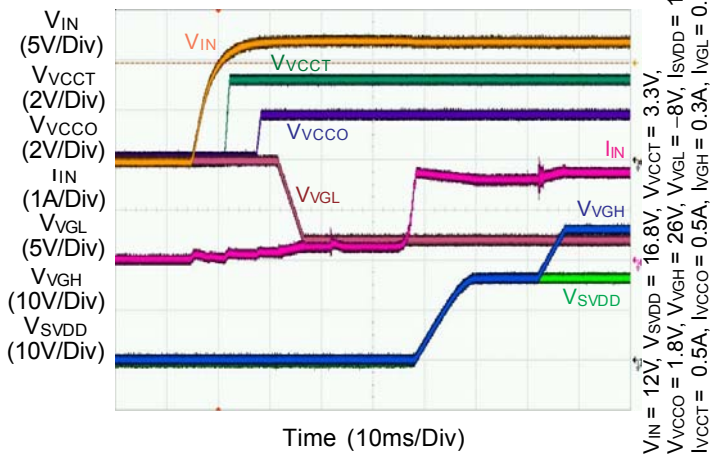
VL Voltage vs. Temperature



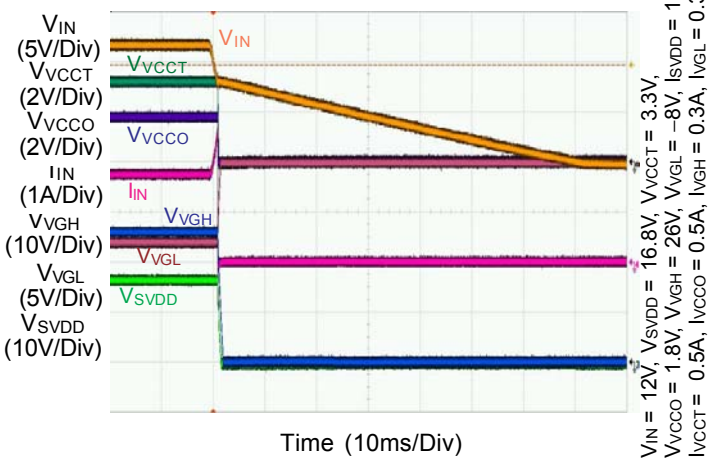
Quiescent Current vs. Temperature



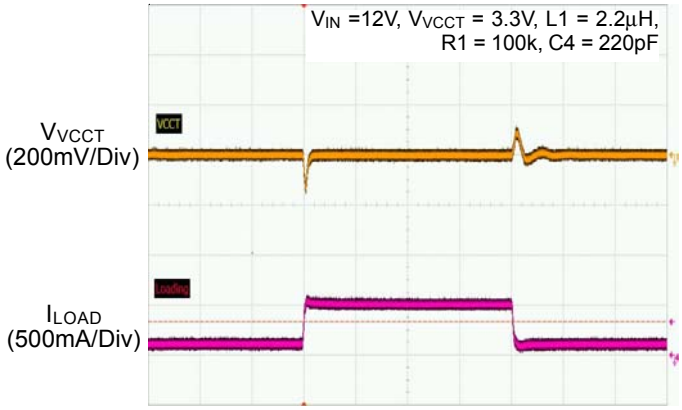
Power On



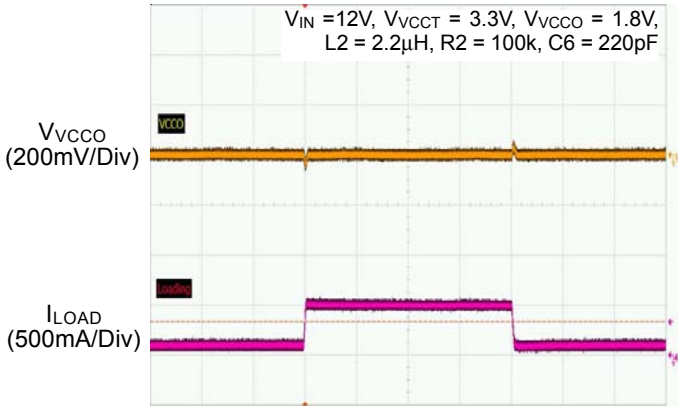
Power Off



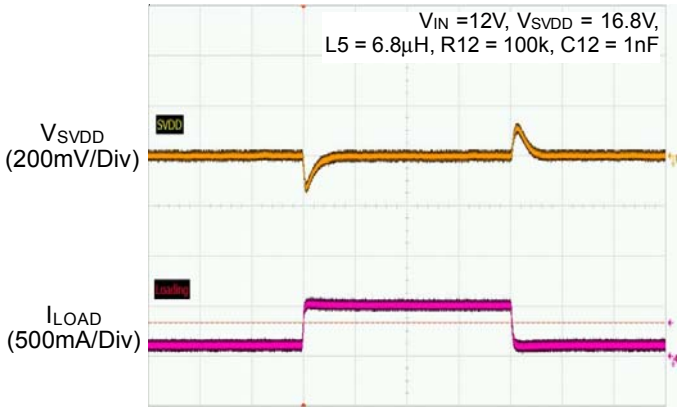
VCCT Load Transient



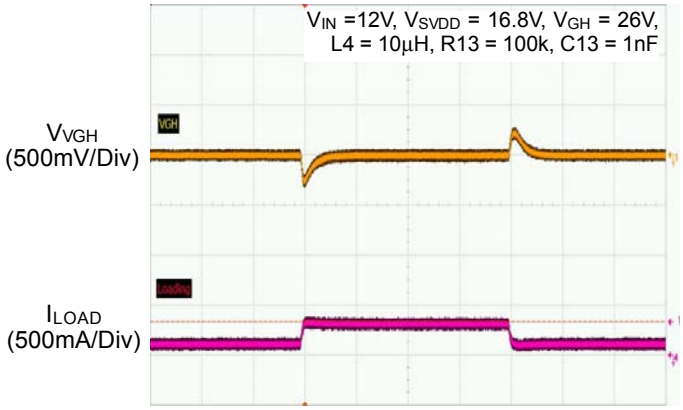
VCCO Load Transient



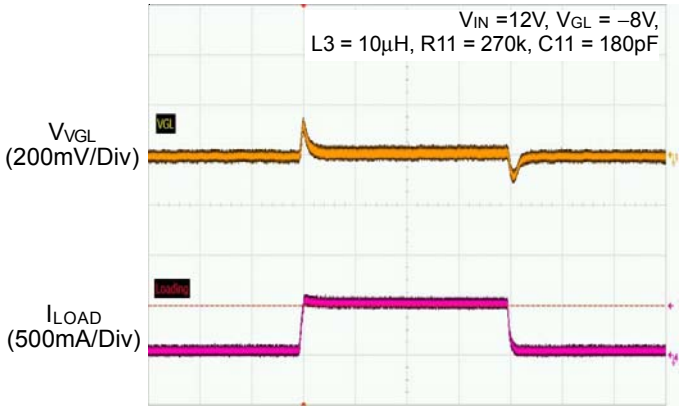
SVDD Load Transient



VGH Load Transient



VGL Load Transient



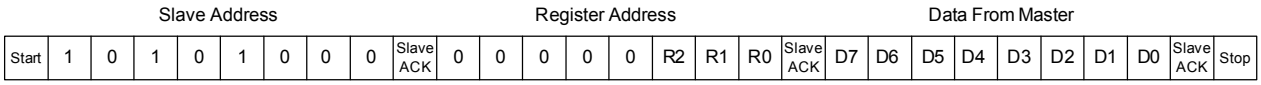
I²C Command

Slave Address (PMIC)

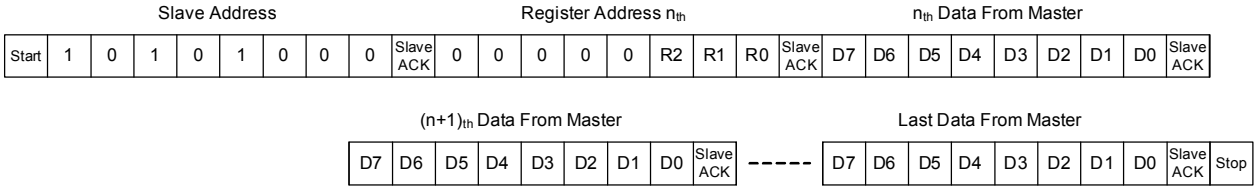
7	6	5	4	3	2	1	0 = LSB
1	0	1	0	1	0	0	R/$\overline{W}$

Write Command

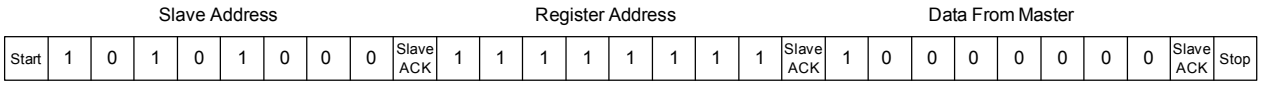
(a) Write single byte of data to Register



(b) Write multiple bytes of data to Registers

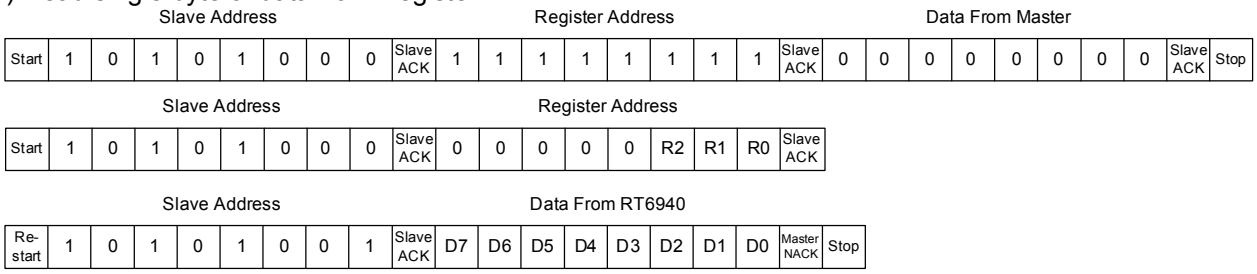


(c) Write All Registers into EEPROM

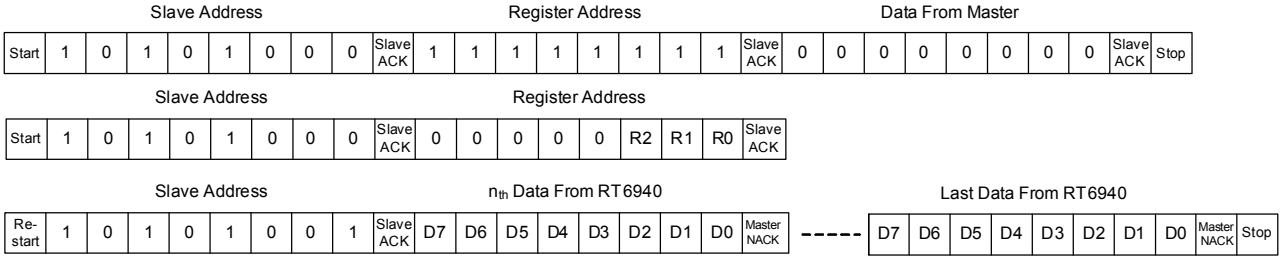


Read Command

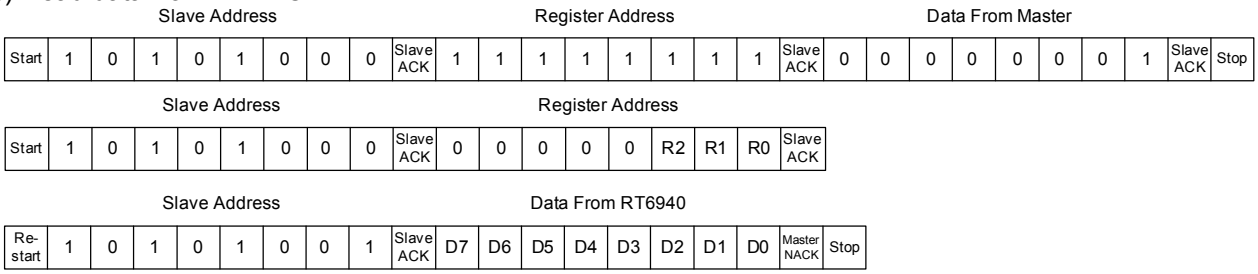
(a) Read single byte of data from Register



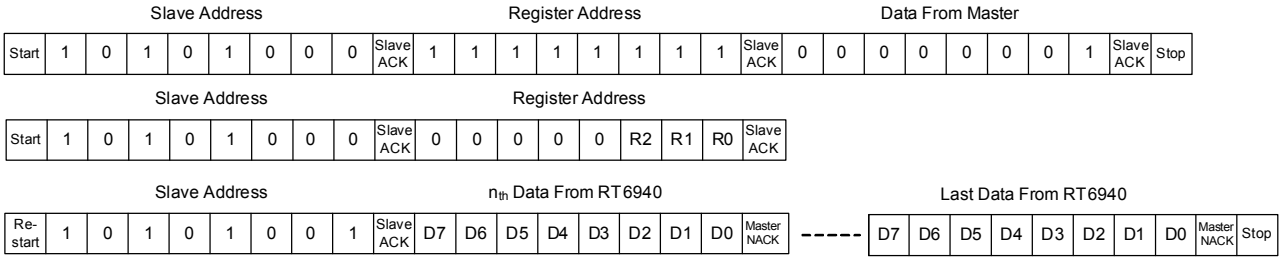
(b) Read multiple bytes of data from Registers



(c) Read data from EEPROM



(d) Read multiple bytes of data from EEPROM



Register Map

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
SVDD_CS	SVDD Current Sense	0x00h	1bit Nonvolatile	52h	0	X	X	X	X	X	X	X
COMP OFF	BDP COMP ON/OFF		1bit Nonvolatile		X	1	X	X	X	X	X	X
SVDD	SVDD Output		6bit Nonvolatile		X	X	0	1	0	0	1	0
T1	T1 Delay Time	0x01h	2bit Nonvolatile	08h	0	0	X	X	X	X	X	X
T3	T3 Delay Time		2bit Nonvolatile		X	X	X	X	1	0	X	X
T4	T4 Delay Time		2bit Nonvolatile		X	X	X	X	X	X	0	0
T6	T6 Delay Time	0x02h	2bit Nonvolatile	15h	0	0	X	X	X	X	X	X
FREQ	SVDD SW Frequency		2bit Nonvolatile		X	X	0	1	X	X	X	X
FREQH	VGH SW Frequency		2bit Nonvolatile		X	X	X	X	0	1	X	X
FREQL	VGL SW Frequency		2bit Nonvolatile		X	X	X	X	X	X	0	1
DSC_On_Off	Channel Discharge Enable	0x03h	5bit Nonvolatile	FFh	1	1	1	1	1	X	X	X
FREQVCCO	VCCO SW Frequency		1bit Nonvolatile		X	X	X	X	X	1	X	X
FREQVCCT	VCCT SW Frequency		1bit Nonvolatile		X	X	X	X	X	X	1	X
OP-Amp_OFF	VPRED Enable		1bit Nonvolatile		X	X	X	X	X	X	X	1
VCCO1.8	VCCO Output	0x04h	4bit Nonvolatile	37h	0	0	1	1	X	X	X	X
VCCT3.3	VCCT Output		3bit Nonvolatile		X	X	X	X	0	1	1	X
VGHVGL BDP OFF	VGHVGL BDP ON/OFF		1bit Nonvolatile		X	X	X	X	X	X	X	1
VPRED	VPRED Output	0x05h	3bit Nonvolatile	FAh	1	1	1	X	X	X	X	X
VPRED_Mode	VPRED Mode Select		1bit Nonvolatile		X	X	X	1	X	X	X	X
VGL_BDP	VGL_BDP Level		2bit Nonvolatile		X	X	X	X	1	0	X	X
VGH_BDP	VGH_BDP Level		2bit Nonvolatile		X	X	X	X	X	X	1	0

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
BDP_STR	BDP Start Delay Time	0x06h	3bit Nonvolatile	28h	0	0	1	X	X	X	X	X
VGH	VGH Output		5bit Nonvolatile		X	X	X	0	1	0	0	0
BDP_END	BDP End Delay Time	0x07h	3bit Nonvolatile	A8h	1	0	1	X	X	X	X	X
VGL	VGL Output		5bit Nonvolatile		X	X	X	0	1	0	0	0
CR	Control Register	0xFFh	Volatile	--	WED	X	X	X	X	X	X	EE (DR)

Note : CR Data
00h : Read data from DAC register (DR).
01h : Read data from EEPROM.
80h : Write all DAC register (DR) into EEPROM.

Output Table

Register Code	SVDD	VGH	VGL	VCCT	VCCO	VPRED
00h	15	22	-4	3	1.5	3
01h	15.1	22.5	-4.5	3.1	1.6	3.5
02h	15.2	23	-5	3.2	1.7	4
03h	15.3	23.5	-5.5	3.3	1.8	4.5
04h	15.4	24	-6	3.4	1.9	5
05h	15.5	24.5	-6.5	3.5	2	5.5
06h	15.6	25	-7	3.6	2.1	6
07h	15.7	25.5	-7.5		2.2	6.5
08h	15.8	26	-8		2.3	
09h	15.9	26.5	-8.5		2.4	
0Ah	16	27	-9		2.5	
0Bh	16.1	27.5	-9.5		2.6	
0Ch	16.2	28	-10		2.7	
0Dh	16.3	28.5	-10.5		2.8	
0Eh	16.4	29	-11			
0Fh	16.5	29.5	-11.5			
10h	16.6	30	-12			
11h	16.7	30.5	-12.5			
12h	16.8	31	-13			
13h	16.9	31.5				
14h	17	32				
15h	17.1					
16h	17.2					
17h	17.3					
18h	17.4					
19h	17.5					
1Ah	17.6					
1Bh	17.7					
1Ch	17.8					
1Dh	17.9					
1Eh	18					
1Fh	18.1					

Register Code	SVDD	VGH	VGL	VCCT	VCCO	VPRED
20h	18.2					
21h	18.3					
22h	18.4					
23h	18.5					
24h	18.6					
25h	18.7					
26h	18.8					
27h	18.9					
28h	19					
29h	19.1					
2Ah	19.2					
2Bh	19.3					
2Ch	19.4					
2Dh	19.5					
2Eh	19.6					
2Fh	19.7					
30h	19.8					
31h	19.9					
32h	20					
33h						
34h						
35h						
36h						
37h						
38h						
39h						
3Ah						
3Bh						
3Ch						
3Dh						
3Eh						
3Fh						

Address : 00

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
SVDD_CS	SVDD Current Sense	0x00h	1bit Nonvolatile	52h	0	X	X	X	X	X	X	X
COMP OFF	BDP COMP ON/OFF		1bit Nonvolatile		X	1	X	X	X	X	X	X
SVDD	SVDD Output		6bit Nonvolatile		X	X	0	1	0	0	1	0

SVDD Current Sense Setting

00h x <7>	
→ Data	Function
0	0.2
1	0.4

BDP COMP ON/OFF Setting

00h x <6>	
→ Data	Function
0	OFF
1	ON

Address : 01

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
T1	T1 Delay Time	0x01h	2bit Nonvolatile	08h	0	0	X	X	X	X	X	X
T3	T3 Delay Time		2bit Nonvolatile		X	X	X	X	1	0	X	X
T4	T4 Delay Time		2bit Nonvolatile		X	X	X	X	X	X	0	0

T1 Delay Time Setting

01h x <7:6>	
→ Data	Function
0	1ms
1	3ms
2	5ms
3	7ms

T4 Delay Time Setting

01h x <1:0>	
→ Data	Function
0	1ms
1	3ms
2	5ms
3	7ms

T3 Delay Time Setting

01h x <3:2>	
→ Data	Function
0	1ms
1	3ms
2	5ms
3	7ms

Address : 02

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
T6	T6 Delay Time	0x02h	2bit Nonvolatile	15h	0	0	X	X	X	X	X	X
FREQ	SVDD SW Frequency		2bit Nonvolatile		X	X	0	1	X	X	X	X
FREQH	VGH SW Frequency		2bit Nonvolatile		X	X	X	X	0	1	X	X
FREQL	VGL SW Frequency		2bit Nonvolatile		X	X	X	X	X	X	0	1

T6 Delay Time Setting

02h x <7:6>	
→ Data	Function
0	1ms
1	3ms
2	5ms
3	7ms

SVDD SW Frequency Setting

02h x <5:4>	
→ Data	Switching Frequency
0	500KHz
1	700KHz
2	900KHz
3	900KHz

VGH SW Frequency Setting

02h x <3:2>	
→ Data	Switching Frequency
0	SVDD Frequency *1
1	SVDD Frequency *1.33
2	SVDD Frequency *1.66
3	SVDD Frequency *2

VGL SW Frequency Setting

02h x <1:0>	
→ Data	Switching Frequency
0	SVDD Frequency *1
1	SVDD Frequency *1.33
2	SVDD Frequency *1.66
3	SVDD Frequency *2

Address : 03

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
DSC_On_Off	Channel Discharge Enable	0x03h	5bit Nonvolatile	FFh	1	1	1	1	1	X	X	X
FREQVCCO	VCCO SW Frequency		1bit Nonvolatile		X	X	X	X	X	1	X	X
FREQVCCT	VCCT SW Frequency		1bit Nonvolatile		X	X	X	X	X	X	1	X
OP-Amp_OFF	VPRED Enable		1bit Nonvolatile		X	X	X	X	X	X	X	1

Channels Discharge Enable (Low:No Discharge, High:Dicharge) Setting

03h x <7:3>	
→ Data	Function
0	ALL_OFF
1	SVDD
2	VGH
4	VGL
8	VCCT
16	VCCO

VCCO SW Frequency Setting

03h x <2>	
→ Data	Function
0	SVDD Frequency *1
1	SVDD Frequency *2

VCCT SW Frequency Setting

03h x <1>	
→ Data	Function
0	SVDD Frequency *1
1	SVDD Frequency *2

VPRED Enable Setting

03h x <0>	
→ Data	Function
0	OFF
1	ON

Address : 04

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
VCCO1.8	VCCO Output	0x04h	4bit Nonvolatile	37h	0	0	1	1	X	X	X	X
VCCT3.3	VCCT Output		3bit Nonvolatile		X	X	X	X	0	1	1	X
VGHVGL BDP OFF	VGHVGL BDP ON/OFF		1bit Nonvolatile		X	X	X	X	X	X	X	1

VGHVGL BDP ON/OFF Setting

04h x <0>	
→ Data	Function
0	OFF
1	ON

Address : 05

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
VPRED	VPRED Output	0x05h	3bit Nonvolatile	FAh	1	1	1	X	X	X	X	X
VPRED_Mode	VPRED Mode Select		1bit Nonvolatile		X	X	X	1	X	X	X	X
VGL_BDP	VGL BDP Level		2bit Nonvolatile		X	X	X	X	1	0	X	X
VGH_BDP	VGH BDP Level		2bit Nonvolatile		X	X	X	X	X	X	1	0

VPRED Mode Select

05h x <4>	
→ Data	Function
0	CASE1
1	CASE2

VGL BDP Level Setting

05h x <3:2>	
→ Data	Function
0	450mA
1	600mA
2	750mA
3	900mA

VGH BDP Level Setting

05h x <1:0>	
→ Data	Slew Rate
0	600mA
1	750mA
2	900mA
3	1050mA

Address : 06

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
BDP_STR	BDP Start Delay Time	0x06h	3bit Nonvolatile	28h	0	0	1	X	X	X	X	X
VGH	VGH Output		5bit Nonvolatile		X	X	X	0	1	0	0	0

BDP Start Delay Time Setting

06h x <7:5>	
→ Data	Function
0	0ms
1	10ms
2	20ms
3	30ms
4	40ms
5	50ms
6	50ms
7	50ms

Address : 07

Name	Function	Address	Volatile/ Nonvolatile	Factor (Power-Up Default)	MSB							LSB
BDP_END	BDP End Delay Time	0x07h	3bit Nonvolatile	A8h	1	0	1	X	X	X	X	X
VGL	VGL Output		5bit Nonvolatile		X	X	X	0	1	0	0	0

BDP End Delay Setting

07h x <7:5>	
→ Data	Function
0	0ms
1	45ms
2	75ms
3	120ms
4	150ms
5	300ms
6	300ms
7	300ms

Protection Function

Block	Protection	Work Condition	Action	Remark
VCCT	OCP	2.0A(min)	Cycle by cycle limit. LXT peak current > 2.0A, LXT stops switching. LXT peak current < 2.0A, LXT resumes switching	Auto recovery
	OVP	VCCT > 120%	VCCT > 120%, LXT stops switching. VCCT < 110%, LXT resumes switching.	Auto recovery
	UVP	VCCT < 65%, Freq →Freq/2	After 50ms, all channels shut down.	Release < VIN UVLO
	SCP	VCCT < 20%	After 10us, all channels shut down. After shutdown 50ms, restarts all channels. IC maintains shutdown state after IC restarts 3 times.	Release < VIN UVLO
VCCO	OCP	1.5A(min)	Cycle by cycle limit. LXO peak current > 1.5A, LXO stops switching. LXO peak current < 1.5A, LXO resumes switching	Auto recovery
	OVP	VCCO > 120%	VCCO > 120%, LXO stops switching. VCCO < 110%, LXO resumes switching.	Auto recovery
	UVP	VCCO < 65%	After 50ms, all channels shut down.	Release < VIN UVLO
	SCP	VCCO < 20%	After 10us, all channels shut down. After shutdown 50ms, restarts all channels. IC maintains shutdown state after IC restarts 3 times.	Release < VIN UVLO
SVDD	OCP	CSS=0.2V/0.4V	Cycle by cycle limit. CSS peak current > 0.2V/RCS, DRS stops switching. CSS peak current < 0.2V/RCS, DRS resumes switching	Auto recovery
	OVP	SVDDI > 21V	SVDDI > 21V, DRS stops switching. SVDDI < 20.5V, DRS resumes switching.	Auto recovery
	UVP	SVDD < 65%	After 50ms, all channels shut down.	Release < VIN UVLO
	SCP	SVDDI < 20%	After 10us, all channels shut down. After shutdown 50ms, restarts all channels. IC maintains shutdown state after IC restarts 3 times.	Release < VIN UVLO
VGH	OCP	1.5A(min)	Cycle by cycle limit. LXH peak current > 1.5A, LXH stops switching. LXH peak current < 1.5A, LXH resumes switching	Auto recovery
	BDP	600mA/750mA/ 900mA/1050mA	LXH peak current > BDP setting current after 1ms, BDP out latched high.	Release < POR
	OVP	VGH > 35V	VGH > 35.0V, LXH stops switching. VGH < 33.5V, LXH resumes switching.	Auto recovery
	UVP	VGH < 65%	After 50ms, all channels shut down.	Release < VIN UVLO
	SCP	VGH < 20%	After 10us, all channels shut down. After shutdown 50ms, restarts all channels. IC maintains shutdown state after IC restarts 3 times.	Release < VIN UVLO

Block	Protection	Work Condition	Action	Remark
VGL	OCP	1.5A(min)	Cycle by cycle limit. LXL peak current > 1.5A, LXL stops switching. LXL peak current < 1.5A, LXL resumes switching	Auto recovery
	BDP	450mA/600mA/ 750mA/900mA	LXL peak current > BDP setting current after 1ms, BDP out latched high.	Release < POR
	OVP	VGL < -14V	VGL < -14.0V, LXL stops switching. VGL > -13.5V, LXL resumes switching.	Auto recovery
	UVP	VGL < 65%	After 50ms, all channels shut down.	Release < VIN UVLO
	SCP	VGL > -1.3V	After 10us, all channels shut down. After shutdown 50ms, restarts all channels. IC maintains shutdown state after IC restarts 3 times.	Release < VIN UVLO
VPRED	OCP	±300mA	Continuously limit	Auto recovery
	SCP	VPRED < 20%	After 10us, all channels shut down. After shutdown 50ms, restarts all channels. IC maintains shutdown state after IC restarts 3 times.	Release < VIN UVLO
GPM	SCP	VGHM < 20%, FLK switching	All channels shut down after FLK switches 8 times.	Release < VIN UVLO
		VGHM < 20%, FLK keeps high	All channels shut down after FLK keeps high 16us.	Release < VIN UVLO

Application Information

The RT6940 is an I²C interface programmable power management IC. Main function includes one SVDD Boost converter, one VGH boost converter, one Async-Buck converter, one Sync- Buck converter, one VGL negative inverting converter, one VPRED OP- amplifier and BDP compactor. This device is suitable for OLED TV panels.

All channels of converters can be used to program such as output voltage, switching frequency of converter, delay time, BDP COMP selection, VPRED mode selection, Current sense selection of SVDD, VGH BDP level selection, VGL BDP level selection and discharge function of SVDD/VGH/VGL/VCCT/VCCO.

After VIN voltage rises above UVLO rising threshold, the IC will download data from MTP to set the initial parameters of RT6940. After MTP data download are finished, all channels will start soft-start procedure individually.

Under-Voltage Lockout

The UVLO circuit divides the input voltage from VIN pin with the UVLO threshold (9V rising, typ.) to ensure that the input voltage is high enough for reliable operation. The 1V (typ.) hysteresis of UVLO prevents shutdown caused by supply transients. Once the input voltage exceeds the UVLO rising threshold, start-up begins. When the input voltage falls below the UVLO falling threshold, all IC internal functions will be turned off by the controller.

Over-Temperature Protection

The RT6940 equips an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C, the main converter will resume operation. To maintain continuous operation maximum, the junction temperature should be prevented from rising above 120°C.

Fast Discharge Function

The SVDD, VGH, VCCT, VCCO and VGL channels embedded discharge function to discharge the remaining output to 0V rapidly, preventing phenomena such as residual image on the display during shutdown.

Soft-Start Function

All channels has soft-start function to reduce input rush current such that the switching duty is increased linearly. As a result, all channels rises up smoothly while the input current stays limited for the entire soft-start interval.

SVDD Boost Converter

SVDD channel is the asynchronous Boost converter with a current mode topology and fixed frequency operation. Moreover, user can adjust switching frequency by register address 02h respectively. The Boost converter can operate in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM), depending on the load current to gain optimum efficiency and minimum output ripple. It performs fast transient responses to generate source driver supplies for OLED display. The high operation frequency allows use of smaller components to minimize the thickness of the OLED panel.

SVDD Boost Output Voltage Setting

An SVDD asynchronous Boost converter has the I²C adjustable output voltage from 15V to 20V in 0.1V increments. The default SVDD voltage is 16.8V. User can control the SVDD output voltage by register address 00h respectively.

SVDD Boost Over-Voltage Protection

The SVDD Boost converter has an over-voltage protection to protect the SVDD switch at the SVDDI pin. When the SVDDI pin voltage rises above 21V (typ.), the Boost converter turns the MOSFET switch off. As soon as the output voltage falls below the over-voltage threshold, the converter will resume operation.

SVDD Boost Over-Current Protection

The SVDD can limit the peak current to achieve over-current protection. The IC senses the inductor current that is flowing into the CSS sense resistor during an ON period. The external N-MOSFET will be turned off if CSS pin voltage reaches 0.2V (typ.).

If inductor current peak reaches current limit, the SVDD channel will be keep current limit level.

SVDD Boost Short-Circuit Protection

The SVDD has an advanced short-circuit protection mechanism which prevents the device from damage by unexpected applications. An error condition is detected if the voltage on the converter's SVDD pin remains below SVDD x 20% for longer than 10μs, IC will be shut down and then restart three times. If the failure information is still not released, the chip will be shutdown. Once shut down, the boost converter can only be enabled after the chip is powered on again.

SVDD Boost Fault Protection

The SVDD Boost converter has a fault protection, if SVDD pin voltage is detected to be below SVDD x 65% for longer than 50ms. The SVDD, VGH, VGL, VCCT and VCCO will be shut down. Once the SVDD shuts down, the Boost converter can only be enabled after the chip is powered on again.

VGH Boost Converter

VGH channel is the asynchronous Boost converter with a current mode topology and fixed frequency operation. Moreover, user can adjust switching frequency by register address 02h respectively. The Boost converter can operate in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM), depending on the load current to gain optimum efficiency and minimum output ripple. It performs fast transient responses to generate source driver supplies for OLED display. The high operation frequency allows use of smaller components to minimize the thickness of the OLED panel

VGH Boost Output Voltage Setting

A VGH asynchronous Boost converter has the I^2C adjustable output voltage from 22V to 32V in 0.5V increments. The default VGH voltage is 26V. User can control the VGH output voltage by register address 06h respectively.

VGH Boost Over-Voltage Protection

The VGH Boost converter has an over-voltage protection to protect the VGH switch at LXH pin in case the feedback (VGH) pin is floating. When the VGH pin voltage reaches 35V (typ.), the VGH Boost converter turns off the N-MOSFET switch. As soon as the output voltage falls below the over voltage threshold, the converter will resume operation.

VGH Boost Over-Current Protection

The VGH inductor current is flowing into the LXH pin. When peak inductor current reaches current limit 1.5A (min.).The internal N-MOSFET will be turned off, forcing inductor current to leave charging state and enter discharging state, Therefore, the inductor current can be kept below current limit. The output current at the current limit boundary, denoted as $I_{OUT(LIM)}$, can be calculated according to the following equation :

$$I_{OUT(LIM)} = \eta \cdot \frac{V_{IN}}{V_{OUT}} \cdot \left(I_{LIM} - \frac{1}{2} \cdot \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT}} \cdot \frac{t_S}{L} \right)$$

where η is the efficiency of the Boost converter, I_{LIM} is the value of the current limit and t_S is the switching period. If inductor current peak reaches current limit, the SVDD channel will be keep current limit level.

VGH Boost Short-Circuit Protection

The VGH has an advanced short-circuit protection mechanism which prevents the device from damage by unexpected applications. An error condition is detected if the voltage on the converter's VGH pin remains below VGH x 20% for longer than 10μs, IC will be shut down and then restart three times. If the failure information is still not released, the chip will be shutdown. Once shut down, the boost converter can only be enabled after the chip is powered on again.

VGH Boost Fault Protection

The VGH Boost converter has a fault protection function, if VGH pin is detected to be below VGH x 65% for longer than 50ms. The SVDD, VGH, VGL, VCCT and VCCO will be shut down. Once the SVDD shuts down, the Boost converter can only be enabled after the chip is powered on again.

Boost Converter Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{\eta \cdot V_{IN}}$$

I_{RIPPLE} = 0.4 x $I_{IN(MAX)}$

where η is the efficiency of the Boost converter, $I_{IN(MAX)}$ is the maximum input current, and I_{RIPPLE} is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation:

I_{PEAK} = 1.2 x $I_{IN(MAX)}$

Note that the saturated current of the inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \cdot (V_{IN})^2 \cdot (V_{OUT} - V_{IN})}{0.4 \cdot (V_{OUT})^2 \cdot I_{OUT(MAX)} \cdot f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Converter Diode Selection

Schottky diode is a good choice for an asynchronous Boost converter due to its small forward voltage. However, when selecting Schottky diodes, important parameters such as power dissipation (PD = VF x Id), reverse voltage rating and pulsating peak current should all be taken into consideration. For better performance, it is recommended to choose a suitable diode with reverse voltage rating greater than the maximum output voltage.

Boost Converter Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input ripple voltage caused by switching operation. Two 22µF low ESR ceramic capacitors are sufficient for most applications. Nevertheless, this value can be decreased for applications with lower output current requirement. Note that the voltage rating of the input capacitor must be greater than the maximum input voltage.

Boost Converter Output Capacitor Selection

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in following figure, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation:

$$Q = \frac{1}{2} \cdot \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \cdot \frac{V_{IN}}{V_{OUT}} \cdot \frac{1}{f_{OSC}} = C_{OUT} \cdot \Delta V_{OUT1}$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. Move C_{OUT} to the left side to estimate the value of ΔV_{OUT1} according to the following equation :

$$\Delta V_{OUT1} = \frac{D \cdot I_{OUT}}{\eta \cdot C_{OUT} \cdot f_{OSC}}$$

where D is the duty cycle and η is the Boost converter efficiency. Finally, taking ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = \Delta V_{ESR} + \frac{D \cdot I_{OUT}}{\eta \cdot C_{OUT} \cdot f_{OSC}}$$

where $\Delta V_{ESR} = \Delta I_C \times R_{C\_ESR} = I_{PEAK} \times R_{C\_ESR}$

The output capacitor, C_{OUT}, should be selected accordingly.

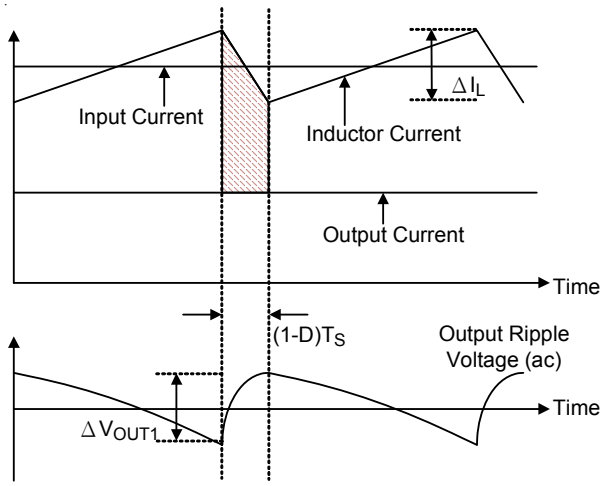


Figure 1. The Output Ripple Voltage without the Contribution of ESR

Boost Converter Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of R and C. Choose R to set the high frequency integrator gain for fast transient response and C to set the integrator zero to maintain stability. The frequency of the zero set by the compensation components can be calculated using the following equation :

$$f_Z = \frac{1}{2 \cdot \pi \cdot R \cdot C}$$

where R and C are the COMP pin outer resistance and capacitance.

VCCT Asynchronous Buck Converter

The VCCT asynchronous Buck converter is high efficiency PWM architecture with 1.4MHz (typ.) operation frequency and fast transient response. Moreover, user can adjust switching frequency by register address 03h respectively. The converter drives an internal 2.5A (typ.) N-MOSFET which is connected between the VIN and LXT pin. Connect a 100nF low ESR ceramic capacitor between the CBT and LXT pins to provide gate driver voltage for the high-side MOSFET.

VCCT Asynchronous Buck Soft-Start

The VCCT asynchronous Buck converter has an internal soft-start to reduce the input inrush current respectively. When the converter is enabled, the output voltage rises slowly from zero to target output voltage. The typical soft-start time is around 1ms.

VCCT Asynchronous Buck Output Voltage Setting

VCCT asynchronous Buck converter has the I^2C adjustable output voltage from 3V to 3.6V in 0.1V increments. The default VCCT voltage is 3.3V. User can control the Buck output voltage by register address 04h respectively.

VCCT Asynchronous Buck Over-Voltage Protection

The VCCT asynchronous Buck converter has the over-voltage protection to protect the main switch at the VCCT pin. When the VCCT pin voltage rises above (VCCT x 120%) V (typ.), VCCT will be shut down. As soon as the output voltage falls below the over-voltage threshold, the VCCT will resume operation.

VCCT Asynchronous Buck Over-Current Protection

The VCCT senses the inductor current that is flowing out the LXT pin. The internal MOSFET will be turned off if the peak inductor current reaches 2A (min.). Thus, the output current at the current limit boundary, denoted as $I_{OUT(LIM)}$, can be calculated according to the following equation :

$$I_{OUT(LIM)} = I_{LIM} - \frac{\left(1 - \frac{V_{OUT}}{\eta \cdot V_{IN}}\right) \cdot V_{OUT}}{2 \cdot L \cdot f_{SW}}$$

where η is the efficiency of the Buck converter, I_{LIM} is the value of the current limit and f_{SW} is the switching frequency.

VCCT Asynchronous Buck Short-Circuit Protection

The VCCT has an advanced short-circuit protection mechanism which prevents the device from damage by unexpected applications. An error condition is detected if the voltage on the converter's VCCT pin remains below VCCT x 20% for longer than 10μs, IC will be shut down and then restart three times. If the failure information is still not released, the chip will be shutdown. Once shut down, the boost converter can only be enabled after the chip is powered on again.

VCCT Asynchronous Buck Fault Protection

The VCCT asynchronous Buck converter has a fault protection feature to protect the IC when the output becomes shorted to GND. This is achieved by using the comparator to monitor the VCCT voltage. If VCCT remains below VCCT x 65% for 50ms, the VCCT Buck converter will be disabled. Once shut down, the regulator can only be enabled after the chip is powered on again.

VCCO Synchronous Buck Converter

The VCCO synchronous converter is high efficiency PWM architecture with 1.4MHz (typ.) operation frequency and fast transient response. Moreover, user can adjust switching frequency by register address 03h respectively. VCCO converter has one internal P-MOSFET and one internal N-MOSFET as synchronous rectifier and do not require Schottky diode on the switching Pin. The high-side MOSFET is connected between the VIN and switching pins, while the low-side MOSFET is connected between the switching pin and GND. The synchronous Buck converter's loop compensation network is builds in inside RT6940.

VCCO Synchronous Buck Soft-Start

The VCCO synchronous Buck converter has an internal soft-start to reduce the input inrush current respectively. When the converter is enabled, the output voltage rises slowly from zero to target output voltage. The typical soft-start time is around 1ms.

VCCO Synchronous Buck Output Voltage Setting

VCCO synchronous Buck converter has the I^2C adjustable output voltage from 1.5V to 2.8V in 0.1V increments. The default VCCO voltage is 1.8V. User can control the Buck output voltage by register address 04h respectively.

VCCO Synchronous Buck Over-Voltage Protection

The VCCO synchronous Buck converter has the over-voltage protection to protect the main switch at the VCCO pin. When the VCCO pin voltage rises above (VCCO x 120%) V (typ.), VCCO will be shut down. As soon as the output voltage falls below the over-voltage threshold, the VCCO will resume operation.

VCCO Synchronous Buck Over-Current Protection

The VCCO senses the inductor current that is flowing out the LXO pin. The internal MOSFET will be turned off if the peak inductor current reaches 1.5A (min.). Thus, the output current at the current limit boundary, denoted as $I_{OUT(LIM)}$, can be calculated according to the following equation :

$$I_{OUT(LIM)} = I_{LIM} - \frac{\left(1 - \frac{V_{OUT}}{\eta \cdot V_{IN}}\right) \cdot V_{OUT}}{2 \cdot L \cdot f_{SW}}$$

Where η is the efficiency of the Buck converter, I_{LIM} is the value of the current limit and f_{SW} is the switching frequency.

VCCO Synchronous Buck Short-Circuit Protection

The VCCO has an advanced short-circuit protection mechanism which prevents the device from damage by unexpected applications. An error condition is detected if the voltage on the converter's VCCO pin remains below VCCO x 20% for longer than 10μs, IC will be shut down and then restart three times. If the failure information is still not released, the chip will be shutdown. Once shut down, the boost converter can only be enabled after the chip is powered on again.

VCCO Synchronous Buck Fault Protection

The VCCO synchronous Buck converter has a fault protection feature to protect the IC when the output becomes shorted to GND. This is achieved by using the comparator to monitor the VCCO voltage. If VCCO remains below VCCO x 65% for 50ms, the VCCO Buck converter will be disabled. Once shut down, the regulator can only be enabled after the chip is powered on again.

Buck Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, will increase with higher VIN and decrease with higher inductance, as shown in the equation below :

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{OSC} \cdot L}\right) \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage

ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $I_{L(MAX)}$ / ΔI_L = 0.4 is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following :

$$L = \left(\frac{V_{OUT}}{f_{OSC} \cdot \Delta I_{L(MAX)}} \right) \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Buck Input Capacitor Selection

To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2 V_{OUT}, where I_{RMS} = I_{OUT} / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10μF low ESR ceramic capacitor is recommended.

Buck Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, V_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_{OUT}} \right)$$

The output ripple will be the highest at the maximum input voltage since I_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Buck-Boost Converter

The inverting buck-boost non-synchronous converter uses a peak current mode topology and fixed frequency operation. Moreover, user can adjust switching frequency by register address 02h respectively. Inverting buck-boost converter generates the negative voltage VGL for scan driver.

The converter drives an internal 2A (typ.) P-MOSFET which is connected between the VINL and LXL pin.

Buck-Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the buck-boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g.,80%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor and external Schottky diode have to be able to handle this current.

1. Converter Duty Cycle :

$$D = \frac{-V_{OUT}}{V_{IN} \times \eta - V_{OUT}}$$

2. Maximum output current :

$$I_{OUT} = \left(I_{LXLPEAK} - \frac{V_{IN} \times D}{2 \times f_{OSC} \times L} \right) \times (1 - D)$$

3. Peak switch current :

$$I_{LXLPEAK} = \frac{I_{OUT}}{1 - D} + \frac{V_{IN} \times D}{2 \times f_{OSC} \times L}$$

Buck-Boost Over-Voltage Protection

The VGL Buck-Boost converter has an over voltage protection to protect the VGL switch at LXL pin in case the feedback (VGL) pin is floating. When the VGL pin voltage reaches -14V (typ.), the VGL Buck-Boost converter turns off the P-MOSFET switch. As soon as the output voltage falls below the over voltage threshold, the converter will resume operation.

Buck-Boost Fault Protection

The VGL Buck-Boost converter has a fault protection feature to protect the IC when the output becomes shorted to GND. This is achieved by using the comparator to monitor the VGL voltage. If VGL remains below VGL x 65% for 50ms, the VGL Buck-Boost converter will be disabled. Once shut down, the regulator can only be enabled after the chip is powered on again.

VGL Buck-Boost Short-Circuit Protection

The VGL has an advanced short-circuit protection mechanism which prevents the device from damage by unexpected applications. An error condition is detected if the voltage on the converter's VGL pin remains below –1.3V for longer than 10μs, IC will be shut down and then restart three times. If the failure information is still not released, the chip will be shutdown. Once shut down, the boost converter can only be enabled after the chip is powered on again.

VGL Buck-Boost Output Voltage Setting

VGL Buck-Boost converter has the I^2C adjustable output voltage from –4V to –13V in 0.5V increments. The default VGL voltage is –8V. User can control the Buck-Boost output voltage by register address 07h respectively.

Buck-Boost Converter Inductor Selection

The buck-boost converter is able to operate with 10μH to 47μH inductors, but a 10μH inductor is typical. The main parameter for inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the Design Procedure section with additional margin to cover for heavy load transients. As for inductance, we are going to derive the transition point, where the converter toggles from CCM to DCM. We need to define the point at which the inductor current ripple touches zero, and as the power switch is immediately reactivated, the current ramps up again. Figure 2 portrays the input current activity of the Buck-Boost converter.

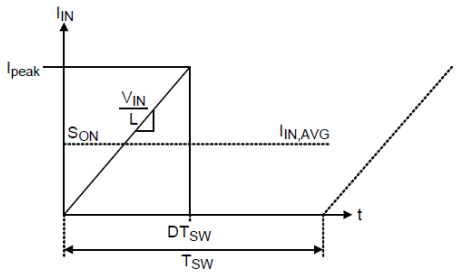


Figure 2. The Buck-Boost input signature in BCM

Figure 2. The Buck-Boost Input Signature in BCM

The inductance can eventually be determined according to the following equation :

$$Lcritical = \frac{|V_{OUT}| \times \eta}{2 \times f_{OSC} \times I_{OUT}} \times \left(\frac{V_{IN}}{V_{IN} + |V_{OUT}|} \right)^2$$

As a general rule, the inductor ripple current range is 20% to 40% of the average DC inductor current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$L = \frac{|V_{OUT}| \times \eta}{0.4 \times f_{OSC} \times I_{OUT}} \times \left(\frac{V_{IN}}{V_{IN} + |V_{OUT}|} \right)^2$$

Buck-Boost Converter Diode Selection

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the buck-boost converter. The average rectified forward current, I_{AVG}, the Schottky diode needs to be rated for, is equal to the output current, I_{OUT}.

$P_D = I_{AVG} \times V_{FORWARD}$

Buck-Boost Converter Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One 22μF or two 10μF output capacitors with sufficient voltage ratings in parallel are adequate for most applications. Additional capacitors can be added to improve load transient regulation.

To calculate the output voltage ripple, the following equation can be used :

$$\Delta V = \frac{D \times |V_{OUT}|}{f_{OSC} \times R_{LOAD} \times C_{OUT}} + \Delta V_{ESR}$$

where $\Delta V_{ESR} = \Delta I_C \times R_{C\_ESR} = I_{PEAK} \times R_{C\_ESR}$

ΔV_{ESR} can be neglected in many cases since ceramic capacitors provides very low ESR.

VPRED OP-Amplifier

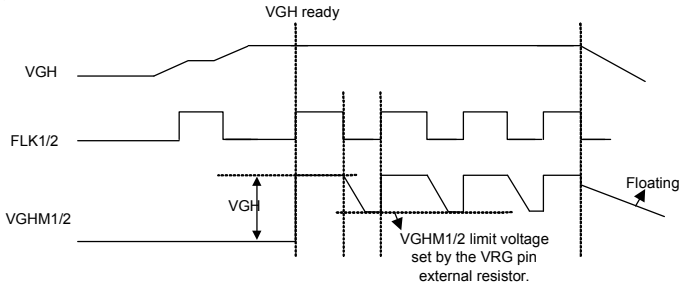
VPRED OP-Amplifier has the I2C adjustable mode select and output voltage from 3V to 6.5V in 0.5V increments. The default VPRED voltage is 6.5V. User can control the amplifier mode and output voltage by register address 05h respectively.

VPRED OP-Amplifier Short-Circuit Condition

An internal short-circuit protection circuit is implemented to protect the device from output short circuit. The amplifier limits the short circuit current to ±300mA if the output is directly shorted to positive/negative supply rails. An error condition is detected if the voltage on the amplifier VPRED pin remains below VPRED x 20% for longer than 10μs, IC will be shut down and then restart three times. If the failure information is still not released, the chip will be shutdown. Once shut down, the amplifier can only be enabled after the chip is powered on again.

Gate Pulse Modulation

The gate modulation is controlled by FLK1/2 signal, except during startup where it is kept at low state until VGH build up is ready. The discharge slope is set by the RE1/2 pin external resistor, the internal MOSFET and the VGHM1/2 pin gate line capacitance. A gate pulse modulation limited voltage can be set by VRG pin external resistor. When the limit voltage is reached, the discharging of VGHM1/2 through RE1/2 is stopped and the VGHM1/2 output is high impedance until FLK1/2 goes high again.



BDP Comparator

The BDP function is open drain contains an independent current-limit mechanism. It prevents large current from damaging the inductor and diode. If the inductor current exceeds the current limit of BDP or BS_SNS voltage exceeds the BD_REF, BDP voltage will be pulling high. Once pull high, the open drain can only be enabled after the chip is powered on again.

BDP Start Delay Time

BDP start has the I^2C adjustable delay time from 0ms to 50ms in 10ms increments. User can control the BDPSTR delay time by register address 06h respectively.

BDP End Delay Time

BDP end has the I^2C adjustable delay time from 0ms to 300ms. User can control the BDPEND delay time by register address 07h respectively.

EVDD Voltage Detector

The ED_RST and NMOS_CON function are open-drain architecture. While VIN and ED_SNS power on sequence are normal, once the ED_SNS voltage exceeds the ED_REF rising threshold (Typ. 1.2V), IC will count delay time of BDPSTR and BDPEND. After count delay time of BDPSTR is finished, NMOS_CON voltage will pull low. After count delay time of BDPEND is finished, NMOS_CON voltage will pull high. After NMOS_CON voltage pull high is finished, ED_RST voltage will pull high after count delay time (1ms). If VIN and ED_SNS power on sequence are reverse, NMOS_CON voltage will kept high. After count delay time of BDPEND is finished, ED_RST voltage will pull high after count delay time (1ms). The EVDD detector function can be determined according to page 5.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-56L 7x7, the thermal resistance, θ_{JA}, is 27°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27°C/W) = 3.7W for a WQFN-56L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

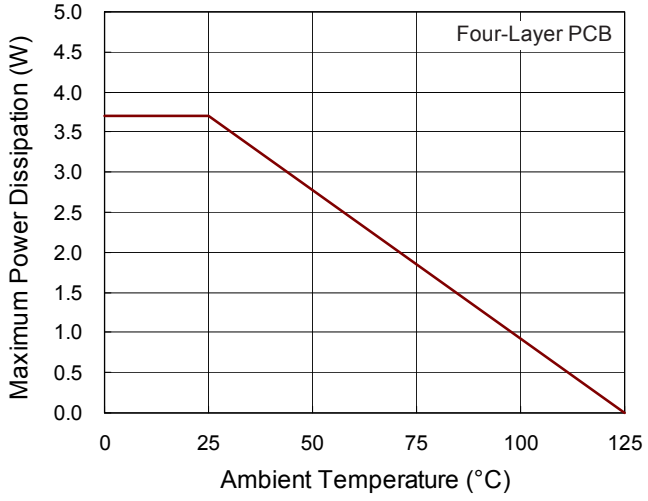


Figure 3. Derating Curve of Maximum Power Dissipation

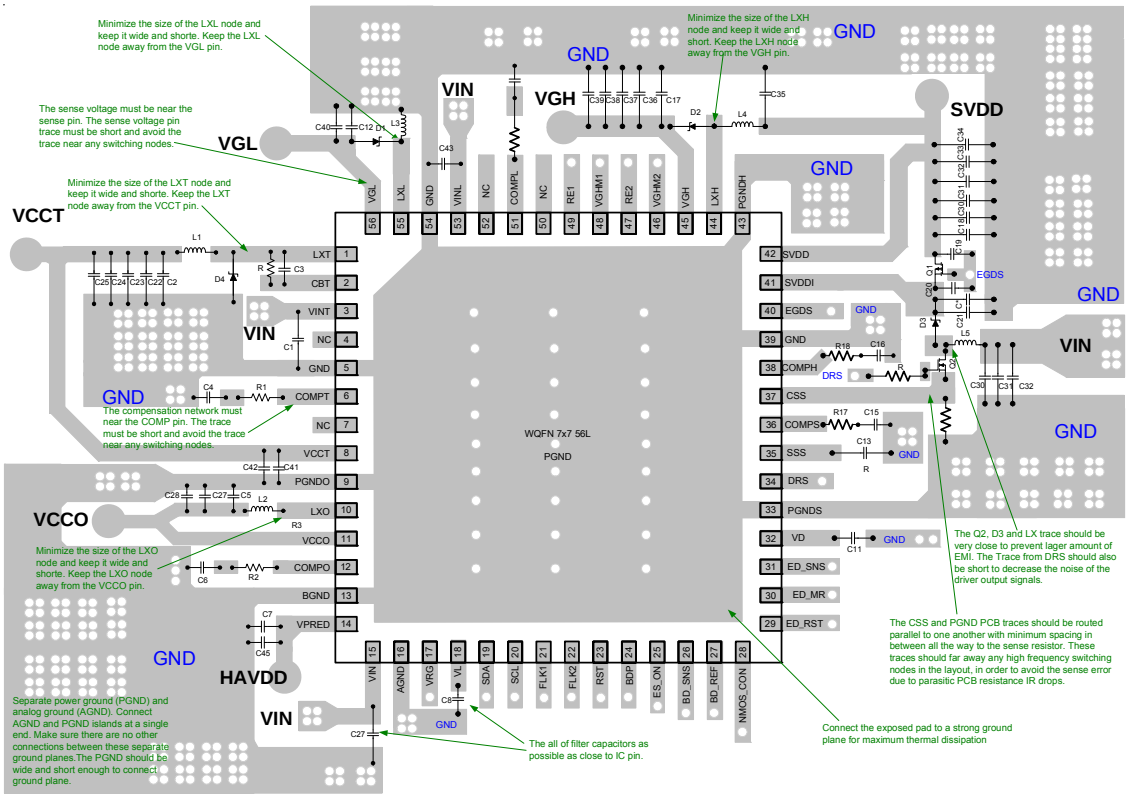
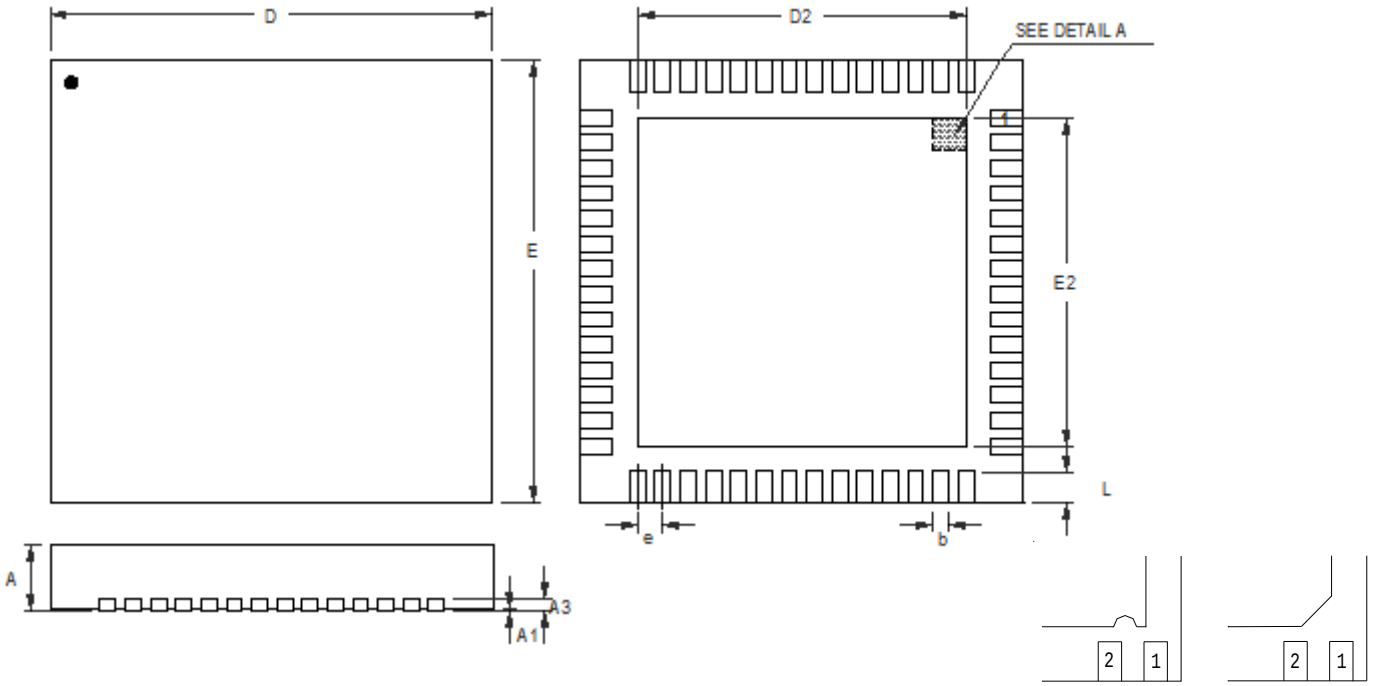


Figure 3. PCB Layout Guide

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.150	5.250	0.203	0.207
E	6.900	7.100	0.272	0.280
E2	5.150	5.250	0.203	0.207
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 56L QFN 7x7 Package

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