EA40_BM
Schematics Document

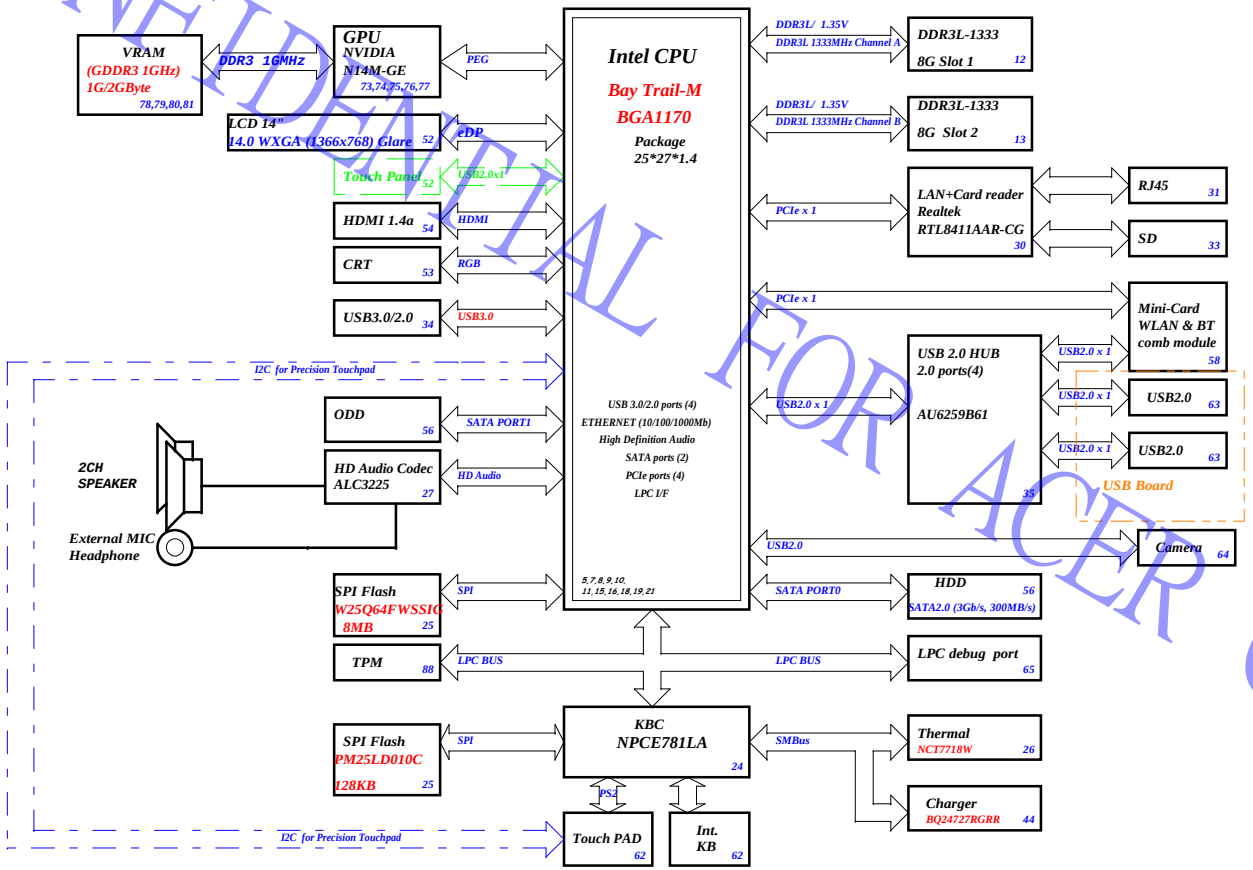
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A3	Document Number: EA40_BM	Rev: -1
Date: Tuesday, November 19, 2013	Sheet 1 of 102	

EA40_BM Board Block Diagram

Project code : 91.4OC01.001
PCB P/N : 13233
Revision : -1



CHARGER BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC ISL95833	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SY8208	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

SYSTEM DC/DC SY8208DQNC	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM LDO TLV70218	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM LDO S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

SYSTEM LDO TLV70012	51
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5

Step Down Regulator SYW232	51
INPUTS	OUTPUTS
1D0V_S0_PG	1D05V_S0

GPU Core RT8812	82
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

LOAD SWITCH TPS22966	37
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0

LOAD SWITCH TPS22965	37
INPUTS	OUTPUTS
1D0V_S5	1D0V_S0

SYSTEM DC/DC SY8208	83
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

LOAD SWITCH TPS22966	83
INPUTS	OUTPUTS
1D05V_S0	1D5V_VGA_S1
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title: Block Diagram

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 2 of 102

N15M UMA TOUCH 1DIMM

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 3 of 102

SSID = CPU

Blanking

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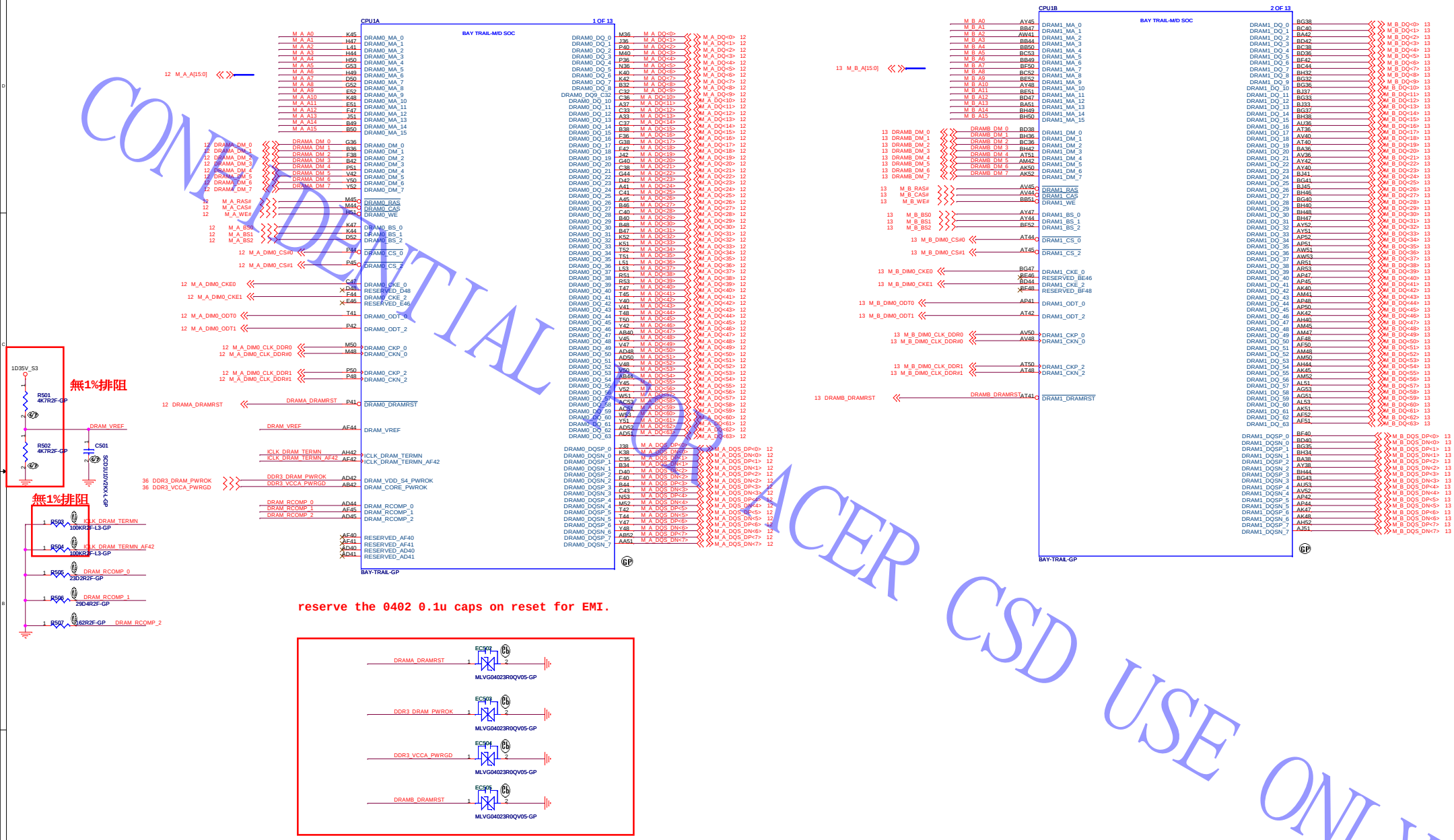
Title	CPU (Reserved)	
Size A4	Document Number EA40 BM	Rev -1
Date: Tuesday, November 19, 2013	Sheet 4 of 102	

SSID = CPU



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Title: CPU (DDR)

Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 5 of 102

SSID = CPU

Blanking

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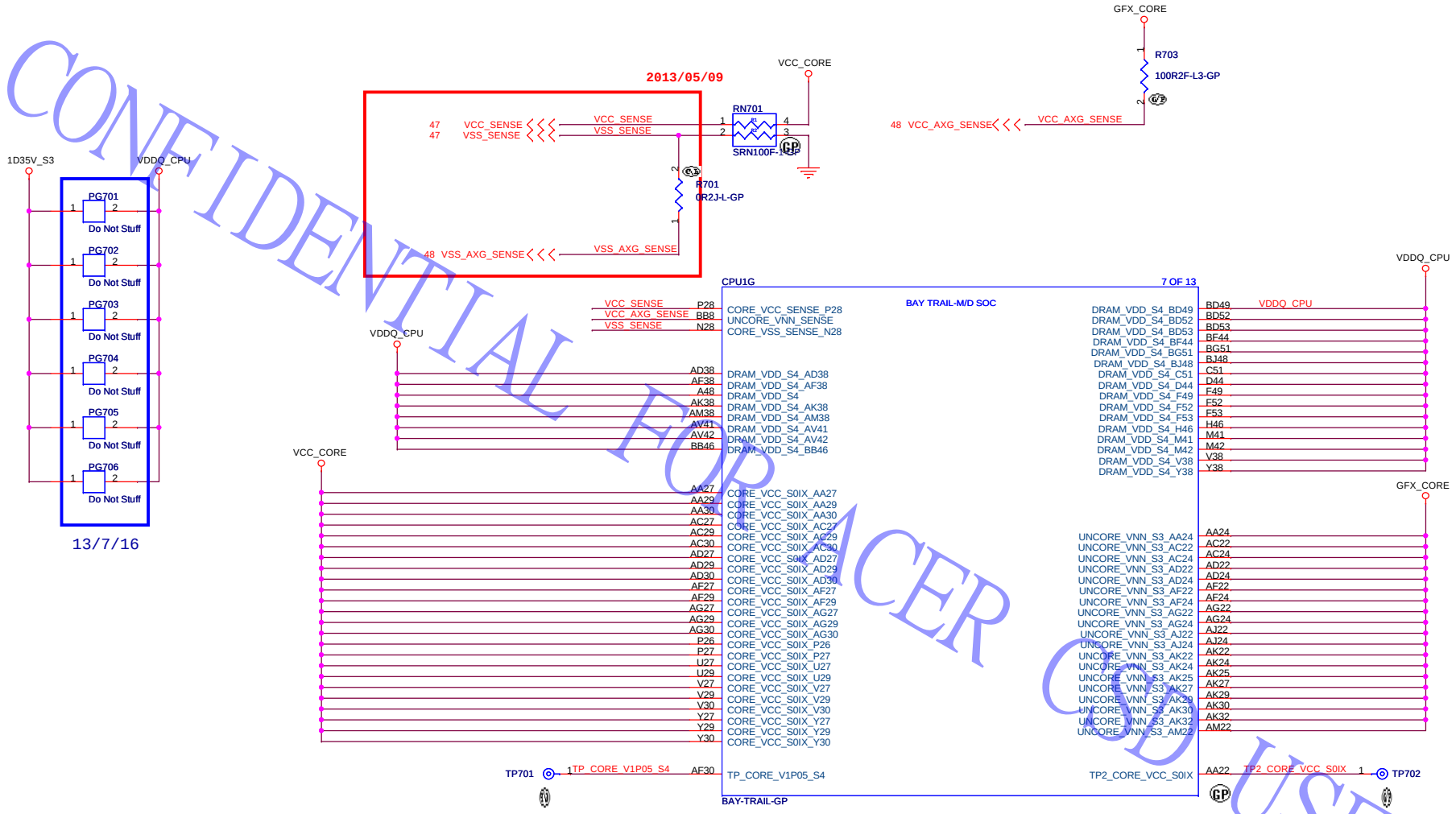
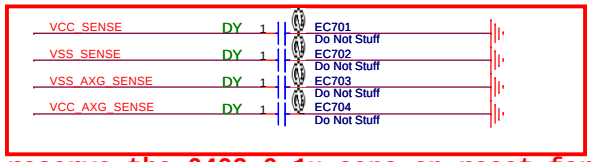
Title: CPU (CFG)

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 6 of 102

SSID = CPU





reserve the 0402 0.1u caps on reset for EMI.

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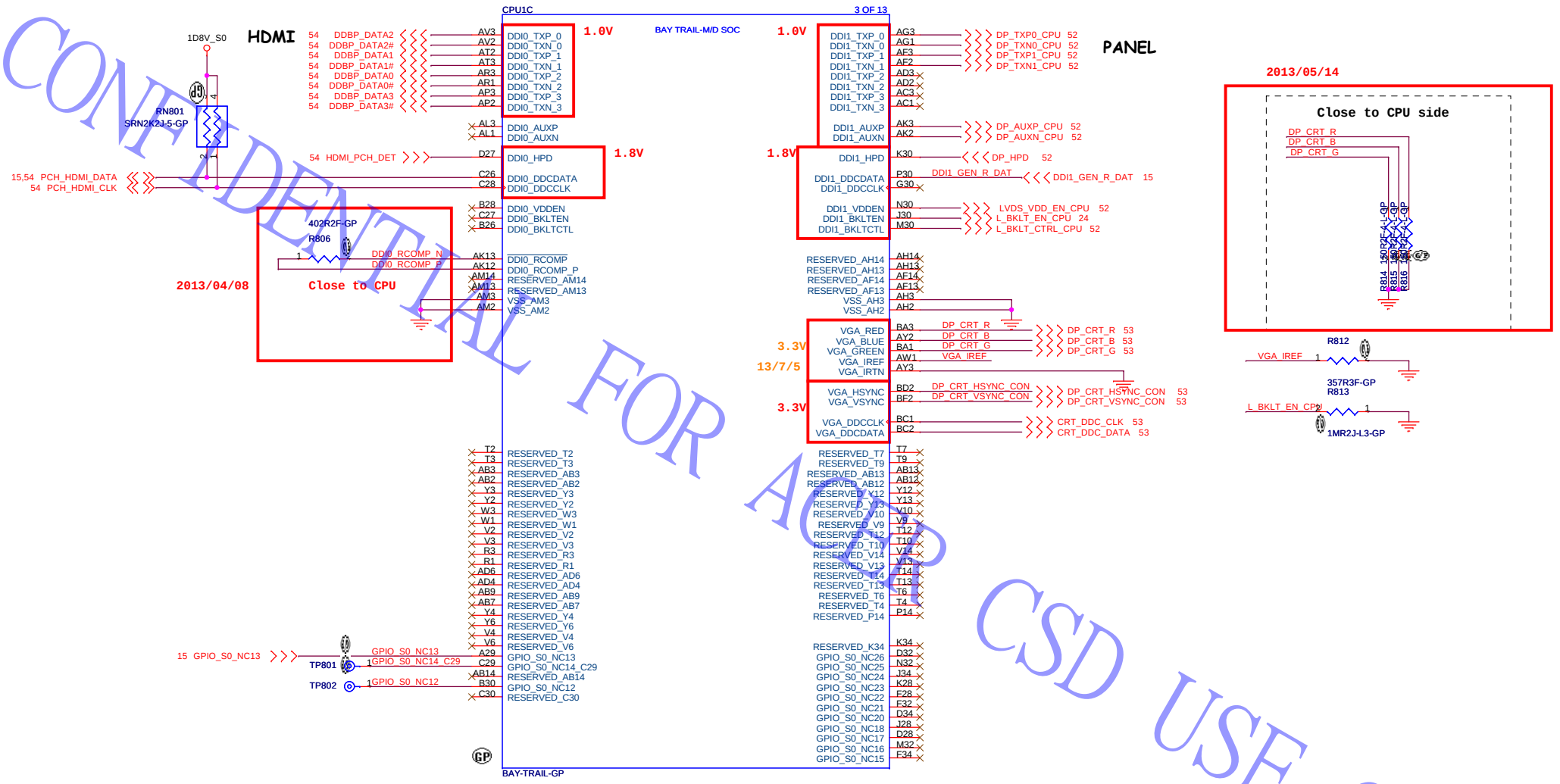
Title: CPU (VCC_CORE)

Size: A3 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 7 of 102

SSID = CPU



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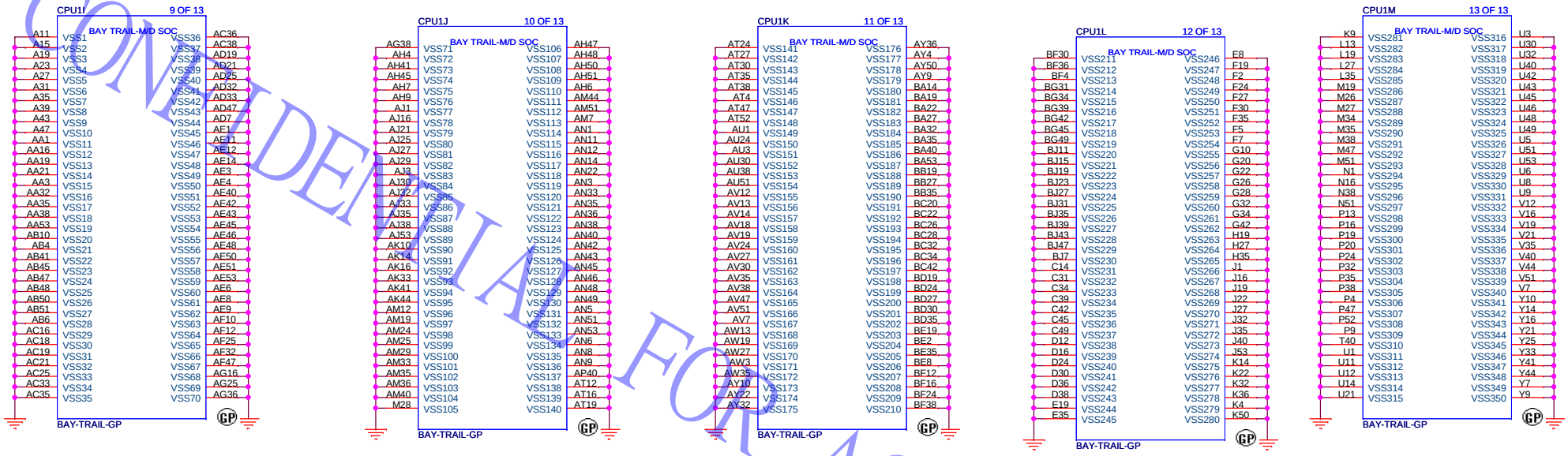
Title: CPU (DDI/EDP/GPIO)

Size	Document Number	Rev
A3	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 8 of 102

SSID = CPU



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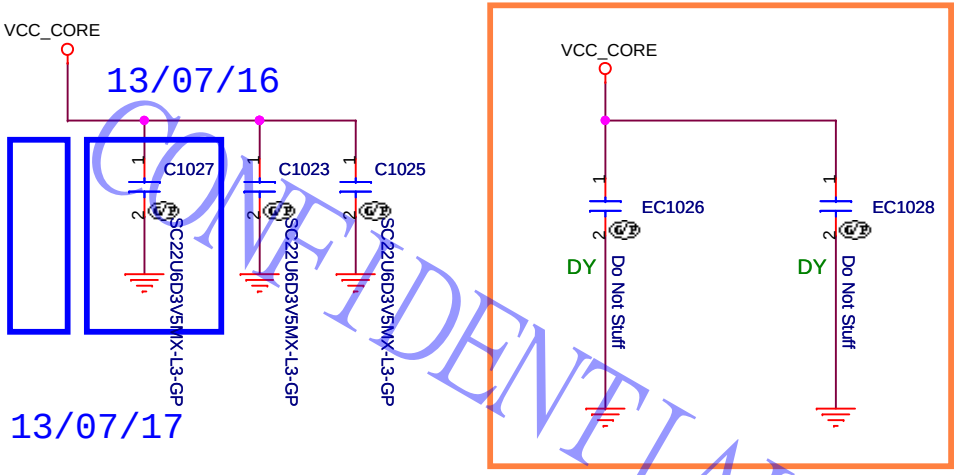
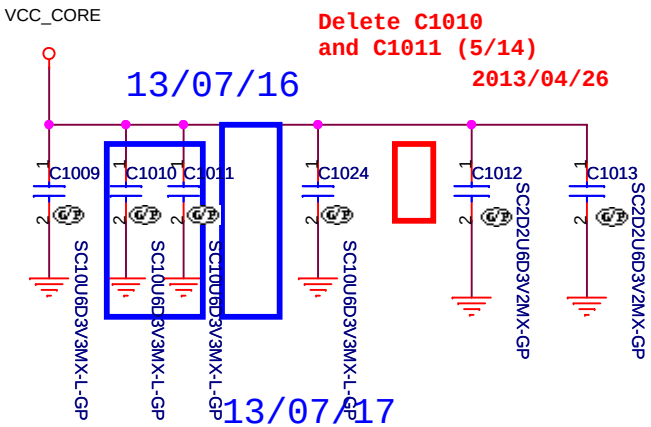
Title: CPU (VSS)

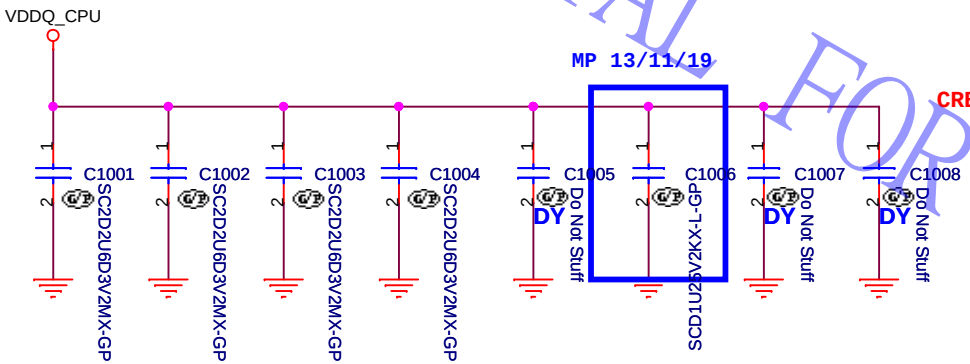
Size	Document Number	Rev
A3	EA40_BM	-1

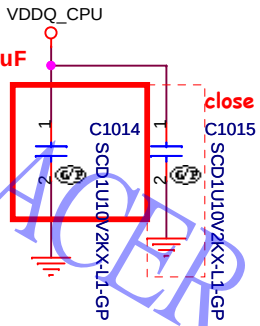
Date: Tuesday, November 19, 2013 Sheet 9 of 102

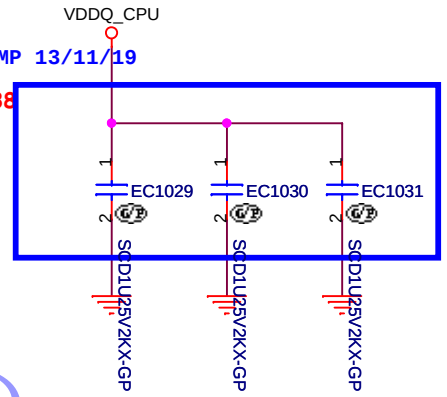
reserve the 0402 0.1u caps on reset for EMI(5/9).

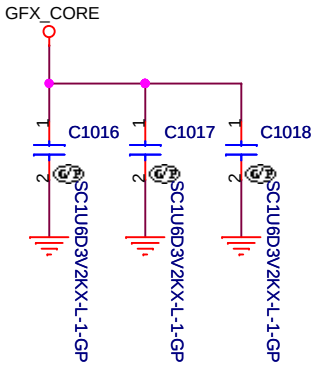


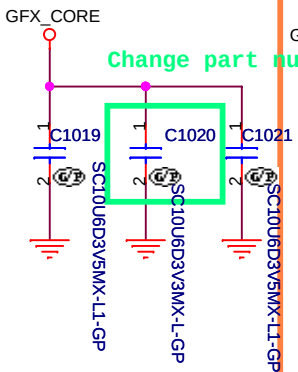


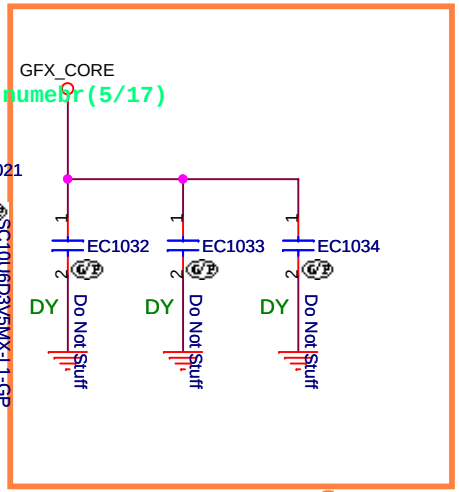












reserve the 0402 0.1u caps on reset for EMI(5/9).

reserve the 0402 0.1u caps on reset for EMI(5/9).

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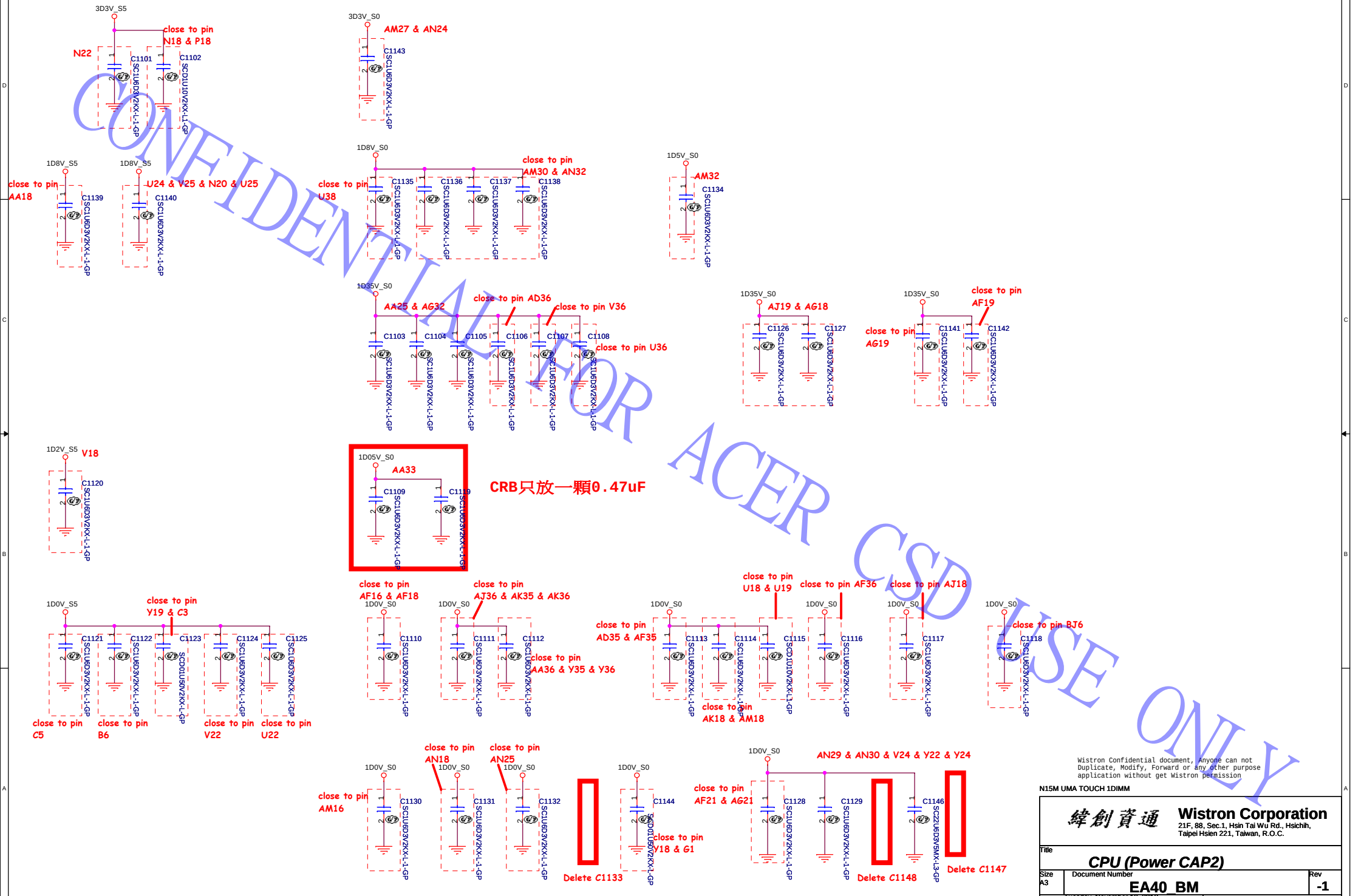
Title: CPU (Power CAP1)

Size: A4 | Document Number: EA40 BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 10 of 102



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Title: CPU (Power CAP2)

Size: A3 | Document Number: EA40_BM | Rev: -1

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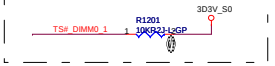
SSID = MEMORY

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

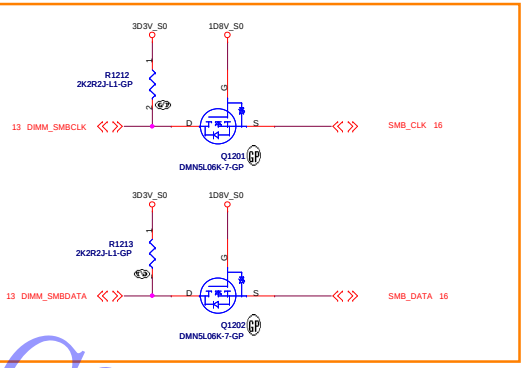
0726_SA

Thermal EVENT

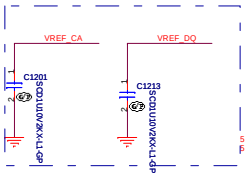


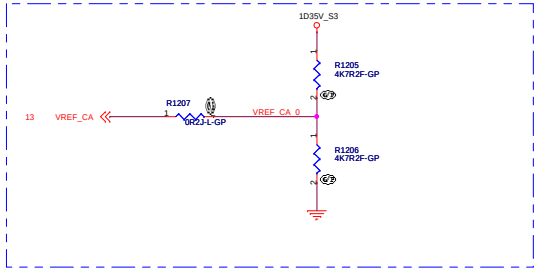
13/7/5

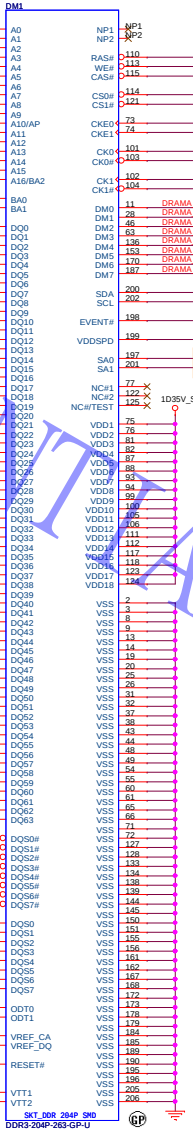
Level shift



VGS(th) = 1V



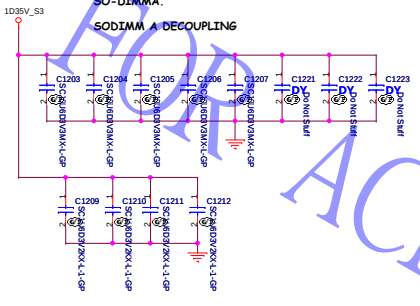


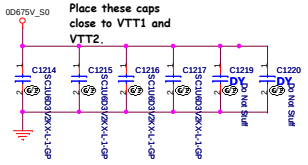


13/7/5

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

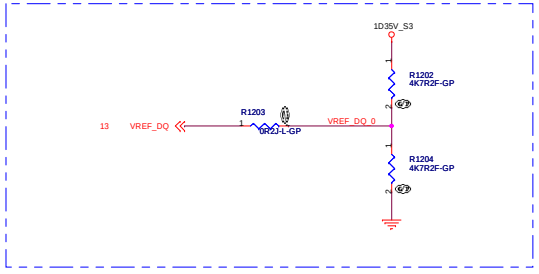


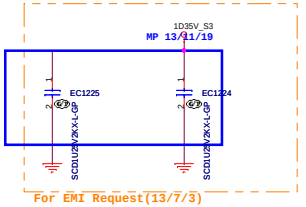


DM1 change part number to 62.10024.S61(13/7/3)

For Intel Recommend Close to DIMM(Bay Trail)

For Intel Recommend Close to DIMM(Bay Trail)





N15M UMA TOUCH 1DIMM

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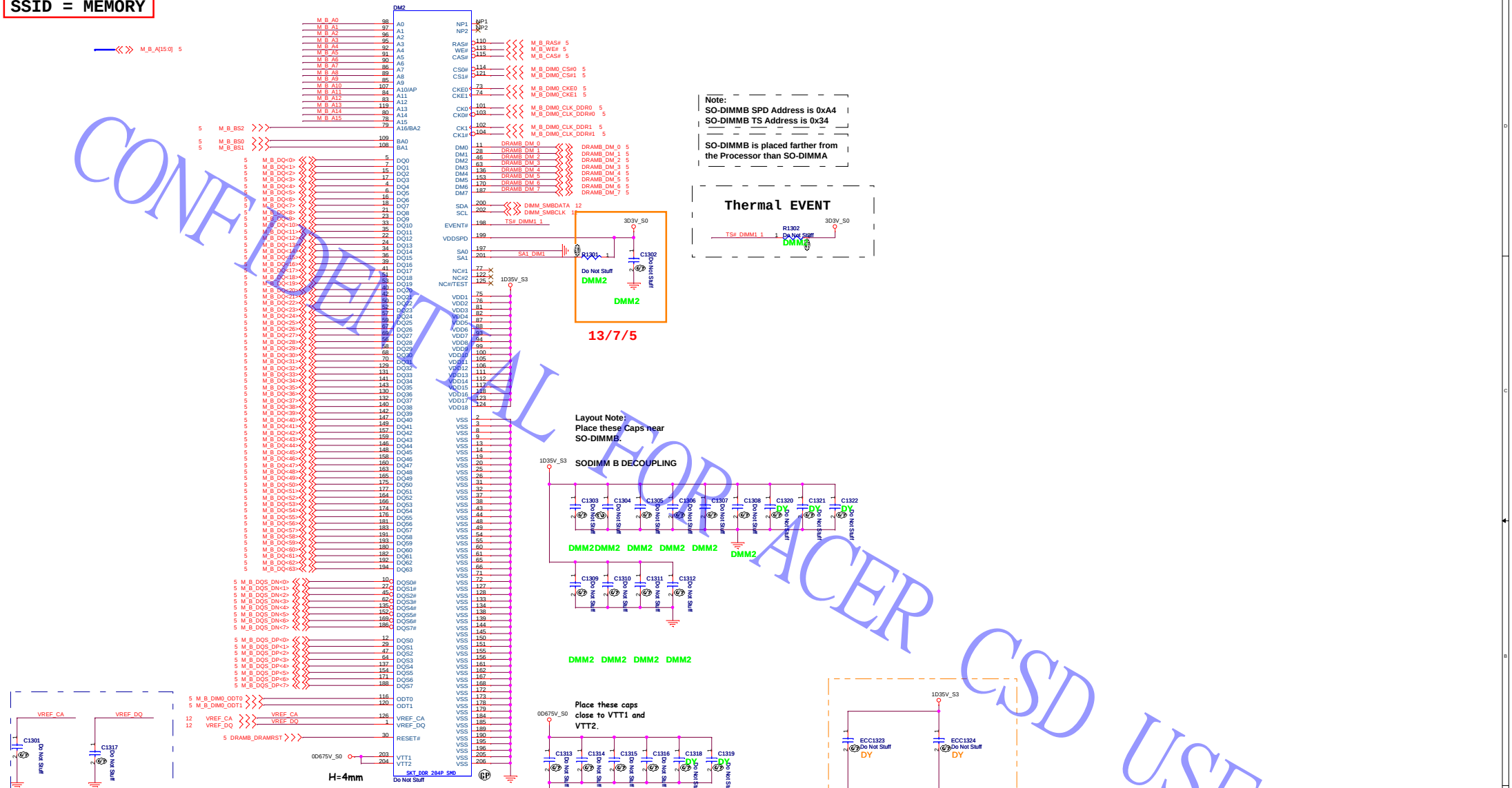
Title: ***DDR3-SODIMM1***

Size: A2 | Document Number: **EA40_BM** | Rev: **-1**

Date: Tuesday, November 19, 2013 | Sheet 12 of 102

SSID = MEMORY



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Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A2	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 13 of 102

Blanking

N15M UMA TOUCH 1DIMM

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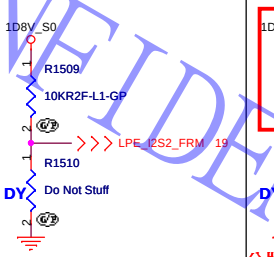
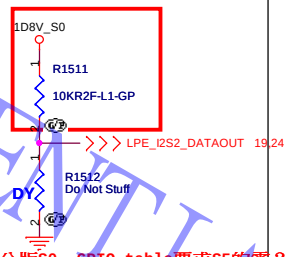
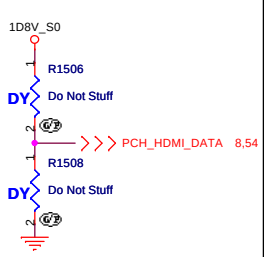
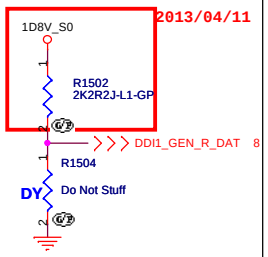
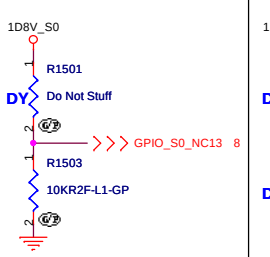
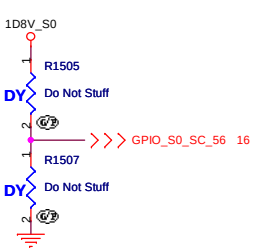
Title	***Reserved***	
Size A4	Document Number **EA40 BM**	Rev **-1**
Date: Tuesday, November 19, 2013	Sheet 14 of 102	

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic		 公版S0，GPIO table要求S5的電？				
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

N15M UMA TOUCH 1DIMM

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Title: CPU(STRAP)

Size: A3 | Document Number: EA40_BM | Rev: -1

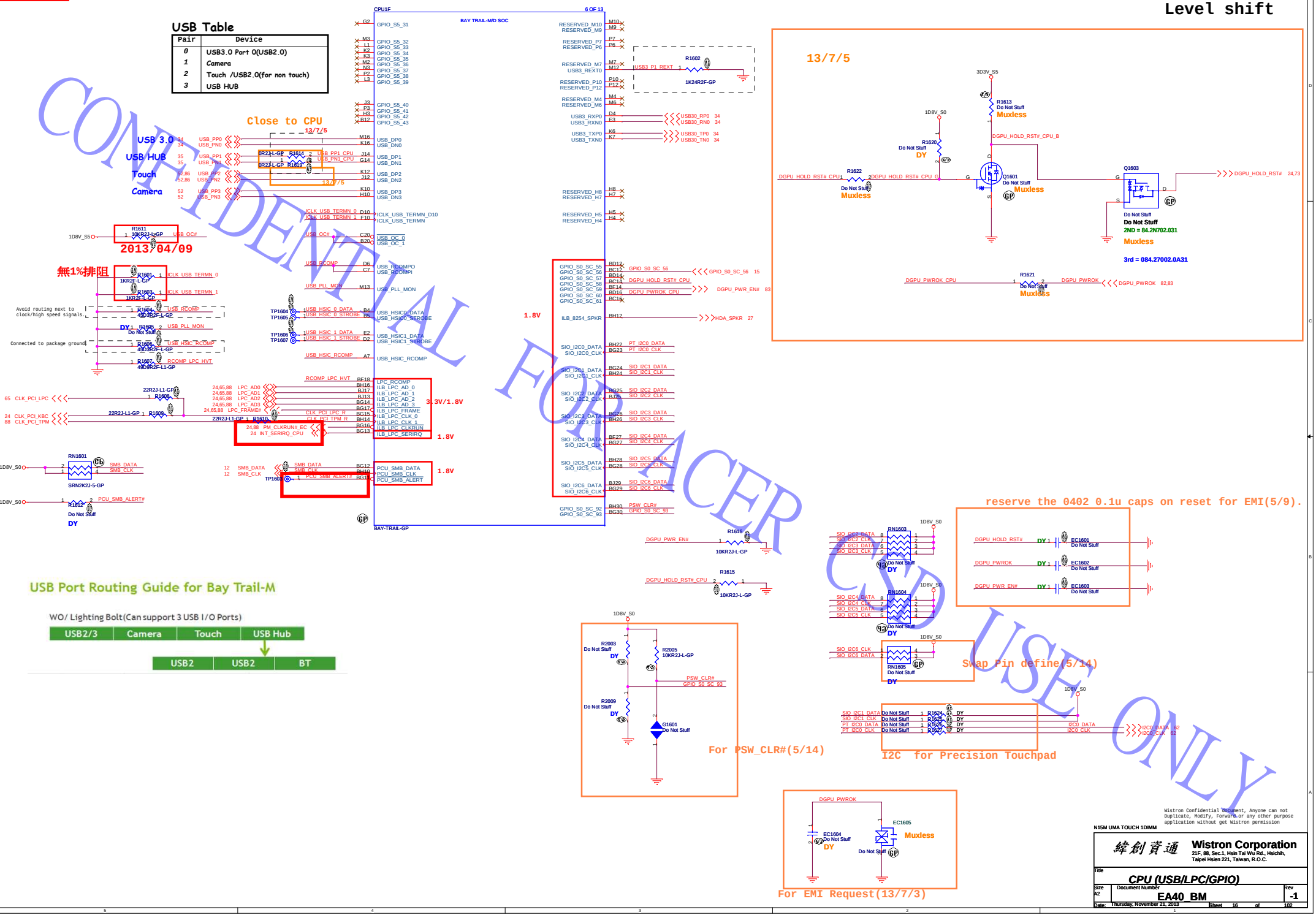
Date: Tuesday, November 19, 2013 | Sheet 15 of 102

SSID = PCH

Level shift

USB Table

Pair	Device
0	USB3.0 Port 0(USB2.0)
1	Camera
2	Touch /USB2.0(for non touch)
3	USB HUB



N15M UMA TOUCH 1DIMM

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Title: CPU (USB/LPC/GPIO)

Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Thursday, November 21, 2013 | Sheet 16 of 102

SSID = PCH

Blanking

N15M UMA TOUCH 1DIMM

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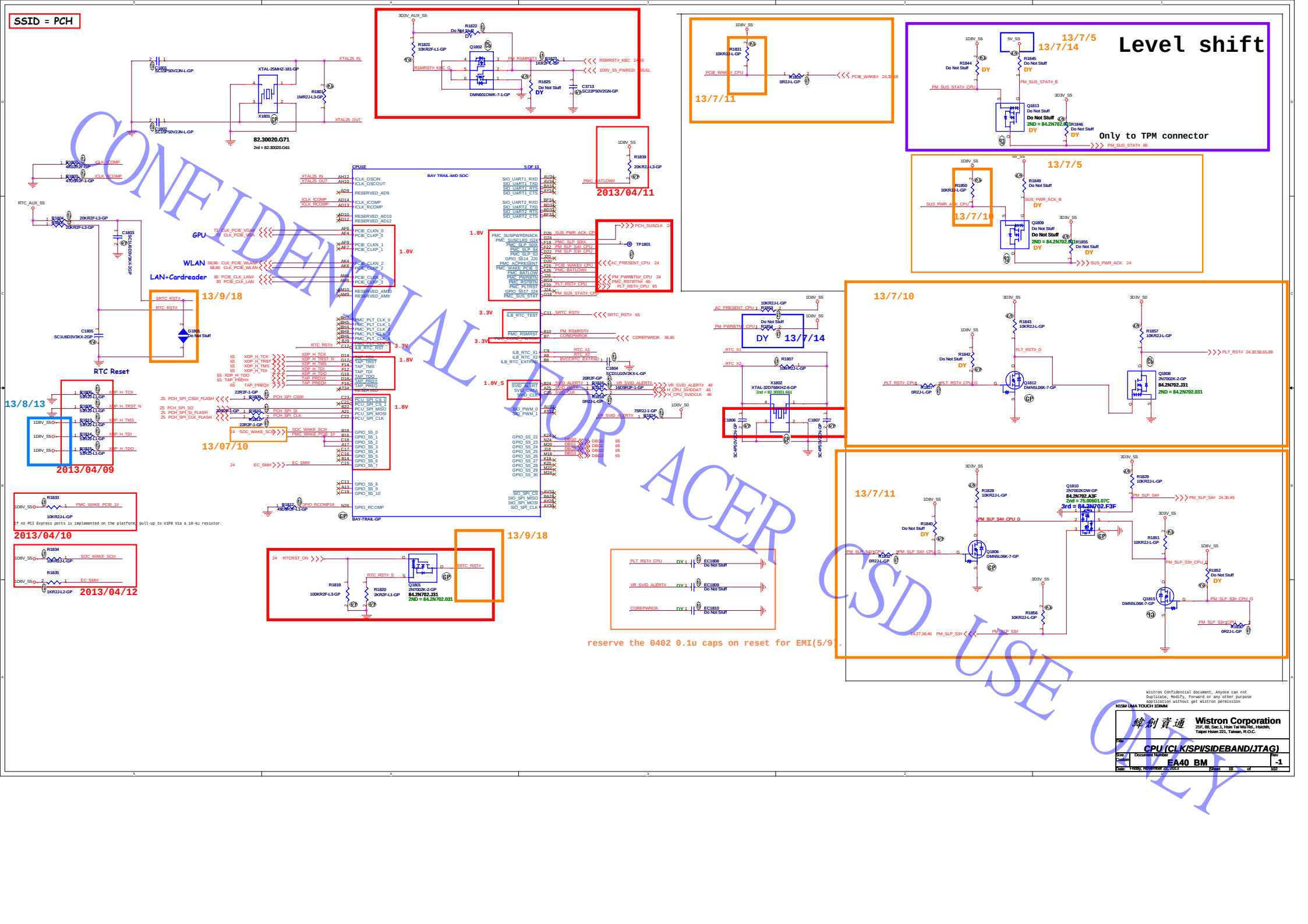
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DMI/FDI/PM)

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 17 of 102

SSID = PCH



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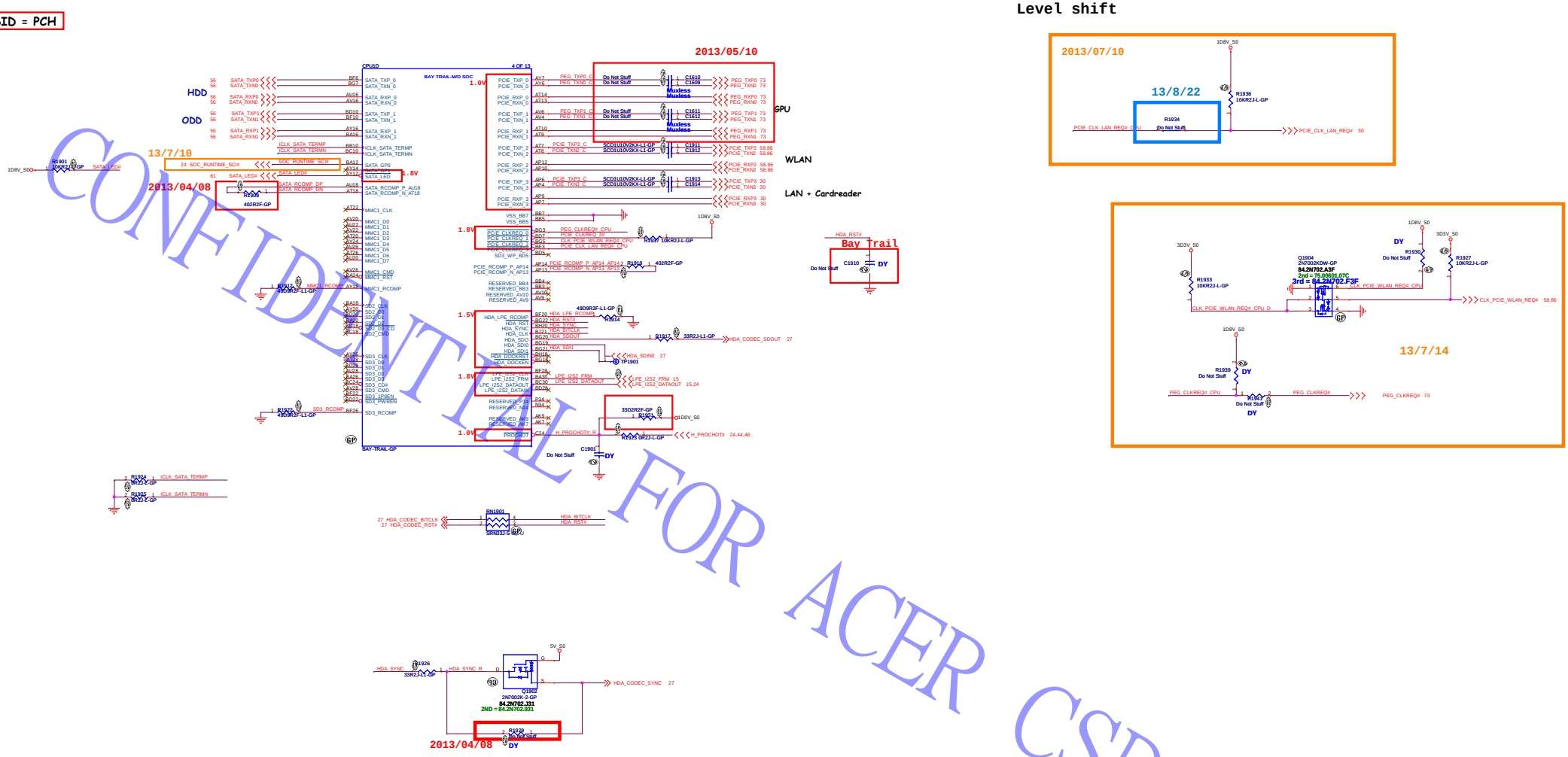
Title: CPU (CLK/SPI/SIDEBAND/JTAG)

Size: Document Number: EA40 BM Rev: -1

Date: Friday, November 22, 2013 Sheet 18 of 102

SSID = PCH



Level shift

N15M LMA TOUCH 10IMA

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Title	CPU (SATA/PCIE/IHDA)
Size: Custom	Document Number: EA40_BM
Rev: -1	
Date: Wednesday, November 20, 2013	Sheet 19 of 103

SSID = PCH

Blanking

N15M UMA TOUCH 1DIMM

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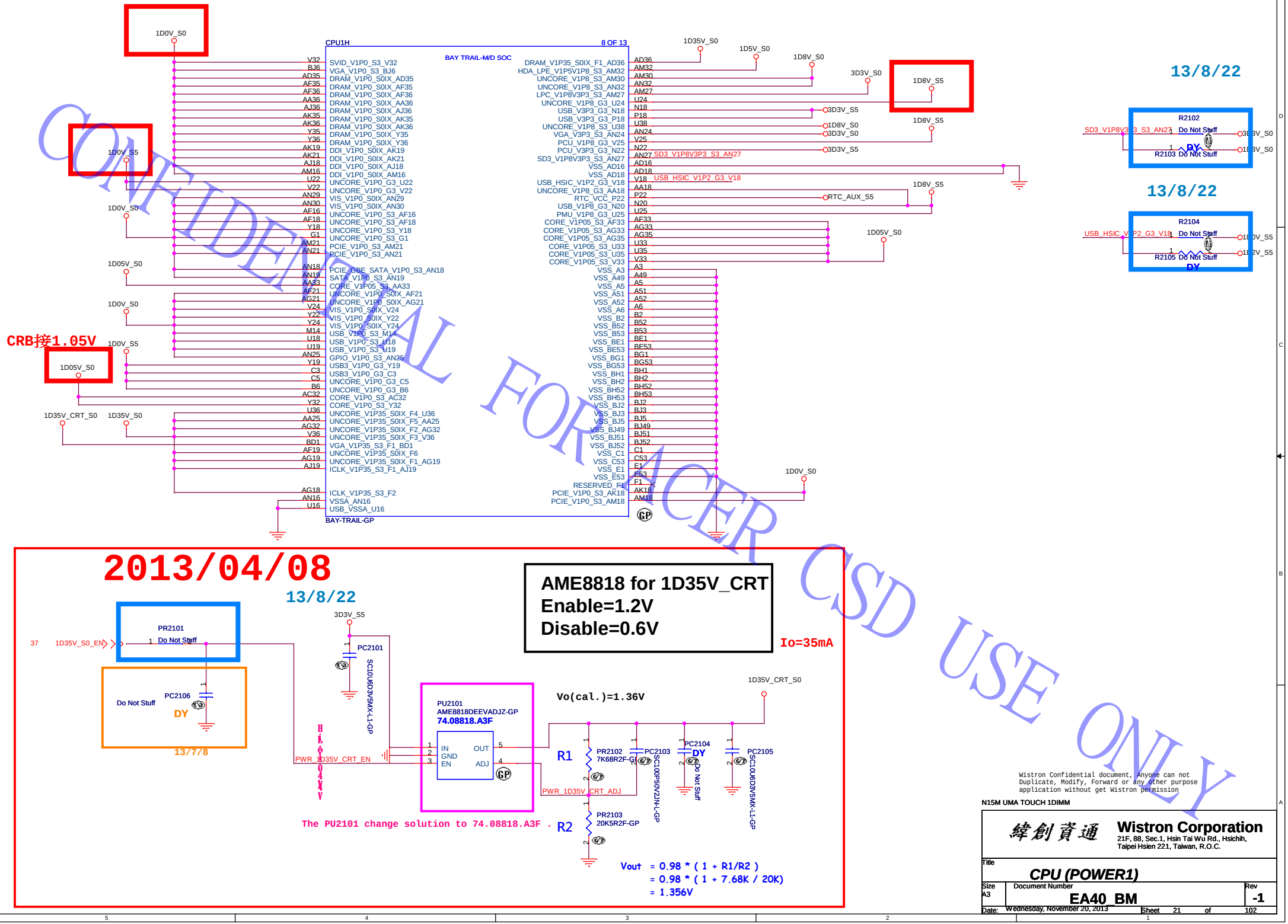
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 20 of 102



N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A3 | Document Number: EA40_BM | Rev: -1

Date: Wednesday, November 20, 2013 | Sheet 21 of 102

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 22 of 102

SSID = PCH

Blanking

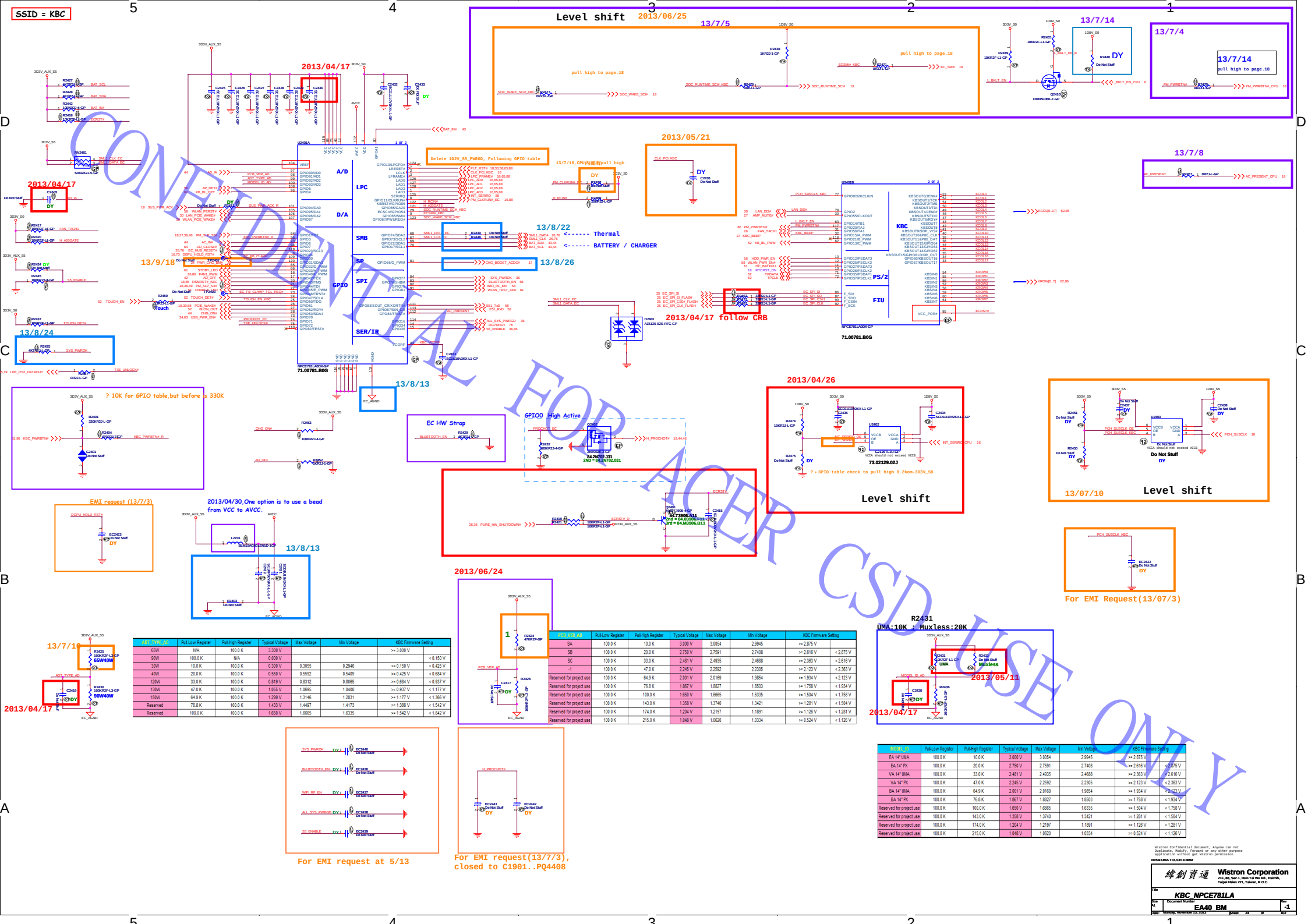
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 23 of 102



ADT_TYP_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V			>= 3.000 V
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2946	>= 0.150 V < 0.425 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V < 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8312	0.8065	>= 0.684 V < 0.937 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V < 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	1.2831	>= 1.177 V < 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V < 1.542 V
Reserved	100.0 K	100.0 K	1.659 V	1.6865	1.6335	>= 1.542 V < 1.842 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
SB	100.0 K	20.0 K	2.759 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.524 V	< 1.126 V

MODEL_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
EA 14" UMA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
EA 14" PX	100.0 K	20.0 K	2.759 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
VA 14" UMA	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
VA 14" PX	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
BA 14" UMA	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
BA 14" PX	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.524 V	< 1.126 V

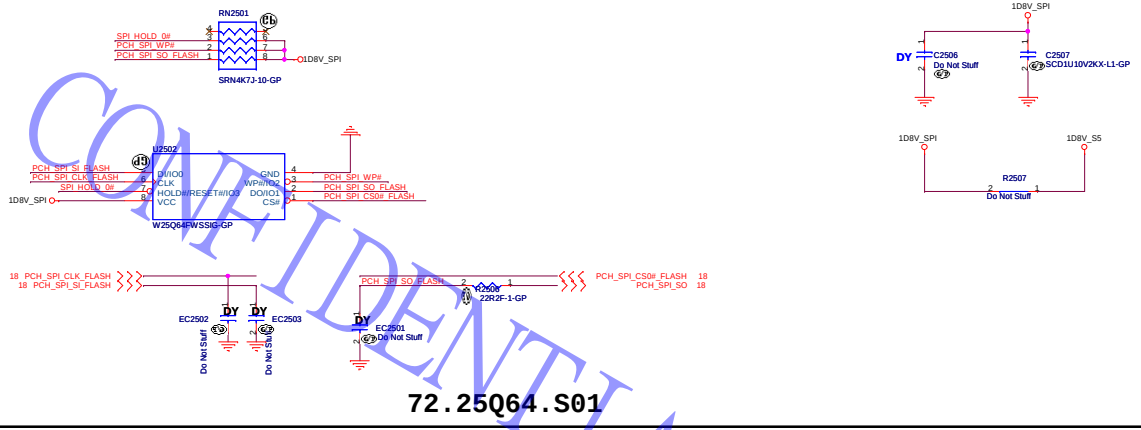
N15M UMA TOUCH SDIMM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_NPCE781LA
Size: A4 | Document Number: EA40_BM | Rev: -1
Date: Monday, November 25, 2013 | Sheet 28 of 102

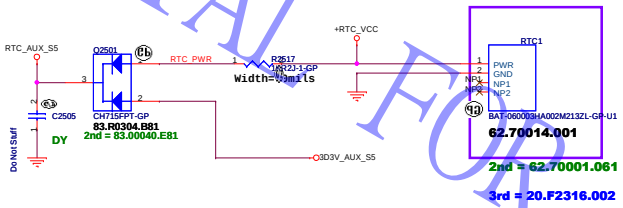
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



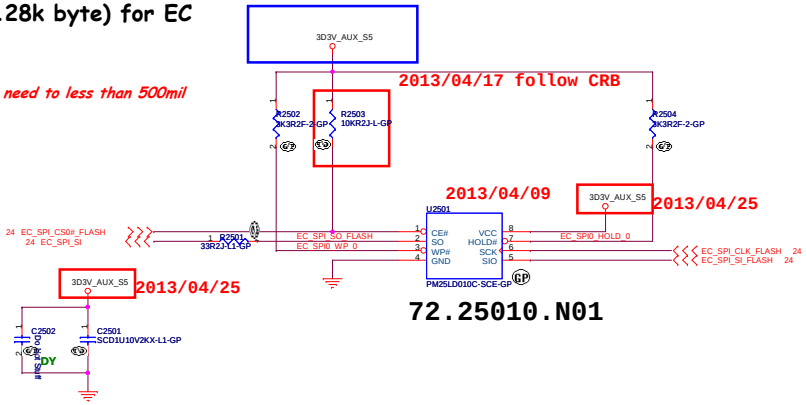
72.25Q64.S01

SSID = RBAT



SPI FLASH ROM (128k byte) for EC

SPI ROM Equal length need to less than 500mil



72.25010.N01

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC

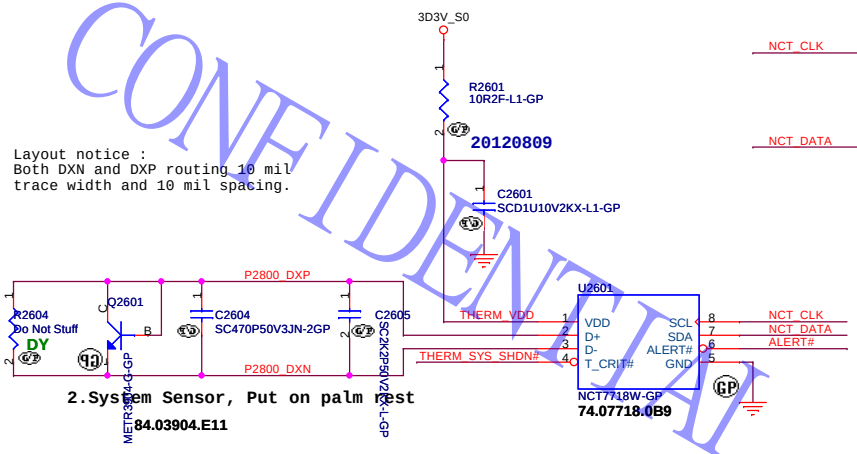
Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 25 of 102

SSID = Thermal

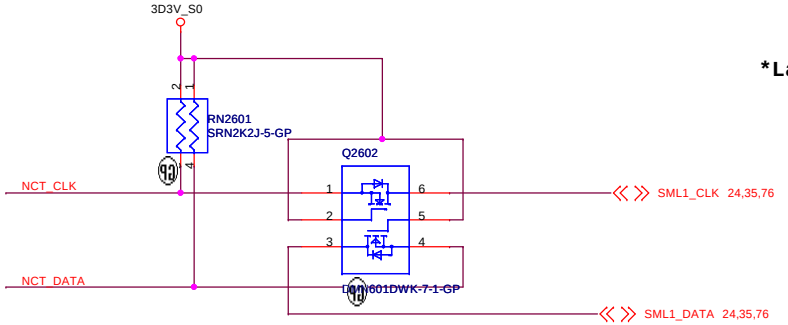
Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

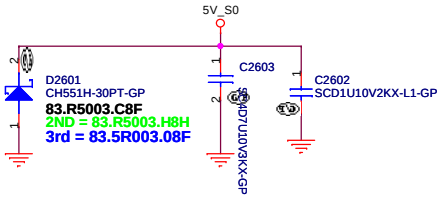


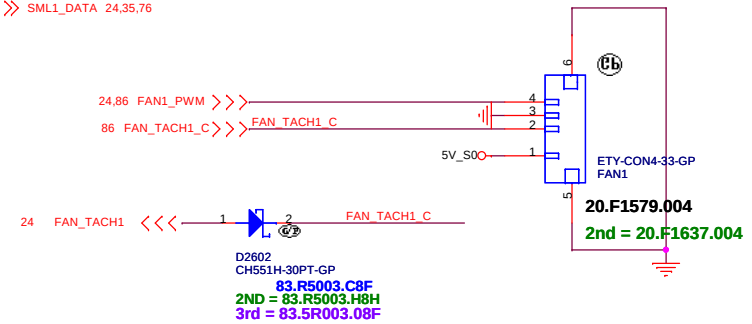
2.System Sensor, Put on palm rest
84.03904.E11

1.H/W T8 Shutdown



Layout 15 mil



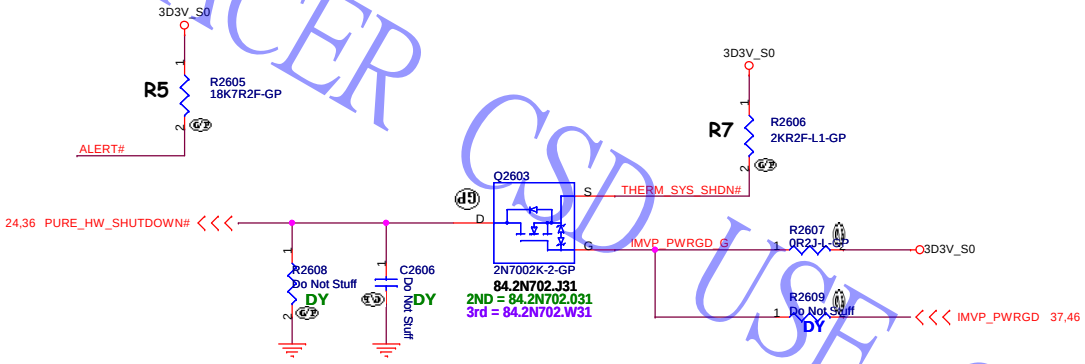


ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

T8=85 degree



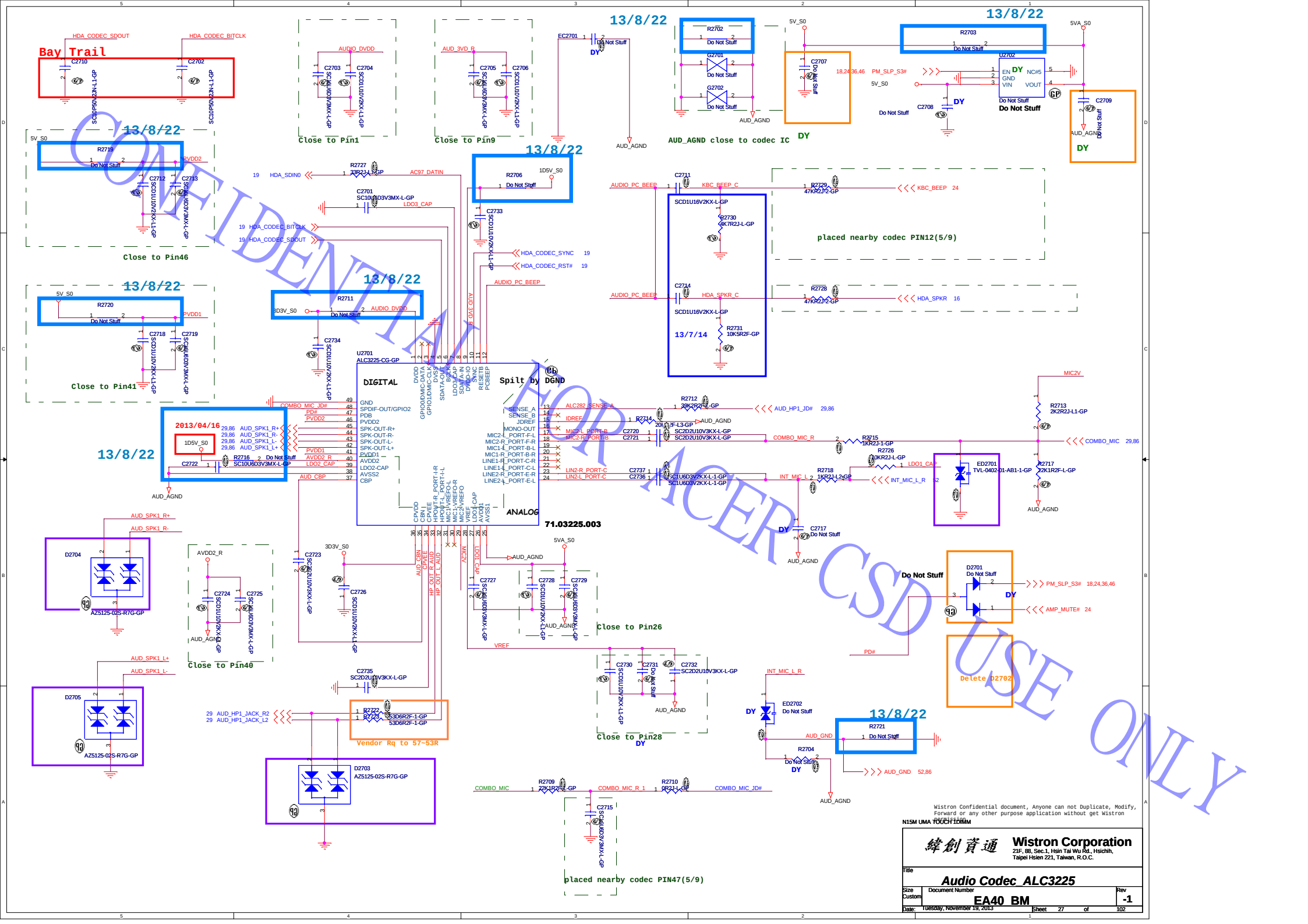
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

Size	Document Number	Rev
A3	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 26 of 102


Bay Trail
13/8/22
Close to Pin1
Close to Pin9
AUD_AGND close to codec IC
Close to Pin46
Close to Pin41
Close to Pin40
Close to Pin26
Close to Pin28
placed nearby codec PIN12(5/9)
placed nearby codec PIN47(5/9)
DIGITAL
ANALOG
Spilt by DGND
71.03225.003
U2701
ALC3225-CG-GP
2013/04/16
Vendor Rq to 57~53R
13/7/14
Delete D2702
Do Not Stuff
DY
Wistron Corporation
21F, 88, Sec.1. Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec_ALC3225
EA40_BM
-1
Tuesday, November 19, 2013
27
102
CONFIDENTIAL FOR ACER CSD USE ONLY

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

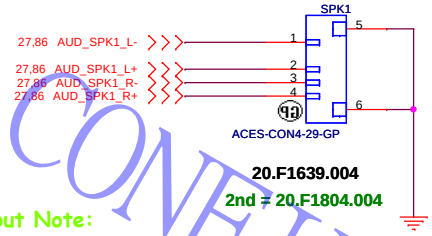
Title: ***Reserved***

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 28 of 102

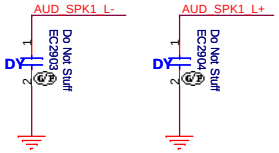
SSID = AUDIO

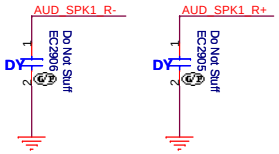
Speaker



20.F1639.004

2nd = 20.F1804.004



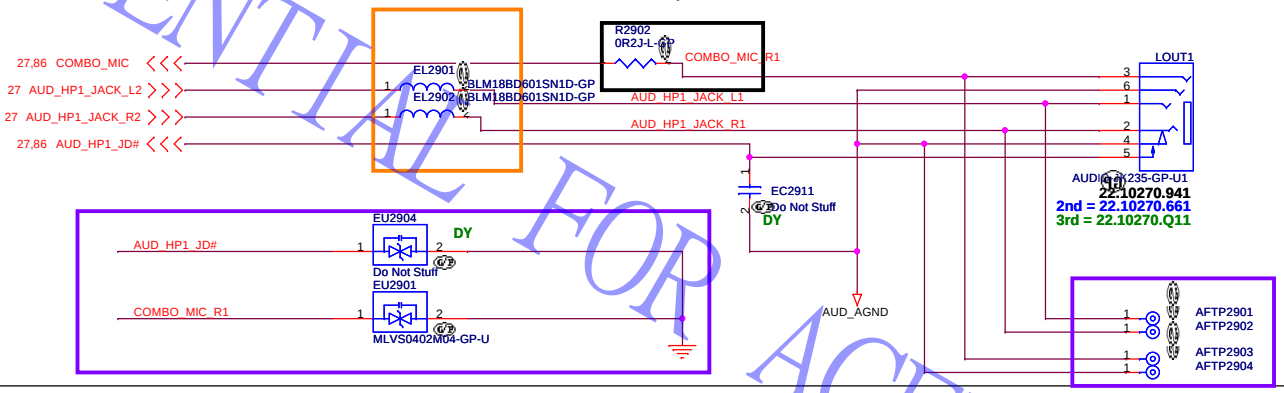


Layout Note:

Trace width=40mil

Combo Jack

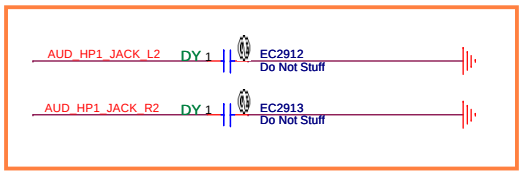
Vendor Rq



22.10270.941

2nd = 22.10270.661

3rd = 22.10270.Q11



reserve the 0402 0.1u caps on reset for EMI(5/9).

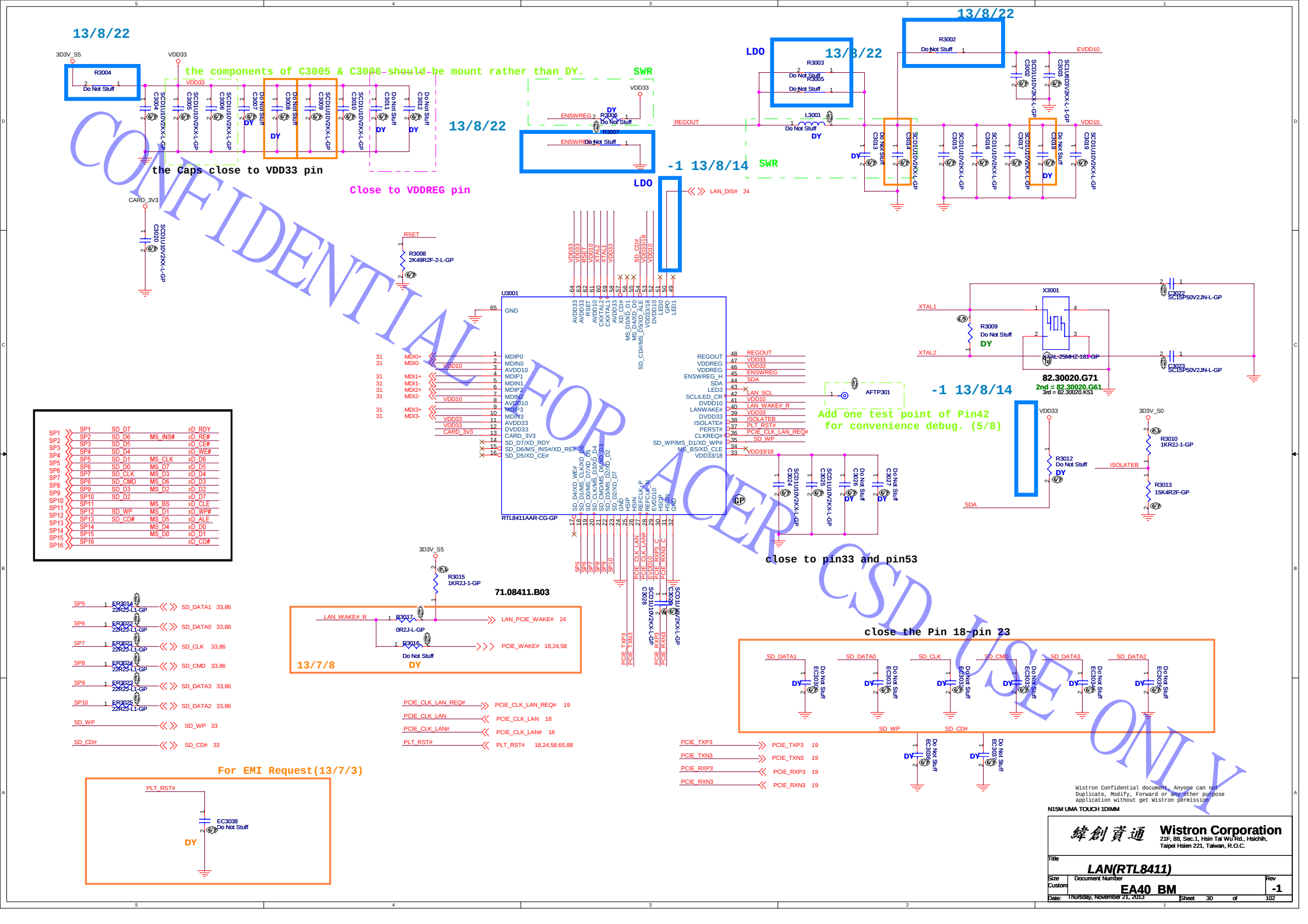
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

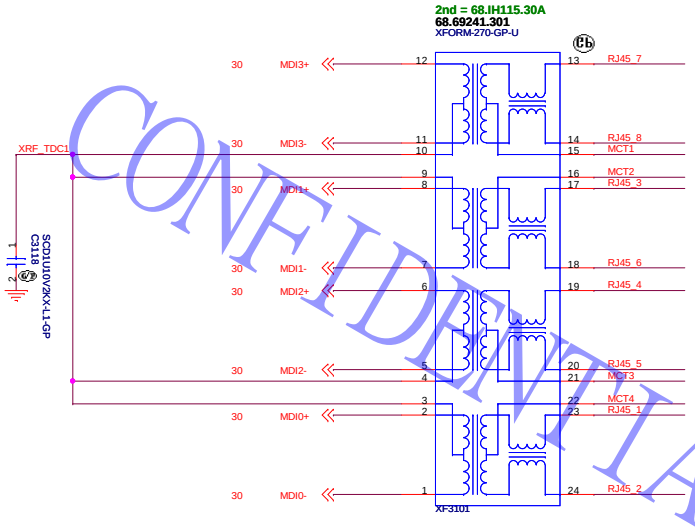
Title: Audio Jack

Size: Custom | Document Number: EA40_BM | Rev: -1

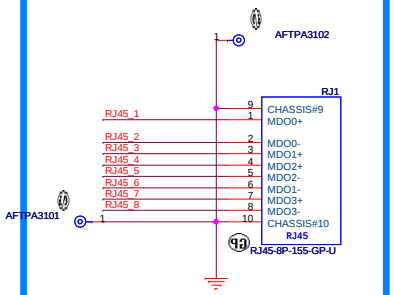
Date: Tuesday, November 19, 2013 | Sheet 29 of 102


13/8/22
the components of C3005 & C3006 should be mount rather than DY.
the Caps close to VDD33 pin
Close to VDDREG pin
SWR
LDO
-1 13/8/14
13/8/22
Add one test point of Pin42 for convenience debug. (5/8)
close to pin33 and pin53
close the Pin 18 pin 23
71.08411.B03
13/7/8
For EMI Request(13/7/3)
RTL8411AAR-CG-GP
82.30020.G71
2nd = 82.30020.G61
3rd = 82.30020.K51
CONFIDENTIAL FOR ACER CSD USE ONLY
Wistron Corporation
LAN(RTL8411)
EA40 BM
-1
Thursday, November 21, 2013
30
102

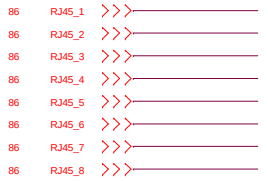
SSID = LAN



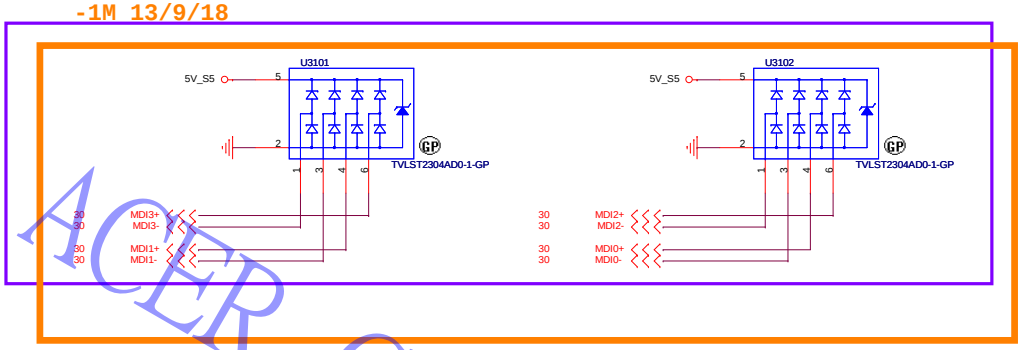
-1 13/8/14



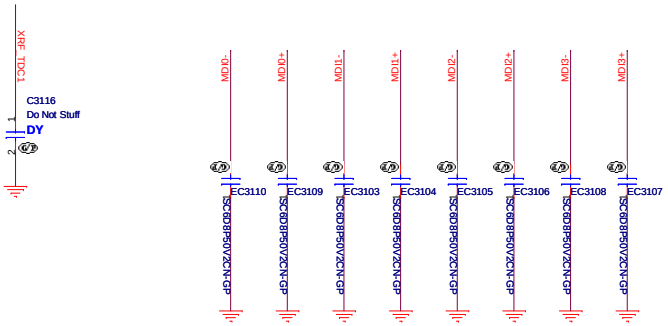
-1 13/8/14

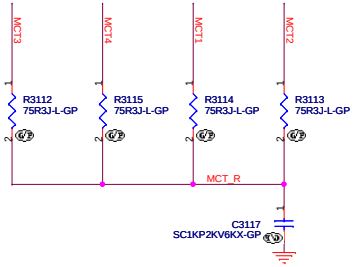


-1M 13/9/18



-1 13/8/14





N15M UMA TOUCH 1DIMM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (LAN+VGA) CONNECTOR

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 31 of 102

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

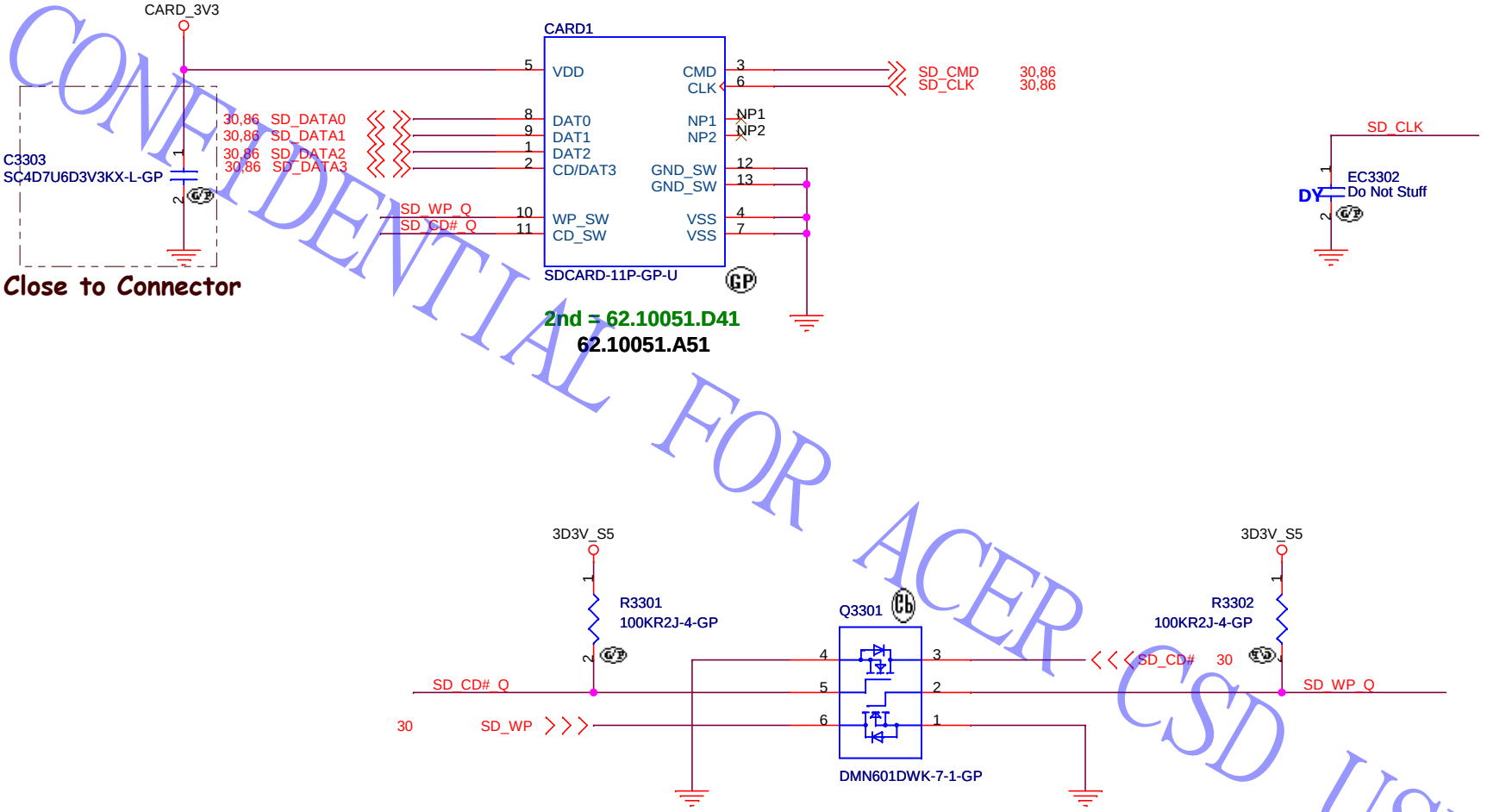
Title: *RTS5170(CARD READER)*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 32 of 102

SSID = SDIO

SD//MS Card Reader



86 SD_WP_Q

86 SD_CD#_Q

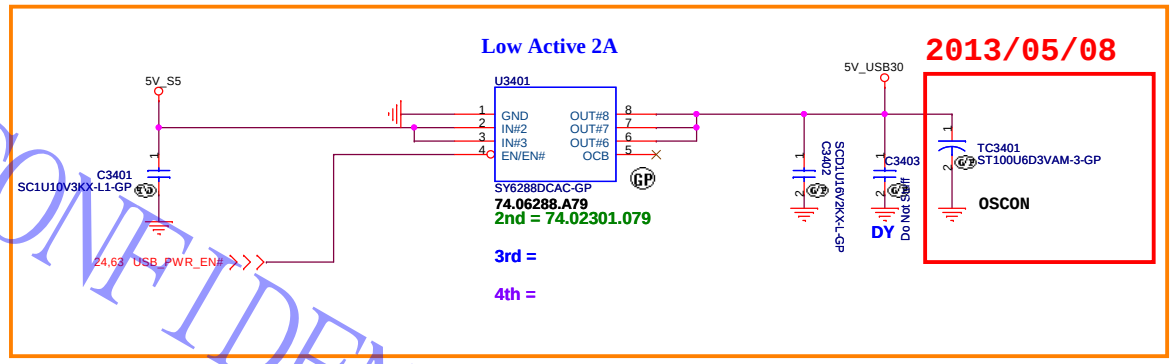
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

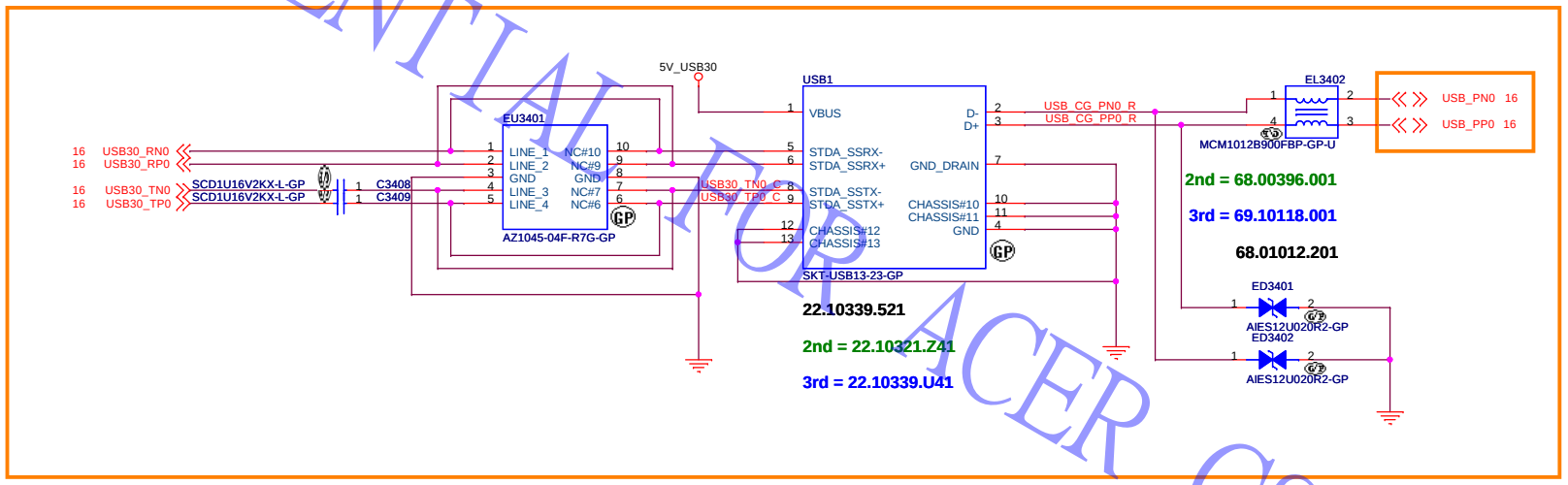
Title: CARD Reader CONN

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 33 of 102



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0 / 3.0 Port

Size: A3 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 34 of 102

USB Table

Pair	Device
1	WLAN(Bluetooth)
2	CCD
3	USB 2.0
4	

13/8/22

13/07/14
Del R3507

5V_S5
R3503 Do Not Stuff DY
HUB_RESET#
R3510 0R2J-L-GP
C3512 Do Not Stuff DY
R8803 Do Not Stuff DY
13/07/15

EC_HUB_RESET# 24

R3518 10KR2J-3-GP
3D3V_S5
HUB_PSELF

U3501
GL850G-OHY31-GP

3D3V_HUB
AVDD AVDD AVDD DVDD
V5
V33
DVDD1_HUB
C3501 SCD1U10V2KX-L1-GP
AVDD5V
3D3V_HUB
HUB_XSCI
HUB_XSCO
X1
X2
R3501 619R2F-L1-GP
RREF
HUB_RESET#
HUB_PSELF
HUB_PGANG
RESET#
PSELF
PGANG
HUB_TEST/SCL
HUB_SDA
TEST/SCL
SDA
GND
TP3501
TP3502

DP0 DM0 DP1 DM1 DP2 DM2 DP3 DM3 DP4 DM4
USB_PP1
USB_PN1
USB_HUB_PP2
USB_HUB_PN2
USB_HUB_PP3
USB_HUB_PN3
USB_BT_PP1
USB_BT_PN1
HUB_DP4
HUB_DM4

USB_PP1 16
USB_PN1 16
USB_HUB_PP2 63,86
USB_HUB_PN2 63,86
USB_HUB_PP3 63,86
USB_HUB_PN3 63,86
USB_BT_PP1 58,86
USB_BT_PN1 58,86

USB 2.0
USB 2.0
WLAN(Bluetooth)

OVCUR1#/SMC
OVCUR2#/SMD
OVCUR3#
OVCUR4#
HUB_SML1_CLK
HUB_SML1_DATA
R3511 0R2J-L-GP
R3512 0R2J-L-GP

13/9/18
13/8/22
SML1_CLK 24,26,76
SML1_DATA 24,26,76

POLY-FUSE CIRCUIT

3D3V_HUB
C3503 C3504 C3505 C3506 C3509
SCD1U10V2KX-L1-GP
As close to GL850G-32

3D3V_HUB
R3508 0R2J-L-GP
DVDD1_HUB
C3404 SC10U10V5KX-L1GP
C3514 SCD1U10V2KX-L1-GP
EC1 close to PIN28

13/8/22
3D3V_S5 3D3V_S5 3D3V_S5 3D3V_S5
R3521 DY Do Not Stuff
R3524 DY Do Not Stuff
R3525 10KR2J-L-GP
R3526 10KR2J-L-GP
HUB_SML1_CLK
HUB_SML1_DATA
OVCUR3#
OVCUR4#
PM 13/11/19

3D3V_S5
HUB_DP4 R3522 1KR2J-1-GP
HUB_DM4 R3523 1KR2J-1-GP

OVCUR1#~4# Floating : Non-Removable
(Compound device)

R3509
3D3V_HUB 0R2J-L-GP 3D3V_S5
AVDD5V 0R2J-L-GP R3520 5V_S5
C3518
C3519 SC2D2U10V3KX-1GP
SC4D7P50V2CN-1GP
13/07/15

Individual Mode
HUB_PGANG
R3519 100KR2J-4-GP

higher cost, change to 78.12034.1F1N5(5/9)
C3510 SC12P50V2JN-3GP HUB_XSCO
C3511 SC12P50V2JN-3GP HUB_XSCI
X3501
XTAL-12MHZ-67-GP

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

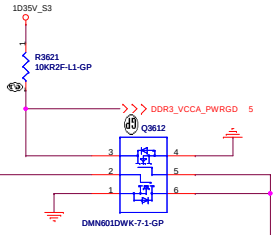
Title: USB HUB
Size: Custom
Document Number: EA40 BM
Rev: -1
Date: Tuesday, November 19, 2013
Sheet 35 of 102

Power Sequence

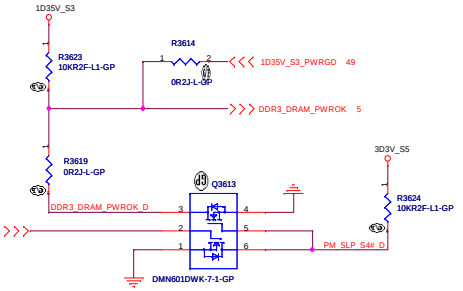
Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

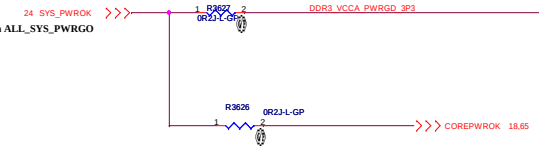
DDR3_VCCA_PWRGD



DDR3_DRAM_PWROK



From EC



COREPWROK

ALL_SYS_PWRGD

13/8/22

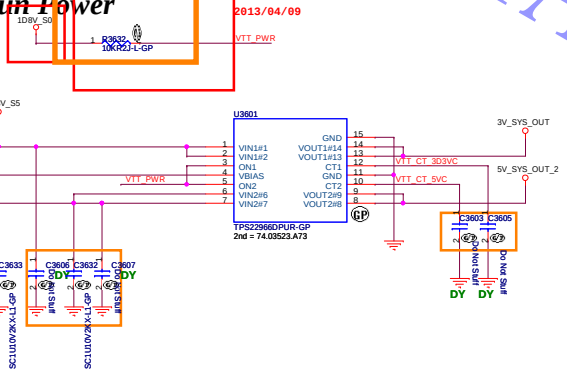
To EC

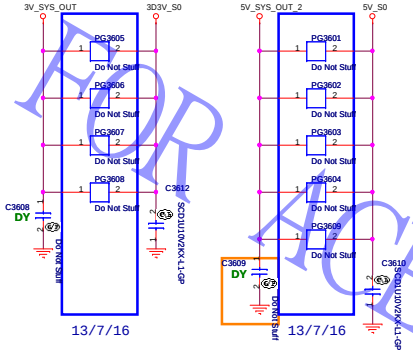
ANNIE Run Power

13/9/18

2013/04/12

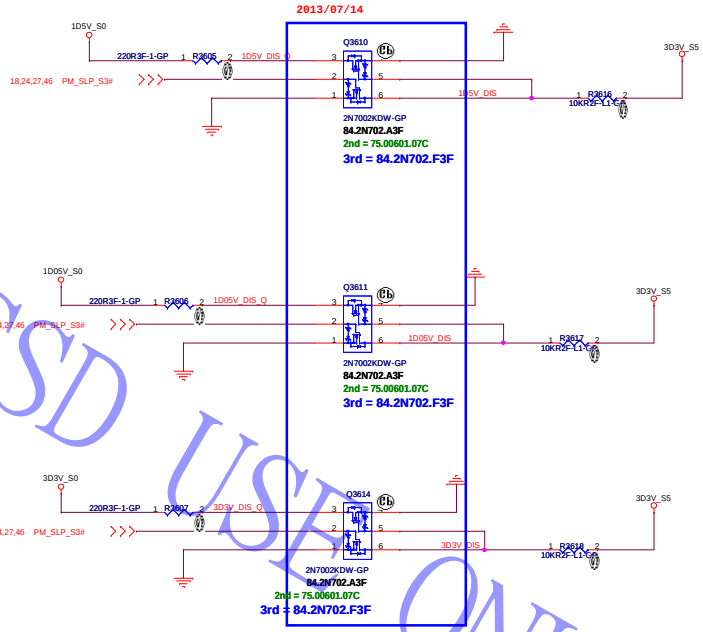
2013/04/09

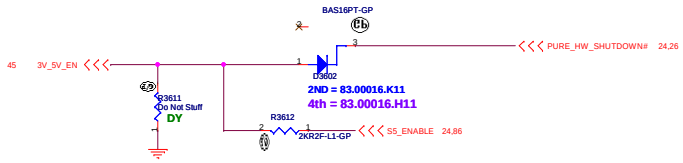




Discharge circuit

2013/07/14





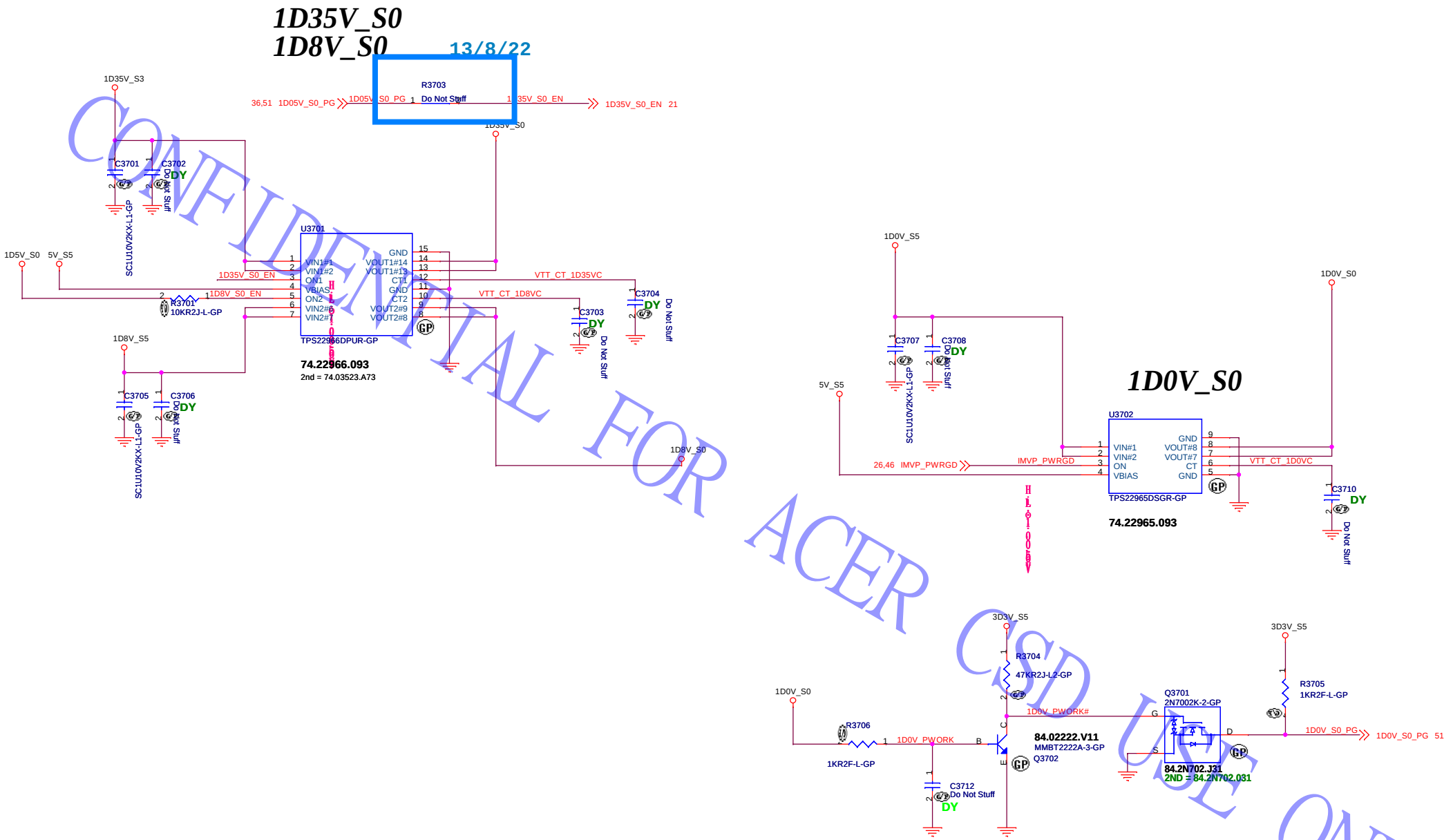
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 36 of 102



N15M UMA TOUCH 1DIMM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER OCP / S3 reduction**

Size	Document Number	Rev
A3	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 37 of 102

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **EA40_BM**	Rev **-1**
Date: Tuesday, November 19, 2013	Sheet 38 of 102	

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 39 of 102

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **EA40_BM**	Rev **-1**
Date: Tuesday, November 19, 2013	Sheet 40 of 102	

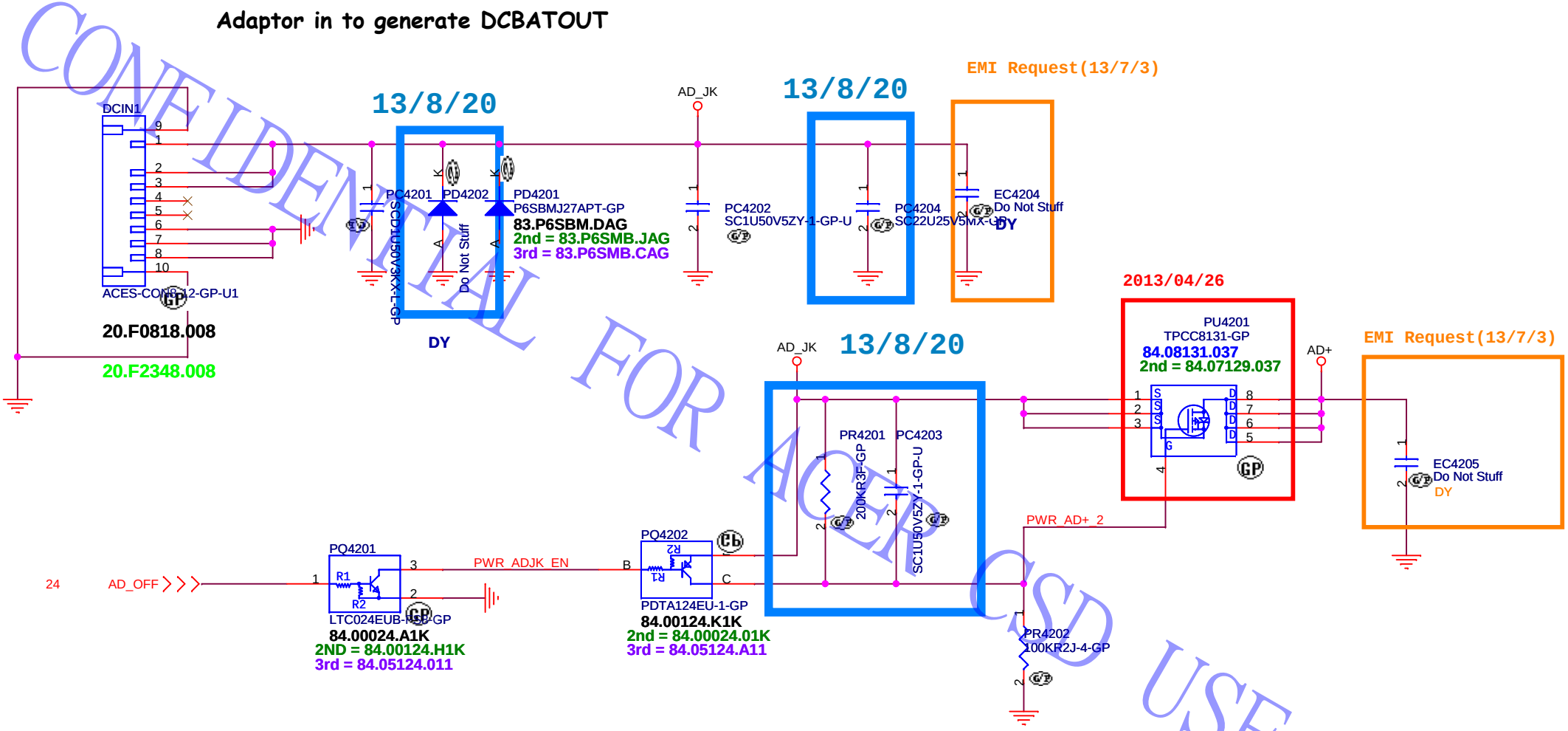
Blanking

N15M UMA TOUCH 1D IMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **EA40 BM**	Rev **-1**
Date: Tuesday, November 19, 2013	Sheet 41 of 102	

ANNIE solution



N15M UMA TOUCH 1DIMM

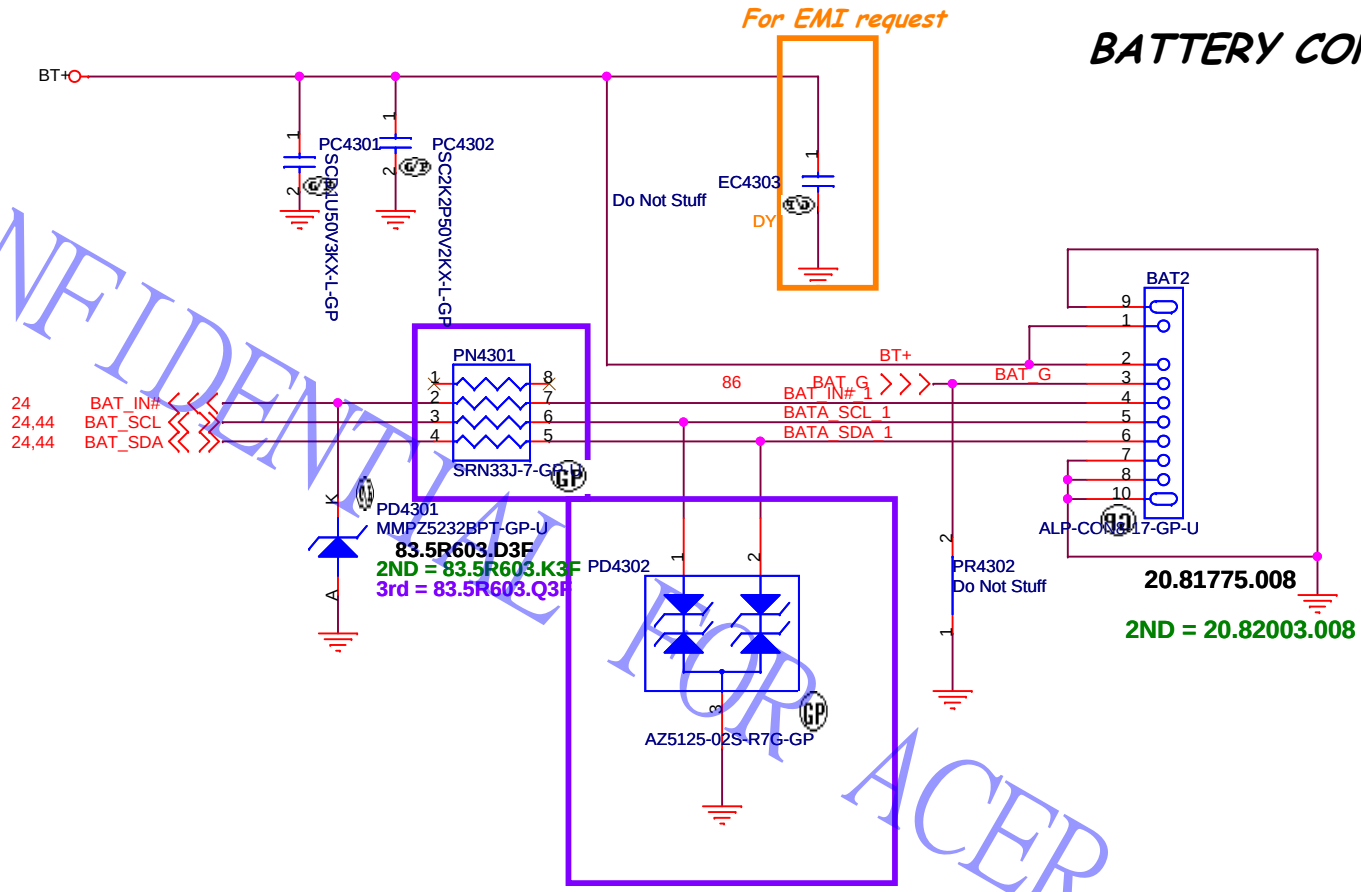
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 42 of 102

BATTERY CONNECTOR



86 BAT_IN#_1 — BAT_IN#_1
86 BATA_SCL_1 — BATA_SCL_1
86 BATA_SDA_1 — BATA_SDA_1

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A4	EA40 BM	-1

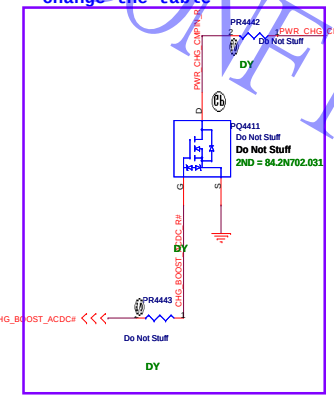
Date: Tuesday, November 19, 2013 Sheet 43 of 102

SSID = Charger

SSID = Charger

AD+ total power	R1	R2
65w	12.1K	100K

change the table



N15M UMA TOUCH 1DIMM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

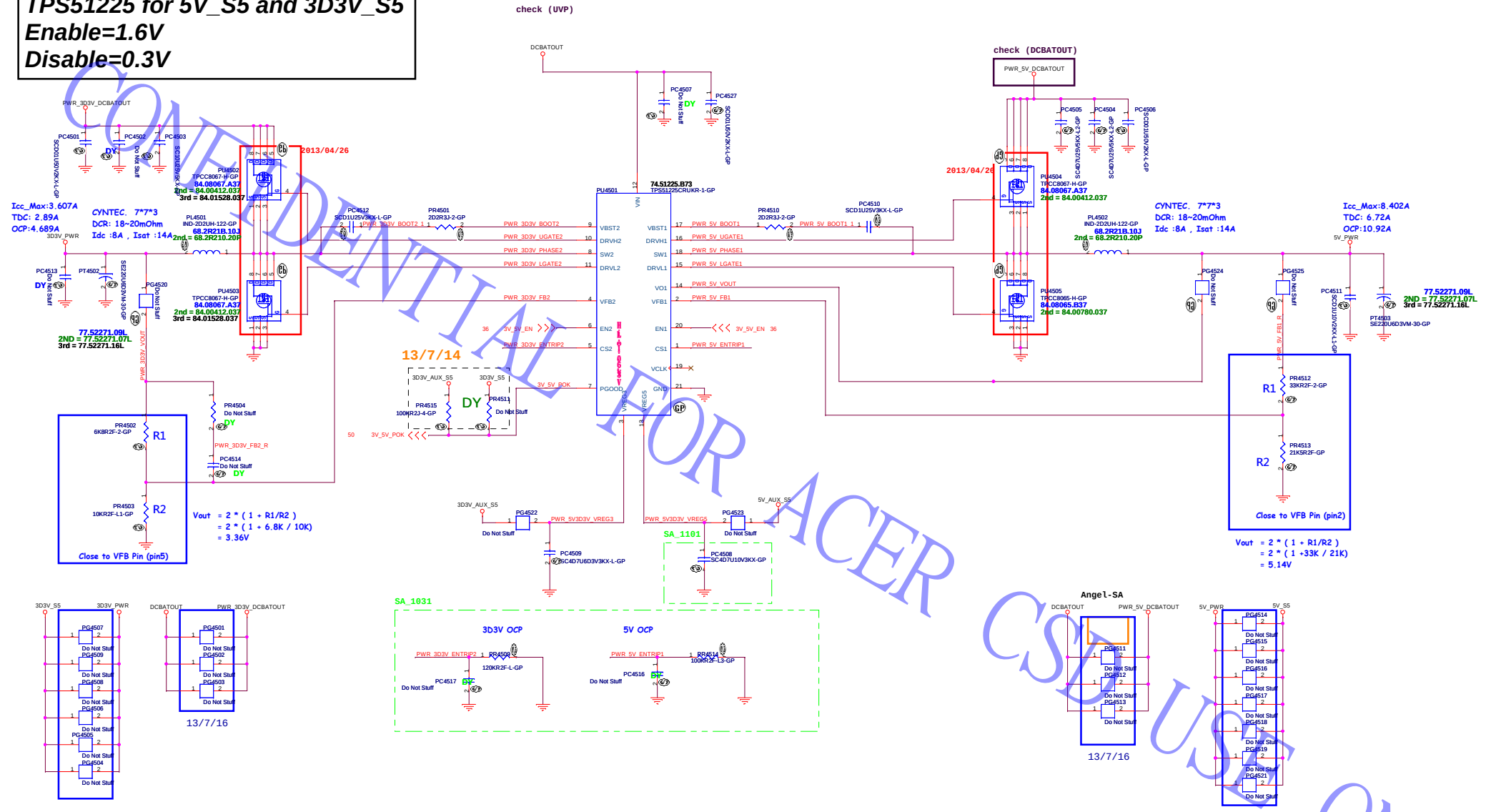
Title: CHARGER_BQ24727

Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 44 of 102

SSID = PWR.Plane.Regulator_3p3v5v

TPS51225 for 5V_S5 and 3D3V_S5
Enable=1.6V
Disable=0.3V



N15M UMA TOUCH 1DIMM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51225 5V/3D3V**

Size	Document Number	Rev
A2	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 45 of 102

SSID = CPU.Regulator

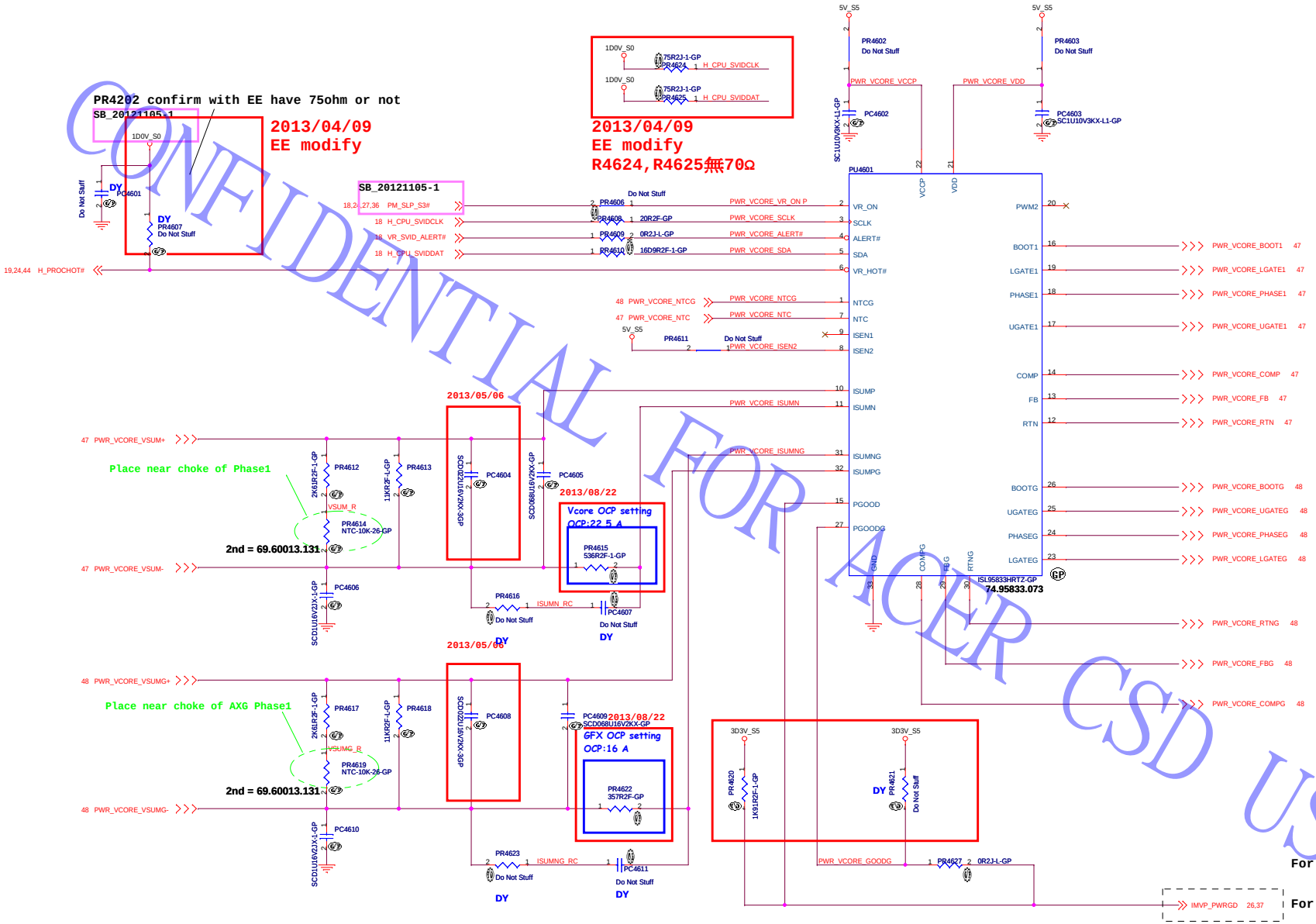
SB_20121105-1

PR4202 confirm with EE have 75ohm or not

SB_20121105-1

2013/04/09
EE modify

2013/04/09
EE modify
R4624,R4625無70Ω



N15M DMA TOUCH 1DMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_CPUCORE(1/3)

Size: C | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 46 of 102

SB_20121105-1

BOM control

	Main source	2nd source
PU4701	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

BOM control

2013/04/26

PU4701 FDMS3600-02-R-K0215-COLAY-GP

1st = 84.00920.037

2nd = 84.08107.B37

DCBATOUT

PC4702 SC10U25V5KX-GP

PC4703 SC10U25V5KX-GP

PC4704 SC470U25V5KX-GP

2D2R3F-L-GP PR4701

PC4701 SCD22U25V3KX-3-GP

46 PWR_VCORE_BOOT1

46 PWR_VCORE_UGATE1

46 PWR_VCORE_PHASE1

46 PWR_VCORE_LGATE1

BOOT1_RC

Pana . 7 x 7 x 4

DCR 1.8~2.3 mOhm

Isat : 32A

2013/08/22

PL4701 IND-D36UH-42-GP

68.R361A.10B

VCC_CORE

PT4702 SE560U2D5VM-9-GP

77.55671.06L

2nd = 77.55671.03L

3rd = 77.55671.05L

PG4701 Do Not Stuff

PG4708 Do Not Stuff

PR4702 3K83R2F-GP

16K9R2F-GP PR4703

PR4704 NTC-470K-8-GP

2nd = 69.60013.141

NTC_RC

PWR_VCORE_NTC 46

NTC Place near high side MOSFET of Phase1

PR4705 3K65R2F-1-GP

PR4706 1R2F-L-GP

46 PWR_VCORE_VSUM+

46 PWR_VCORE_VSUM-

PWR_VCORE_VSUM+_GAP

PWR_VCORE_VSUM-_GAP

Parallel

46 PWR_VCORE_COMP

46 PWR_VCORE_FB

PR4707 64K9R2F-1-GP

Vboot setting

Vout = 1.1V

SC470P50V2KX-3GP

PR4708 499R2F-2-GP

PC4705

FB_RC

PC4706 SC470P50V2JN-3GP

2013/04/26

PR4709 2K32R2F-1-GP

Vcore LL setting

LL : 5.9mOhm

PR4710 267KR2F-GP

PC4707 SC150P50V2JN-3GP

COMP_RC

PC4708 SC680P50V2KX-2GP

COMP_R

PR4711 2KR2F-L1-GP

PC4709 Do Not Stuff

DY

PC4710 SCD01U50V2KX-L-GP

PR4712 Do Not Stuff

VCC_SENSE 7

VSS_SENSE 7

Parallel

46 PWR_VCORE_RTN

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_CPUCORE(2/3)

Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Friday, November 22, 2013 | Sheet 47 of 102

SB_20121105-1

BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

BOM control

2013/04/26

PU4801 FDMS3600-02-R-KO225-COLAY-GP

1st = 84.00920.037

2nd = 84.08107.B37

DCBATOUT

PC4802 SC10U25V5KX-GP

PC4803 SC10U25V5KX-GP

PC4804 SCAD71V5VSKX-GP

PC4805 Do Not Stuff DY

2D2R3F-L-GP PR4801

PC4801 SCD22U25V3KX-3-GP

BOOTG_RC

46 PWR_VCORE_BOOTG

46 PWR_VCORE_UGATEG

46 PWR_VCORE_PHASEG

46 PWR_VCORE_LGATEG

Pana . 7 x 7 x 4

DCR 1.8~2.3 mOhm

Isat : 32A

2013/08/22

PL4801 IND-D36UH-42-GP

68.R361A.10B

GFX_CORE

PT4801 SESS601U2D5VM-9-GP

77.55671.06L

2nd = 77.55671.03L

3rd = 77.55671.05L

GFX_CORE

PC4812 SC22U6D3V5MX-13-GP

PC4813 SC22U6D3V5MX-13-GP

PC4814 SC22U6D3V5MX-13-GP

PR4802 3K83R2F-GP

NTCG_RC

PR4803 16KR2F-GP

PR4804 NTC-470K-8-GP

2nd = 69.60013.141

PWR_VCORE_NTCG

PWR_VCORE_NTCG 46

NTC place near high side MOSFET of AXG Phase1

PG4801 Do Not Stuff

PG4802 Do Not Stuff

PR4805 3K65R2F-1-GP

PR4806 1R2F-L-GP

46 PWR_VCORE_VSUMG+

46 PWR_VCORE_VSUMG-

PWR_VCORE_VSUMG+_GAP

PWR_VCORE_VSUMG-_GAP

Parallel

46 PWR_VCORE_COMPG

46 PWR_VCORE_FBG

PR4807 21KR2F-GP

Freq. setting

FSW = 450KHz

2013/05/06

PR4808 499R2F-2-GP

FBG_RC

SC470P50V2KX-3GP PC4806

PC4807 SC47P50V2JN-3GP

PR4809 1K58R2F-GP

Vcore LL setting

LL : 5.9mOhm

2013/05/06

PR4810 2667KR2F-GP

COMPG_R

PC4808 SC150P50V2JN-3GP

PC4809 SC330P50V2KX-3GP

PR4811 2KR2F-L1-GP

PC4810 Do Not Stuff DY

SCD01U50V2KX-L-GP

PR4812 Do Not Stuff

46 PWR_VCORE_RTNG

VCC_AXG_SENSE 7

VSS_AXG_SENSE 7

Parallel

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_AGX_CORE(3/3)

Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v

# SY8208D for VDDQ
Enable=0.8V
Disable=0.4V

OCP setting	
High	16A
Float	12A
Low	8A

13/8/22

Freq=800KHz

PU4901 SY8208DQNC-GP-U 74.08208.K73

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

IccMAX = 8 A
IccTDC = 6.4A
OCP > 10.4 A

PWR_VDDQ_EN

PWR_VTT_EN

R1 PR4906 127KR2F-GP
R2 PR4907 100KR2F-L3-GP

Vo=0.6x(1+R1/R2)
=0.6x(1+127/100)
=1.362

+0.675VS
Iomax: 1.2A

VDDQ Vin

PU4902 APL5338XAI-TRG-GP 74.05338.079

Design Current = 2A
OCP = 3 A

0D675V Vout

VDDQ Enable

13/7/16

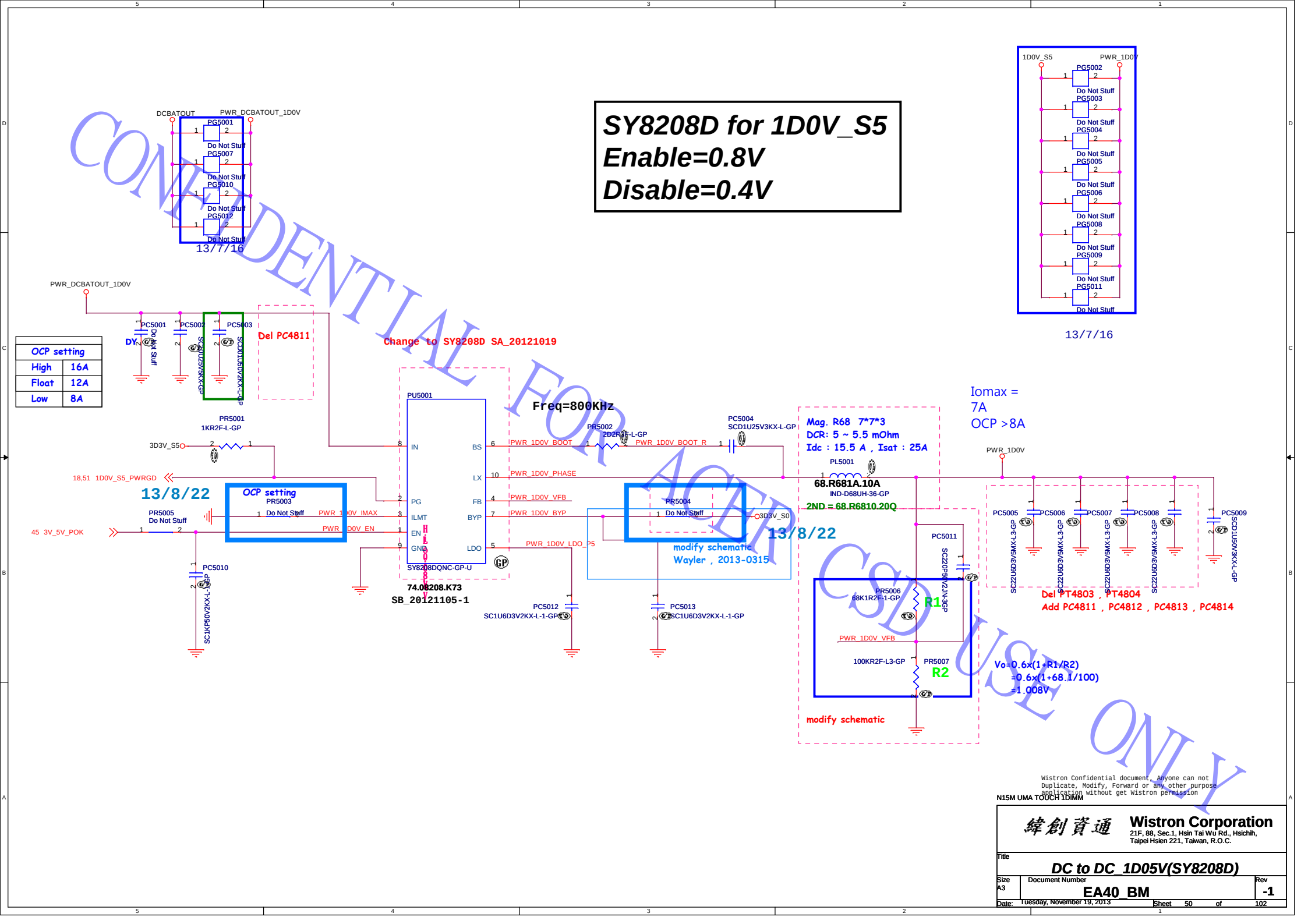
N15M UMA TOUCH 1DIMM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8208DQNC(1.35V_S3/0.675V_S0)

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 49 of 102



N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC_1D05V(SY8208D)

Size	Document Number	Rev
A3	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 50 of 102

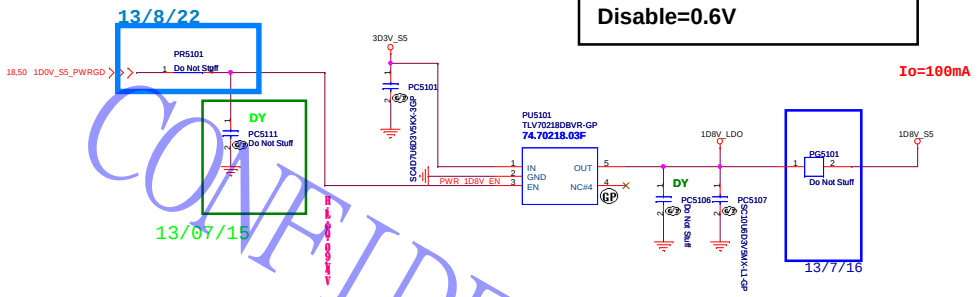
SSID = PWR.Plane.Regulator_1p8v

2013/04/18

TLV70218DBVR for 1D8V_S5
Enable=0.9V
Disable=0.6V

13/8/22

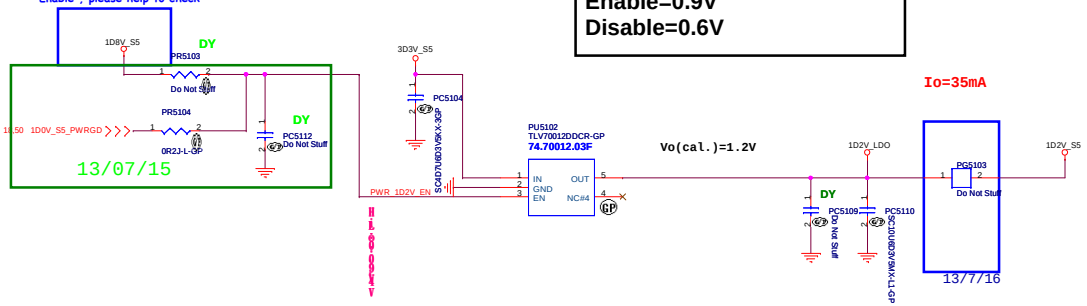
Io=100mA



Enable , please help to check

TLV70012DDCR for 1D2V_S5
Enable=0.9V
Disable=0.6V

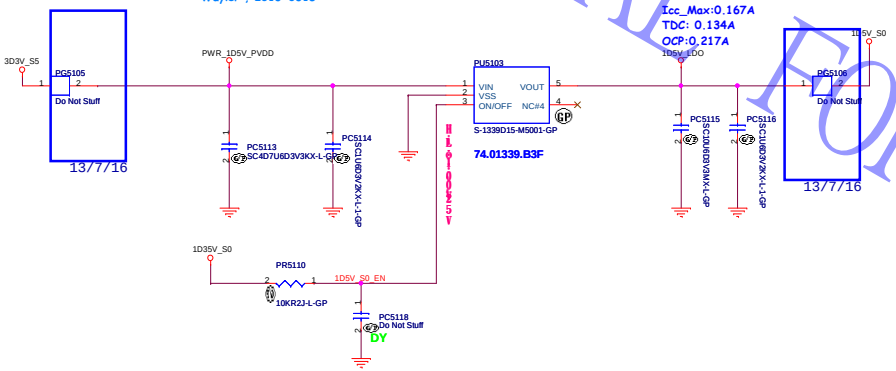
Io=35mA



S-1339D15 for 1D5V_S0
Enable=1.0V
Disable=0.25V

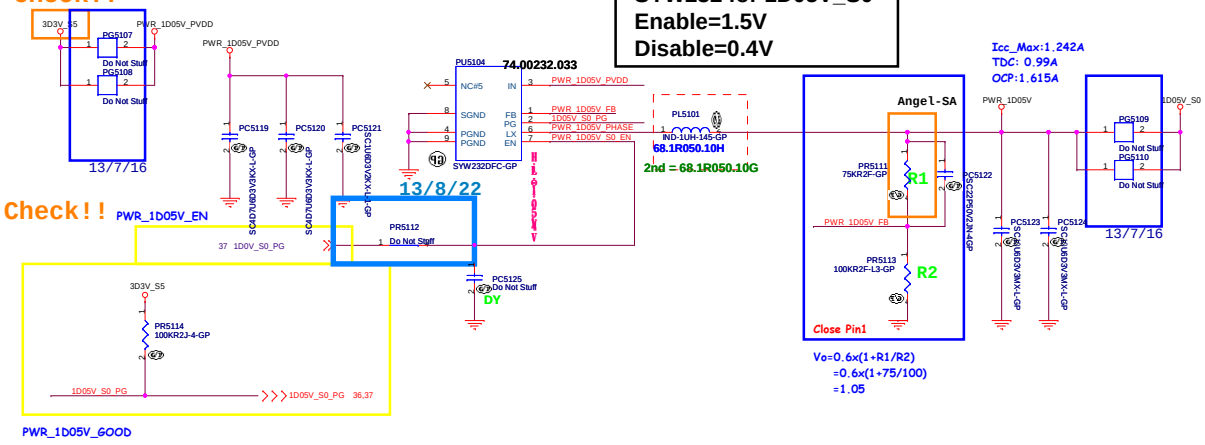
modify schematic
Wayler , 2013-0315

Io=100mA



SYW232 for 1D05V_S0
Enable=1.5V
Disable=0.4V

Check!!



Vo=0.6x(1+R1/R2)
=0.6x(1+75/100)
=1.05

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

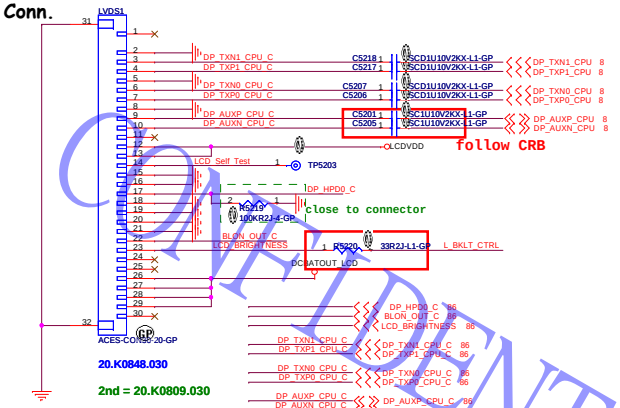
Title: LDO_1D8V&1D5V(RT9025)

Size	Document Number	Rev
A2	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 51 of 102

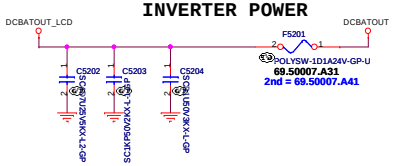
SSID = VIDEO

Panel Conn.

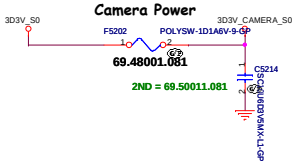


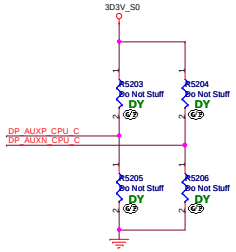
follow CRB

INVERTER POWER

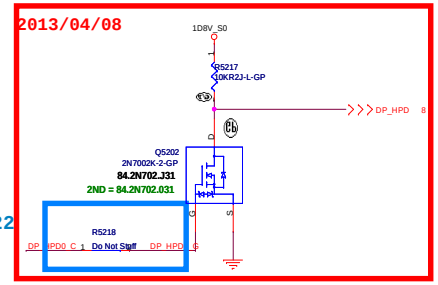


Camera Power





2013/04/08

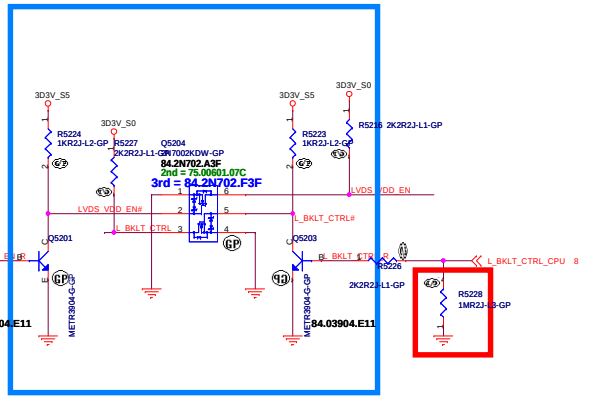


13/8/22

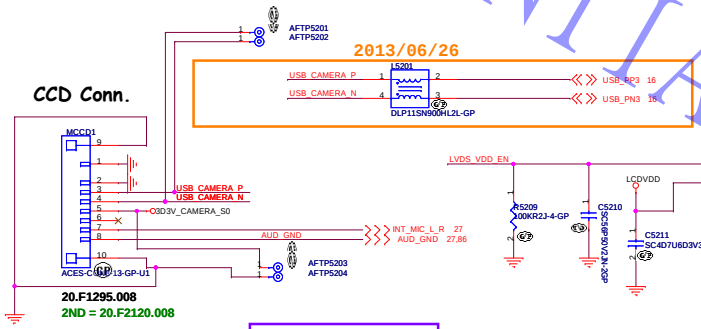
Level shift

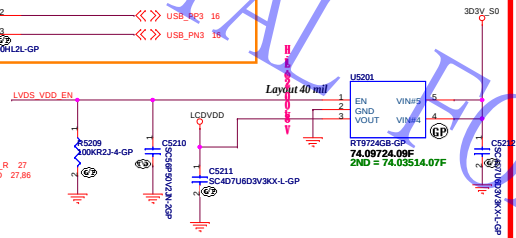
2013/04/10

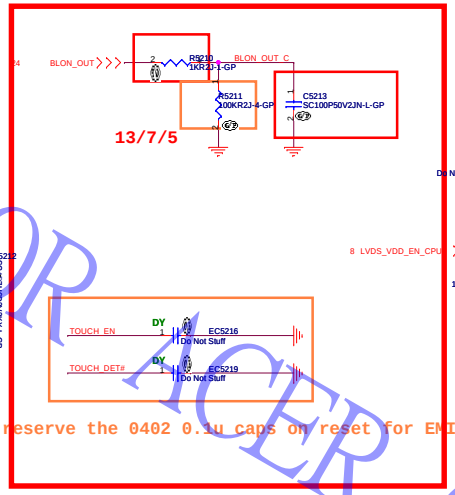
13/8/22

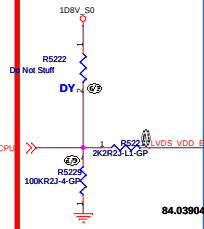


CCD Conn.

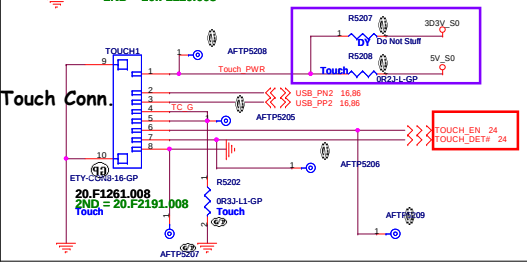


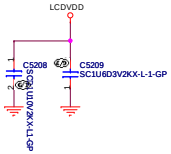






Touch Conn.





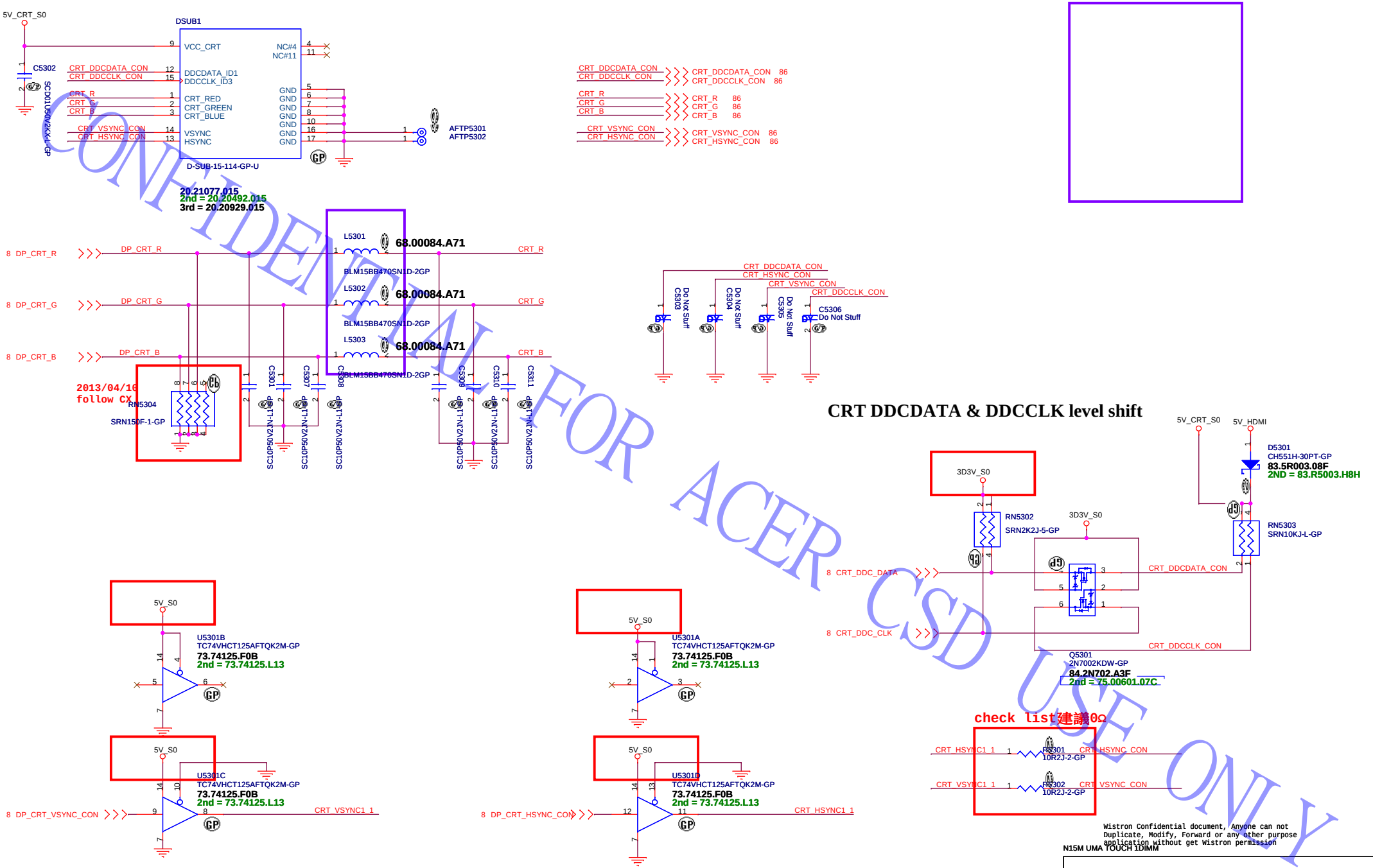
N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 52 of 102



N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

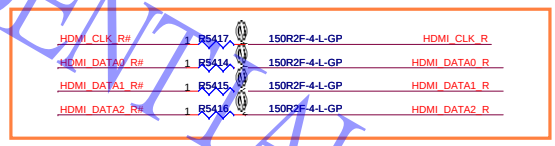
Title: CRT Connector

Size	Document Number	Rev
A3	EA40_BM	-1

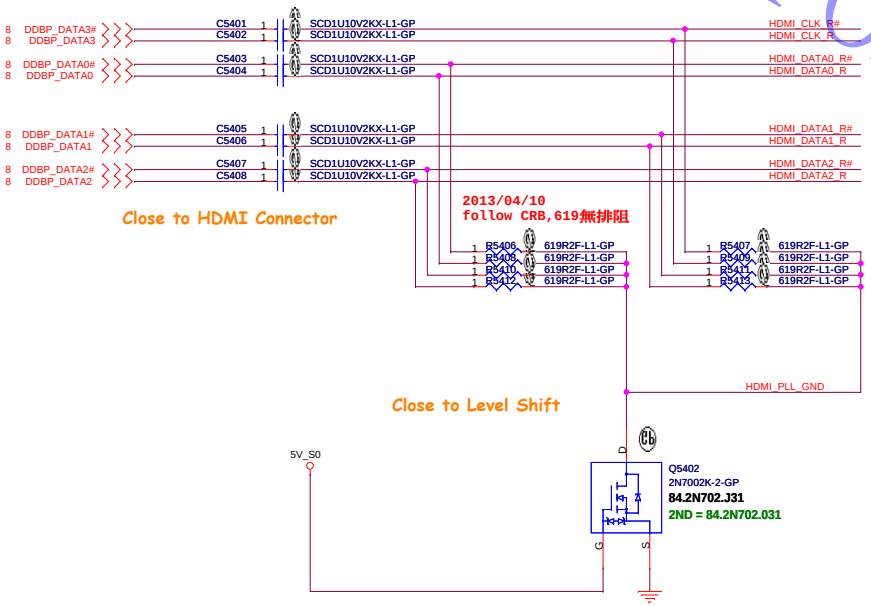
Date: Wednesday, November 20, 2013 Sheet 53 of 102

SSID = VIDEO HDMI Level Shifter & CONNECTOR

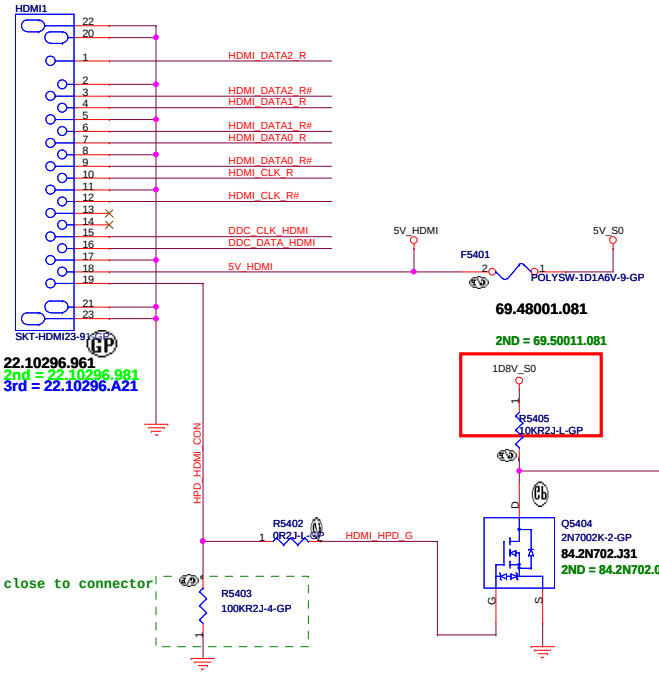
UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

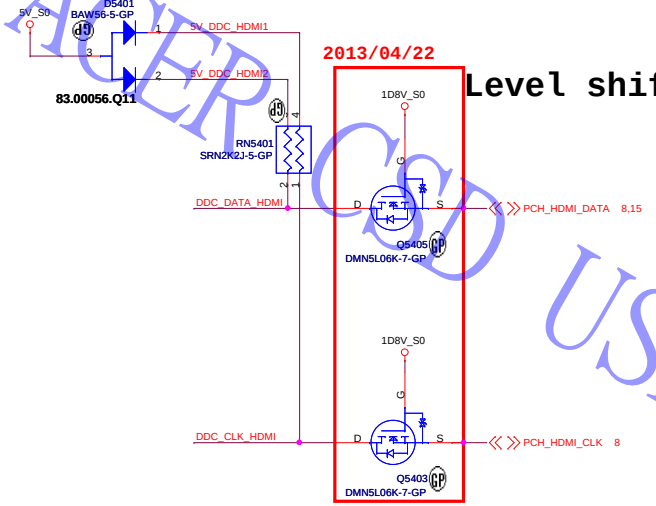


Reseve 150 ohm bridge resistance
on the HDMI trace as circle for EMI(5/9).



HDMI CONN





N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 54 of 102

SSID = Display Port

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

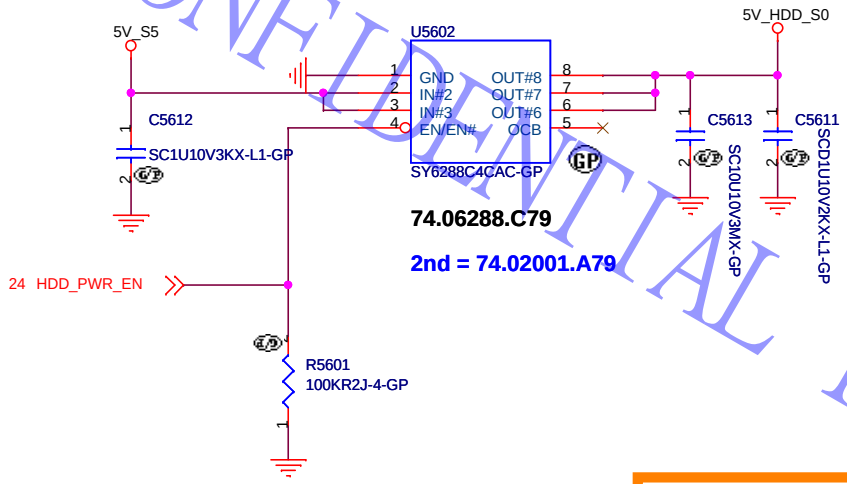
Title: *Reserved*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 55 of 102

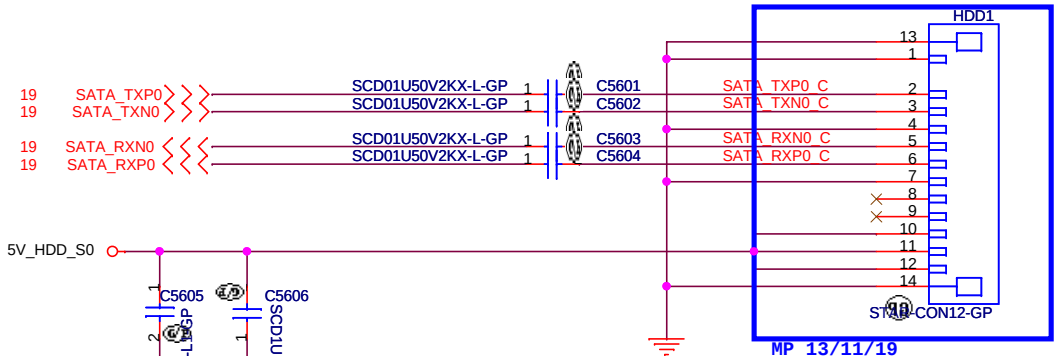
SSID = SATA

SATA HDD Connector



74.06288.C79

2nd = 74.02001.A79



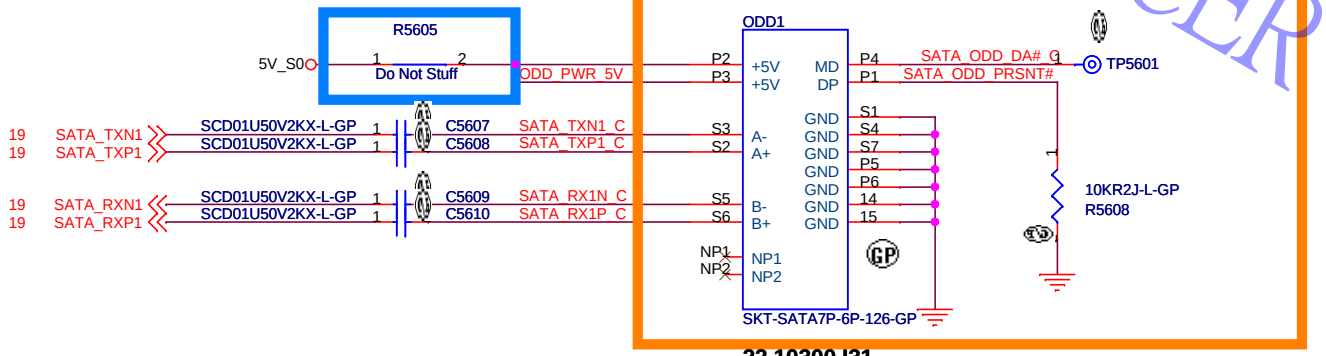
Change part number to 20.K0808.012(13/7/8)

AC coupling caps near connector<100 mils

EMI request(5/13)

Delete 12/7/14

ODD Connector 13/8/22



13/07/08

22.10300.I31

2nd = 22.10300.H91

3rd = 22.10300.J41

EMI request(7/8)

Delete 12/7/14

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD Connector

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 56 of 102

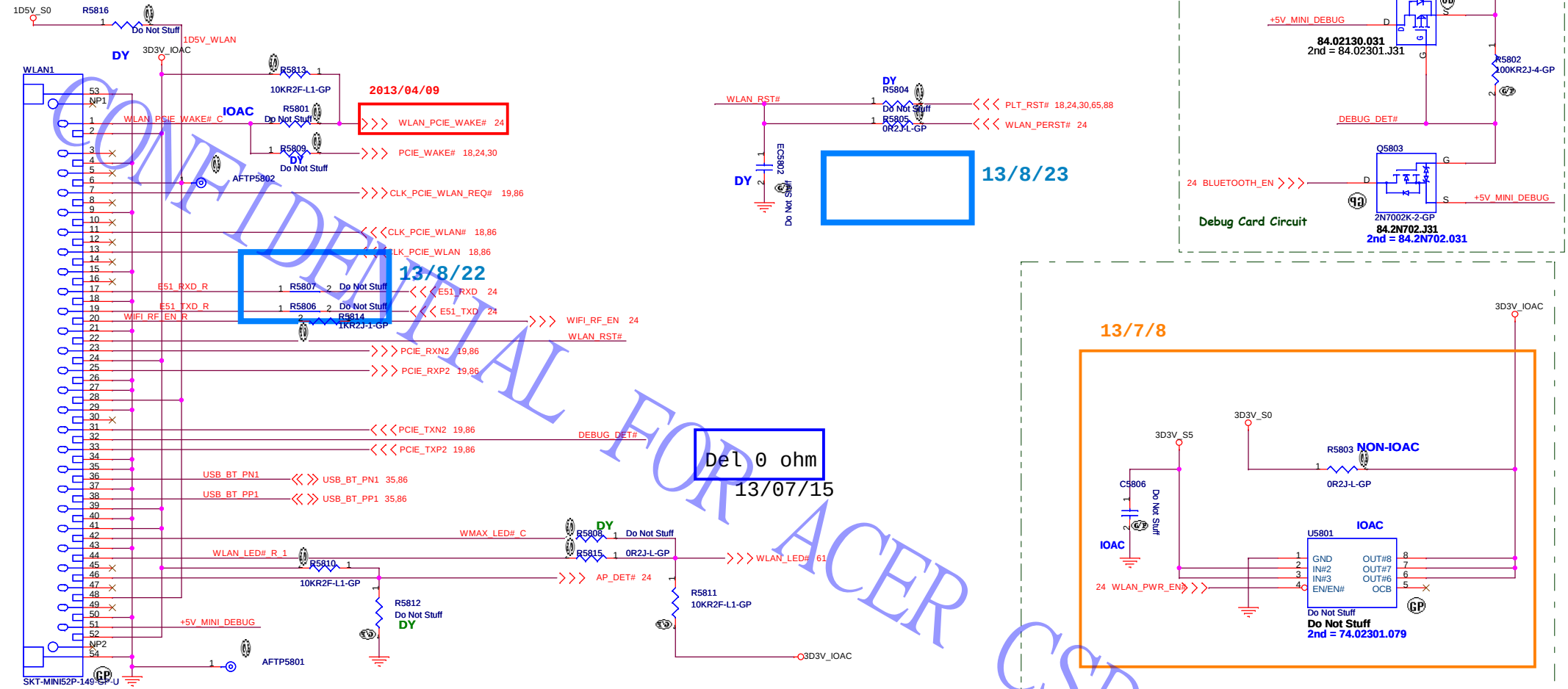
Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*		
Size: A4	Document Number: EA40 BM	Rev: -1
Date: Tuesday, November 19, 2013	Sheet 57 of 102	

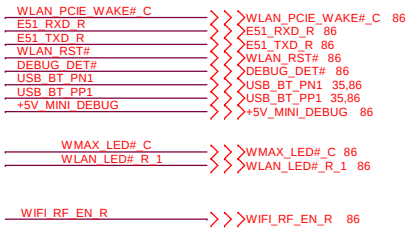
SSID = Wireless Mini Card Connector(802.11a/b/g/n)

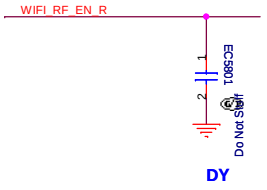


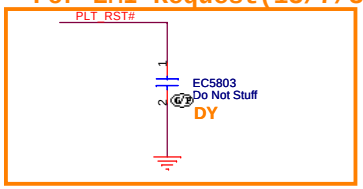
62.10043.I31

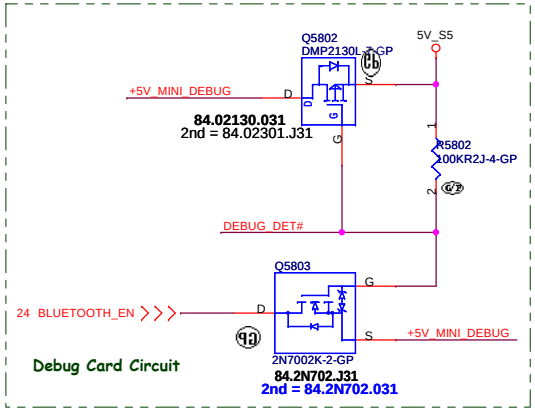
2nd = 62.10043.I51

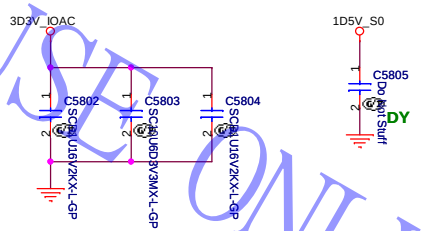
3rd = 62.10043.K81











N15M UMA 3QUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)

Size	Document Number	Rev
Custom	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 58 of 102

SSID = 3G

Mini Card Connector(WWAN)

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN CONN

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 59 of 102

SSID = mSATA

Mini Card Connector(mSATA)

Blanking

N15M UMA TOUCH 1D IMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

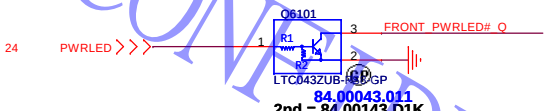
Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 60 of 102

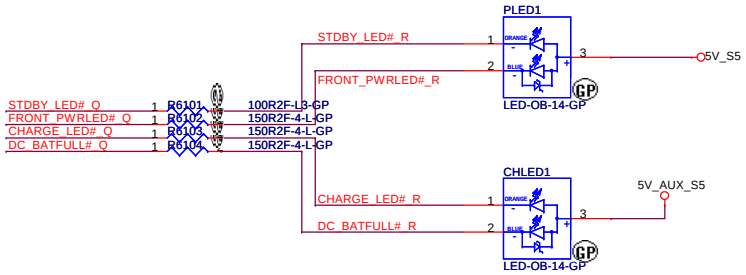
SSID = User.Interface

WLAN_LED

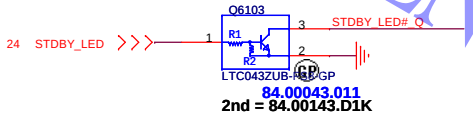
Power button LED



84.00043.011
2nd = 84.00143.D1K

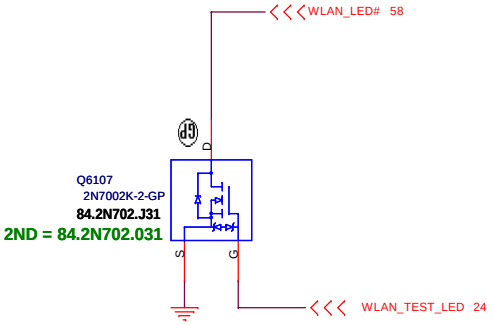


Power STDBY_LED

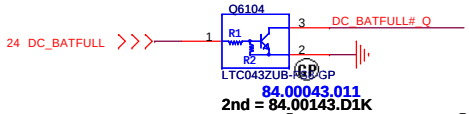


84.00043.011
2nd = 84.00143.D1K

From module

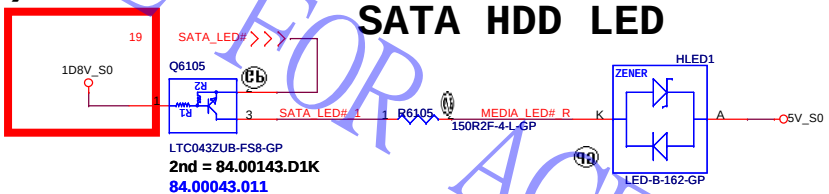


Battery LED2(DC_BATFULL)



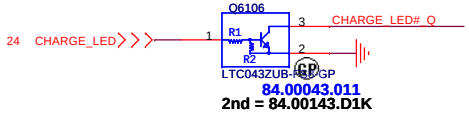
84.00043.011
2nd = 84.00143.D1K

SATA HDD LED



2nd = 84.00143.D1K
84.00043.011
83.00320.B70
2nd = 83.01211.070

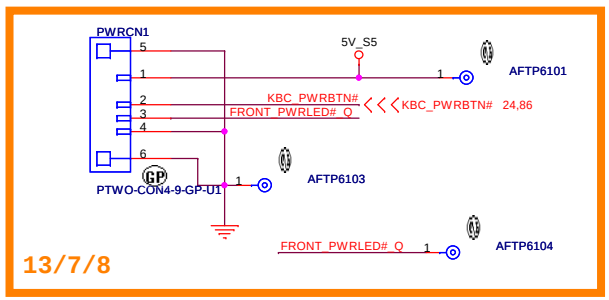
Battery LED1(CHARGE)

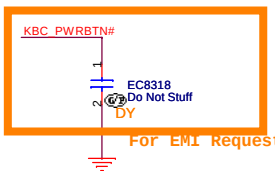


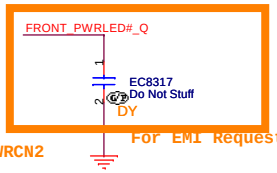
84.00043.011
2nd = 84.00143.D1K

83.00270.D70

Power button BD







N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

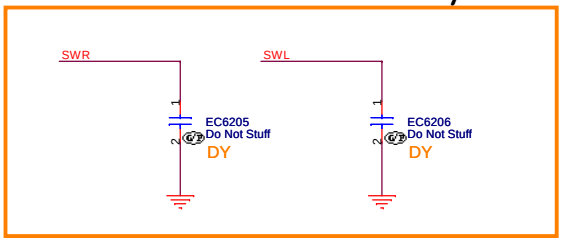
Title: LED Bard/Power Button

Size	Document Number	Rev
A3	EA40_BM	-1

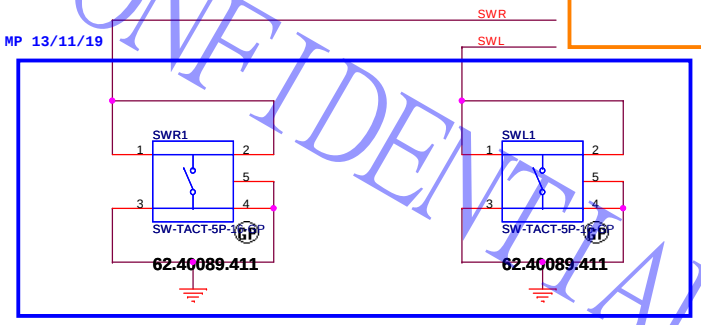
Date: Tuesday, November 19, 2013 Sheet 61 of 102

SSID = KBC

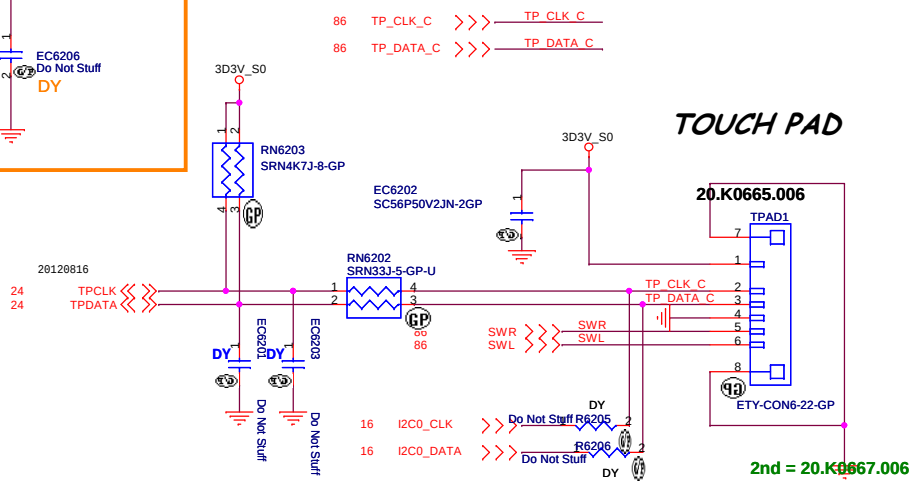
For EMI request



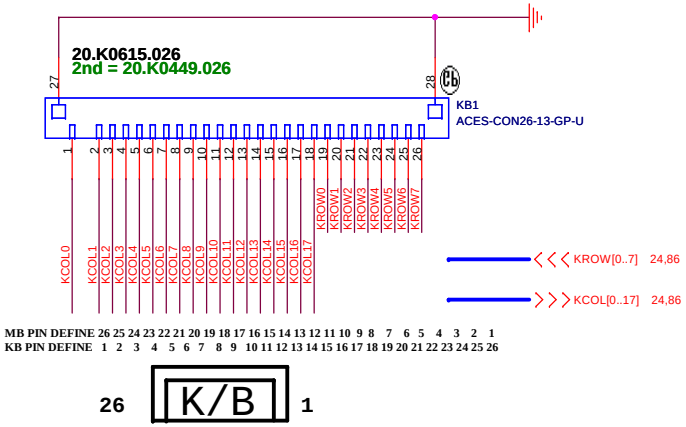
MP 13/11/19



TOUCH PAD



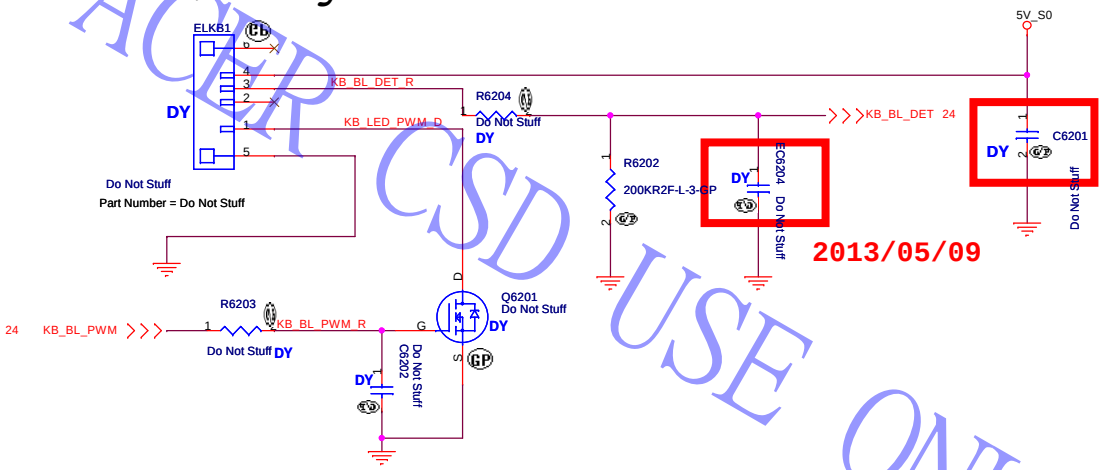
Internal KeyBoard Connector



26 K/B 1

KB Backlight

2013/04/17



N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: EA40_BM | Rev: -1

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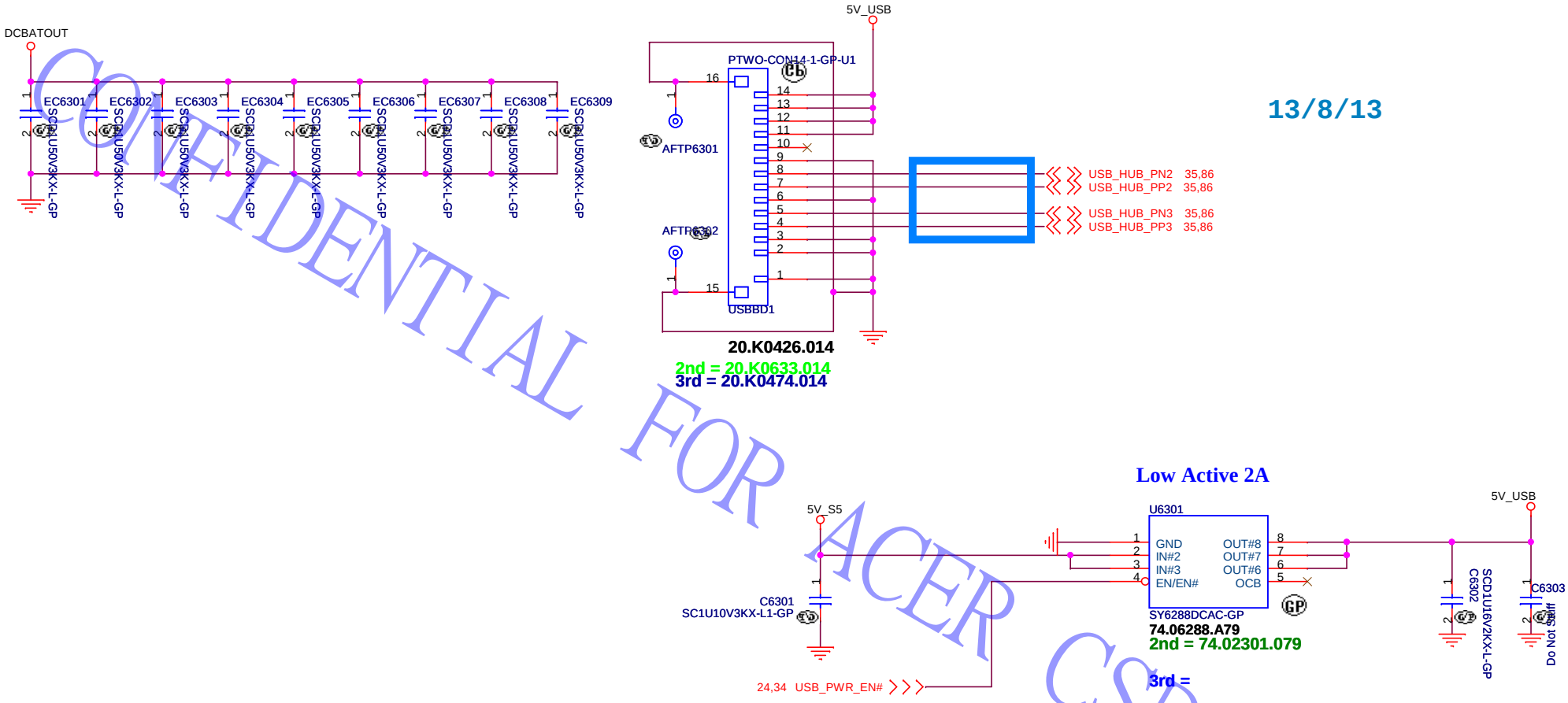
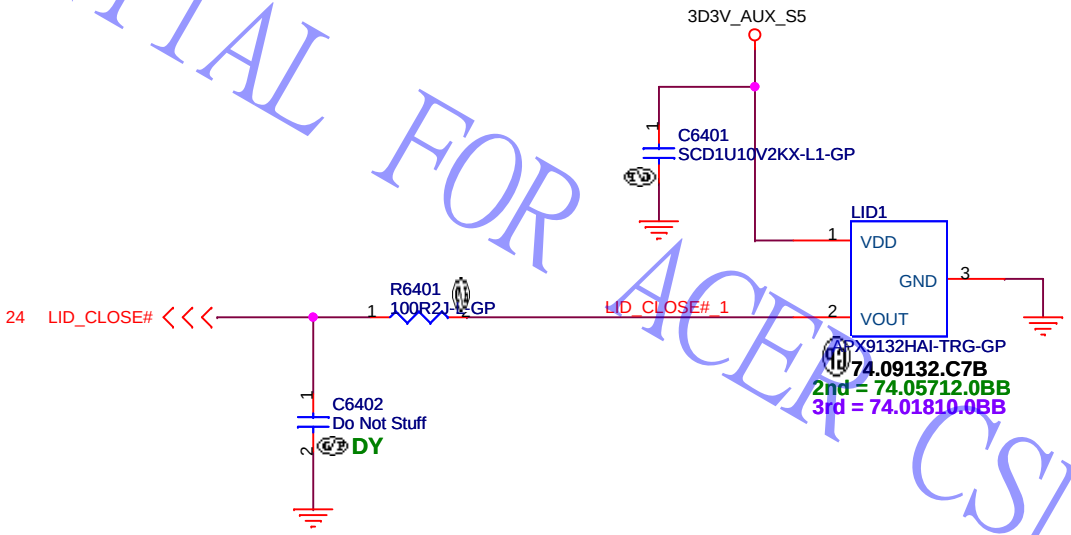


N15M UMA TOUCH 1DIMM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***IO Board Connector***	
Size: Custom	Document Number: **EA40_BM**	Rev: **-1**
Date: Tuesday, November 19, 2013	Sheet 63 of 102	



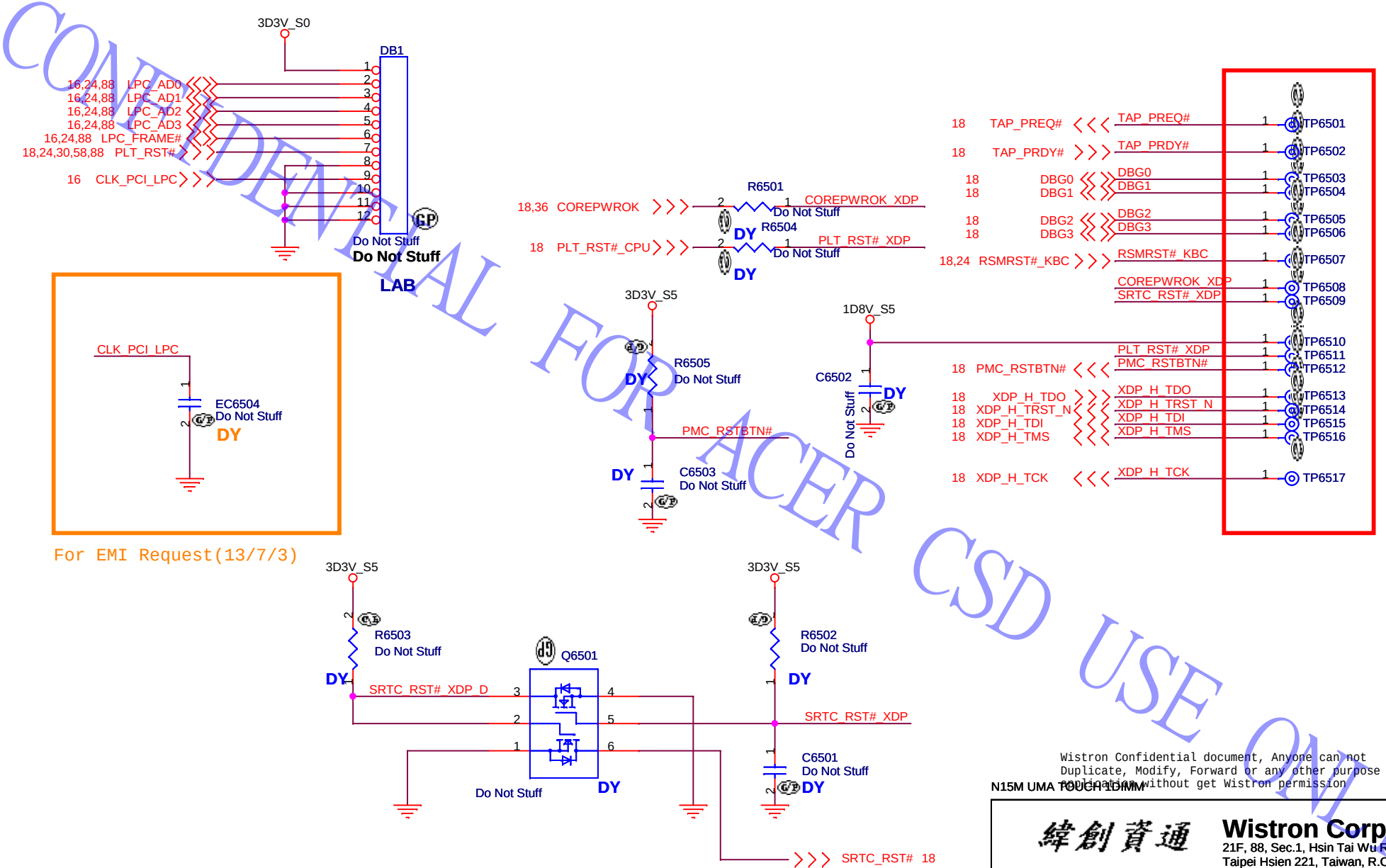
N15M UMA TOUCH 1DIMM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 64 of 102



N15M UMA TOUCH 1DIMM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 65 of 102

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N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **EA40 BM**	Rev **-1**
Date: Tuesday, November 19, 2013	Sheet 66 of 102	

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Blanking

SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G Sensor		
Size: A	Document Number: EA40_BM	Rev: -1
Date: Tuesday, November 19, 2013	Sheet 67 of 102	

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (1/5)*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 68 of 102

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N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (2/5)*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 69 of 102

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N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (3/5)*

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 70 of 102

Blanking

N15M UMA TOUCH 1DIMM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (4/5)*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 71 of 102

Blanking

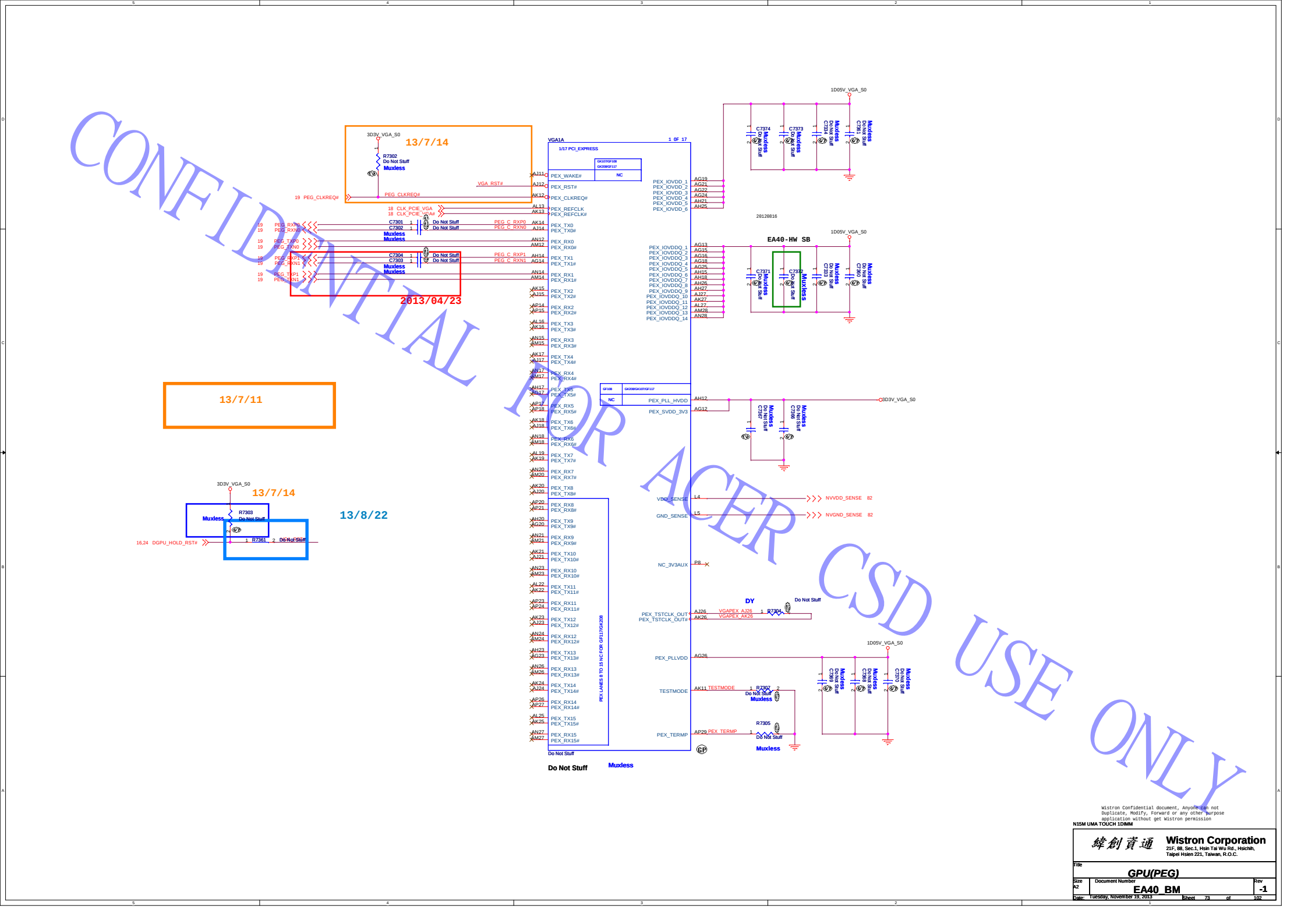
N15M UMA TOUCH 1D1MM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (5/5)*

Size	Document Number	Rev
A4	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 72 of 102



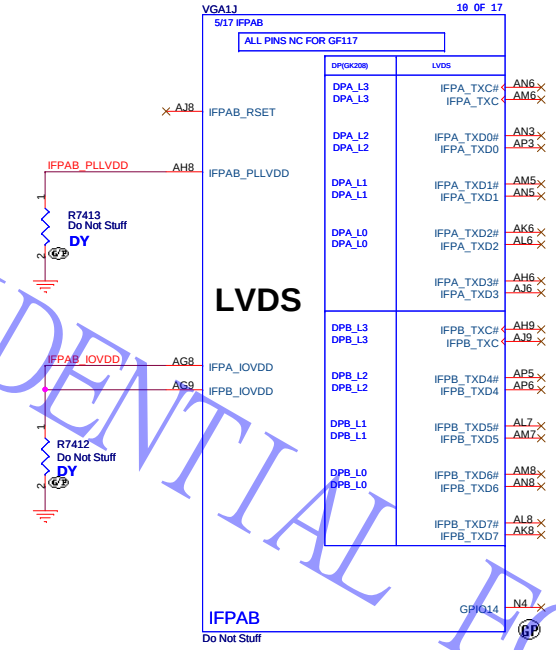
N15M UMA TOUCH 1DIMM

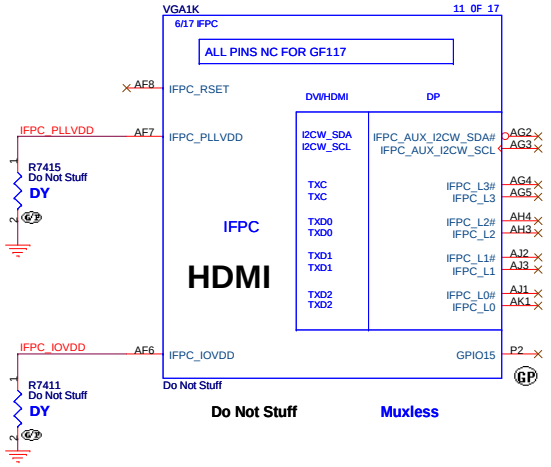
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

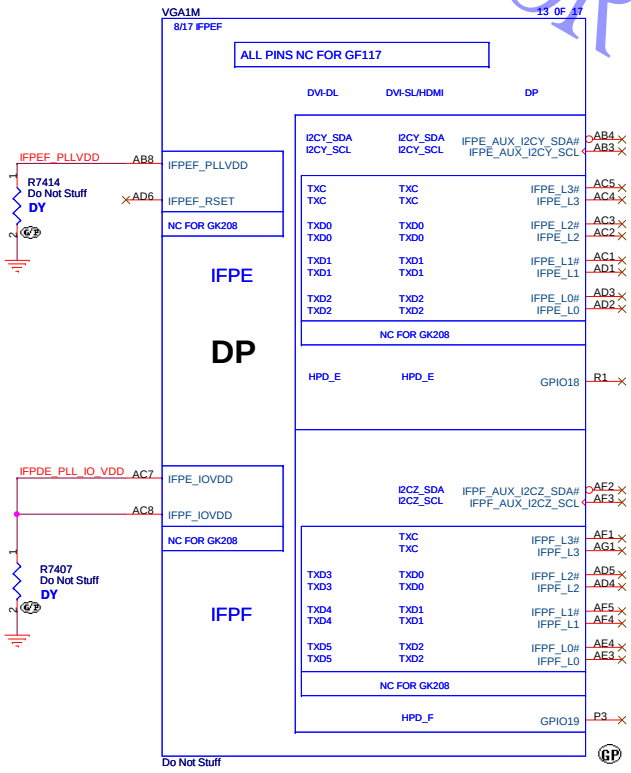
Title: GPU(PEG)

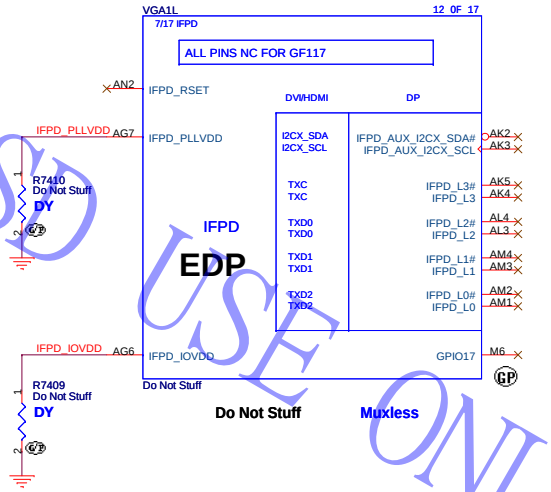
Size: A2 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 73 of 102









N15M UMA TOUCH 1DIMM

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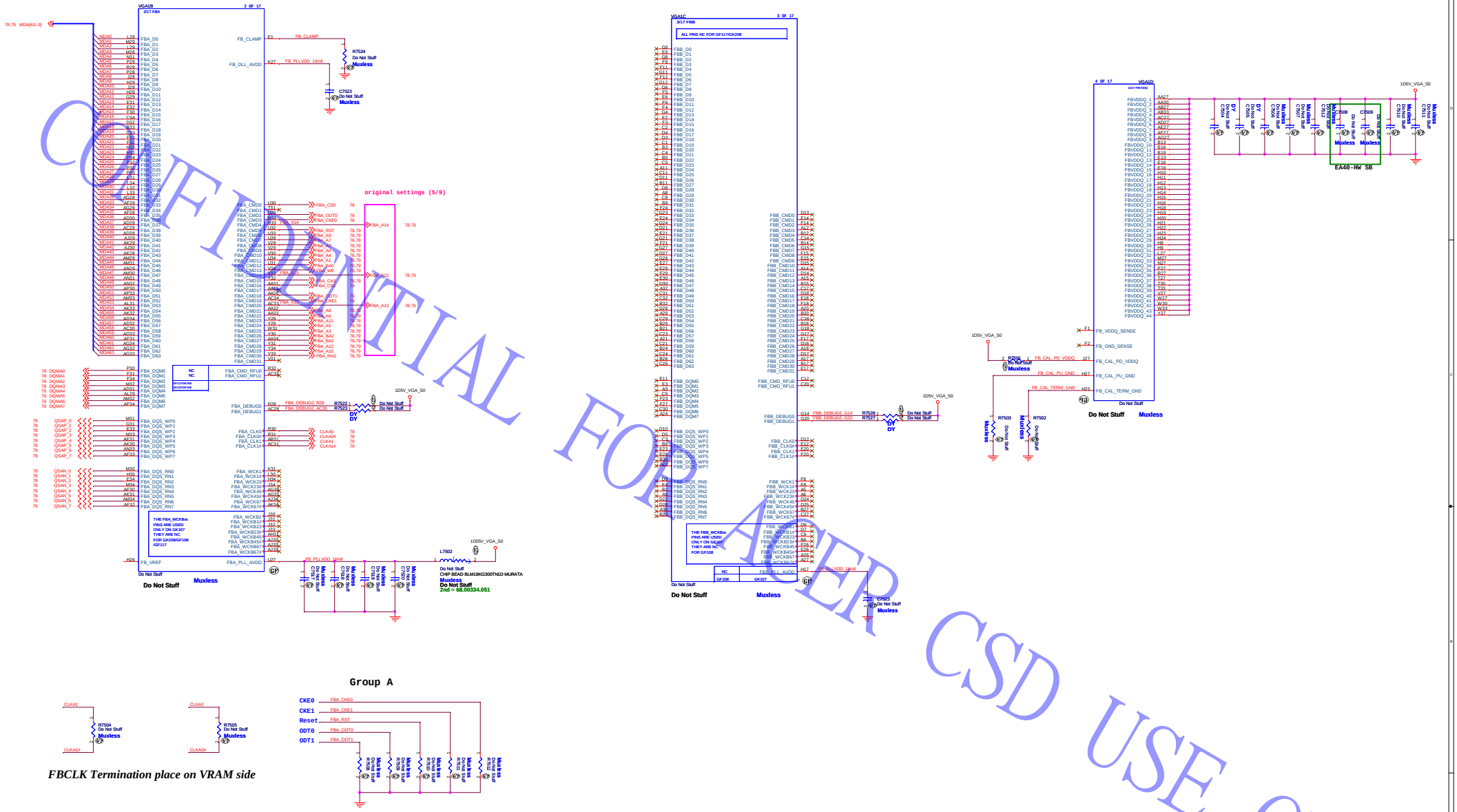
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (DIGITALOUT)

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 74 of 102



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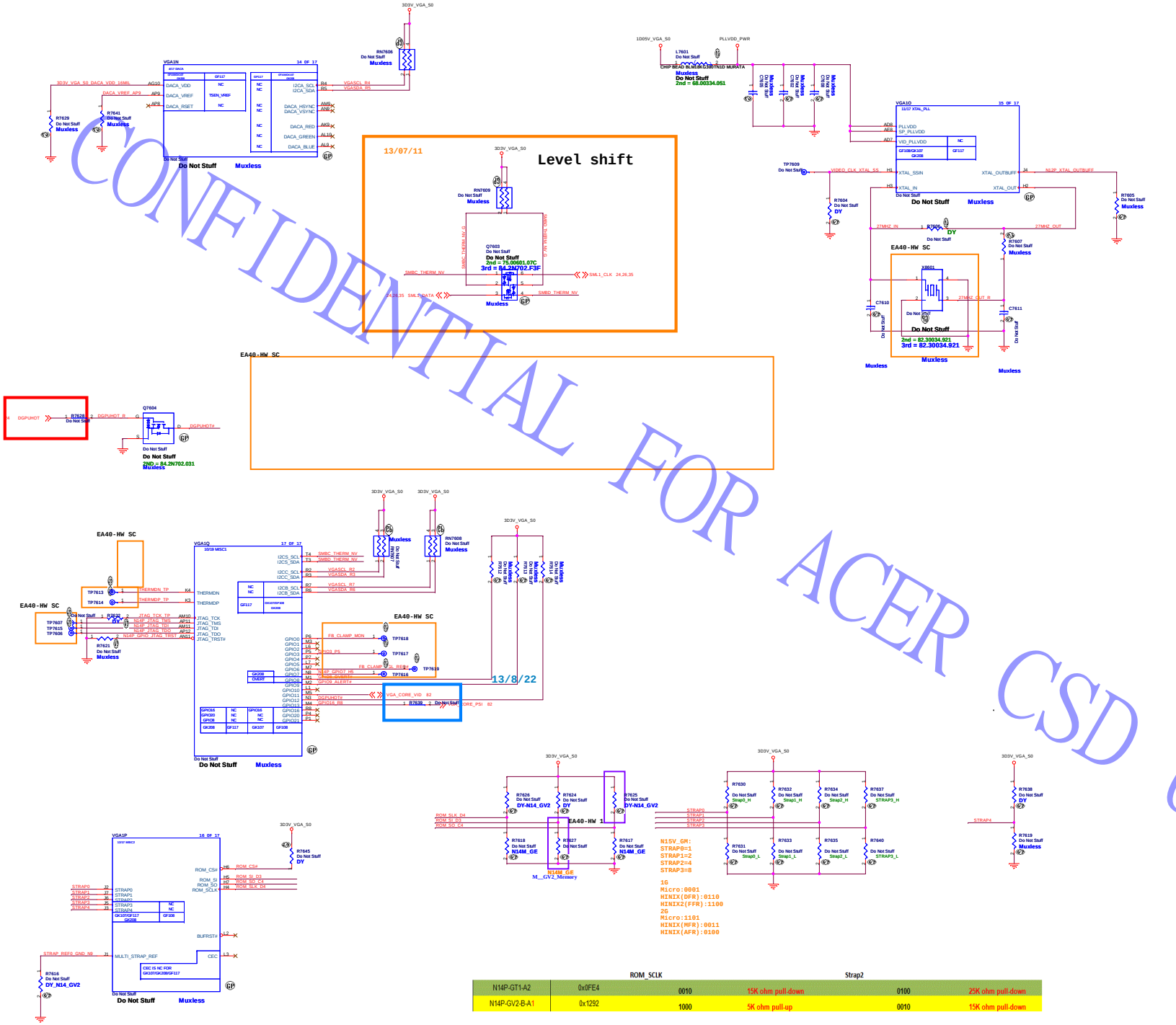
File: GPU (VRAM I/F)

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 18, 2008 Sheet 75 of 100



N14M-GE use Binary Strap. Please see the below information.

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Strap Pin Name	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	1	1	0	0
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
	N	N	N	N
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	1	0	0	1
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
	1	1	1	1
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	0	1	1	0
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	0	0	1	0
STRAP 3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	0	0	0	0
STRAP 4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	0	0	0	1

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M*16 DDR3	Samsung	0xB	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TQ4G63AFR-11C		N/A	Post-Production Candidate

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128M-16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production ready
				H5TQ2G63DFR-11C	900	N/A	Production ready

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm 64.49915.6DL
10Kohm 64.10025.L0L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL

For 1GB VRAM (128x16*4pcs),
VR.2GB0G.005 : VRAM HYNIX Graphic DDRIII 900 2Gb
H5TQ2G63DFR-11C LF+HF 128*16 38nm Gemma die
KN.2GB0G.038 : VRAM HYNIX Graphic DDRIII 900 2Gb
H5TC2G63FFR-11C LF+HF 128*16 29nm, Huma

For 2GB VRAM (256x16*4pcs)
KN.00404.001 : VRAM MICRON Graphic DDRIII 900 4Gb
MT41K256M16HA-107G:E LF+HF 256*16 30nm, V80A
KN.0040G.00 : VRAM HYNIX Graphic DDRIII 900 4Gb
H5TC4G63AFR-11C LF+HF 256*16 29nm, Huma

ROM_SCLK		Strap2			
N14P-GT1-A2	0x0FE4	0010	15K ohm pull-down	0100	25K ohm pull-down
N14P-GV2-B-A1	0x1292	1000	5K ohm pull-up	0010	15K ohm pull-down

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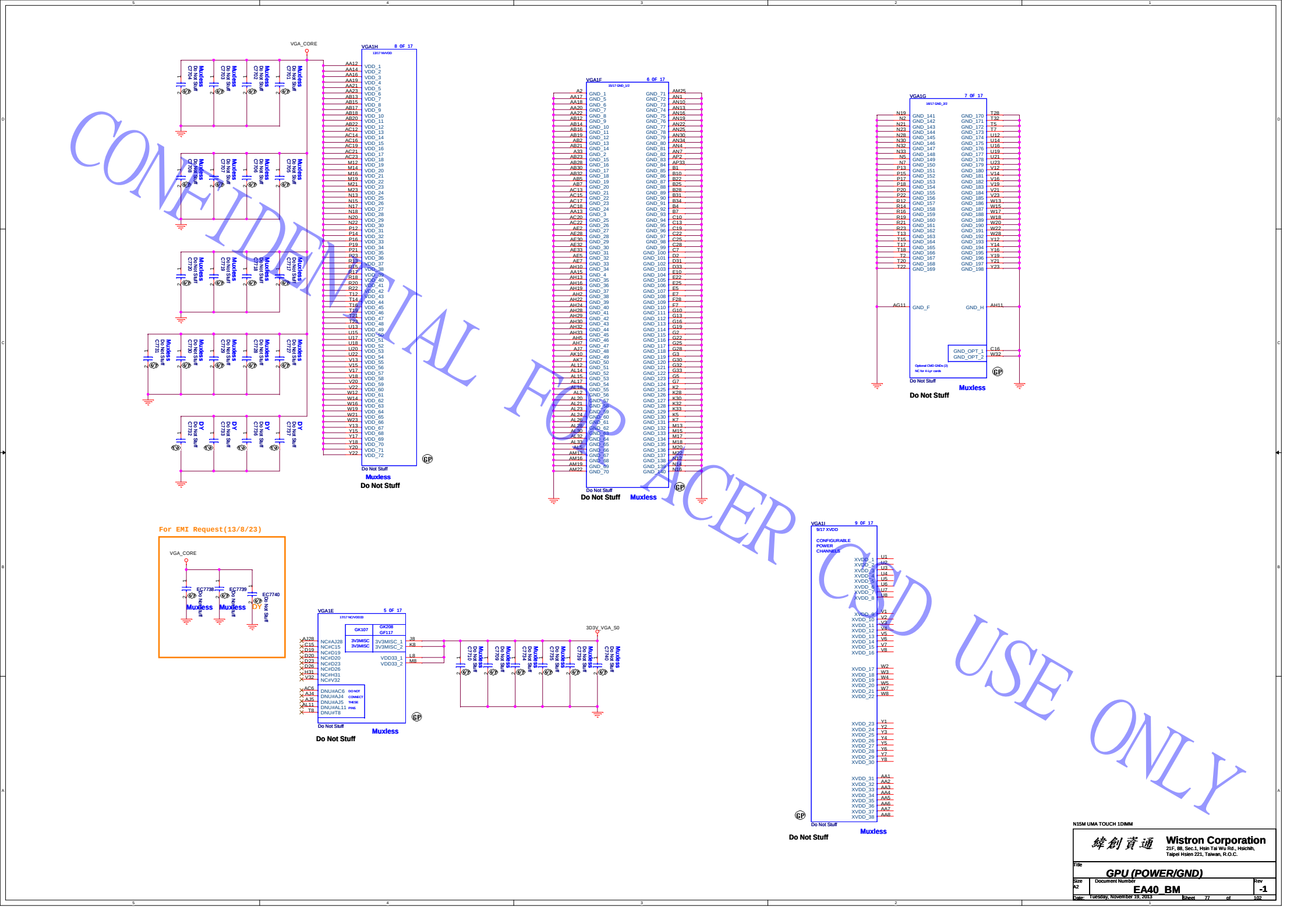
Title: GPU (GPIO/STRAP)
Size: Custom | Document Number: EA40_BM | Rev: -1
Date: Tuesday, November 19, 2013 | Sheet 76 of 102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VGA1H
8 OF 17
1.3/1.7 NVVDD
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
VDD_6
VDD_7
VDD_8
VDD_9
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VDD_11
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VDD_68
VDD_69
VDD_70
VDD_71
VDD_72
Do Not Stuff
Muxless
Do Not Stuff
VGA1F
6 OF 17
2.5/1.7 GND_1/2
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GND_6
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Do Not Stuff
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VGA1G
7 OF 17
1.5/1.7 GND_3/2
GND_141
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GND_195
GND_196
GND_197
GND_198
GND_F
GND_H
GND_OPT_1
GND_OPT_2
Optional GND GNDs (3)
NC for 4-Layr cards
Do Not Stuff
Muxless
Do Not Stuff
For EMI Request(13/8/23)
VGA_CORE
EC7738
EC7739
EC7740
Muxless
Muxless
DY
Do Not Stuff
VGA1E
5 OF 17
1.7/1.7 NCVDD33
GK107
GK208
GF117
3V3MISC
3V3MISC_1
3V3MISC_2
VDD33_1
VDD33_2
NC#AJ28
NC#C15
NC#D19
NC#D20
NC#D23
NC#D26
NC#H31
NC#V32
DNU#AC6
DNU#AJ4
DNU#AJ5
DNU#AL11
DNU#T8
DO NOT CONNECT THESE PINS
J8
K8
L8
M8
3D3V_VGA_S0
Do Not Stuff
Muxless
Do Not Stuff
VGA1J
9 OF 17
9/17 XVDD
CONFIGURABLE POWER CHANNELS
XVDD_1
XVDD_2
XVDD_3
XVDD_4
XVDD_5
XVDD_6
XVDD_7
XVDD_8
XVDD_9
XVDD_10
XVDD_11
XVDD_12
XVDD_13
XVDD_14
XVDD_15
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XVDD_17
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XVDD_36
XVDD_37
XVDD_38
Do Not Stuff
Muxless
Do Not Stuff
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Title
GPU (POWER/GND)
Size
A2
Document Number
EA40_BM
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-1
Date: Tuesday, November 19, 2013
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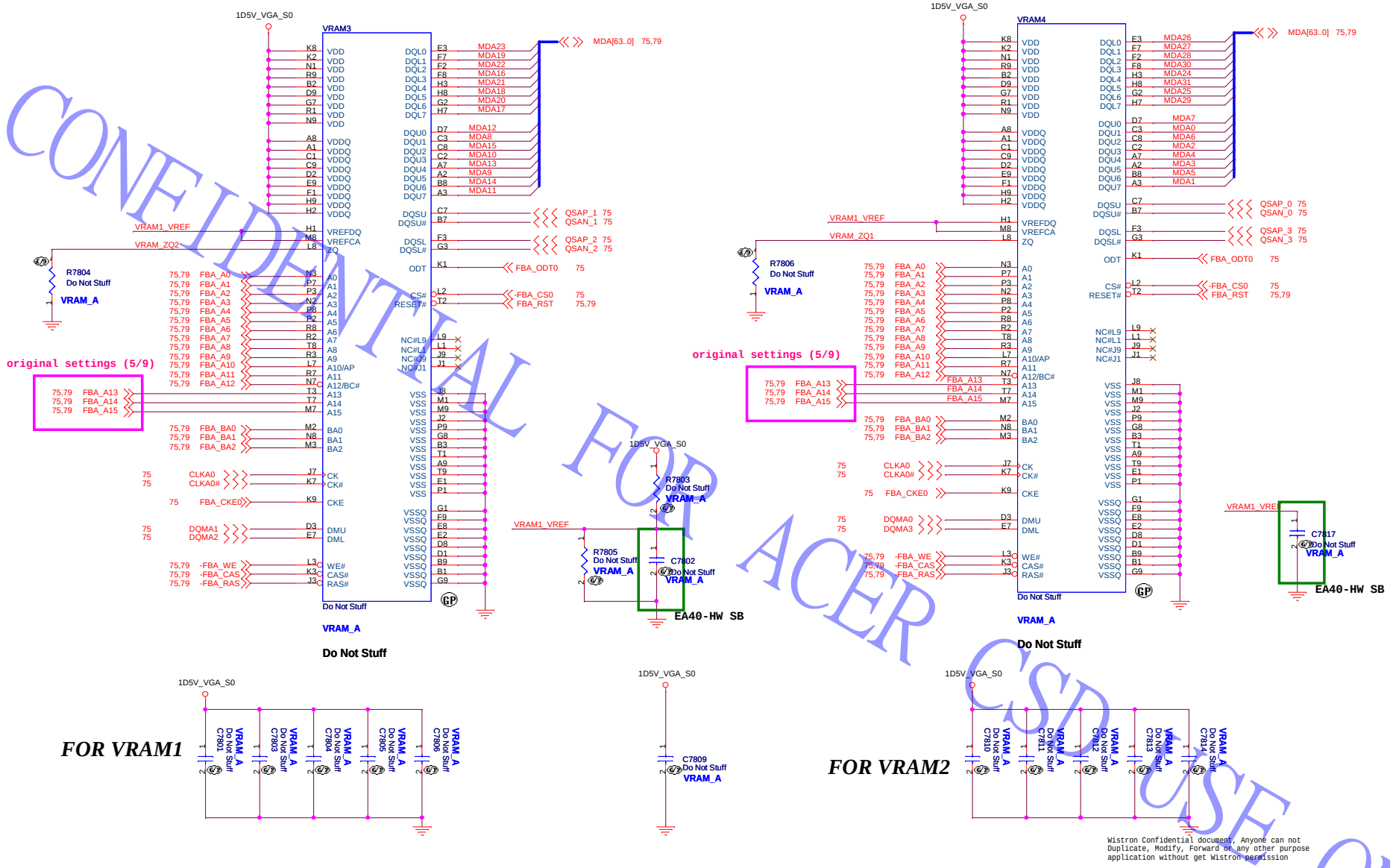

VRAM BOM for EA40_BM

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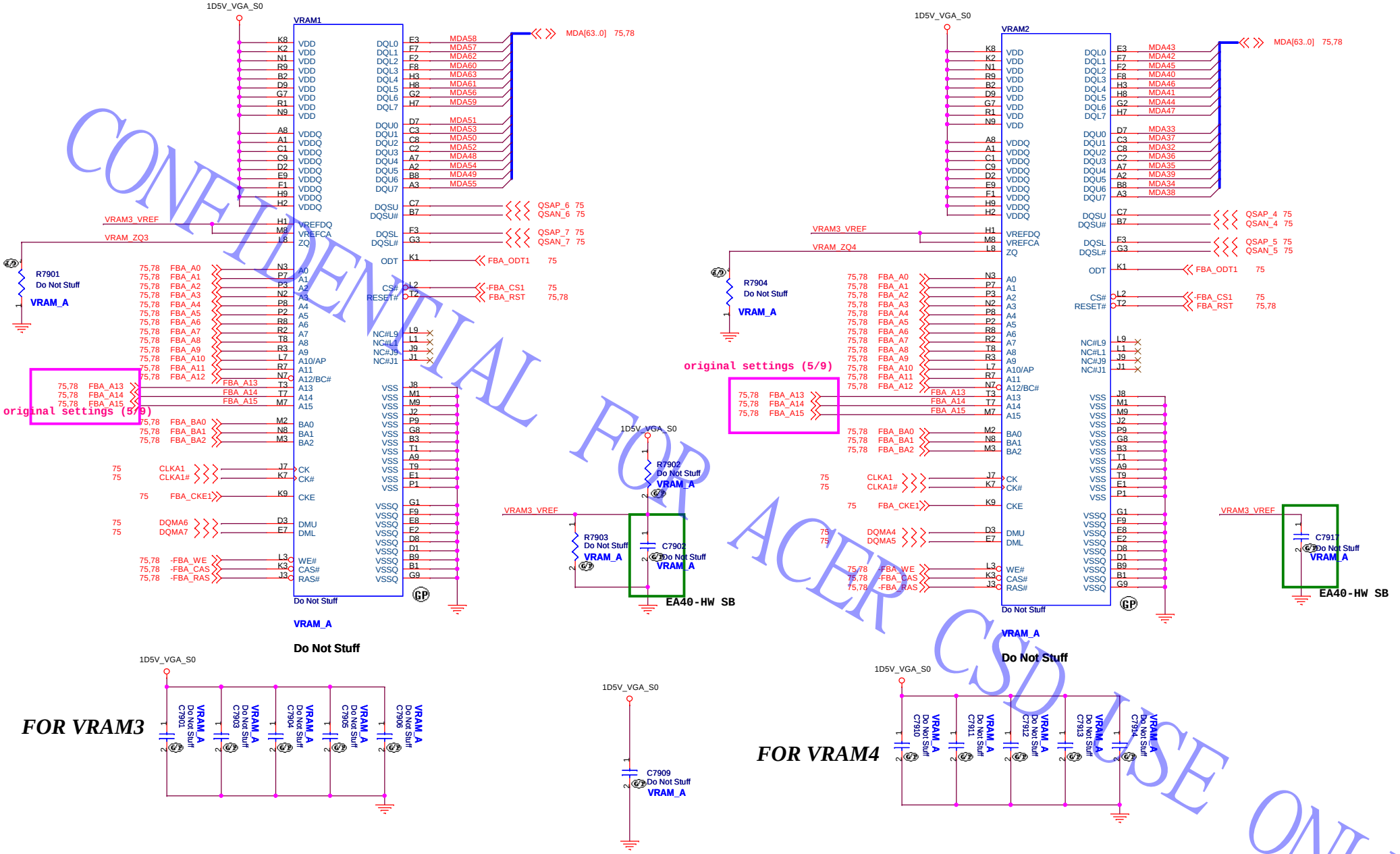
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 78 of 102



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Title: GPU-VRAM3,4 (2/4)

Size: A3 | Document Number: EA40_BM | Rev: -1

Date: Tuesday, November 19, 2013 | Sheet 79 of 102

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Title
GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 80 of 102

N15M UMA TOUCH 1DIMM

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Title
GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	EA40_BM	-1

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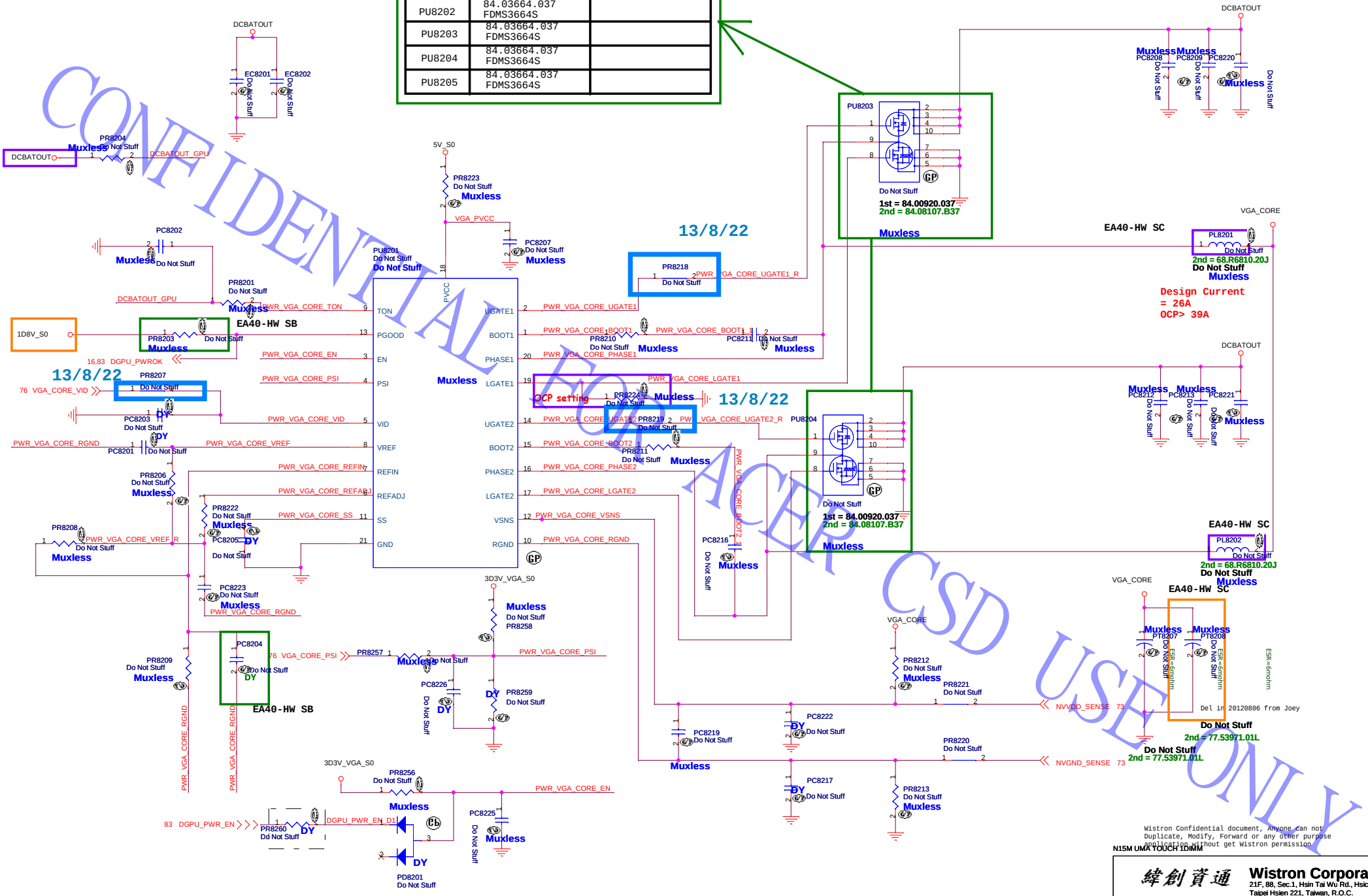
PU8203	84.03664.037 FDMS3664S	
PU8204	84.03664.037 FDMS3664S	
PU8205	84.03664.037 FDMS3664S	



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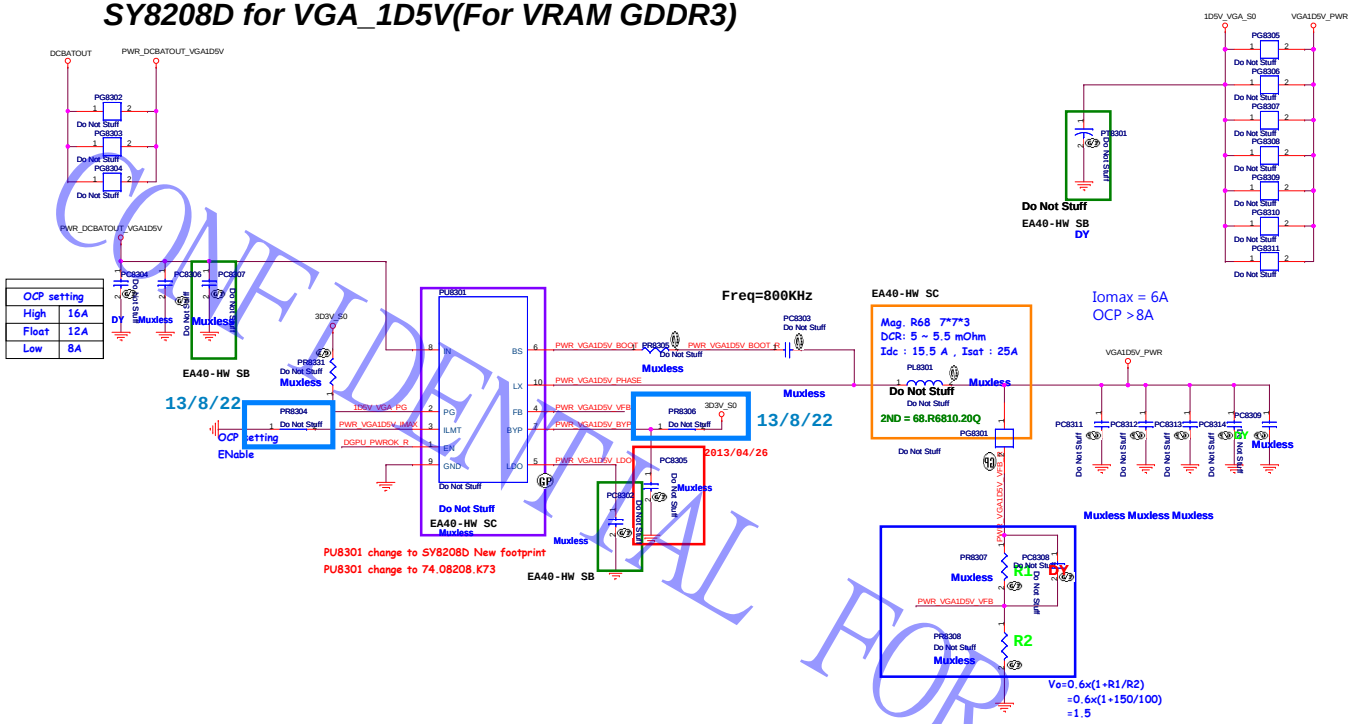
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

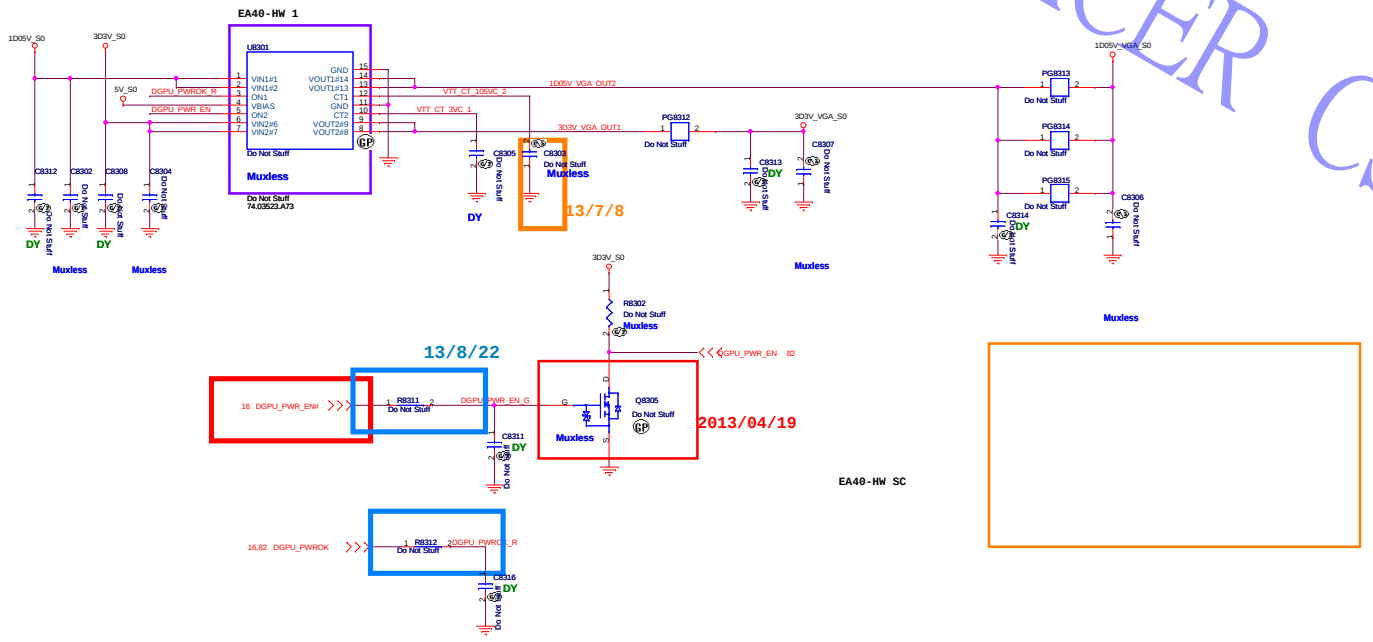
Title: **RT8812A_VGA_CORE**

Size	Document Number	Rev
Custom	EA40_BM	-1

Date: Tuesday, November 19, 2013 Sheet 82 of 102

SY8208D for VGA_1D5V(For VRAM GDDR3)





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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: EA40 BM | Rev: -1

Date: Tuesday, November 05, 2013 | Sheet 83 of 102

Blanking

N15M UMA TOUCH 1DIMM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Switchable GFX LCD(1/2)*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 84 of 102

Blanking

N15M UMA TOUCH 1D1MM

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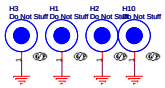
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Switchable GFX LCD(2/2)*

Size	Document Number	Rev
A4	EA40 BM	-1

Date: Tuesday, November 19, 2013 Sheet 85 of 102



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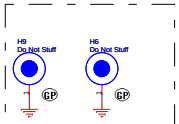

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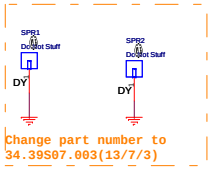
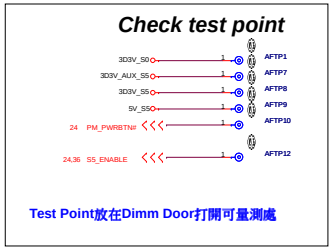
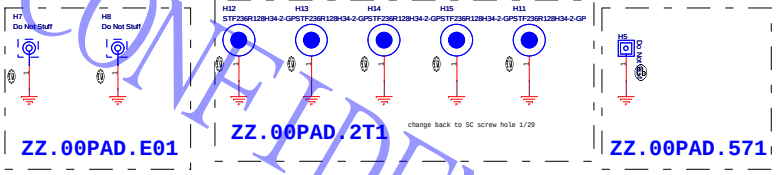




Test Point放在Dimm Door打開可量測處



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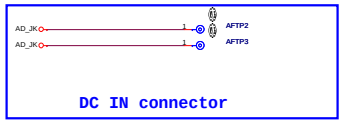
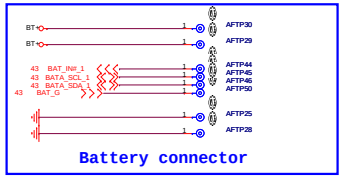
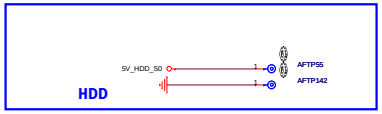


DC IN connector



Battery connector



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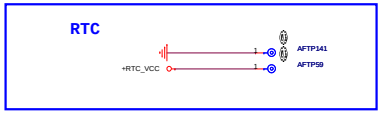

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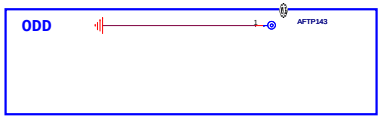

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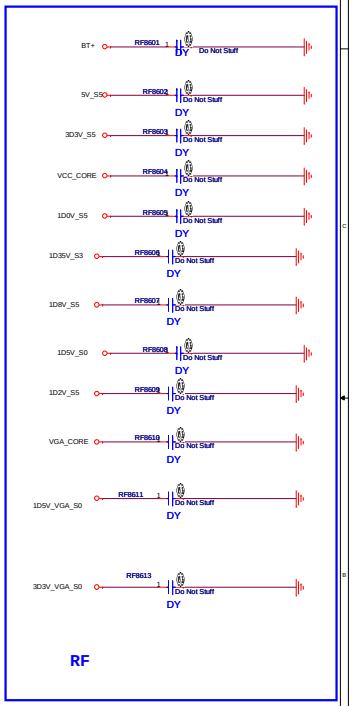

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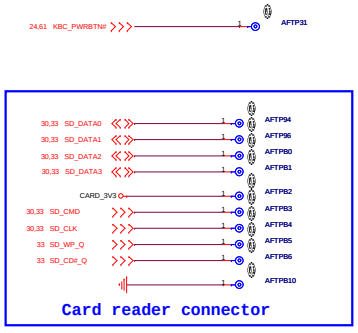
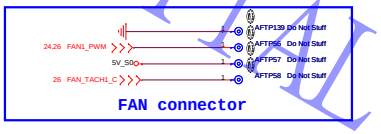
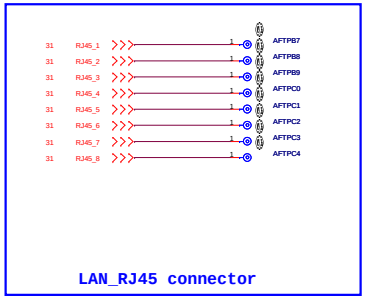


Card reader connector

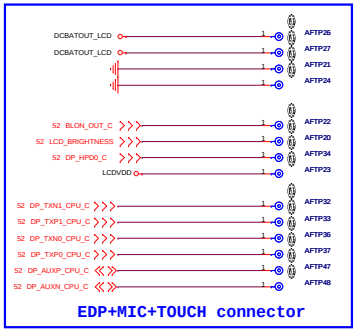


FAN connector

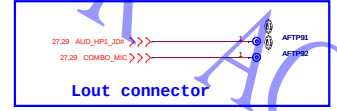
Speaker connector



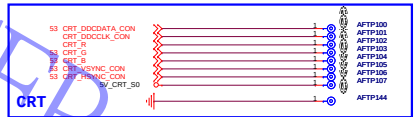
LAN_RJ45 connector



EDP+MIC+TOUCH connector



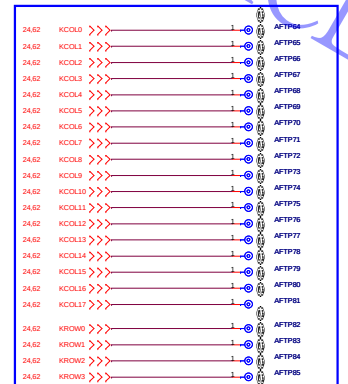
Lout connector



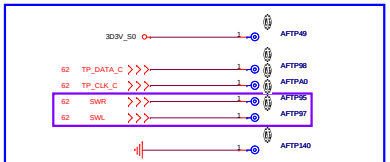
CRT

HDMI

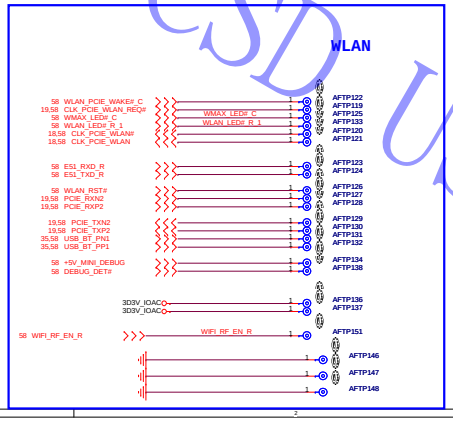
AMIC

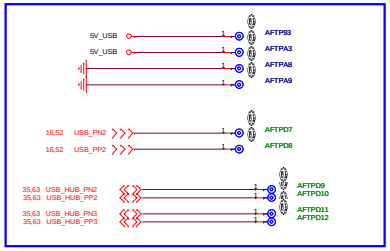


Normal KB connector



Touch Pad connector





USBBD connector

N15M UMA TOUCH 1DIMM

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Title: UNUSED PARTS/EMI Capacitors

Size: Custom | Document Number: EA40 BM | Rev: -1

Date: Wednesday, November 20, 2013 | Sheet 86 of 102

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Title: ***Reserved***

Size	Document Number	Rev
A4	EA40_BM	-1

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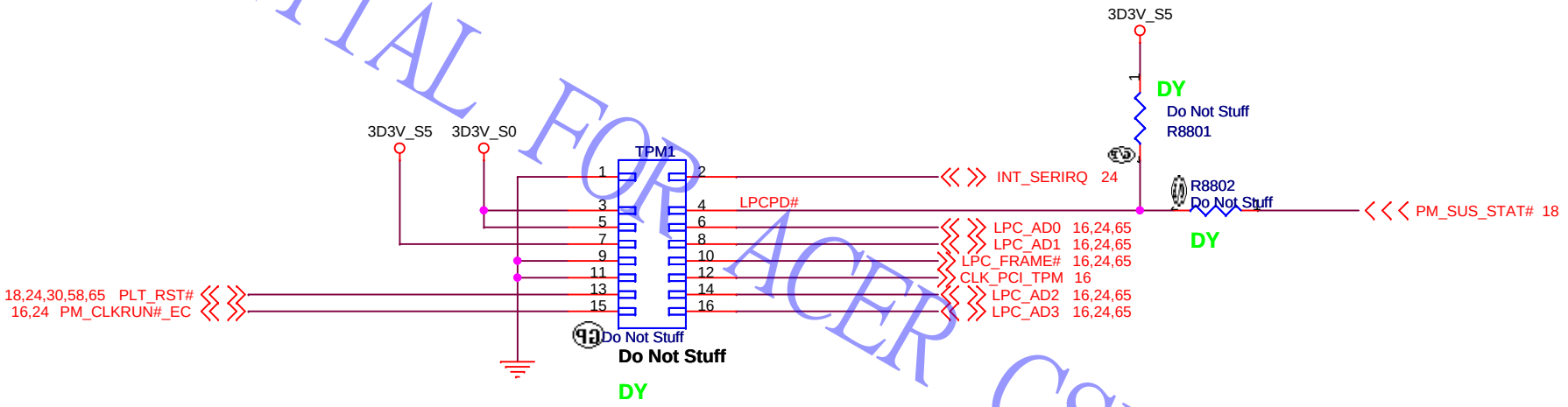

N15M UMA TOUCH 13MM

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Title: ***TPM***

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SSID = Finger Print

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Title	***Reserved***	
Size A4	Document Number **EA40 BM**	Rev **-1**
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SSID = Express Card

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Title: ***Reserved***

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SSID = Smart Card

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Title: Reserved

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Title

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SSID = Docking

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Title: *Reserved*

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SSID = Intel LAN

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N15M UMA TOUCH 1D IMM

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Title: *Reserved*

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N15M UMA TOUCH 1D1MM

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Title: *LAN Switch*

Size	Document Number	Rev
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title: PCH_XDP

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Title: *table of content*

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N15M UMA TOUCH 1DIMM

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Title

Change History

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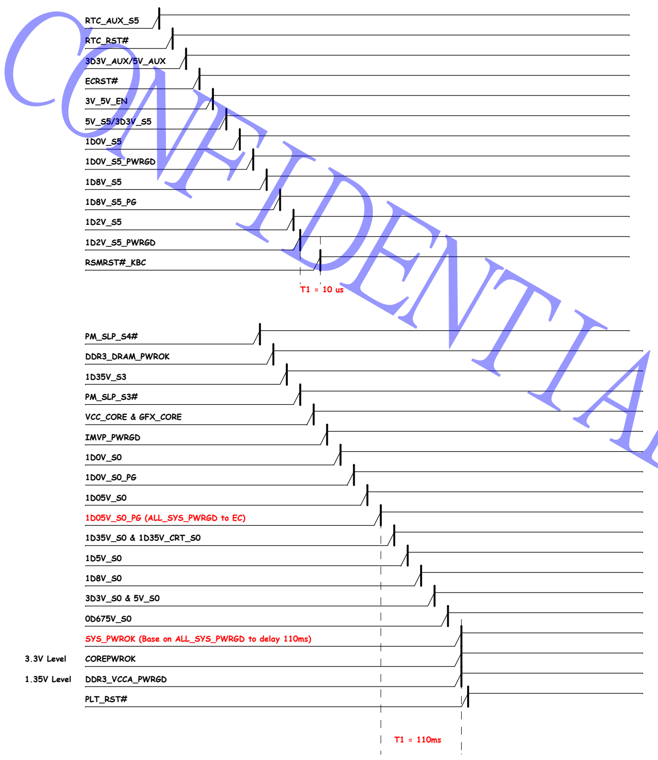
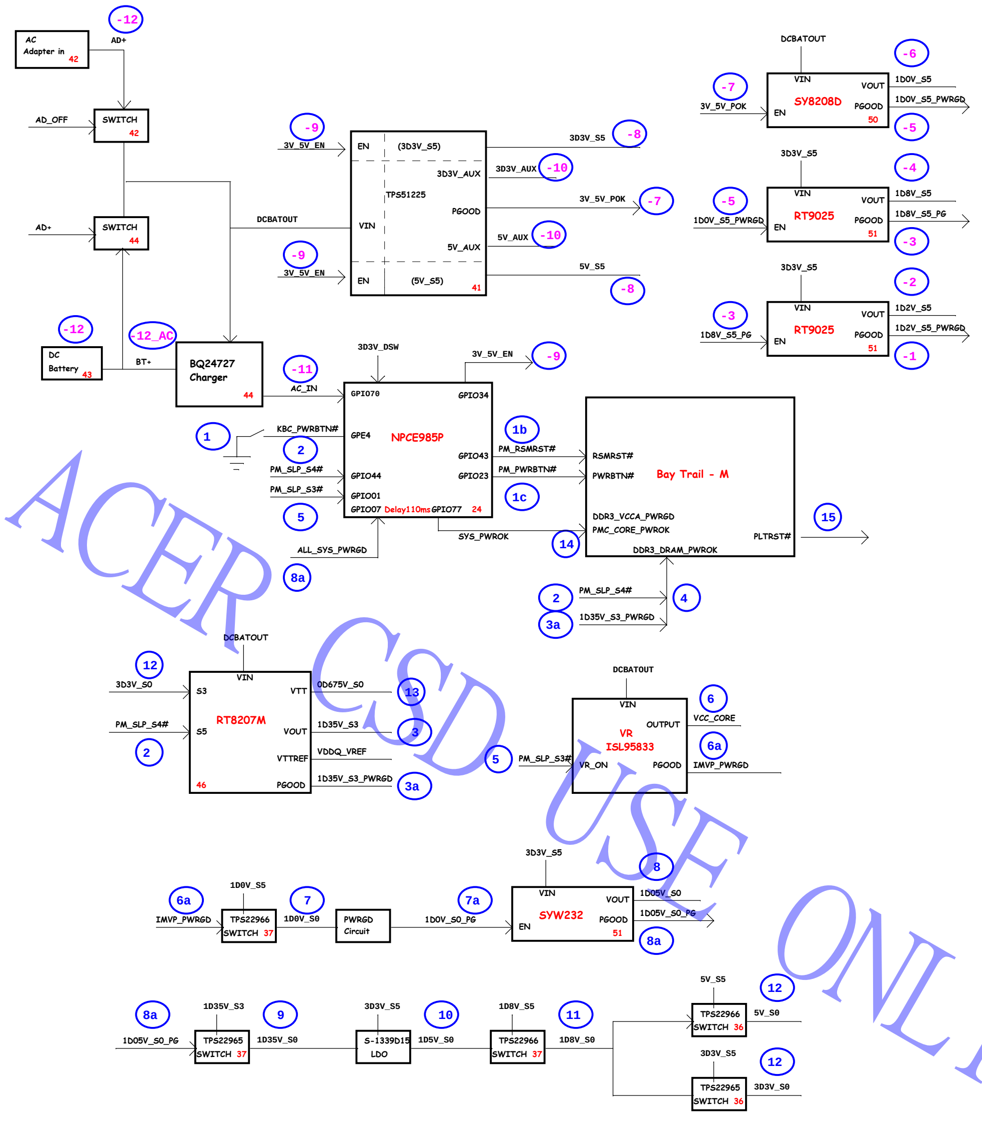
Intel-Power Up Sequence with non-S0ix



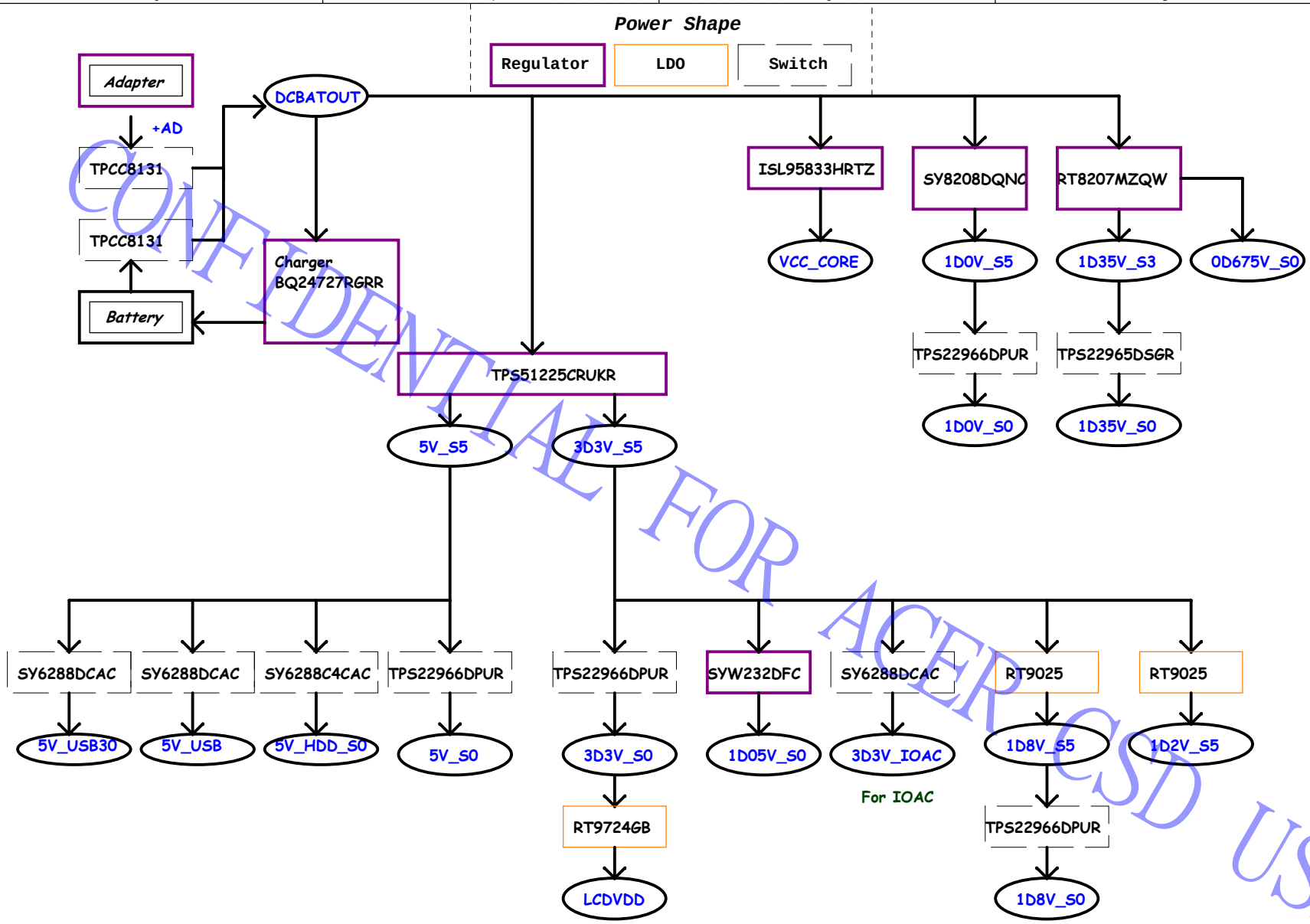
RTC_AUX_S5
RTC_RST#
3D3V_AUX/5V_AUX
ECRST#
3V_5V_EN
5V_S5/3D3V_S5
1D0V_S5
1D0V_S5_PWRGD
1D8V_S5
1D8V_S5_PG
1D2V_S5
1D2V_S5_PWRGD
RSMRST#_KBC
T1 = 10 us
PM_SLP_S4#
DDR3_DRAM_PWROK
1D35V_S3
PM_SLP_S3#
VCC_CORE & GFX_CORE
IMVP_PWRGD
1D0V_S0
1D0V_S0_PG
1D05V_S0
1D05V_S0_PG (ALL_SYS_PWRGD to EC)
1D35V_S0 & 1D35V_CRT_S0
1D5V_S0
1D8V_S0
3D3V_S0 & 5V_S0
0D675V_S0
SYS_PWROK (Base on ALL_SYS_PWRGD to delay 110ms)
3.3V Level
COREPWROK
1.35V Level
DDR3_VCCA_PWRGD
PLT_RST#
T1 = 110ms

Bay Trail - M POWER UP SEQUENCE DIAGRAM



AC Adapter in 42
-12
AD+
AD_OFF
SWITCH 42
AD+
SWITCH 44
DC Battery 43
-12
-12_AC
BT+
BQ24727 Charger 44
DCBATOUT
3V_5V_EN
-9
EN (3D3V_S5)
3D3V_AUX
TPS51225
PGOOD
VIN
5V_AUX
EN (5V_S5) 41
3D3V_S5
-8
-10
3V_5V_POK
-7
5V_S5
DCBATOUT
3V_5V_POK
VIN VOUT
SY8208D
EN PGOOD 50
1D0V_S5
1D0V_S5_PWRGD
-6
-5
3D3V_S5
1D0V_S5_PWRGD
RT9025 51
1D8V_S5
1D8V_S5_PG
-4
-3
1D8V_S5_PG
RT9025 51
1D2V_S5
1D2V_S5_PWRGD
-2
-1
3D3V_DSW
AC_IN
-11
KBC_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
GPIO70 GPIO34
GPE4 NPCE985P
GPIO43
GPIO44 GPIO23
GPIO01
GPIO07 Delay110ms GPIO77 24
ALL_SYS_PWRGD
SYS_PWROK
PM_RSMRST#
PM_PWRBTN#
RSMRST#
PWRBTN#
Bay Trail - M
DDR3_VCCA_PWRGD
PMC_CORE_PWROK
DDR3_DRAM_PWROK
PLTRST#
1 2 5 8a 1b 1c 14 15
PM_SLP_S4#
1D35V_S3_PWRGD
2 3a 4
DCBATOUT
3D3V_S0
PM_SLP_S4#
S3 VIN VTT
RT8207M
S5 VOUT
VTTREF
46 PGOOD
0D675V_S0
1D35V_S3
VDDQ_VREF
1D35V_S3_PWRGD
12 2 13 3 3a
DCBATOUT
VIN
VR ISL95833
OUTPUT
PM_SLP_S3#
VR_ON PGOOD
VCC_CORE
IMVP_PWRGD
5 6 6a
3D3V_S5
1D0V_S5
IMVP_PWRGD
TPS22966 SWITCH 37
1D0V_S0
PWRGD Circuit
1D0V_S0_PG
VIN VOUT
SYW232
EN PGOOD 51
1D05V_S0
1D05V_S0_PG
6a 7 7a 8 8a
1D35V_S3
1D05V_S0_PG
TPS22965 SWITCH 37
1D35V_S0
3D3V_S5
S-1339D15 LDO
1D5V_S0
1D8V_S5
TPS22966 SWITCH 37
1D8V_S0
5V_S5
TPS22966 SWITCH 36
5V_S0
3D3V_S5
TPS22965 SWITCH 36
3D3V_S0
8a 9 10 11 12

N15M UMA TOUCH 1D5MM



N15M UMA TOUCH 1DIMM

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Title: Power Block Diagram

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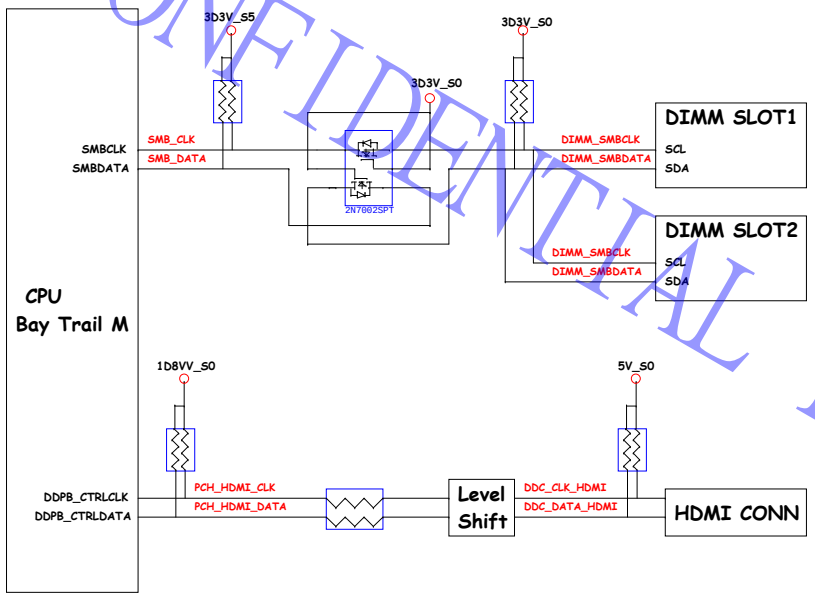
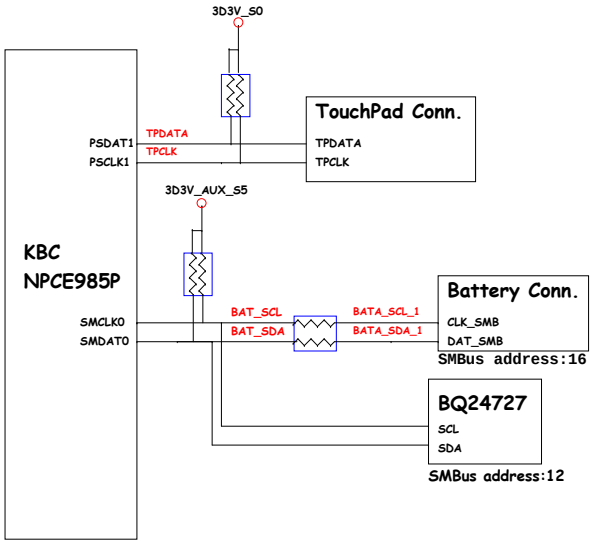
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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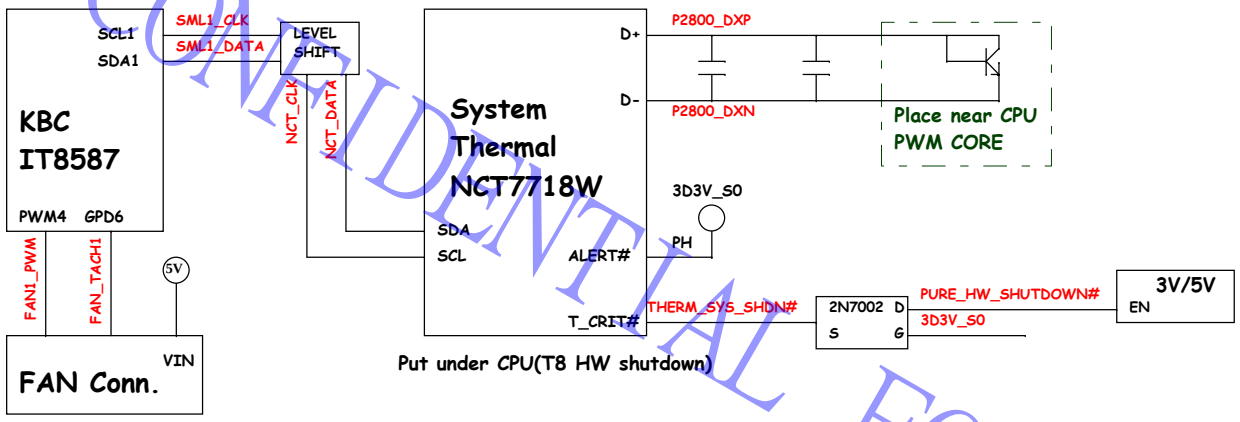
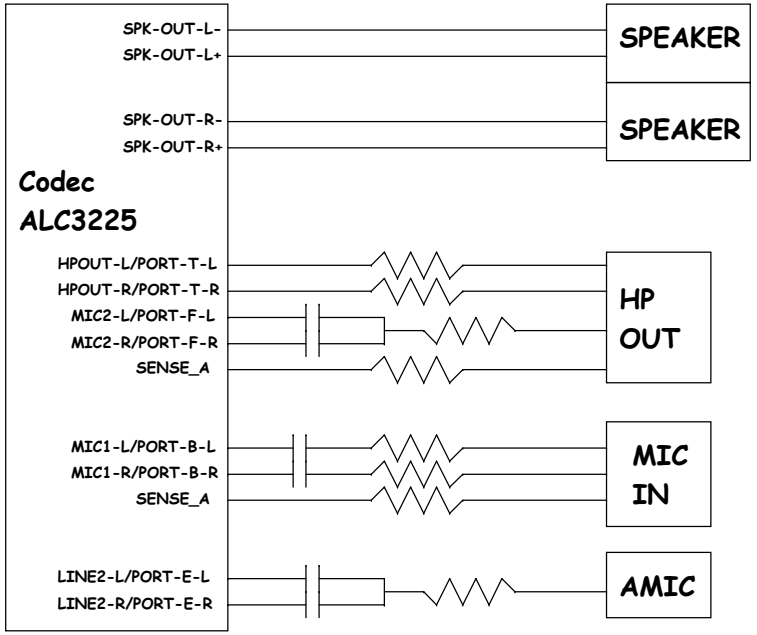
Thermal Block Diagram



Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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