

# Compal Confidential

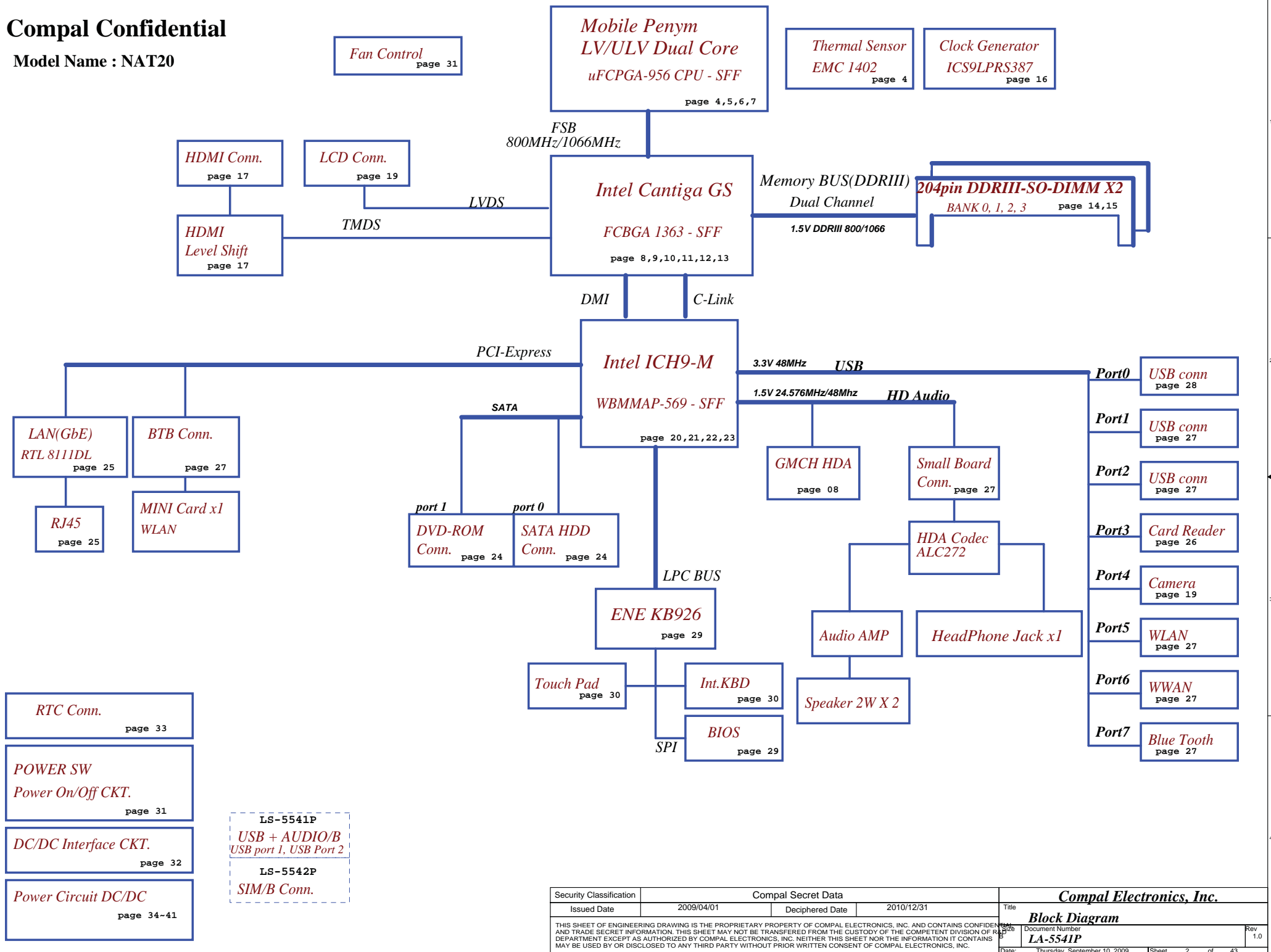
## Schematic Document

**Rev: 1.0**  
**2009.09.10**

Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	Cover Sheet	
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<small>Date:</small> Thursday, September 10, 2009				<small>Sheet</small> 1 of 43	

# Compal Confidential

Model Name : NAT20



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Issued Date	2009/04/01	Deciphered Date	2010/12/31	Block Diagram	
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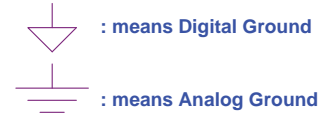
### Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	18K +/- 5%	0.436 V	0.503 V	0.538 V
2	33K +/- 5%	0.712 V	0.819 V	0.875 V
3	56K +/- 5%	1.036 V	1.185 V	1.264 V
4	100K +/- 5%	1.453 V	1.650 V	1.759 V
5	200K +/- 5%	1.935 V	2.200 V	2.341 V
6	NC	2.500 V	3.300 V	3.300 V
7				

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

### Symbol Note :



### SMBUS Control Table

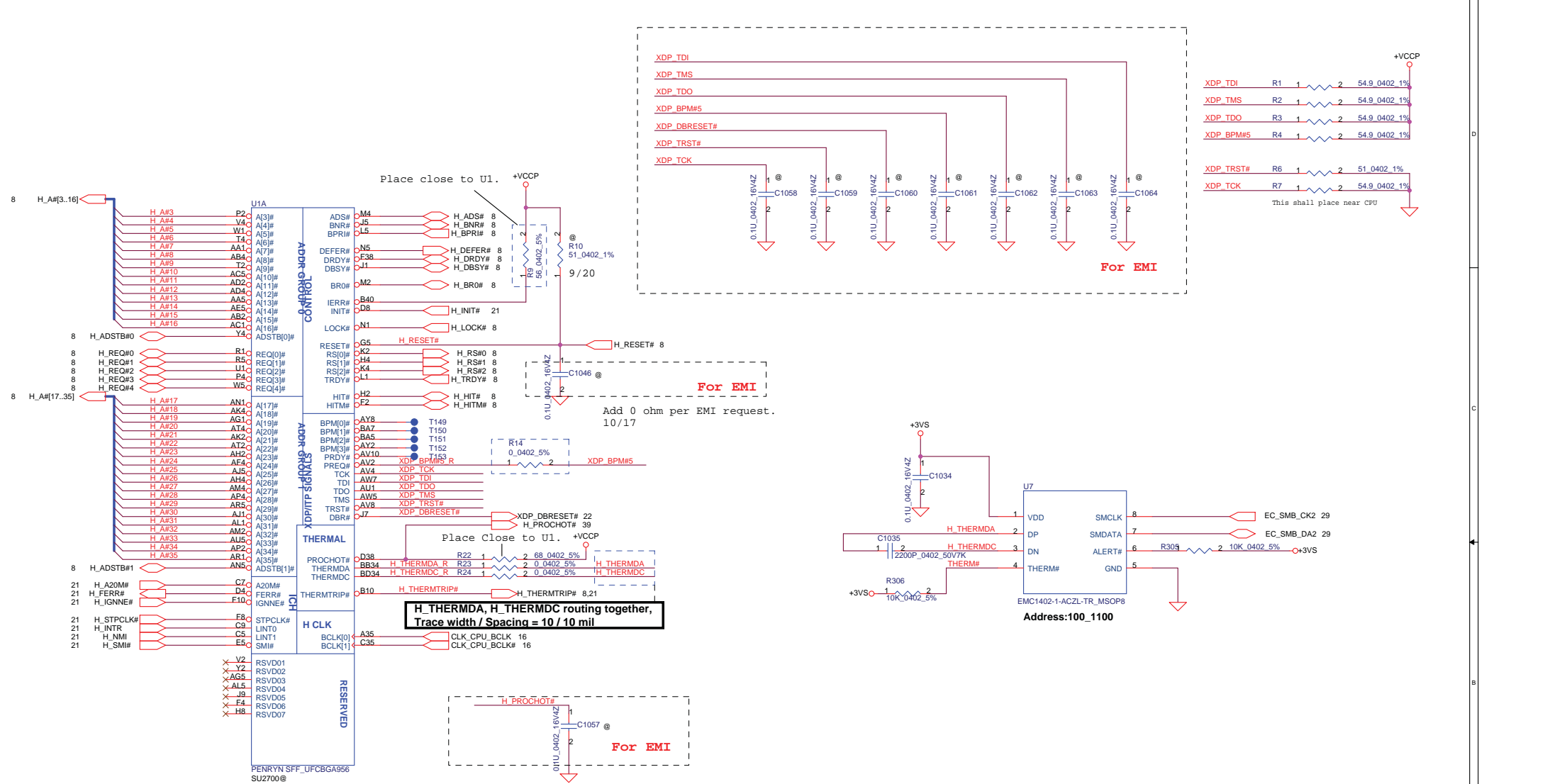
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM
EC_SMB_CK1 EC_SMB_DA1	KB926	X	V	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V
MCP_SMB_CLK MCP_SMB_DATA	ICH9	X	X	X	X	X

MINI CARD 1 RESERVED +3VALW TO PULL HIGH

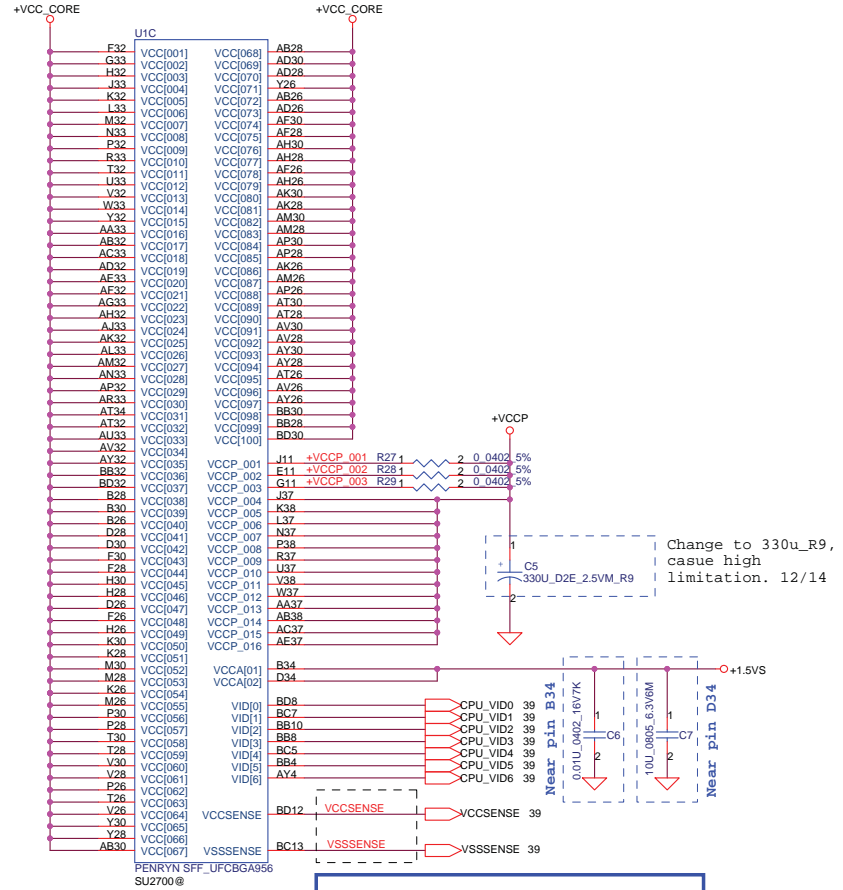
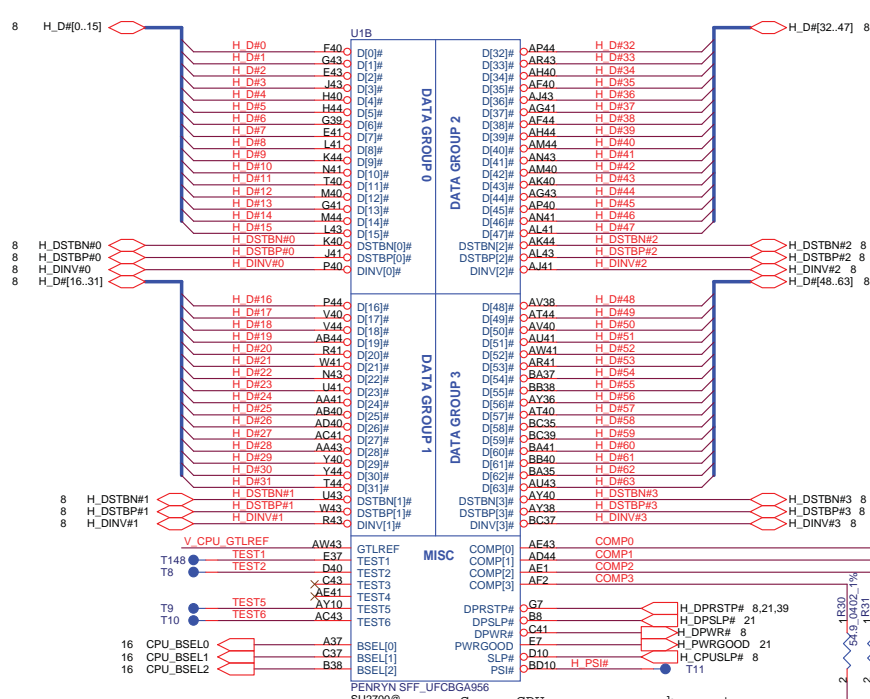
### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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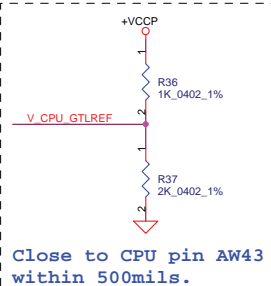
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TFS

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

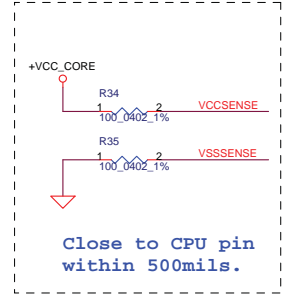
Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

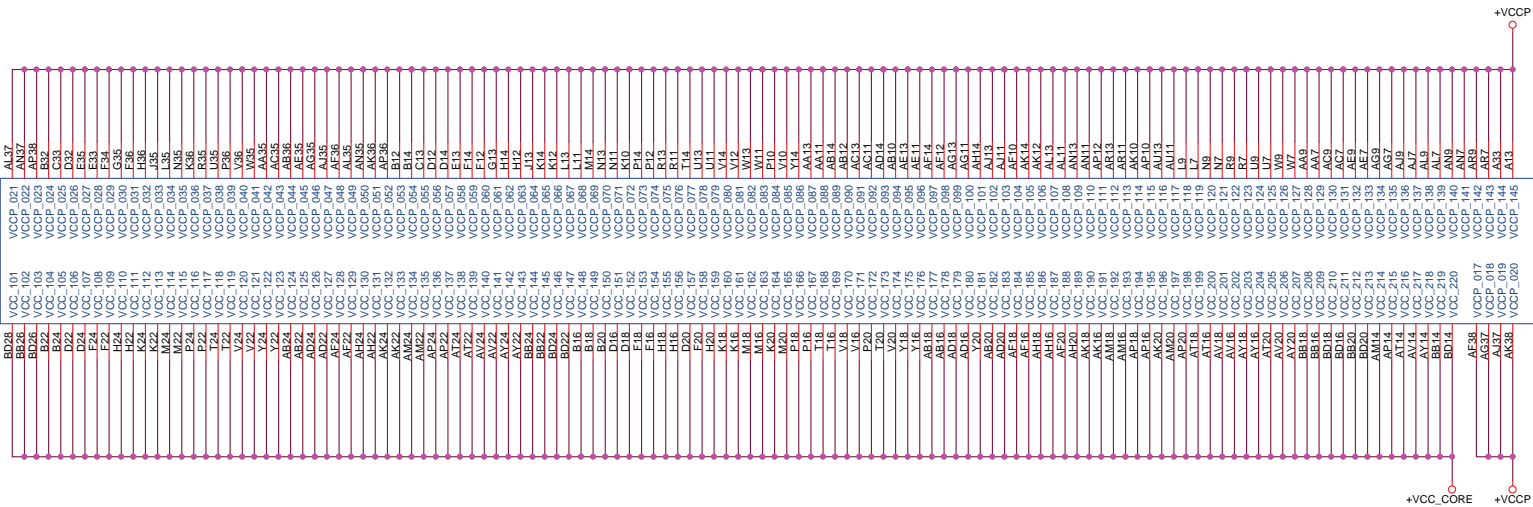
Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.



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<b>Compal Electronics, Inc.</b>	
Title	<b>Penryn(3/4)-PWR</b>
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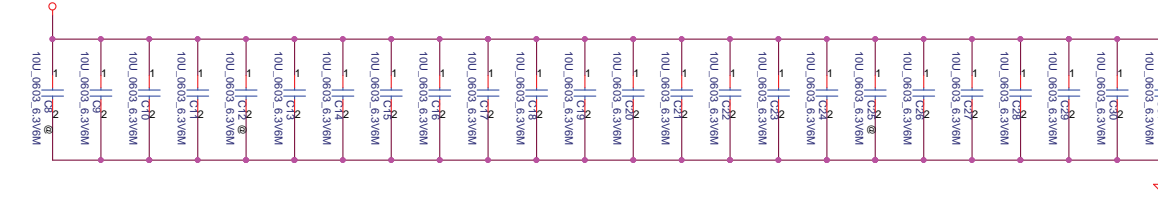
UID	VSS	VSS	AM36
B42	VSS001	VSS082	AM36
F44	VSS002	VSS083	AR35
D42	VSS003	VSS084	AV34
F42	VSS005	VSS086	AW35
H42	VSS006	VSS087	AW34
K42	VSS007	VSS088	AT36
M42	VSS008	VSS089	AT36
P42	VSS009	VSS090	AV36
T42	VSS010	VSS091	BA33
Y42	VSS011	VSS092	AY34
AB42	VSS012	VSS093	BB36
AD42	VSS014	VSS095	CB33
AF42	VSS015	VSS096	CB33
AH42	VSS016	VSS097	CB33
AK42	VSS017	VSS098	E29
AM42	VSS018	VSS099	E27
AY44	VSS019	VSS100	G29
AV44	VSS020	VSS101	E31
AT42	VSS022	VSS103	G31
AV42	VSS023	VSS104	J29
BA43	VSS024	VSS105	L29
BB42	VSS026	VSS107	L27
C49	VSS027	VSS108	N29
G37	VSS028	VSS109	J31
H38	VSS030	VSS111	L31
J39	VSS031	VSS112	N31
M38	VSS032	VSS113	AG23
L39	VSS033	VSS114	AG23
N39	VSS034	VSS115	U29
R39	VSS035	VSS116	U27
T38	VSS036	VSS117	AJ21
U39	VSS036	VSS117	U31
W39	VSS037	VSS118	W29
Y39	VSS038	VSS119	W21
AA39	VSS039	VSS120	W27
AC39	VSS040	VSS121	W31
AD38	VSS041	VSS122	AA27
AG39	VSS042	VSS123	AA29
AE39	VSS043	VSS124	AC29
AG39	VSS044	VSS125	AC27
AH38	VSS045	VSS126	AR21
AJ39	VSS046	VSS127	AC31
AL39	VSS047	VSS128	AE29
AM38	VSS048	VSS129	AE27
AN39	VSS049	VSS130	AW25
AR39	VSS050	VSS131	AG27
AR37	VSS051	VSS132	AJ29
AT38	VSS052	VSS133	AJ27
AU39	VSS053	VSS134	AE31
AW39	VSS054	VSS135	AG31
AW37	VSS056	VSS137	AJ31
BA39	VSS057	VSS138	AL29
BD40	VSS058	VSS139	AN29
BD38	VSS059	VSS140	AN27
B36	VSS060	VSS141	AL31
H34	VSS061	VSS142	AN31
D36	VSS062	VSS143	AR29
M36	VSS063	VSS144	AR27
K34	VSS064	VSS145	AR31
M34	VSS065	VSS146	AR29
M36	VSS065	VSS146	AL27
P34	VSS066	VSS147	AW29
Y36	VSS067	VSS148	AW27
T34	VSS068	VSS149	AW27
V34	VSS069	VSS150	AU31
T36	VSS070	VSS151	AW31
Y34	VSS071	VSS152	BA29
AB34	VSS072	VSS153	BA27
AD34	VSS073	VSS154	BC29
Y36	VSS074	VSS155	W19
AF34	VSS076	VSS157	BA31
AH34	VSS077	VSS158	BC31
AH36	VSS078	VSS159	C21
AK34	VSS079	VSS160	C23
AM34	VSS080	VSS161	C25
AP34	VSS081	VSS162	E25
			E23
			E21

PENRYN SFF\_UFCBGA956  
SU2700®

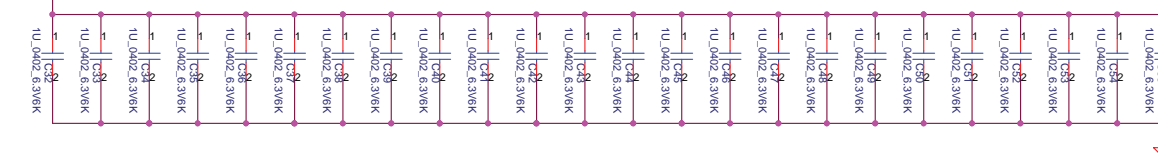
UIE	VSS	VSS	VSS
G25	VSS_164	VSS_280	AA15
G23	VSS_165	VSS_281	AC15
J25	VSS_166	VSS_282	Y10
J23	VSS_167	VSS_283	AD10
W25	VSS_168	VSS_284	AH12
L21	VSS_169	VSS_285	AE15
L23	VSS_170	VSS_286	AJ15
N23	VSS_171	VSS_287	AG15
N25	VSS_172	VSS_288	AM10
N21	VSS_174	VSS_290	AN15
R25	VSS_175	VSS_289	AR15
R23	VSS_176	VSS_292	AM10
R21	VSS_177	VSS_293	AT12
U25	VSS_178	VSS_294	AV12
U23	VSS_179	VSS_295	AW13
U21	VSS_180	VSS_296	AW11
W25	VSS_181	VSS_297	AY12
W23	VSS_182	VSS_298	AU15
W21	VSS_183	VSS_299	AW15
G27	VSS_184	VSS_300	AT10
AA25	VSS_185	VSS_301	BA13
AA23	VSS_186	VSS_302	BA11
I27	VSS_187	VSS_303	BB12
AC25	VSS_188	VSS_304	BC11
AC23	VSS_189	VSS_305	BA15
AC21	VSS_190	VSS_306	BC15
AE27	VSS_191	VSS_307	BE
AE23	VSS_192	VSS_308	DE
AE21	VSS_193	VSS_309	D6
AG25	VSS_194	VSS_310	E6
AG23	VSS_195	VSS_311	G9
AG21	VSS_196	VSS_312	F6
AJ25	VSS_197	VSS_313	H6
AJ23	VSS_198	VSS_314	K8
AJ21	VSS_199	VSS_315	L6
AL25	VSS_200	VSS_316	M8
AL23	VSS_201	VSS_317	M6
AL21	VSS_202	VSS_318	PE
AN25	VSS_203	VSS_319	PE
AN23	VSS_204	VSS_320	T6
AN21	VSS_205	VSS_321	V8
AR25	VSS_206	VSS_322	V6
AR23	VSS_207	VSS_323	U6
AR21	VSS_208	VSS_324	Y8
AU25	VSS_209	VSS_325	Y6
AU23	VSS_210	VSS_326	ABR
AU21	VSS_211	VSS_327	ABE
AW25	VSS_212	VSS_328	ADB
AW23	VSS_213	VSS_329	AD6
AW21	VSS_214	VSS_330	AE6
BA25	VSS_215	VSS_331	AF8
BA23	VSS_216	VSS_332	AF6
BA21	VSS_217	VSS_333	AHR
BC25	VSS_218	VSS_334	AH6
BC23	VSS_219	VSS_335	AK8
BC21	VSS_220	VSS_336	AK6
C17	VSS_221	VSS_337	AM8
C19	VSS_222	VSS_338	AM6
E19	VSS_223	VSS_339	APR
F17	VSS_224	VSS_340	AP6
G19	VSS_225	VSS_341	ATR
G17	VSS_226	VSS_342	AT6
J19	VSS_227	VSS_343	AU9
J17	VSS_228	VSS_344	AV6
L19	VSS_229	VSS_345	AW7
L17	VSS_230	VSS_346	AW9
N19	VSS_231	VSS_347	AY6
N17	VSS_232	VSS_348	BA9
R19	VSS_233	VSS_349	BB6
R17	VSS_234	VSS_350	BC9
U19	VSS_235	VSS_351	BD6
U17	VSS_236	VSS_352	B4
W19	VSS_237	VSS_353	C3
W17	VSS_238	VSS_354	E3
AA19	VSS_239	VSS_355	G3
AA17	VSS_240	VSS_356	J3
AC19	VSS_241	VSS_357	L3
AC17	VSS_242	VSS_358	N3
AE19	VSS_243	VSS_359	R3
AE17	VSS_244	VSS_360	U3
AG19	VSS_245	VSS_361	W3
AG17	VSS_246	VSS_362	AA3
AJ19	VSS_247	VSS_363	AC3
AJ17	VSS_248	VSS_364	AE3
AL19	VSS_249	VSS_365	AG3
AL17	VSS_250	VSS_366	AJ3
AN19	VSS_251	VSS_367	AL3
AN17	VSS_252	VSS_368	AN3
AR19	VSS_253	VSS_369	AR3
AR17	VSS_254	VSS_370	AU3
AU19	VSS_255	VSS_371	AW3
AU17	VSS_256	VSS_372	BA3
AW19	VSS_257	VSS_373	BC3
BA19	VSS_258	VSS_374	E1
BA17	VSS_259	VSS_375	G1
BC19	VSS_260	VSS_376	AW1
C11	VSS_262	VSS_378	BA1
C15	VSS_263	VSS_379	BB2
E15	VSS_265	VSS_381	A41
G15	VSS_266	VSS_382	A39
H10	VSS_267	VSS_383	A29
M12	VSS_268	VSS_384	A27
J15	VSS_269	VSS_385	A25
L15	VSS_270	VSS_386	A23
N15	VSS_271	VSS_387	A21
M10	VSS_272	VSS_388	A19
T12	VSS_273	VSS_389	A17
R15	VSS_274	VSS_390	A11
U15	VSS_275	VSS_391	A15
W15	VSS_276	VSS_392	A7
T10	VSS_277	VSS_393	A5
Y12	VSS_278	VSS_394	A9
VSS_279	VSS_395	BD4	

PENRYN SFF\_UFCBGA956  
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### Mid Frequency Decoupling

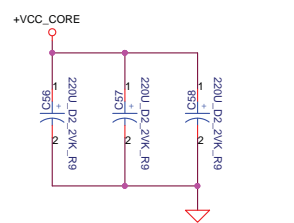


### High Frequency Decoupling

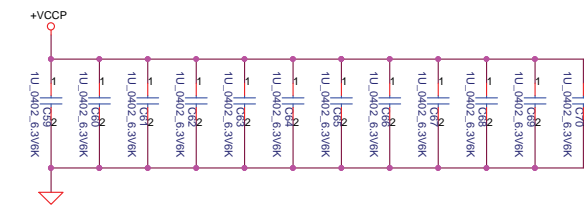


6/14 :Replace 12pcs 10uF\_0805 to 24 pcs 1uF\_0402 for CPU transient fail issue.

**ESR <= 1.5m ohm**  
**Near CPU CORE regulator**



Del C37 to improve power plan. 6/14

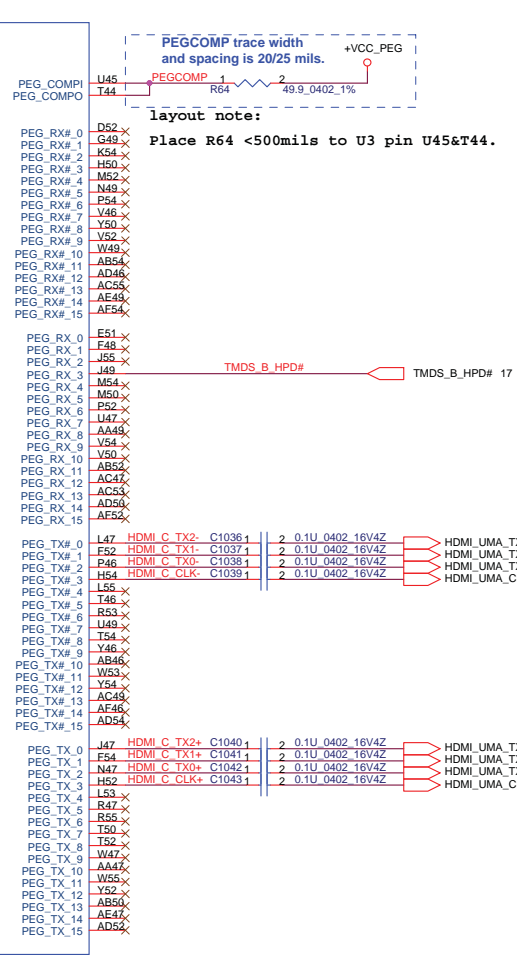
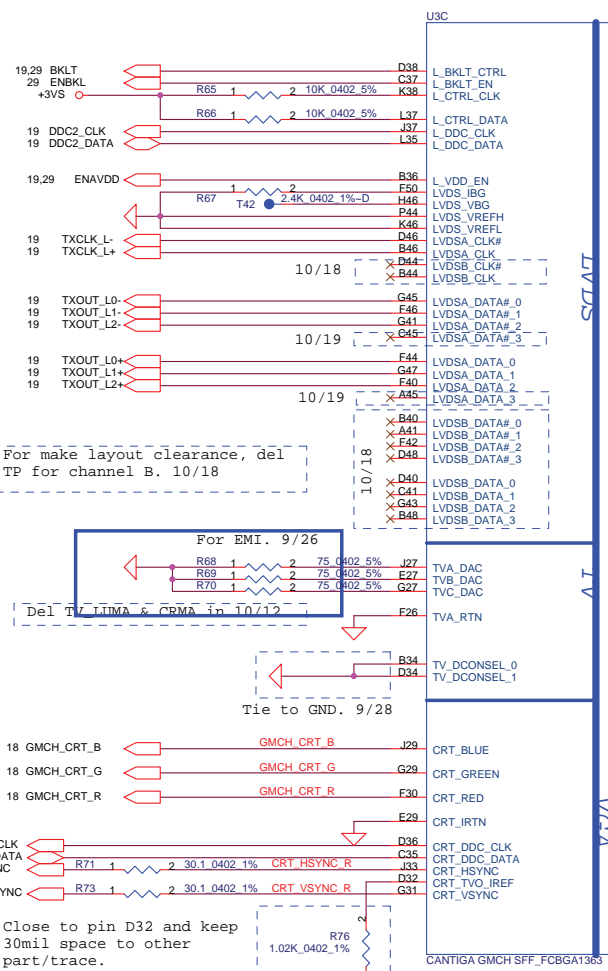


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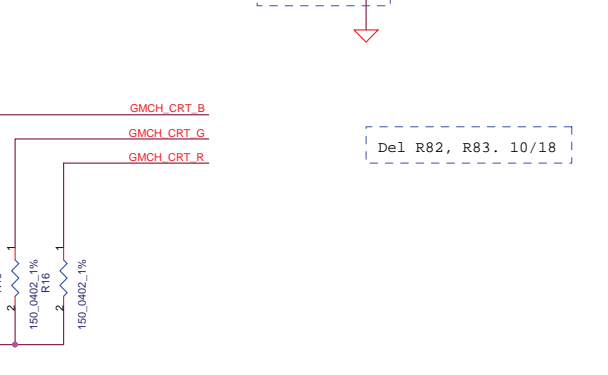




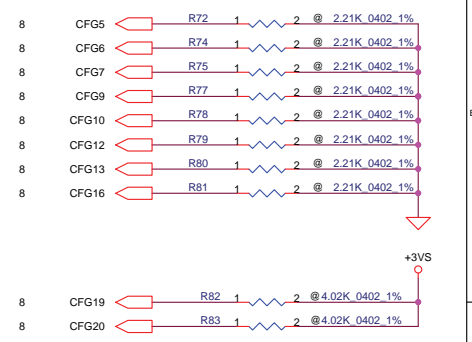


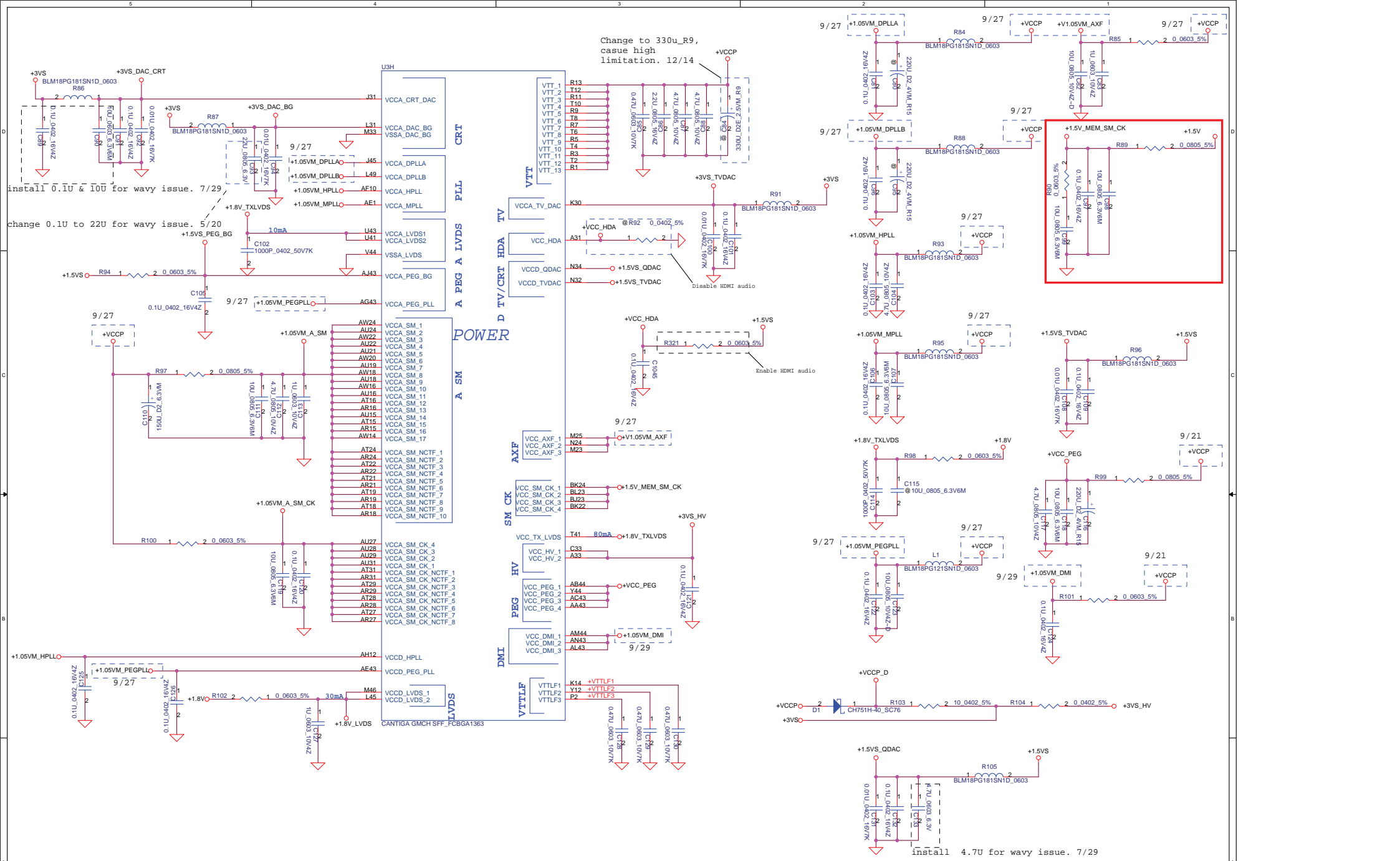
### Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane (Lane number in Order)
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



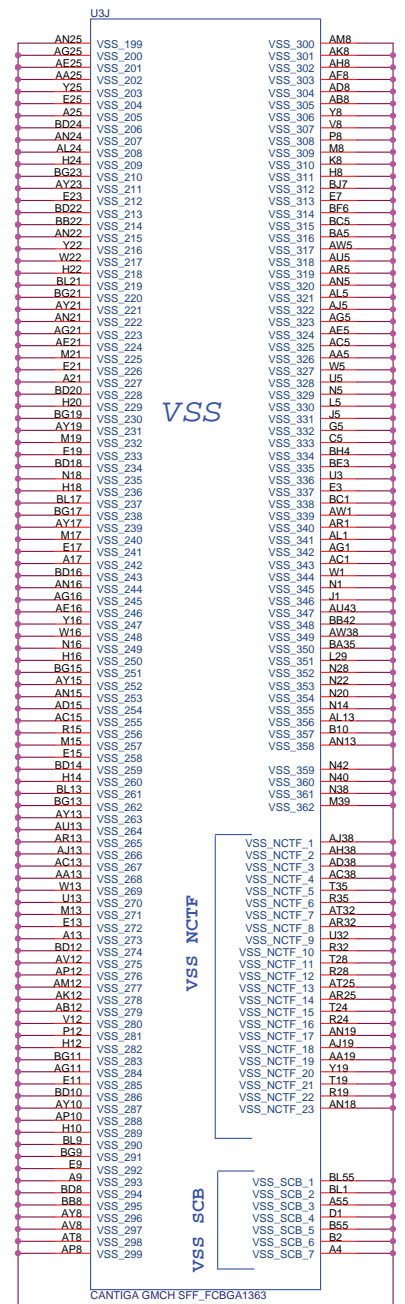
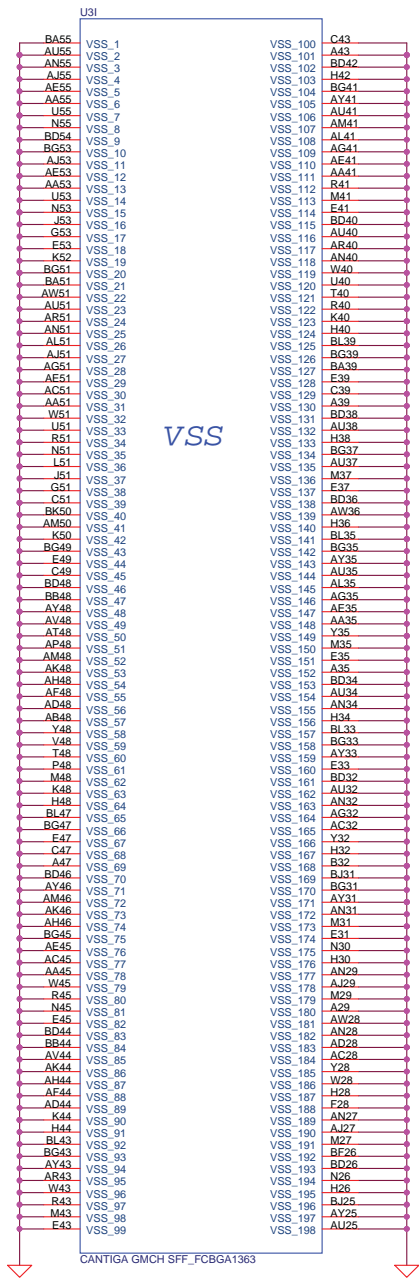
Remove R84 ~ R86 since already have 75ohm of page17. 10/27



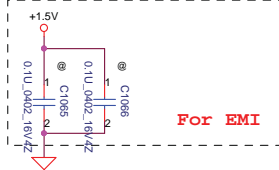


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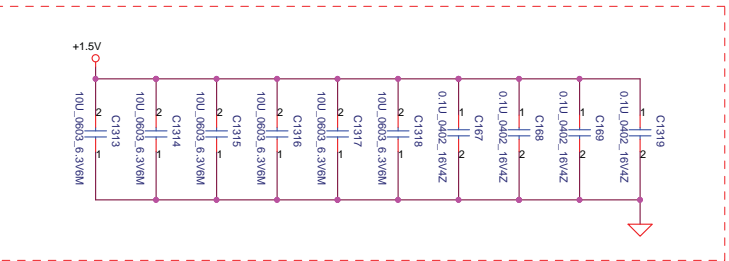


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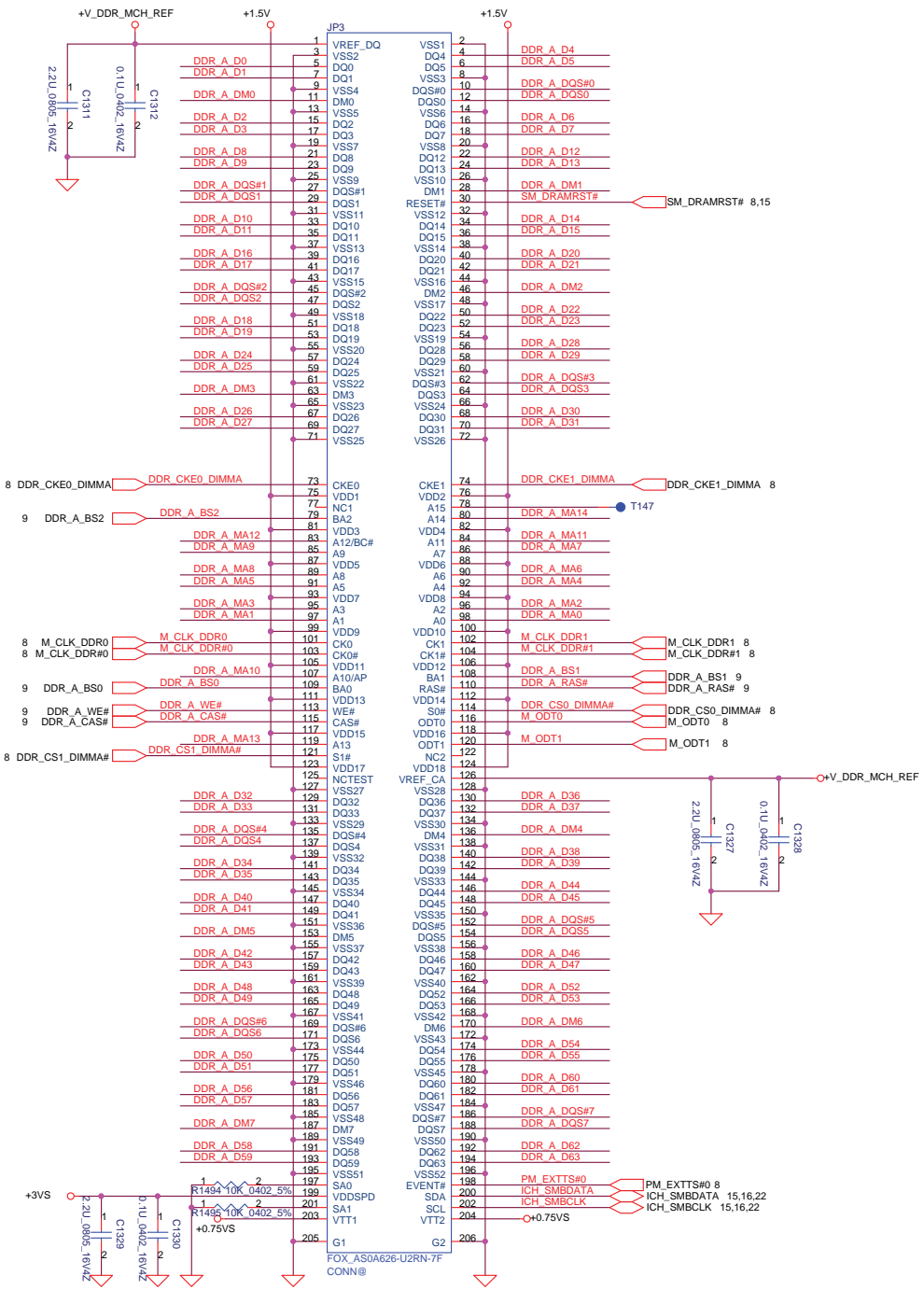
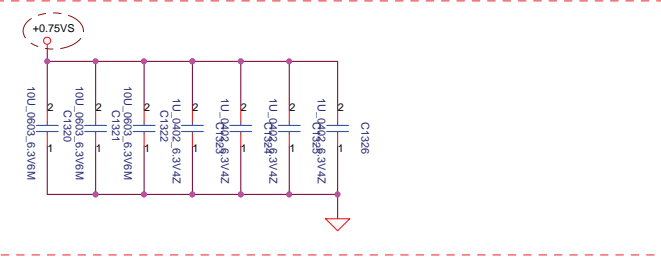


For EMI

Layout Note:  
Place near JP3



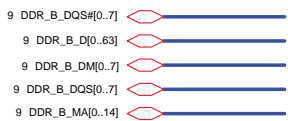
Layout Note:  
Place near JP3.203,204



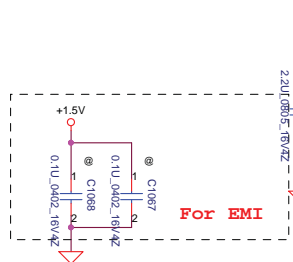
Top side

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Issued Date	2009/04/01	Deciphered Date	2010/12/31	DDR3 SO-DIMM Slot A
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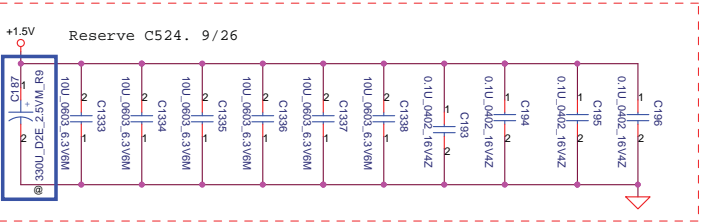




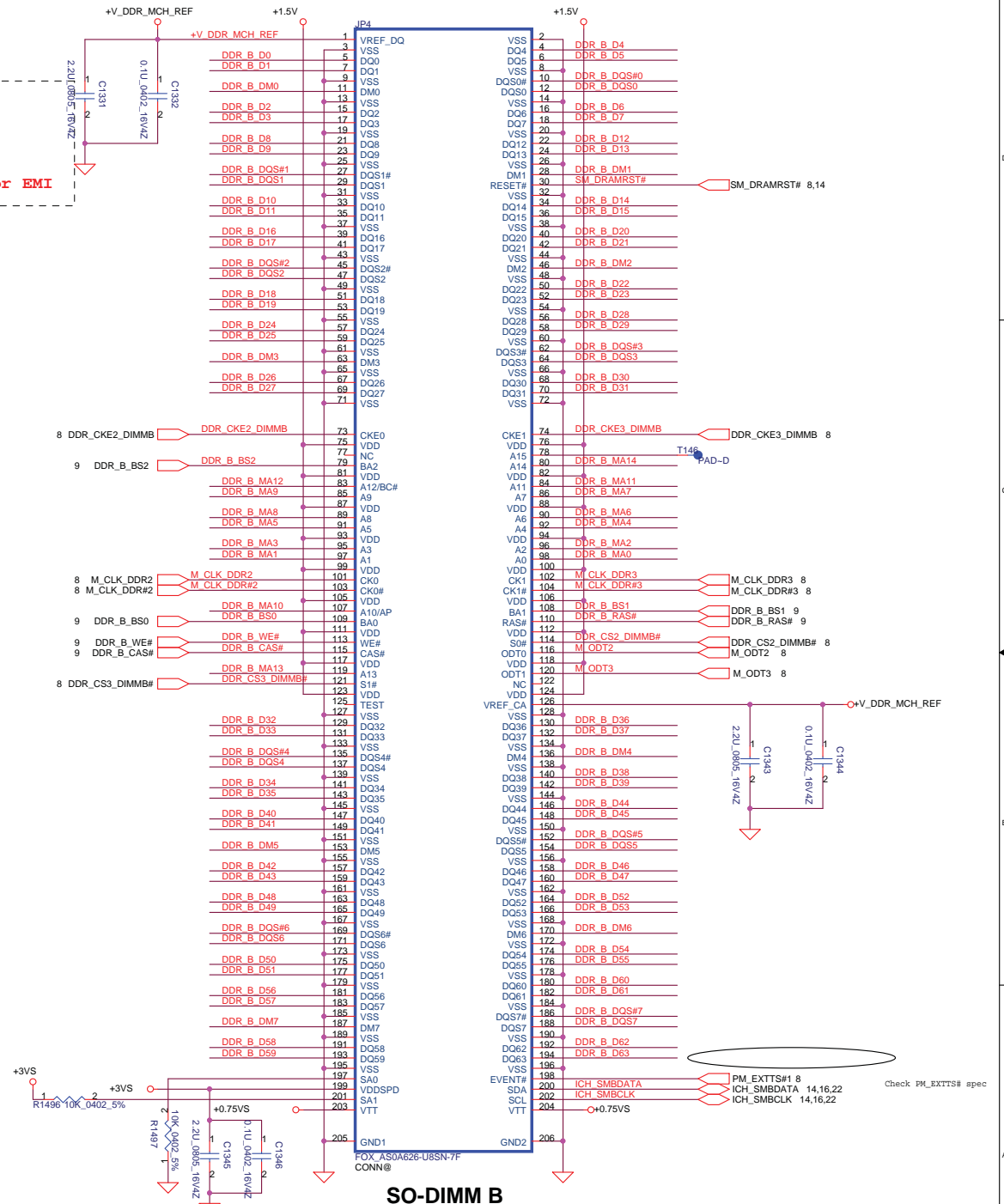
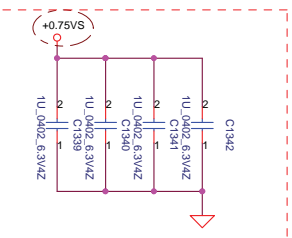
**Layout Note:**  
Place near JP4



**For EMI**



**Layout Note:**  
Place near JP4.203,204



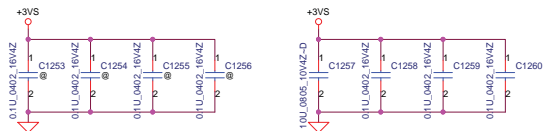
**SO-DIMM B  
Bottom side**

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close to U8 VCC (+3VS) pins (one Pin one Capacitor)

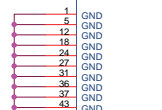


### Intel Cantiga TMDs Pin Definition

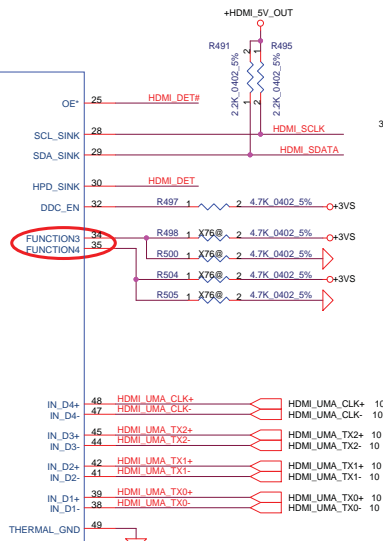
TMDs_B_CLK	PEG_TXP_3
TMDs_B_CLK#	PEG_TXN_3
TMDs_B_DATA0	PEG_TXP_2
TMDs_B_DATA0#	PEG_TXN_2
TMDs_B_DATA1	PEG_TXP_1
TMDs_B_DATA1#	PEG_TXN_1
TMDs_B_DATA2	PEG_TXP_0
TMDs_B_DATA2#	PEG_TXN_0
TMDs_B_HPD#	PEG_RXP_3



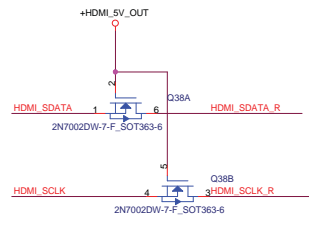
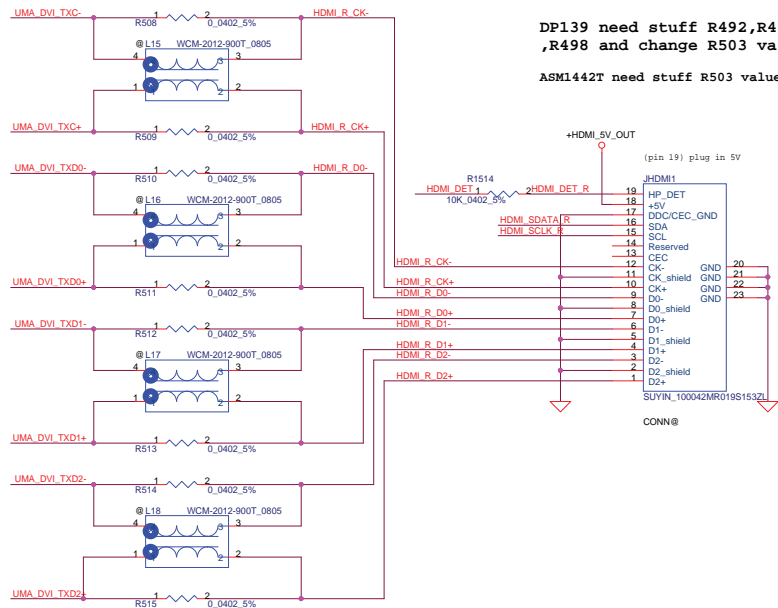
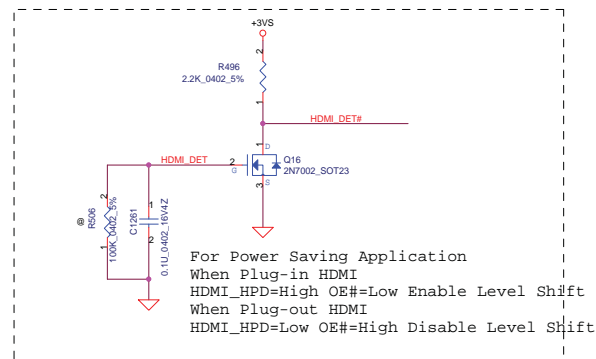
Trace AS Short PASS



DP139 need stuff R492,R494,  
,R498 and change R503 value to 3.9K  
ASM1442T need stuff R503 value 3.6K

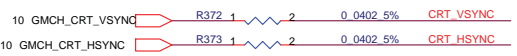
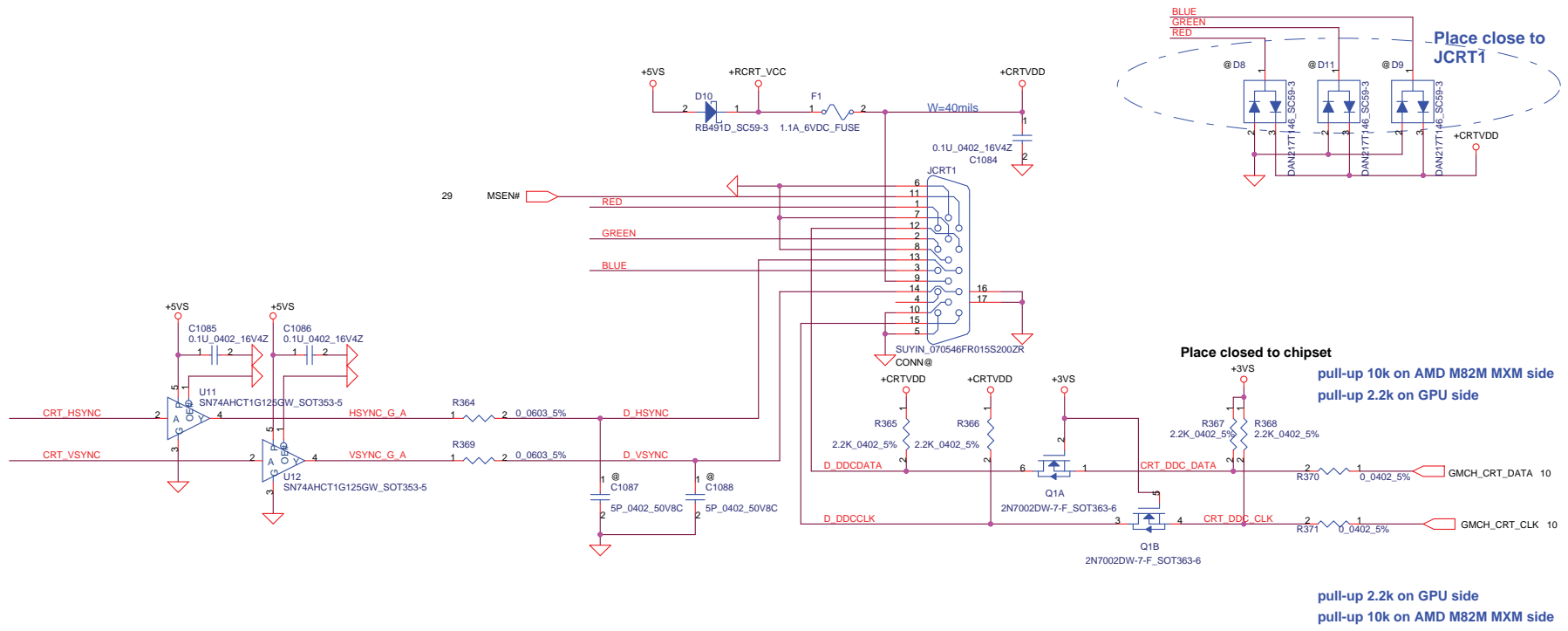


Pin34	Pin35	Equalization	Default
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	*

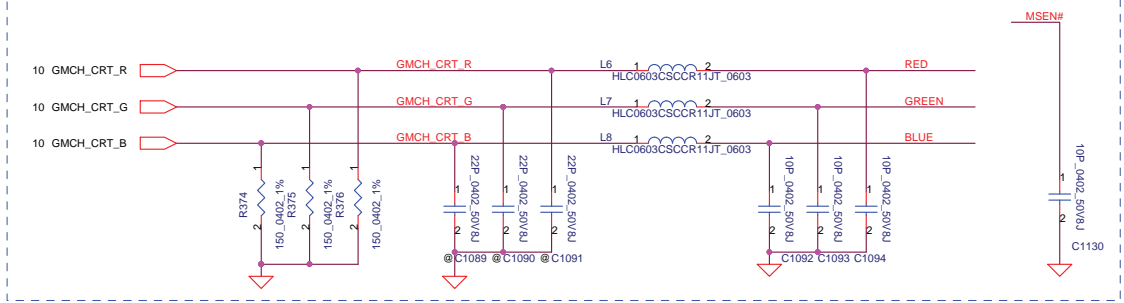


Q38 Please close to JHDMI1

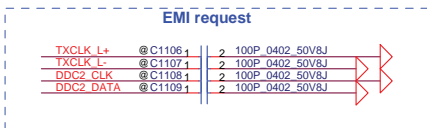
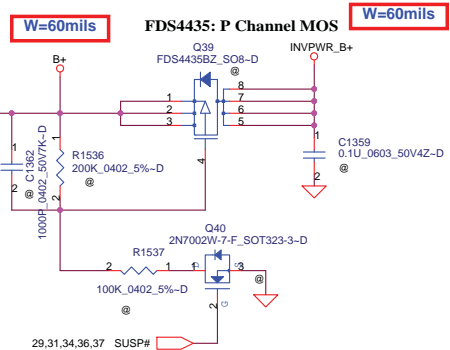
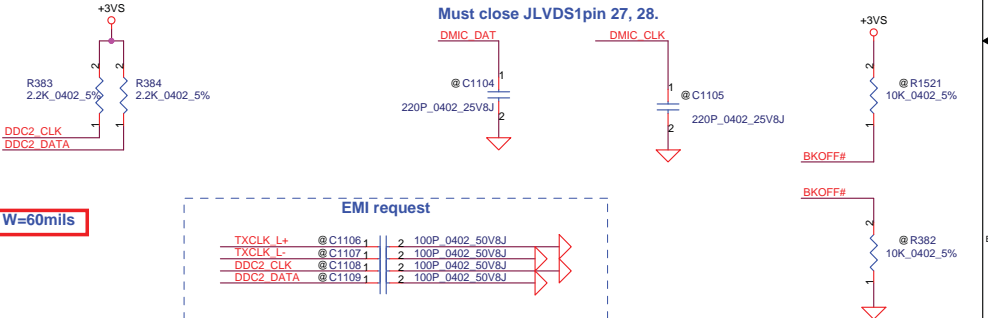
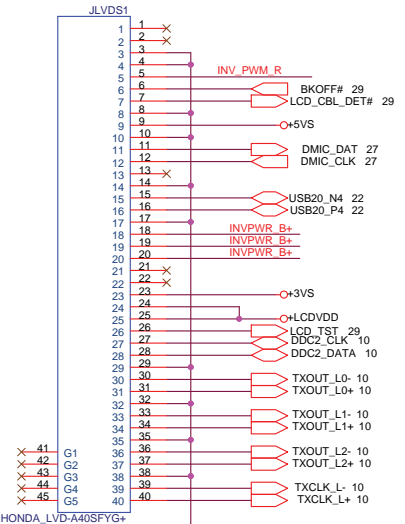
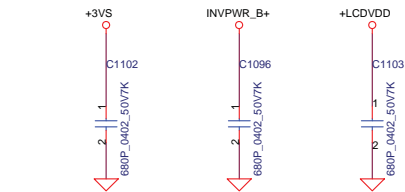
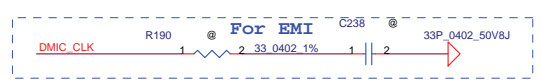
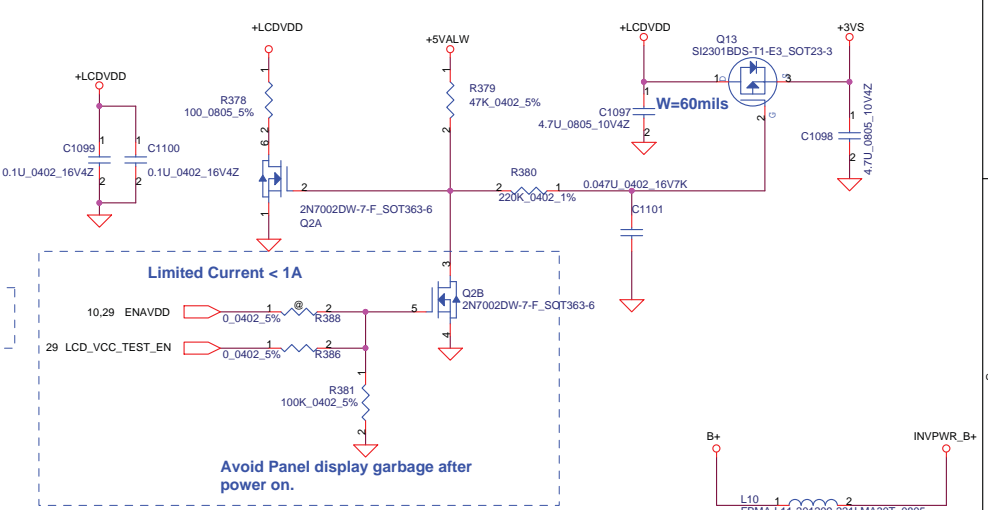
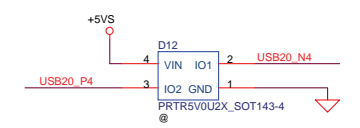
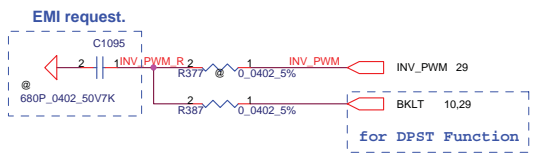
Pin 10	Pin 4	Pin 3	Swing	Pre-amp	Slew-rate	Default
0	0	0	450	0	0	
0	0	1	420	0	0	
0	1	0	450	0	0	
0	1	1	460	0	-4dB	*
1	0	0	340	0	0	
1	0	1	400	2dB	0	
1	1	0	400	2dB	0	
1	1	1	420	0	0	



### CRT Termination/EMI Filter

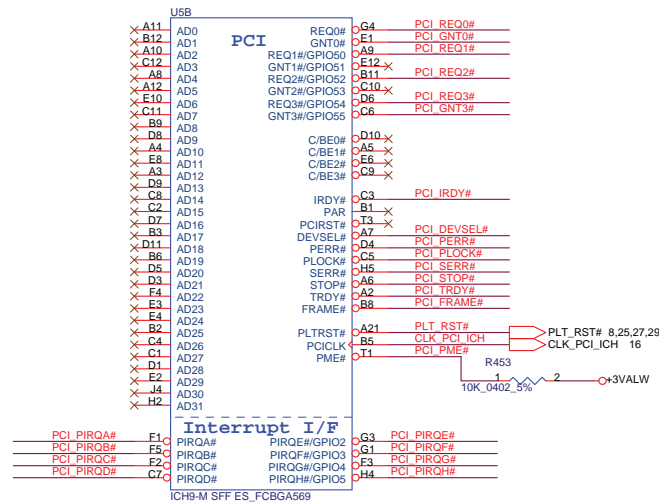
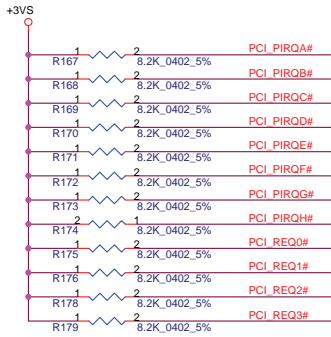
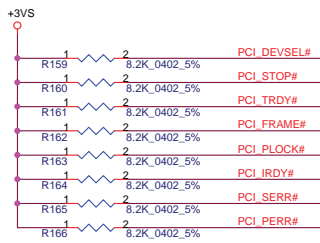


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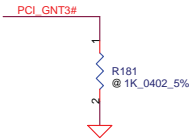


**LVDS CONN & USB Camera + Dig Mic**

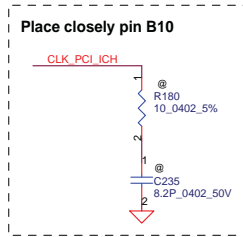
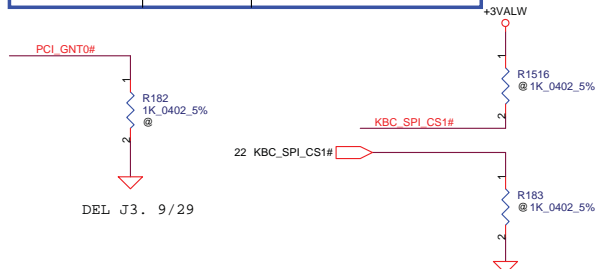
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				Customer	LA-5541P	
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A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

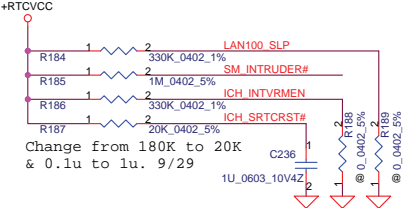


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

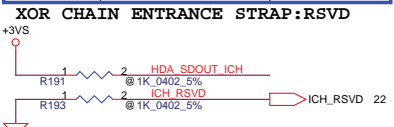


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Title	ICH9M(I/4)-PCI/INT	
Document Number	LA-5541P	
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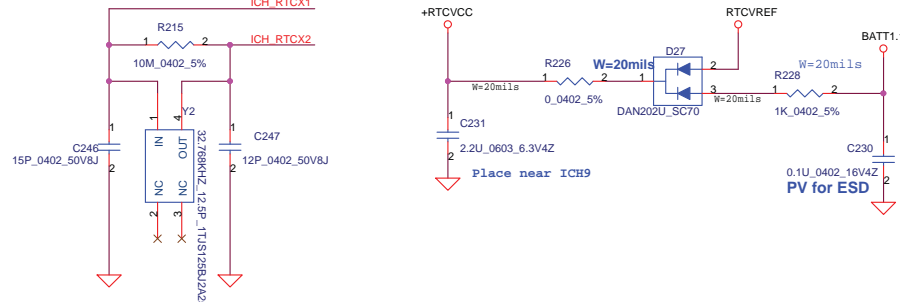
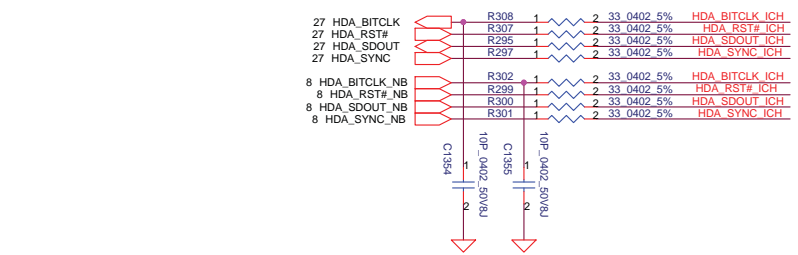
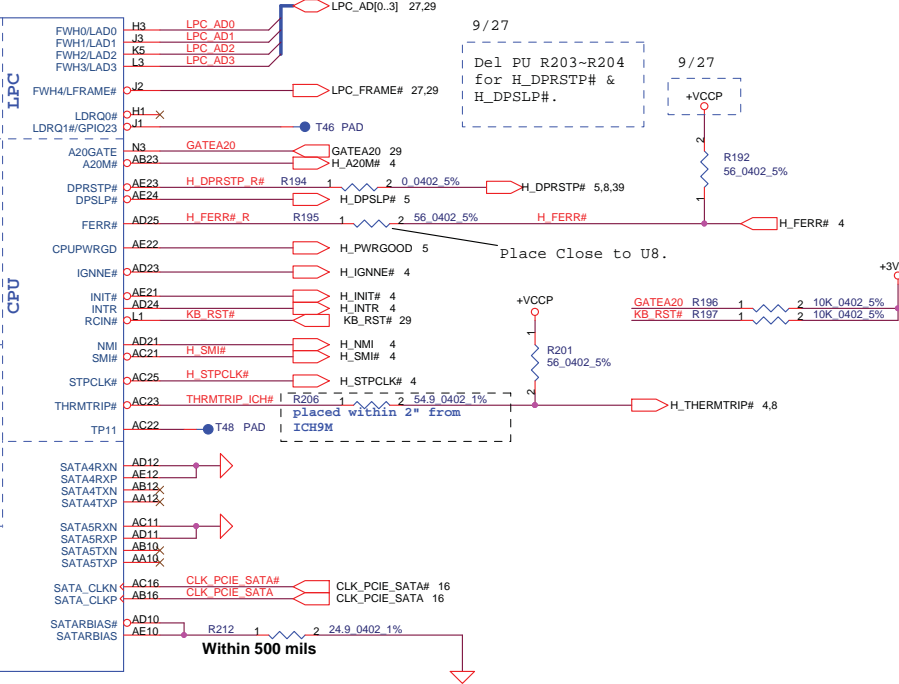
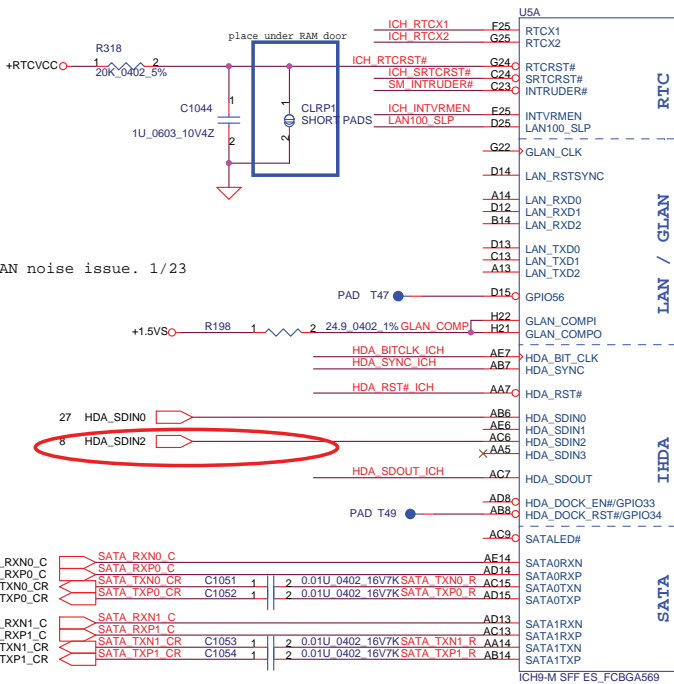


ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal (D)
1	1	PCIE Bit

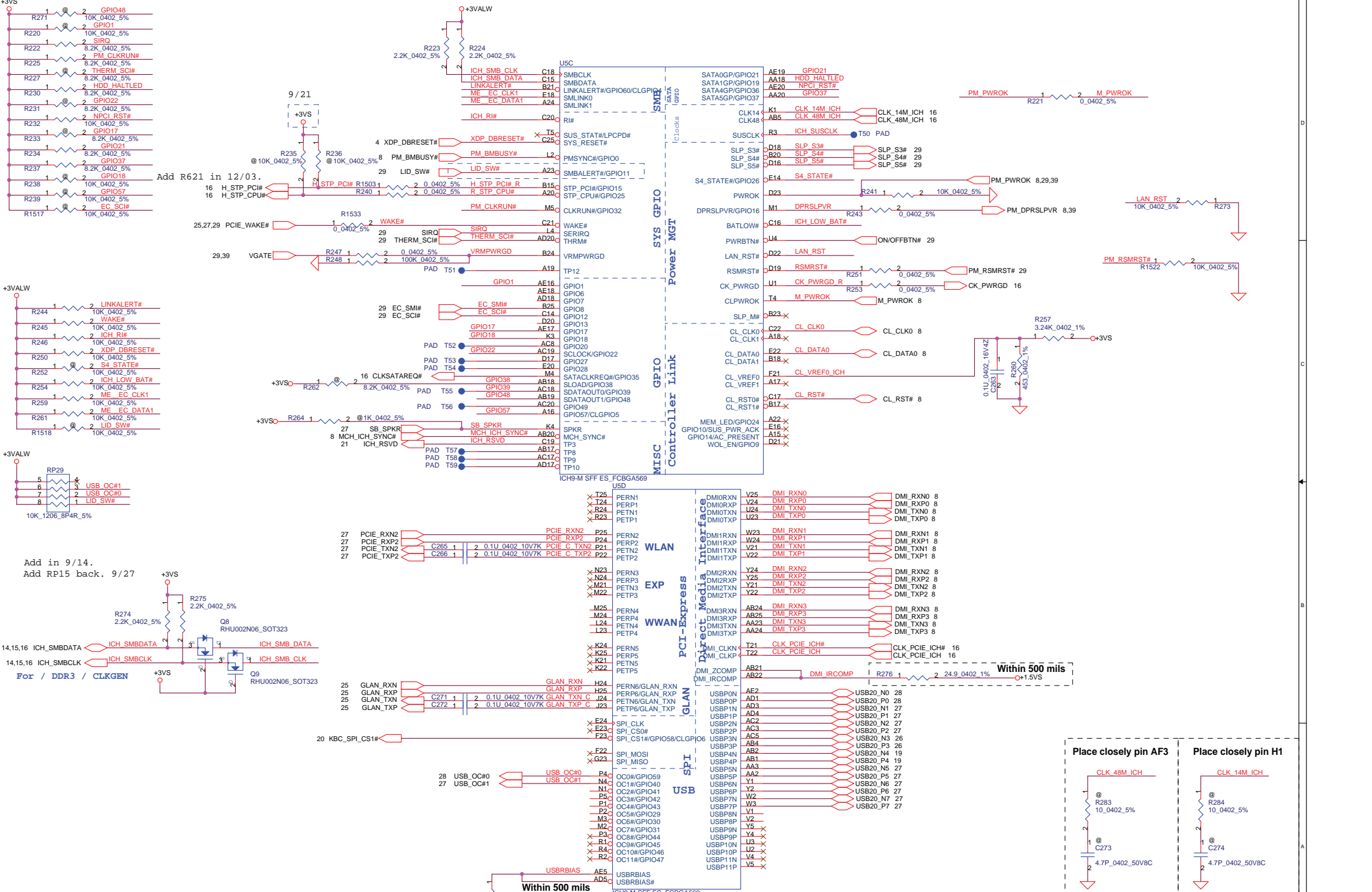


Add C599 ~ C602 to solve WWAN noise issue. 1/23

Remove R227 & C199



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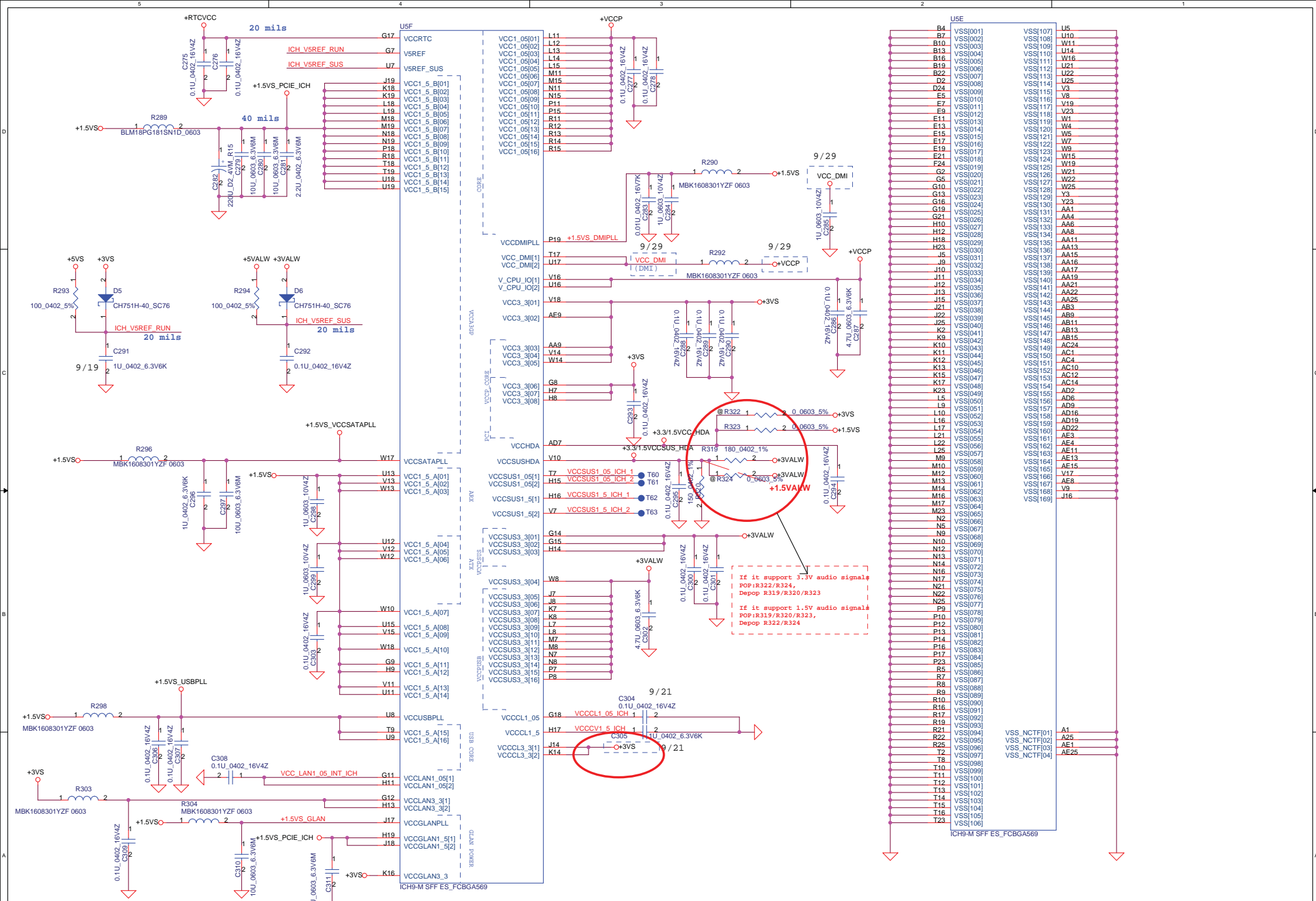
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**Compal Electronics, Inc.**

**ICH9M(3/4)-DMI/USB/GPIO/PCIE**

Document Number  
**LA-5541P**

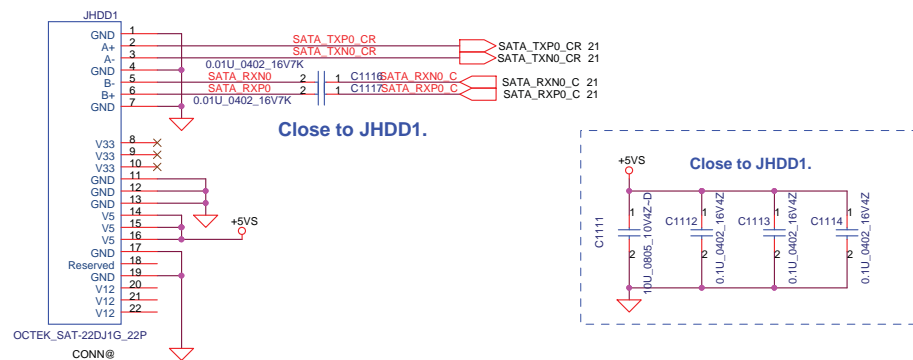
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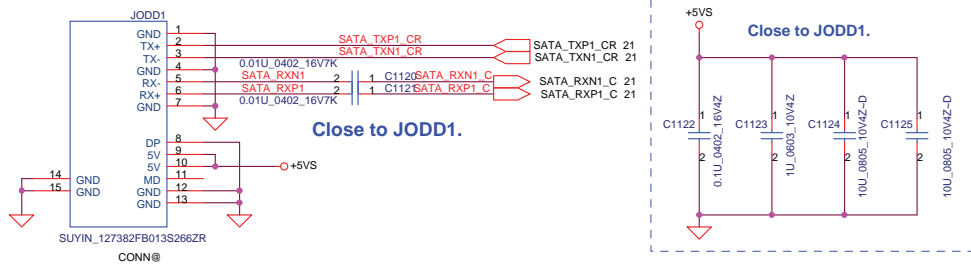
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B4	VSS1001
B7	VSS1002
B10	VSS1003
B13	VSS1004
B16	VSS1005
B19	VSS1006
B22	VSS1007
B25	VSS1008
D24	VSS1009
E5	VSS1010
E8	VSS1011
E9	VSS1012
E11	VSS1013
E13	VSS1014
E15	VSS1015
E17	VSS1016
E19	VSS1017
E21	VSS1018
F24	VSS1019
G2	VSS1020
G5	VSS1021
G10	VSS1022
G13	VSS1023
G16	VSS1024
G19	VSS1025
G21	VSS1026
H10	VSS1027
H12	VSS1028
H18	VSS1029
H23	VSS1030
J5	VSS1031
J9	VSS1032
J10	VSS1033
J11	VSS1034
J12	VSS1035
J13	VSS1036
J15	VSS1037
J21	VSS1038
J25	VSS1039
K2	VSS1040
K9	VSS1041
K10	VSS1042
K11	VSS1043
K12	VSS1044
K13	VSS1045
K15	VSS1046
K17	VSS1047
K23	VSS1048
L5	VSS1049
L10	VSS1050
L16	VSS1051
L17	VSS1052
L21	VSS1053
L22	VSS1054
L25	VSS1055
M9	VSS1056
M10	VSS1057
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M14	VSS1060
M16	VSS1061
M17	VSS1062
M23	VSS1063
N2	VSS1064
N5	VSS1065
N9	VSS1066
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N13	VSS1069
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N22	VSS1074
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P9	VSS1076
P10	VSS1077
P12	VSS1078
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P14	VSS1080
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P17	VSS1082
P23	VSS1083
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R9	VSS1087
R10	VSS1088
R16	VSS1089
R17	VSS1090
R19	VSS1091
R21	VSS1092
R22	VSS1093
R25	VSS1094
T2	VSS1095
T8	VSS1096
T9	VSS1097
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### HDD Connector

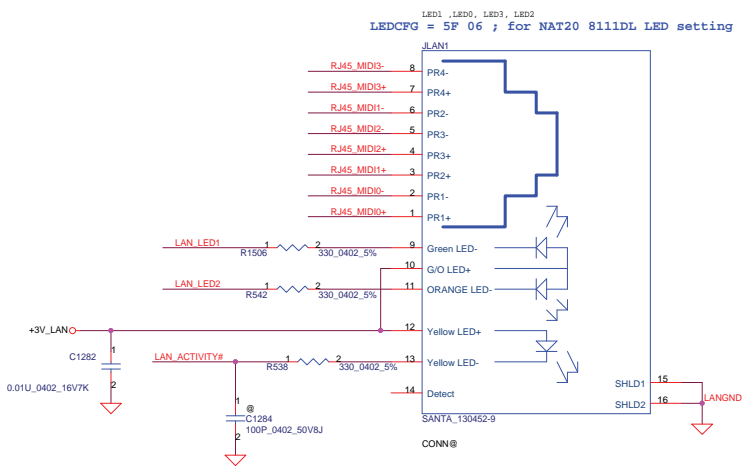
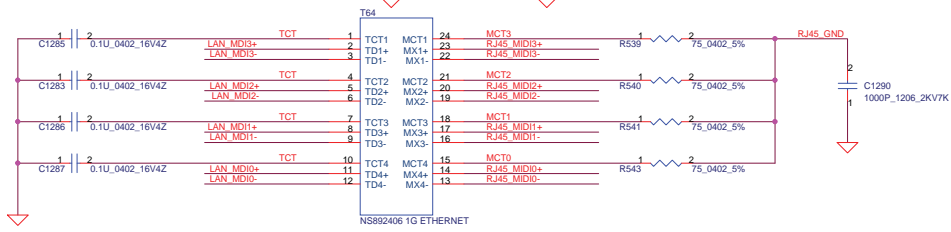
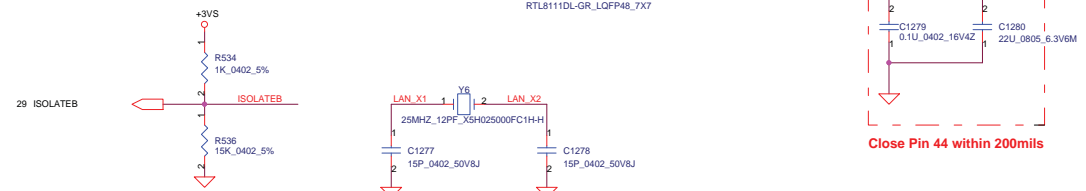
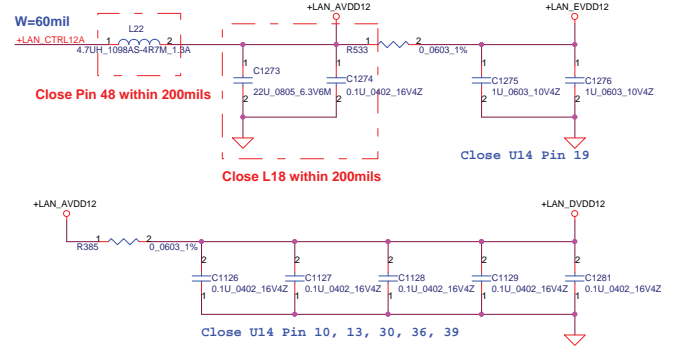
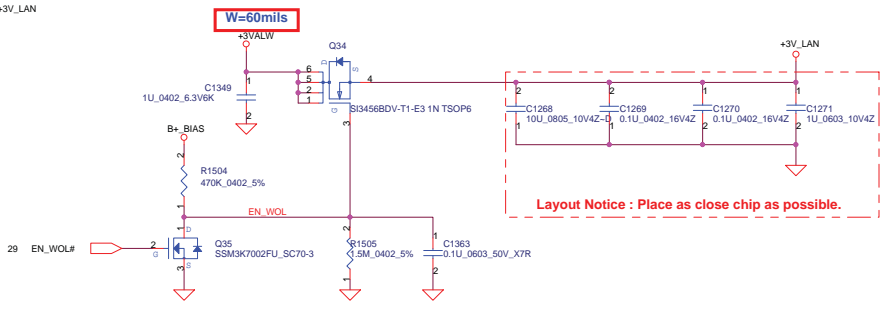
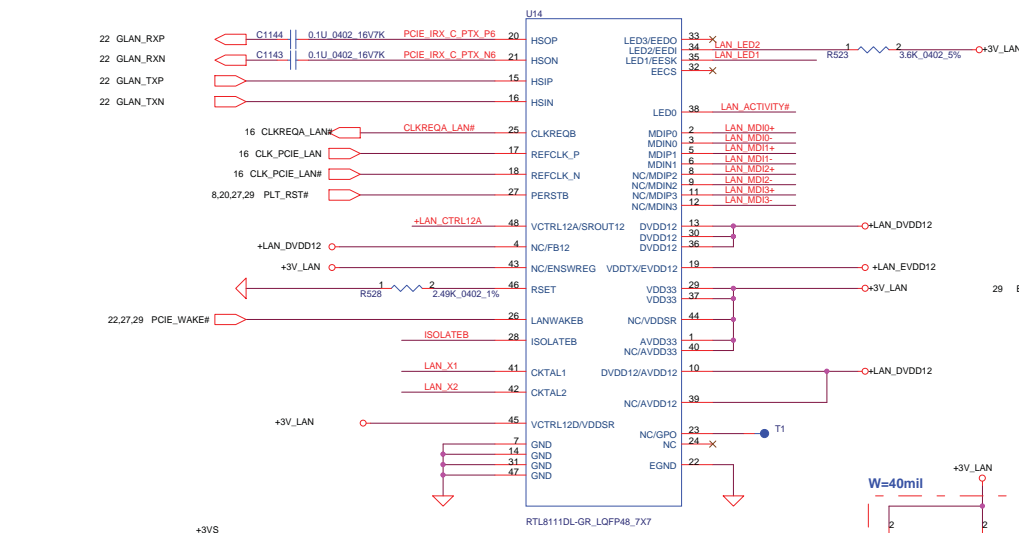


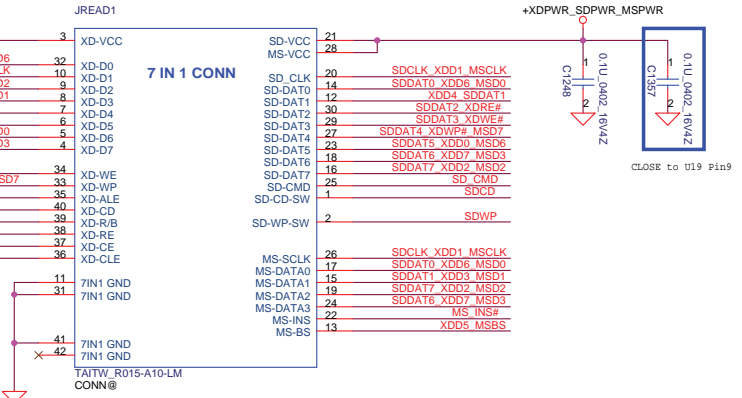
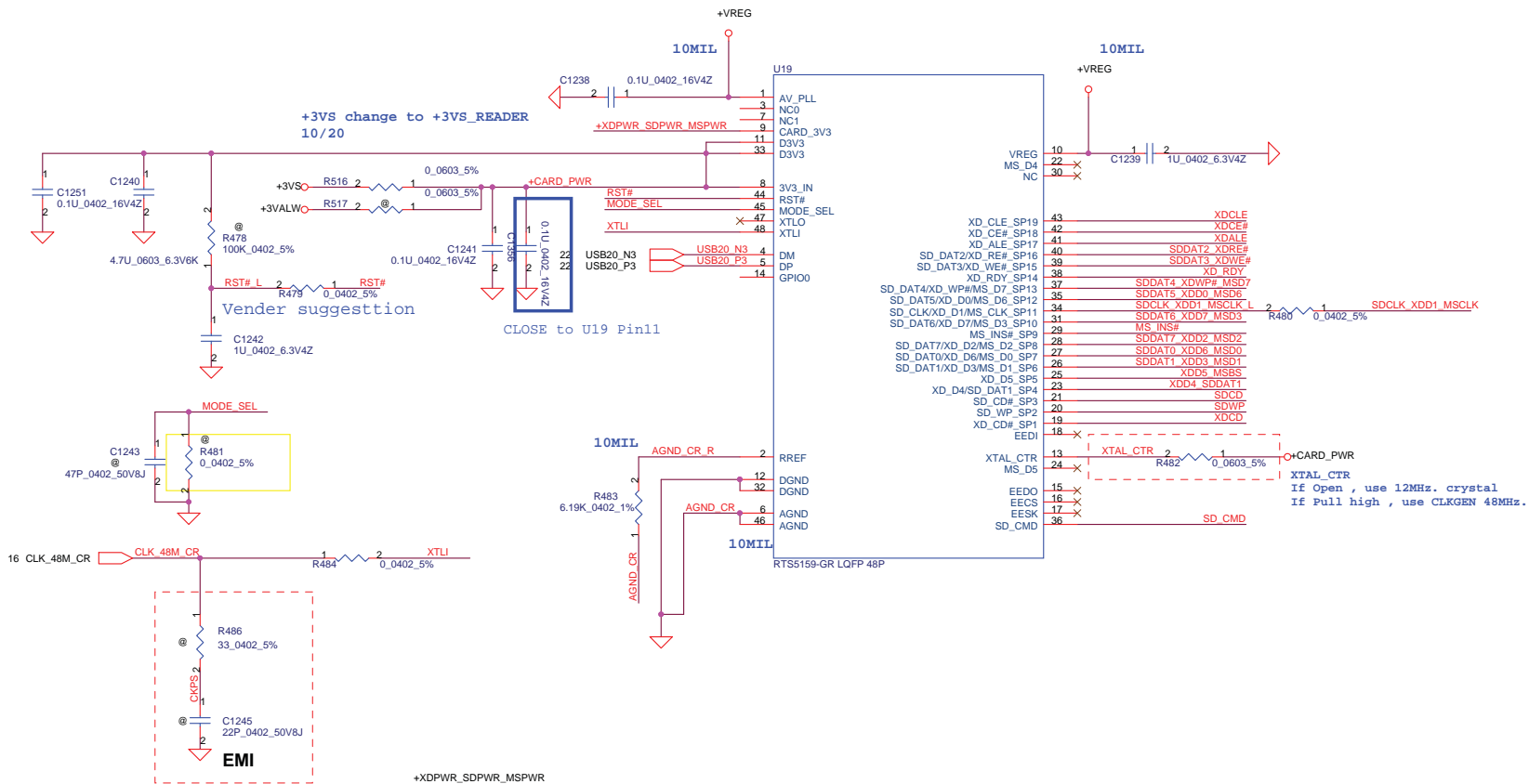
### DVD-ROM Connector



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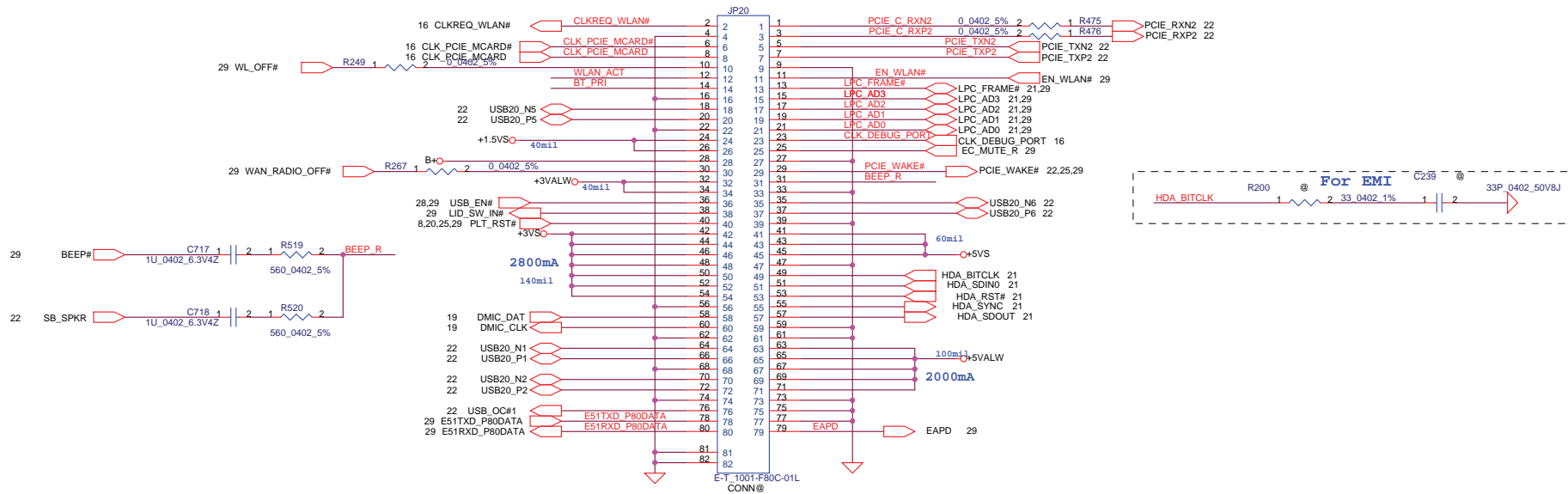


M\_SCLK and S\_DCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158B側).

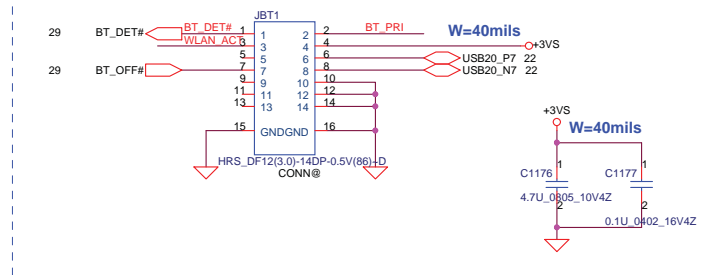
Security Classification	Compal Secret Data	
Issued Date	2009/04/01	Deciphered Date
		2010/12/31
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<b>Compal Electronics, Inc.</b>	
<b>Card Reader RTL5159-GR</b>	
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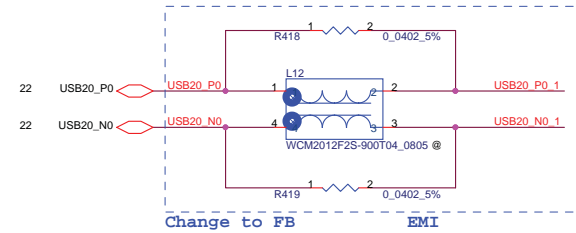
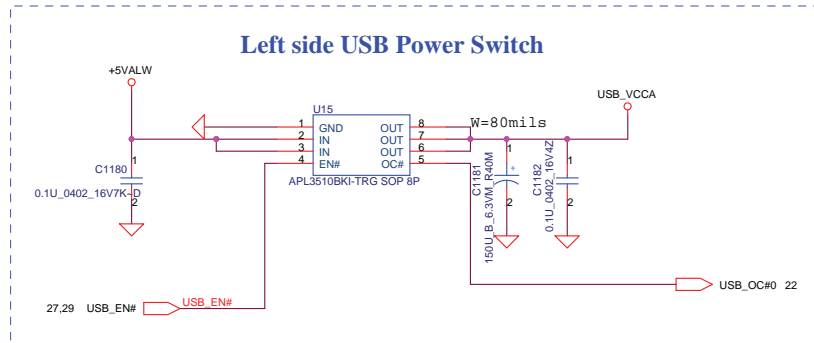
### BTB Conn.



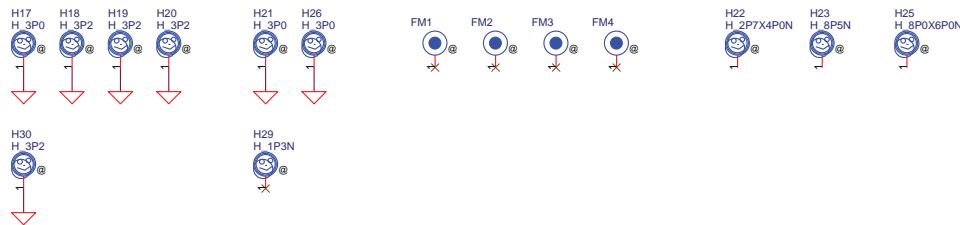
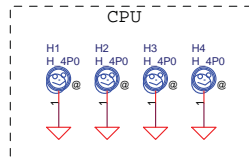
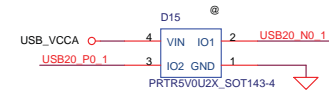
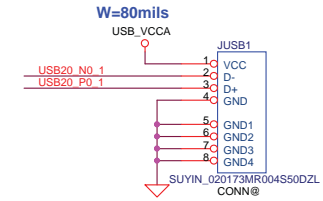
### Blue Tooth Conn.



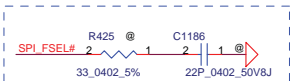
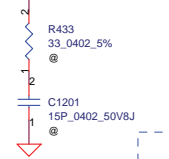
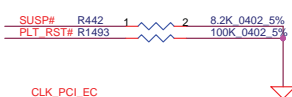
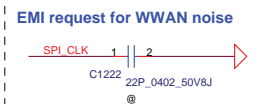
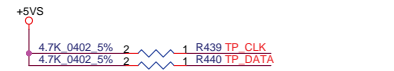
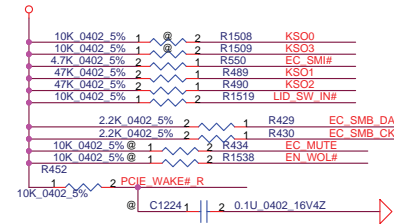
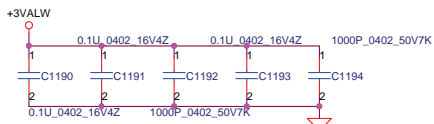
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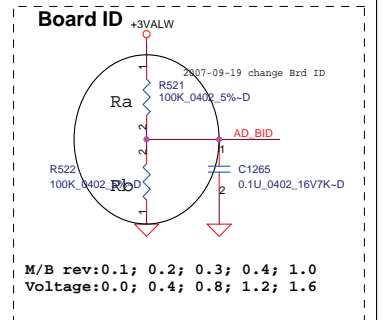
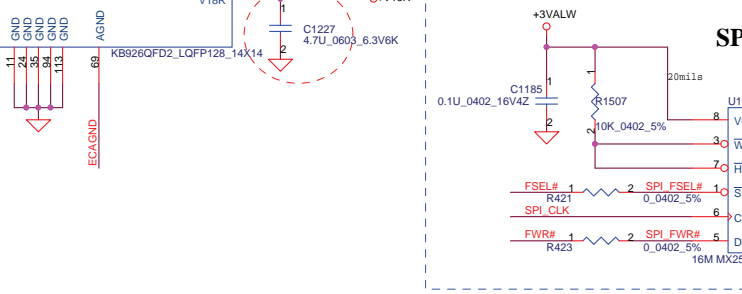
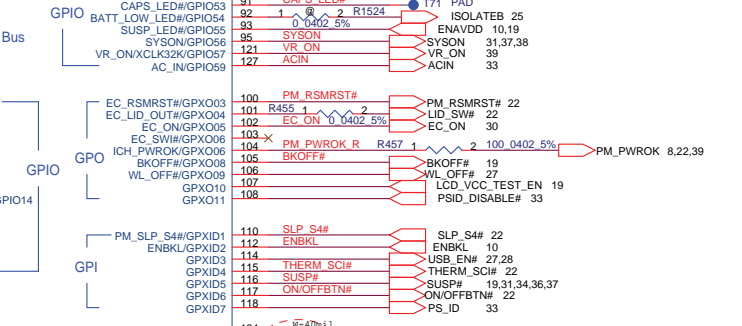
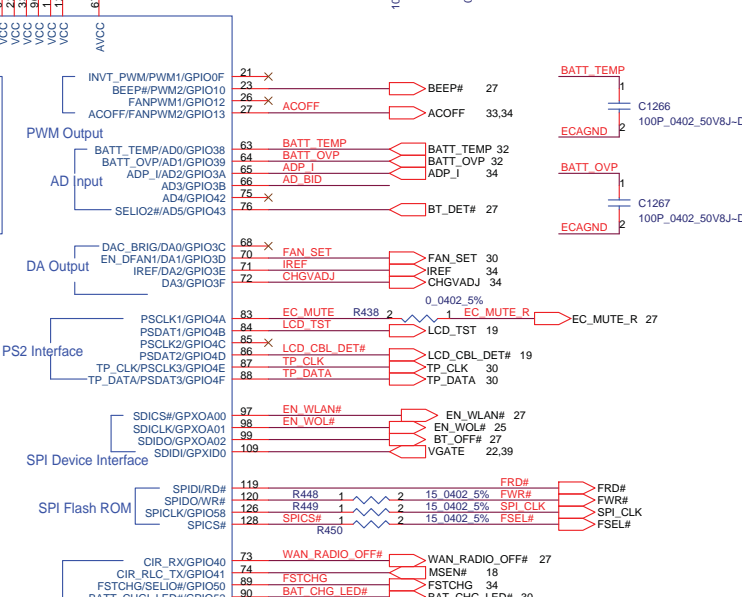
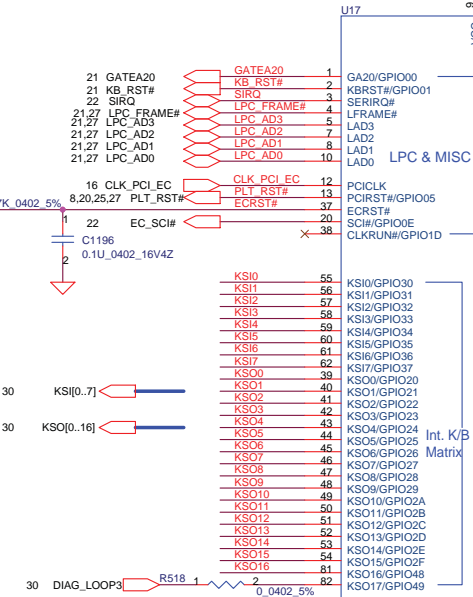
### USB Conn.



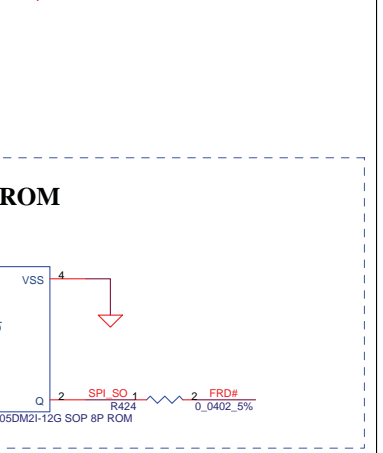
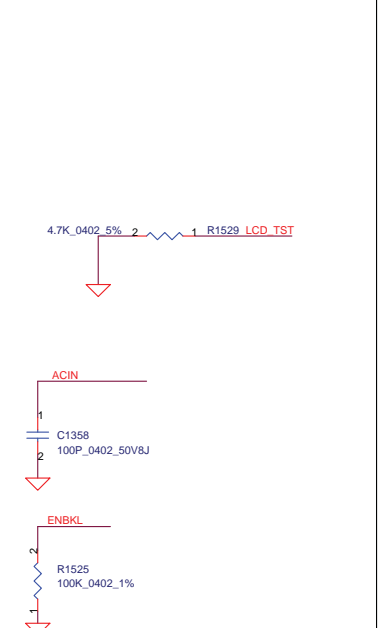
Security Classification	Compal Secret Data			Title	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	USB/Scrows	
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EMi request

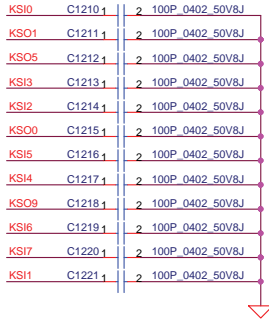
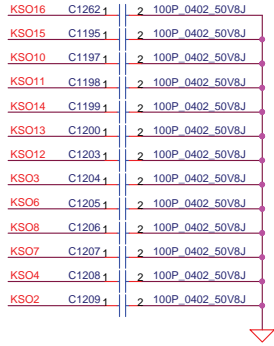


M/B rev:0.1; 0.2; 0.3; 0.4; 1.0  
Voltage:0.0; 0.4; 0.8; 1.2; 1.6

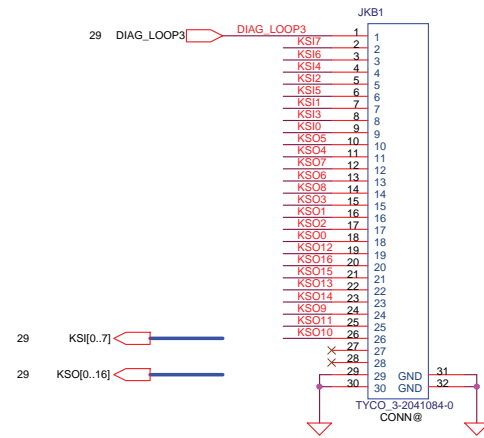


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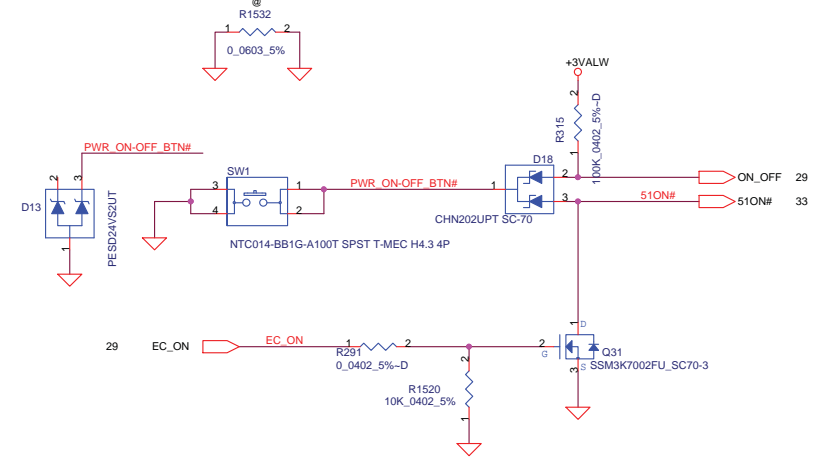
**For EMI**



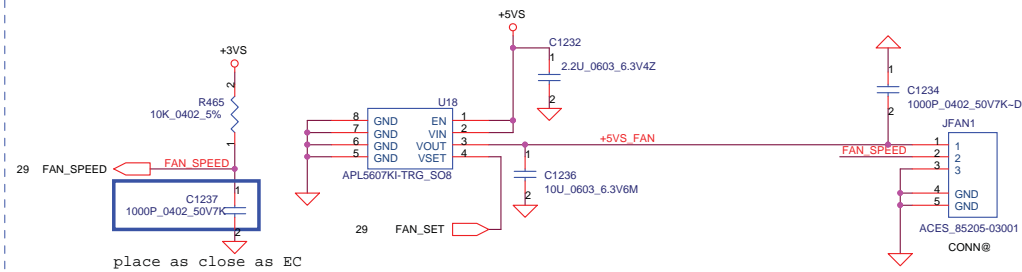
**INT KBD Conn.**



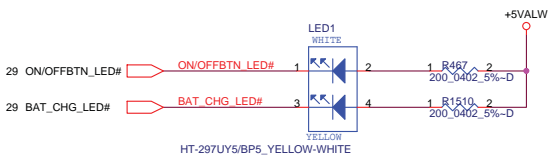
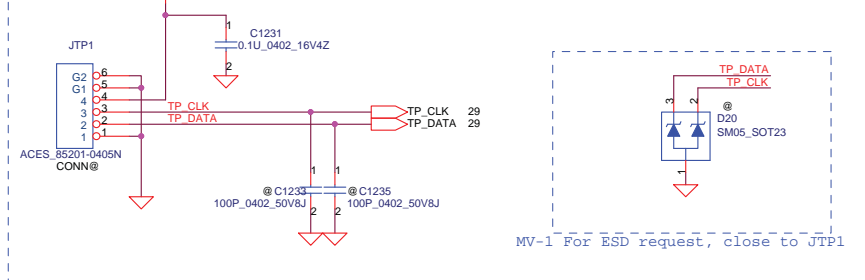
**Power Button**



**Fan Control Circuit**

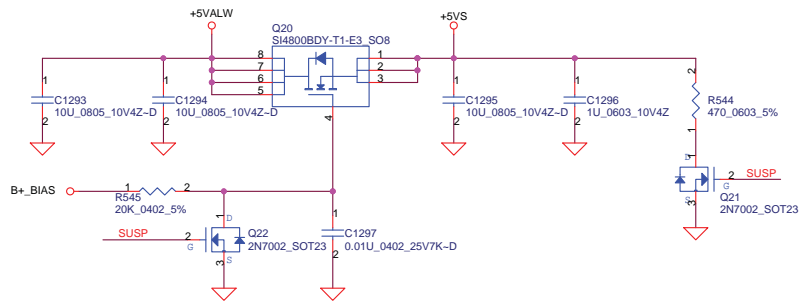


**Touch Pad Connector**

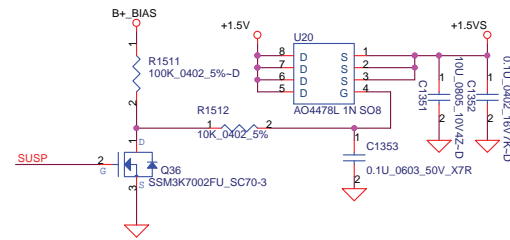


Security Classification		Compal Secret Data		Title	
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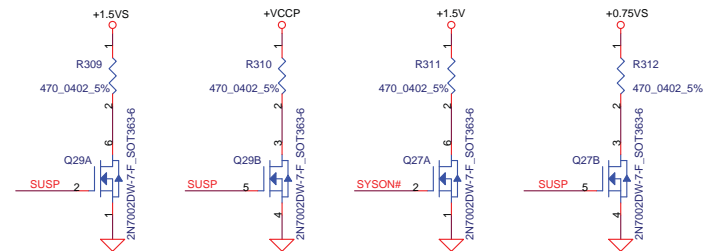
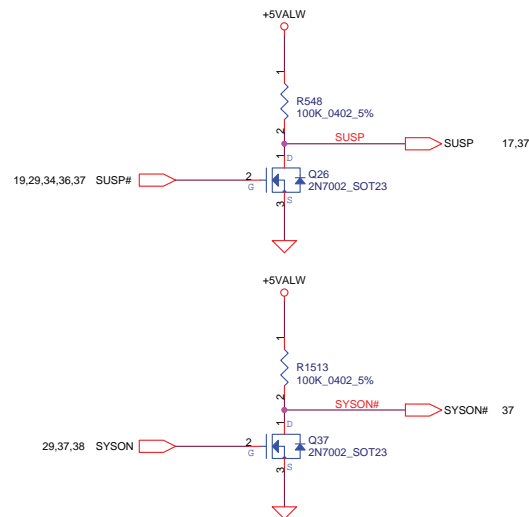
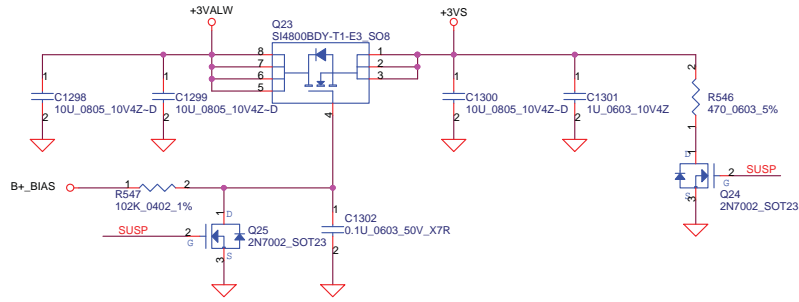
**+5VALW to +5VS**



**+1.5V To +1.5VS**

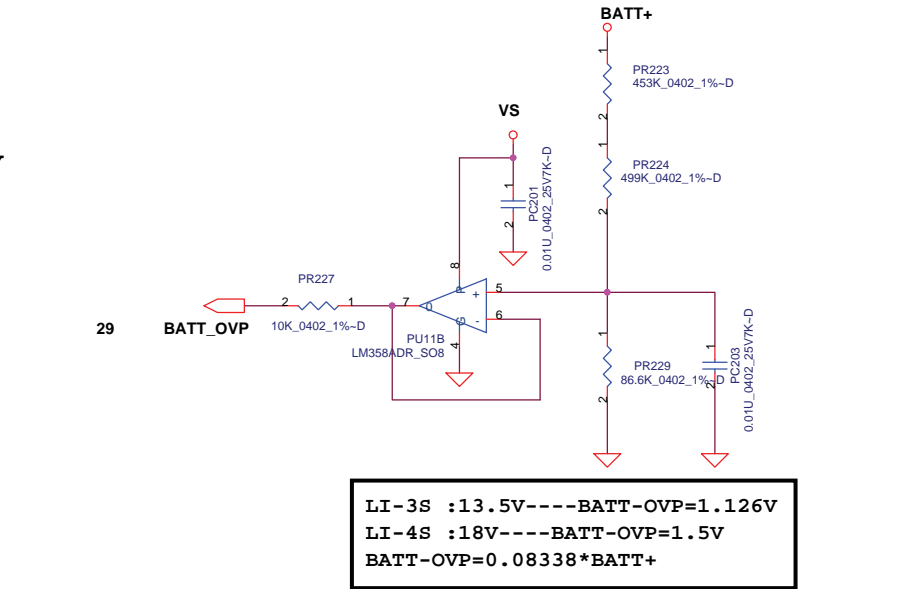
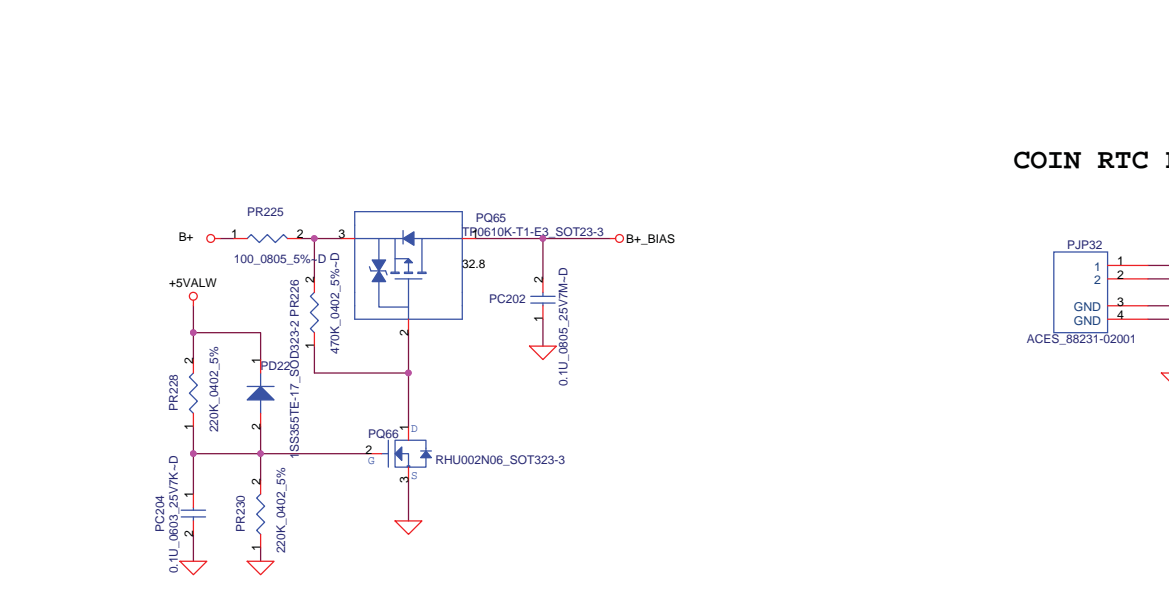
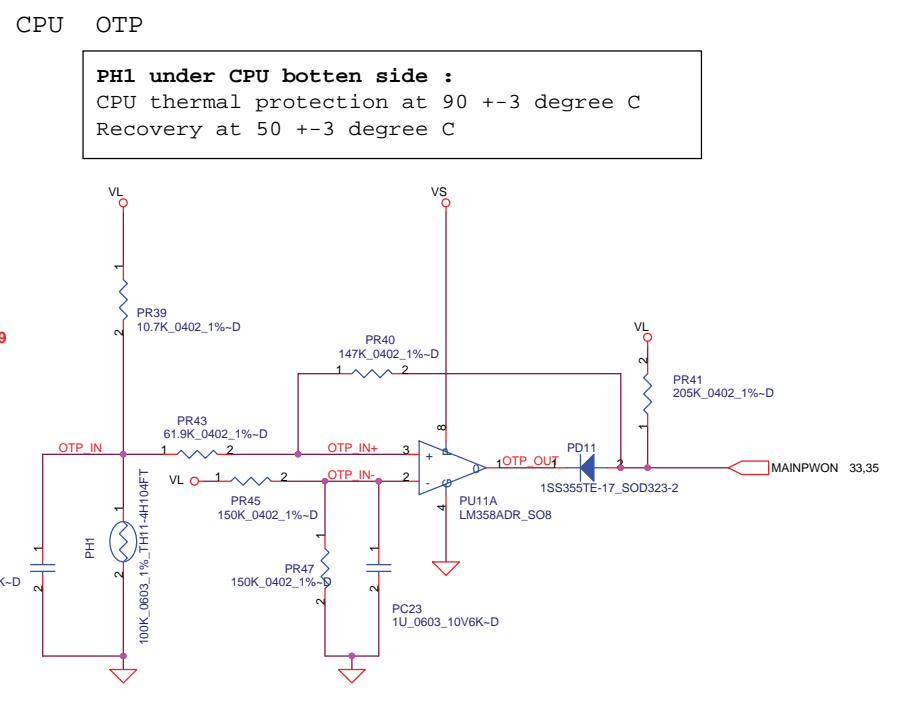
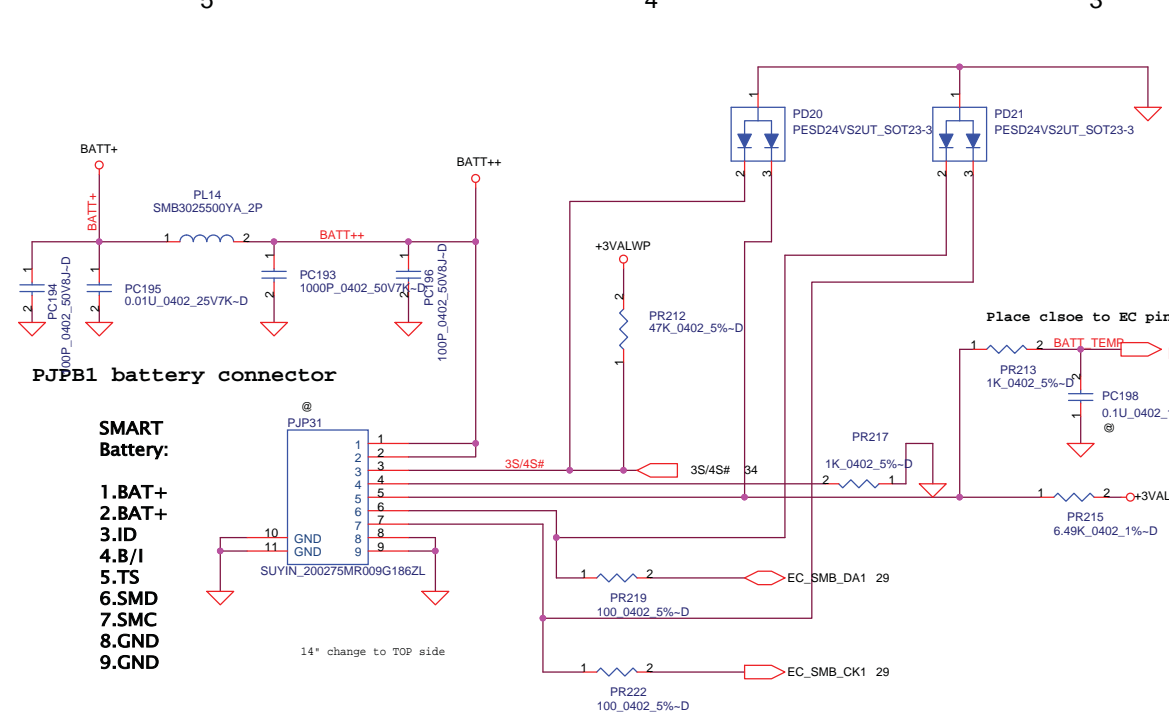


**+3VALW to +3VS**



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**DC/DC Interface**  
**LA-554IP**



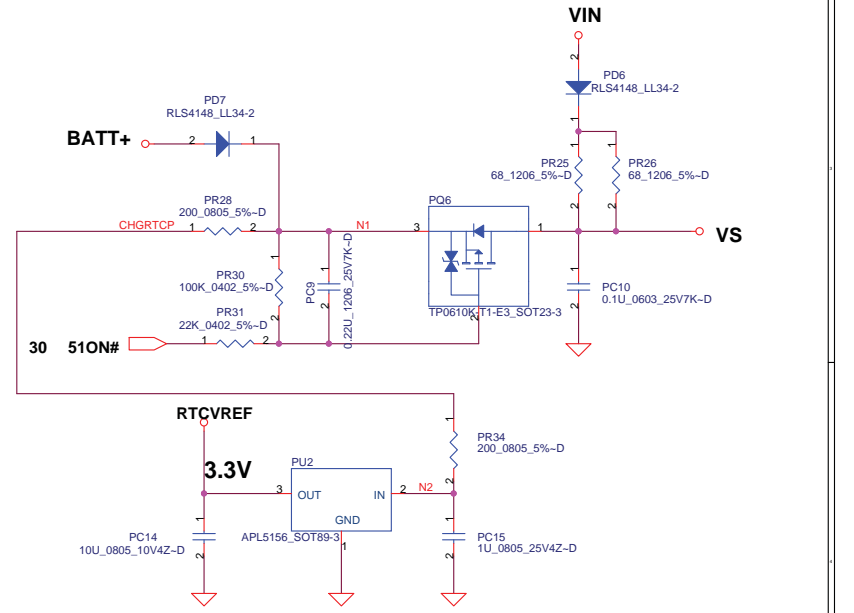
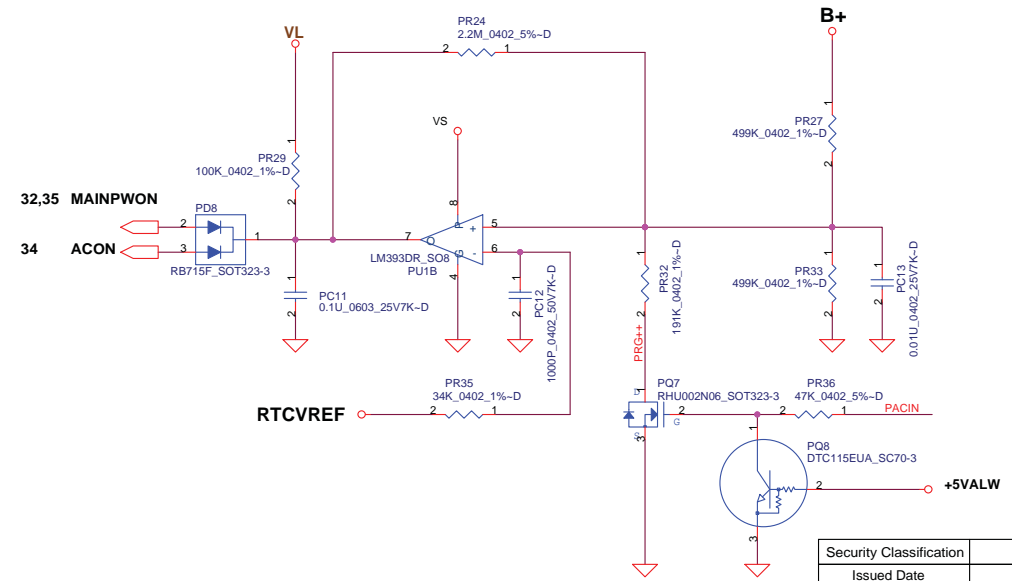
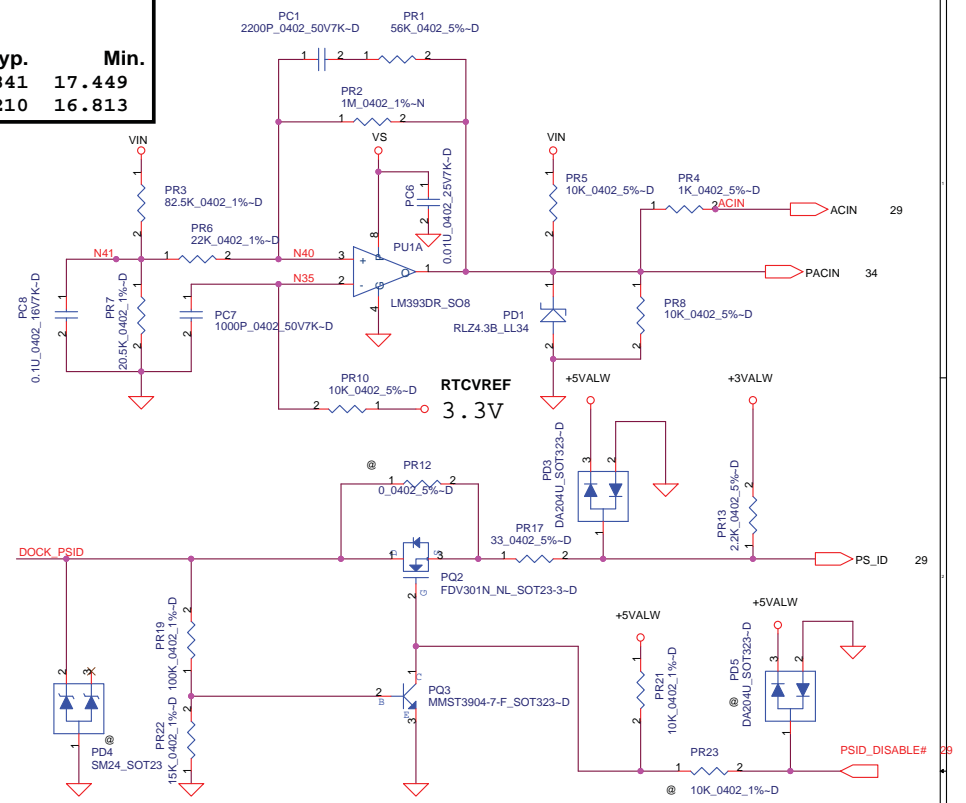
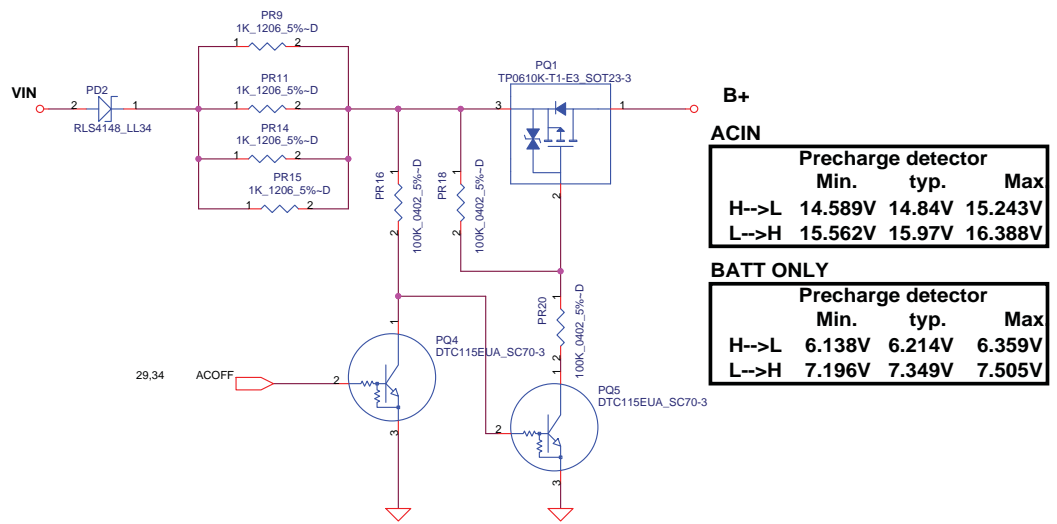
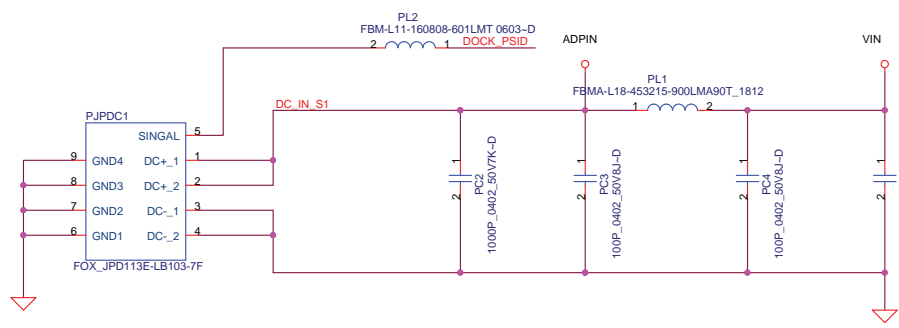
LI-3S :13.5V----BATT-OVP=1.126V  
 LI-4S :18V----BATT-OVP=1.5V  
 BATT-OVP=0.08338\*BATT+

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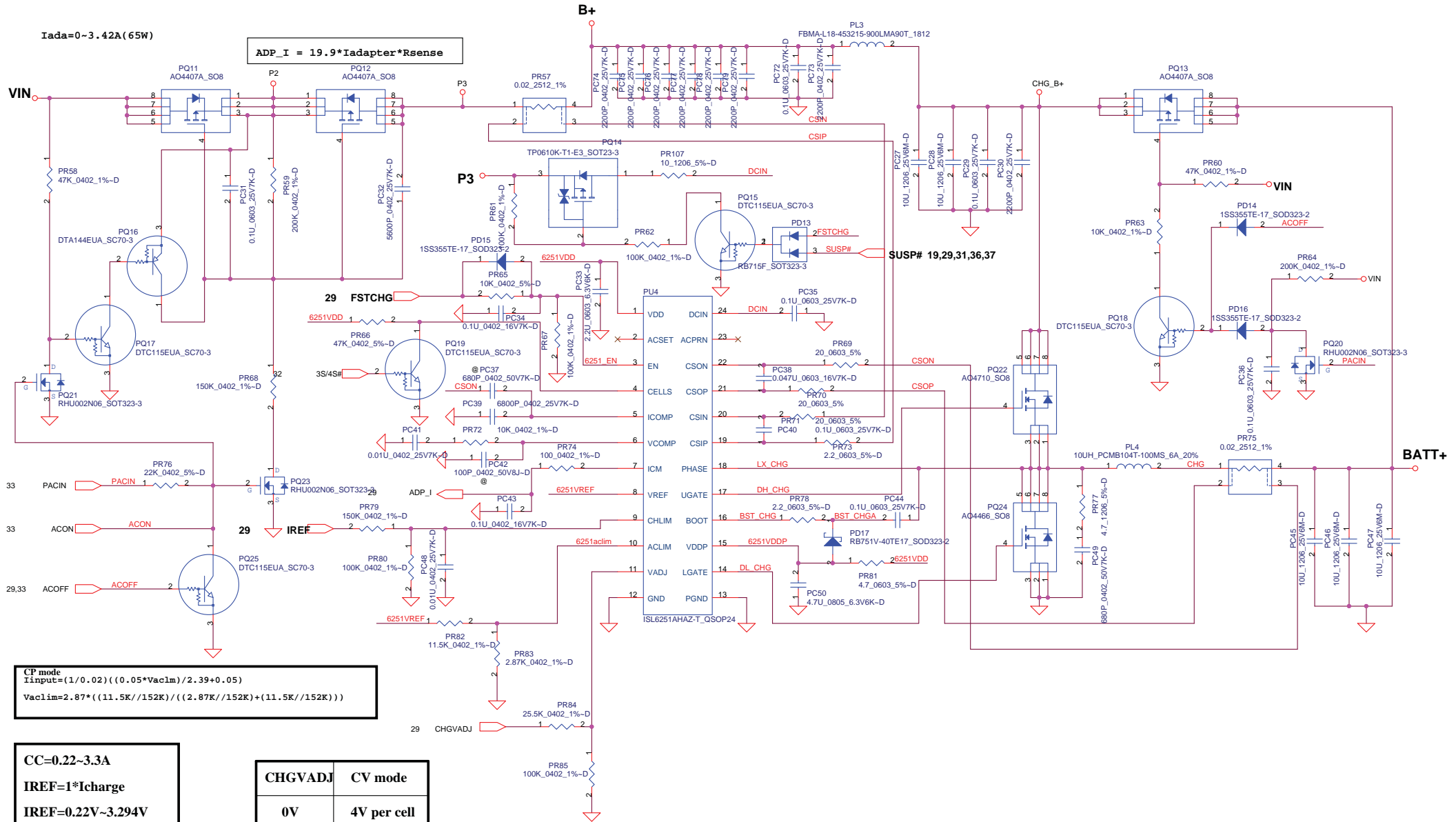


**Vin Detector**

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



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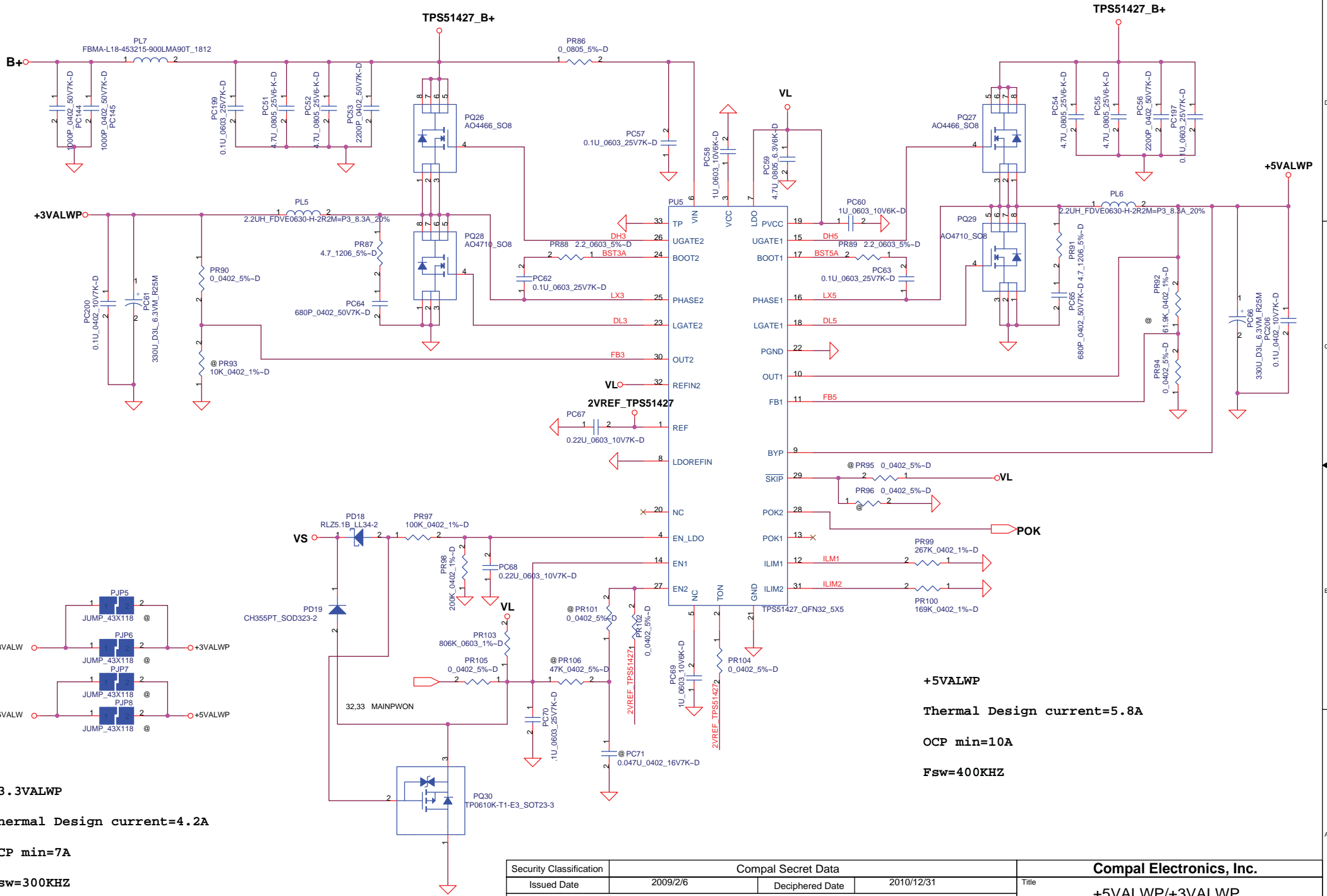
Iada=0~3.42A (65W)

$ADP\_I = 19.9 * I_{adapter} * R_{sense}$

CP mode  
 $I_{input} = (1/0.02) * ((0.05 * V_{ac1m}) / 2.39 + 0.05)$   
 $V_{ac1m} = 2.87 * ((11.5K // 152K) / ((2.87K // 152K) + (11.5K // 152K)))$

CC=0.22~3.3A  
 IREF=1\*Icharge  
 IREF=0.22V~3.294V

CHGVADJ	CV mode
0V	4V per cell
1.882V	4.2V per cell
3.294V	4.45V per cell



**+3.3VALWP**  
 Thermal Design current=4.2A  
 OCP min=7A  
 Fsw=300KHZ

**+5VALWP**  
 Thermal Design current=5.8A  
 OCP min=10A  
 Fsw=400KHZ

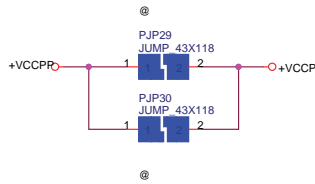
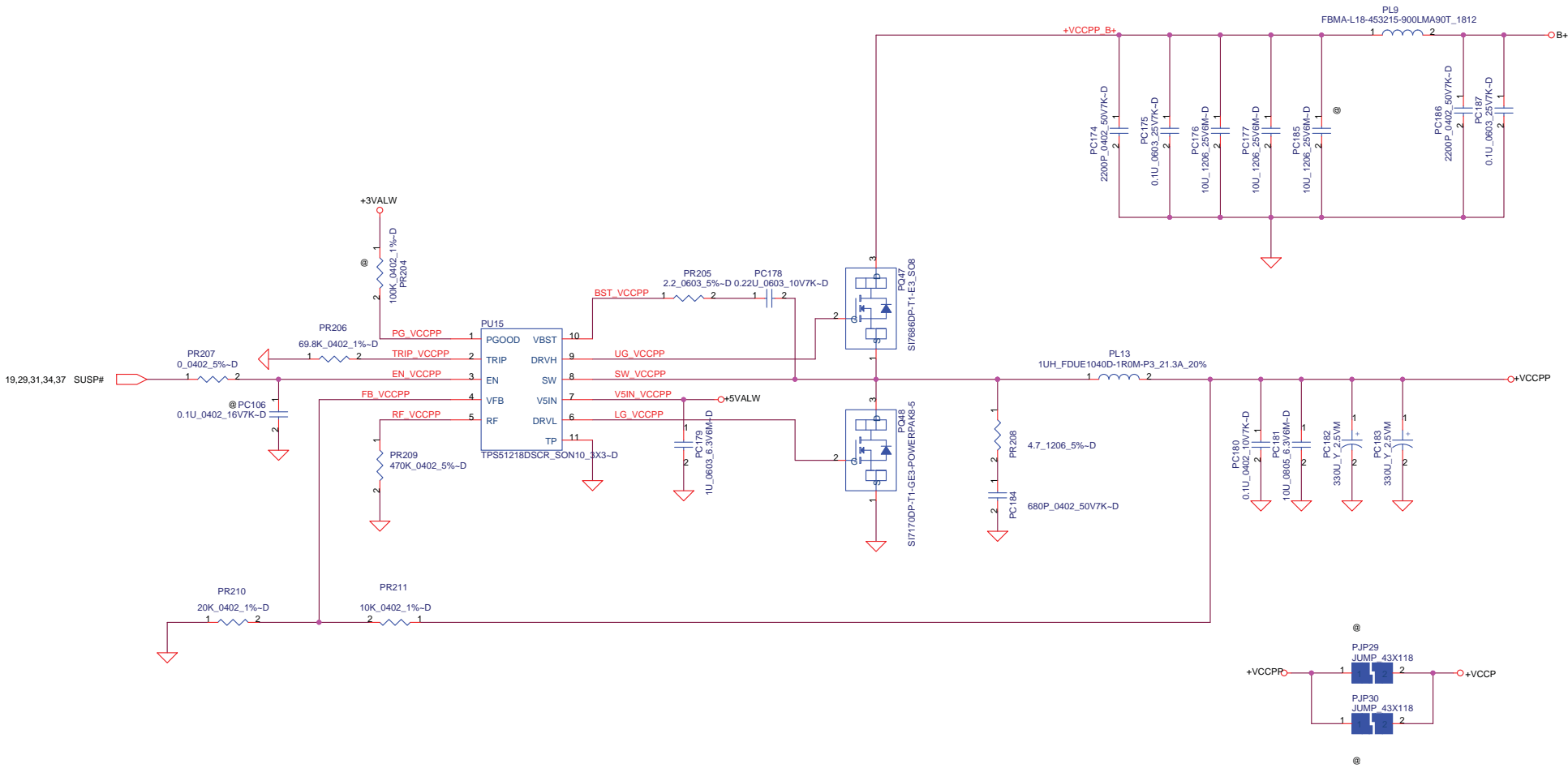
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+VCCPP

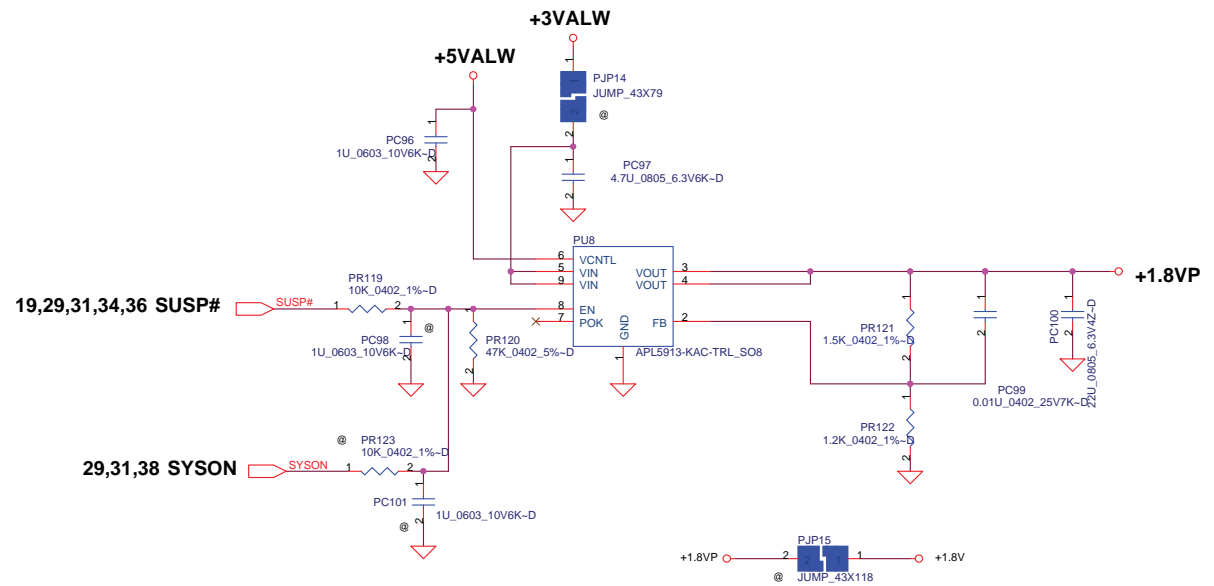
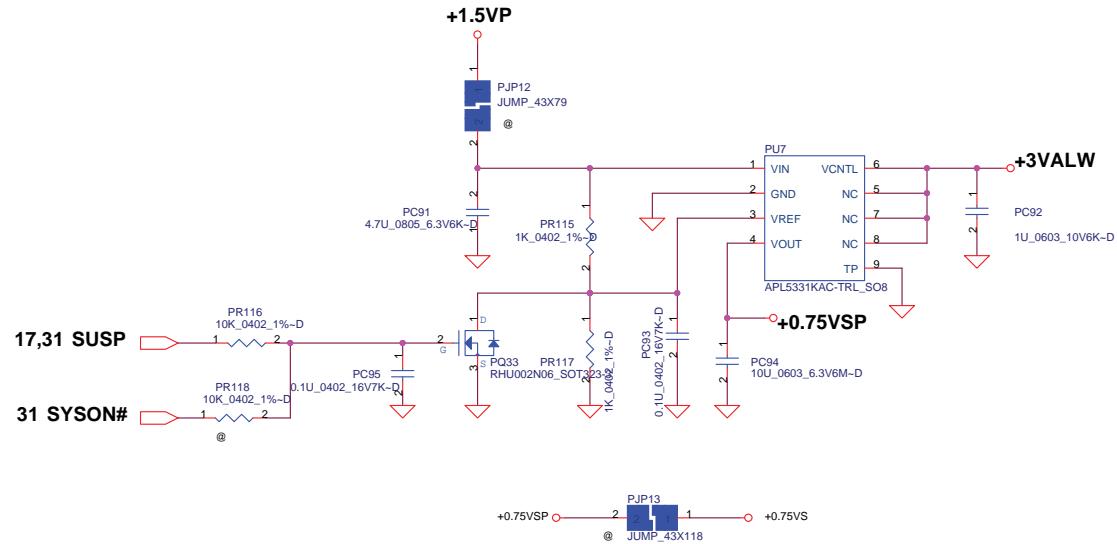
Thermal Design current=11.5A

OCP min=19.5A

Fsw=290KHZ



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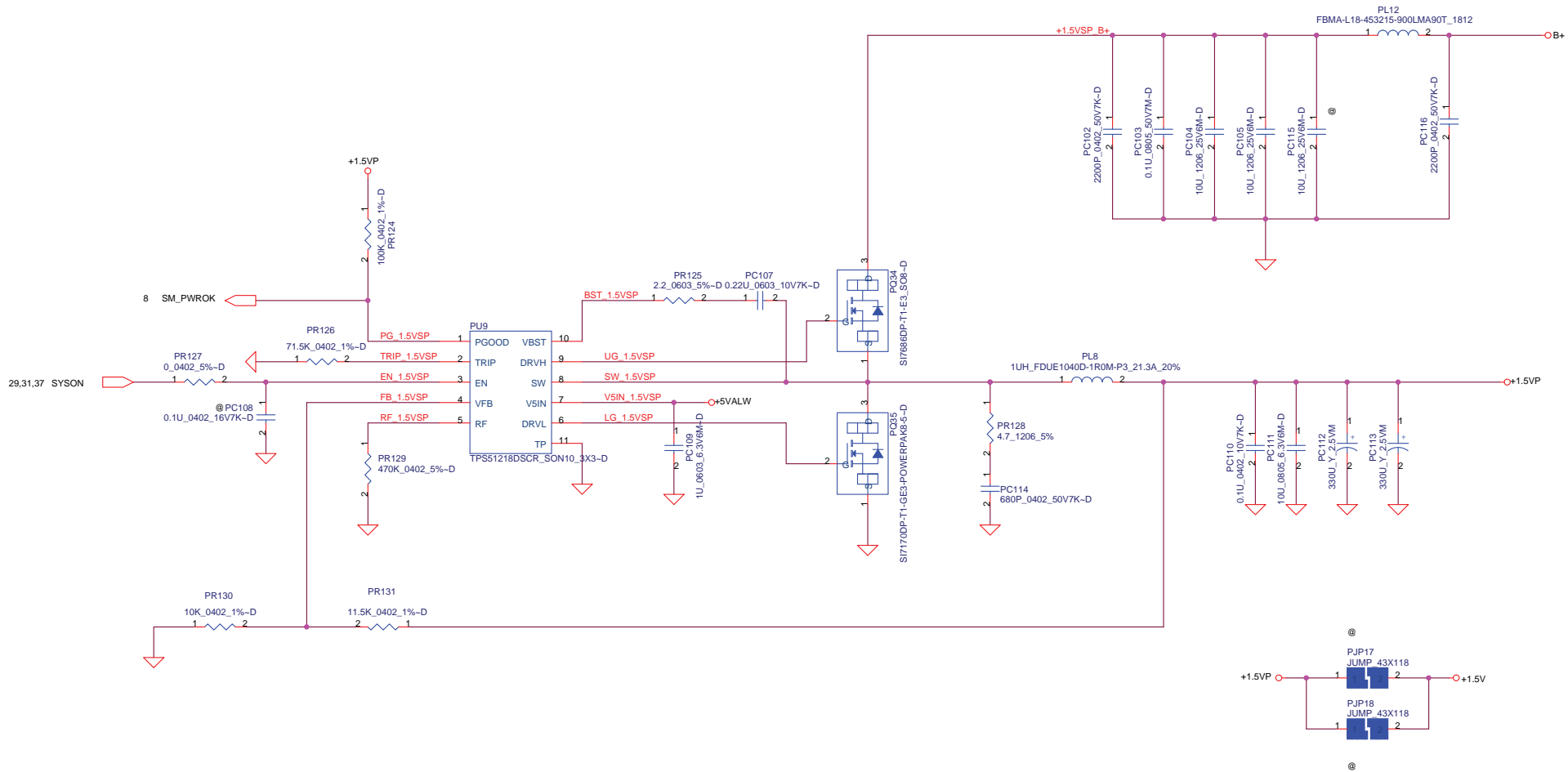
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				+1.8VP / +0.75VP
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+1.5VSP

Thermal Design current=11.5A

OCP min=20A

Fsw=300KHZ



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	CPU_CORE	09' 09/09	Compal_Will	Modify CPU load line	PR170 change 6.65K_1%_0402 to 9.1K_1%_0402	0.5

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Title	
<b>PWR-PIR</b>	
Revision Number	
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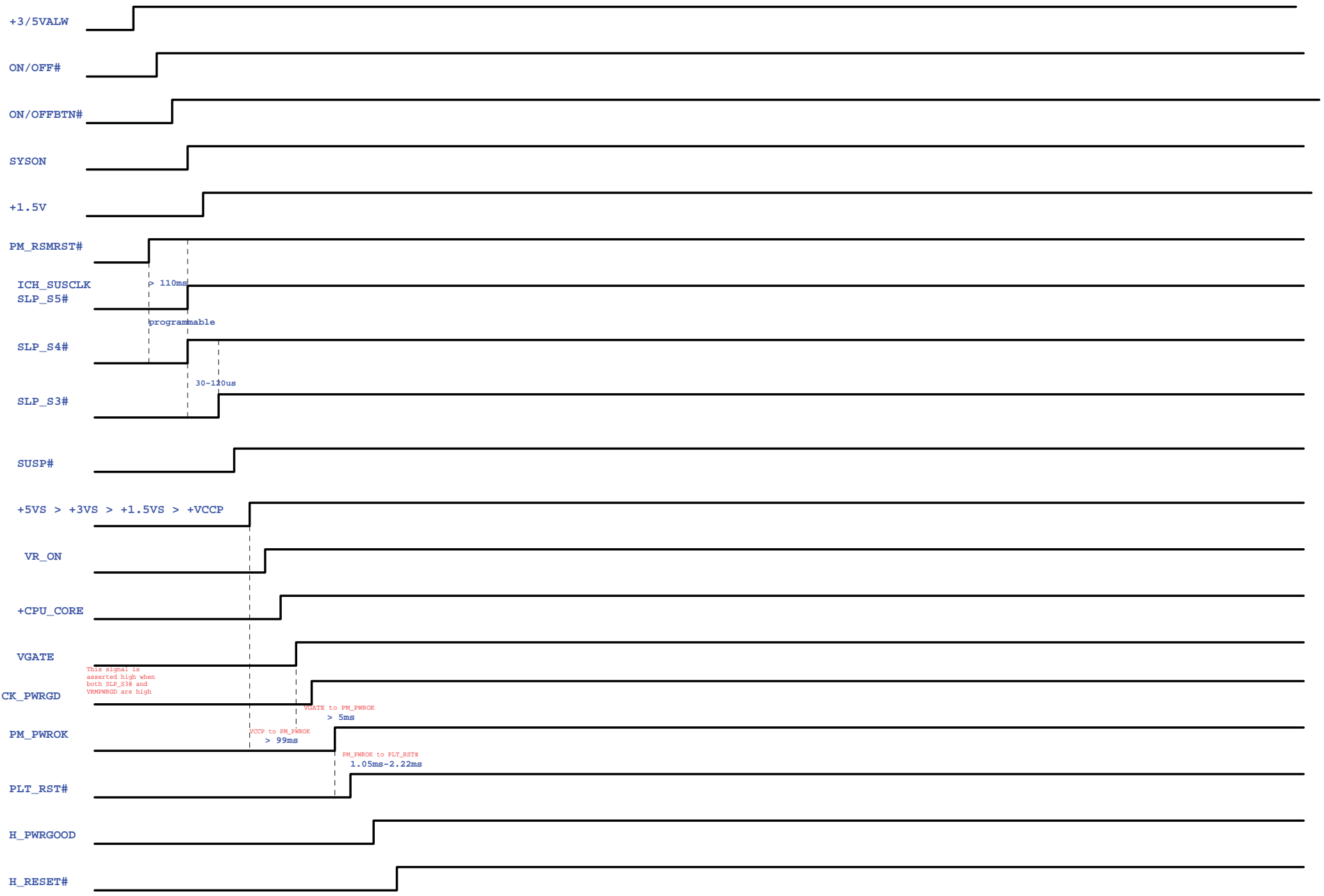


Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21, 23		2009/06/05	Compal	HDMI NO SOUND	ADD R319, R320, R323, R321 DEL R322, R324, R92	0.2
2	29, 30		2009/06/05	Compal	Battery LED can't work	ADD NET BAT_CHG_LED#	0.2
3	19		2009/06/05	Compal		Change JLVDS connect	0.2
4	24		2009/06/05	Compal		Change JODD1 connect	0.2
5	17		2009/06/05	Compal		Change Level shift IC to ASMEDIA	0.2
6	16		2009/06/18	Compal		reserve R1535 to using LOW POWER CLK GEN RTM890-397	0.3
7	26		2009/06/24	Compal		DEL Y5 C1244, C1246	0.3
8	19		2009/07/08	Compal		reserve Q39,Q40,R1536, R1537, C1359, C1360, C1361, C1362	0.3
9	30		2009/07/08	Compal		Del C313 D14	0.3
10	29,30		2009/07/08	Compal		Add EAPD trace	0.3
11	25		2009/07/23	Compal		Add C1363	1.0
12	30		2009/07/23	Compal		Change Keyboard footprint	1.0
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