


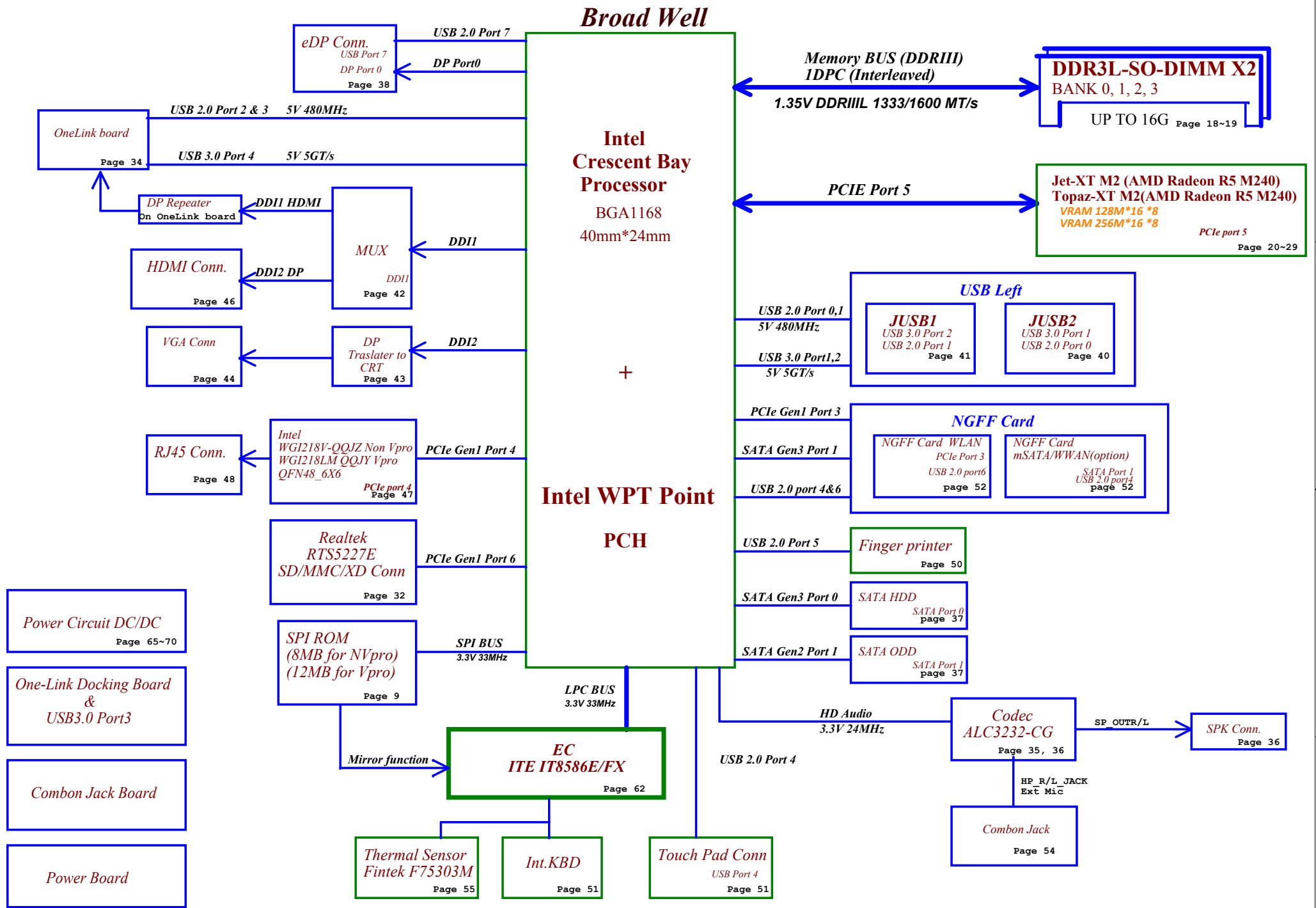
LCFC Confidential

NM-A221 Rev1.0 Schematic

*Intel Crescent Bay Processor with DDRIII + Wild Cat Point PCH
AMD Opal-XT/ Jet-XT*

2013-09-07 Rev1.0

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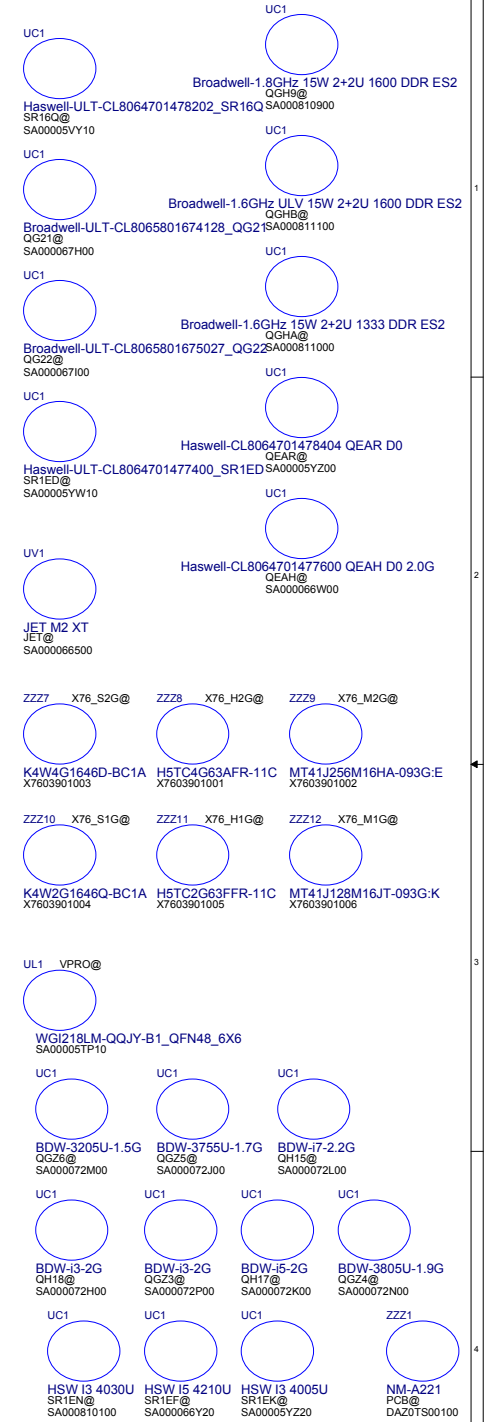
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	B+	+3VALW	+1.5V	+5VS													
				+3VS													
State	B+	+3VALW	+1.5V	+1.5VS													
				+VCCSA													
S0	O	O	O	+V1.5S_VCCP													
				+CPU_CORE													
				+VGA_CORE													
				+GFX_CORE													
				+1.8VS													
				+1.05VS													
				+0.75VS													
				+3.3VS_VGA													
				+1.5VS_VGA													
				+1.05VS_VGA													
				S3	O	O	O	X									
								S5 S4/AC Only	O	O	X	X					
S5 S4 Battery only	O	X	X									X					
													S5 S4 AC & Battery don't exist	X	X	X	X

High Speed I/O port

I/O	High Speed Signal	Configuration	Port assignment
1	USB3 1	USB3 1	On MB USB
2	USB3 2	USB3 2	On MB USB
3	PCIE 1 / USB3 3	NC	NC
4	PCIE 2 / USB3 4	USB3 4	Docking USB
5	PCIE 3	PCIE 3	WLAN
6	PCIE 4	PCIE 4	LAN
7	PCIE 5 L0	PCIE 5 L0	GPU
8	PCIE 5 L1	PCIE 5 L1	GPU
9	PCIE 5 L2	PCIE 5 L2	GPU
10	PCIE 5 L3	PCIE 5 L3	GPU
11	PCIE 6 L0 / SATA 3	PCIE 6	Cardreader
12	PCIE 6 L1 / SATA 2	SATA 2	mSATA
13	PCIE 6 L2 / SATA 1	SATA 1	ODD
14	PCIE 6 L3 / SATA 0	SATA 0	HDD



BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function (Option with TS@)
TPM@	Trusted Platform Module (TPM)
NM14@	14" SKU ID
NM15@	15" SKU ID
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
X76@	GPU VRAM Setting
M2G@	Micron 256Mx16 VRAM
M1G@	Micron 128Mx16 VRAM
S2G@	Samsung 256Mx16 VRAM
S1G@	Samsung 128Mx16 VRAM
ME@	ME Connector
TS@	Touch screen function
DEBUG@	For debug
BYPASS@	For bypass
MIRROR@	For mirror function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
X76_S2G@	For Samsung 2G VRAM

SMBUS Control Table

	SOURCE	Main VGA	LAN	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	CP Module	Charger
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	V +3V_PCH	X	X	X	X	X	X	X	X
PCH_SML1CLK PCH_SML1DATA	PCH +3V_PCH	V +3VS	X	X	V +3VS	X	X	V +3VS	X	X	X
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	X	V +3VL	X	X	X	X	X	X	V +3VL
PCH_SMBCLK PCH_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	X	X	V +3V_PCH	V +3VS	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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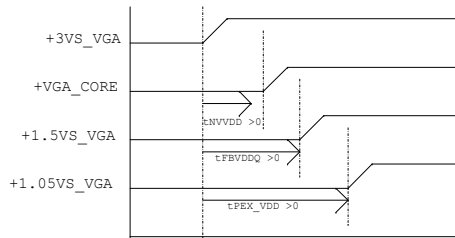
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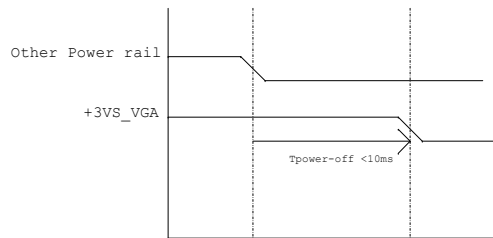
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VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Device ID	setting	I2C Slave address ID
N13P-GT (28nm)	0x0FDB	
	SMB_ALT_ADDR (ROM_SO Bit 1)	0 0x9E
		1 0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU	N13P-GT		
FB Memory (GDDR5)	ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04		
	32Mx32	PD 45K	
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	
Samsung 2500MHz	K4G20325FD-FC04		
	64Mx32	PD 30K	
Hynix 2500MHz	H5GQ2H24MFR-T2C		
	64Mx32	PD 25K	

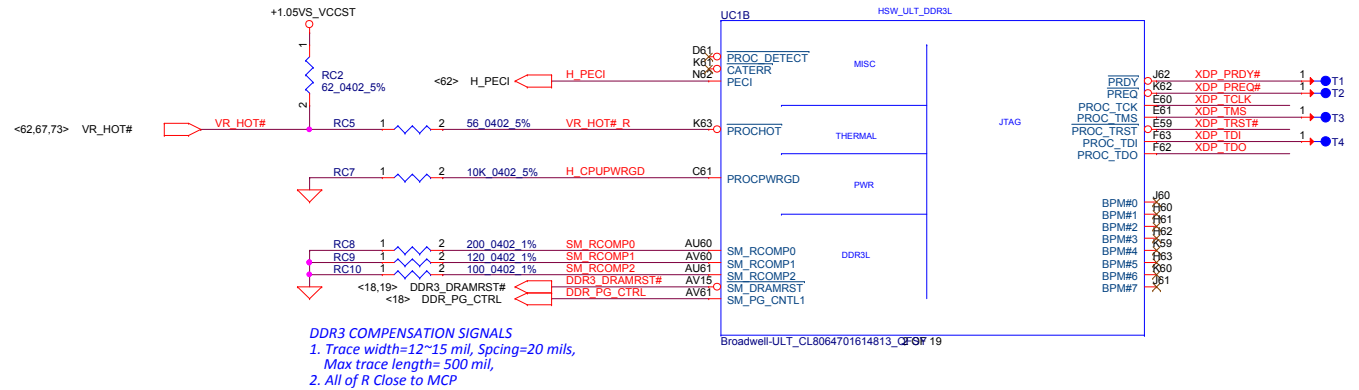
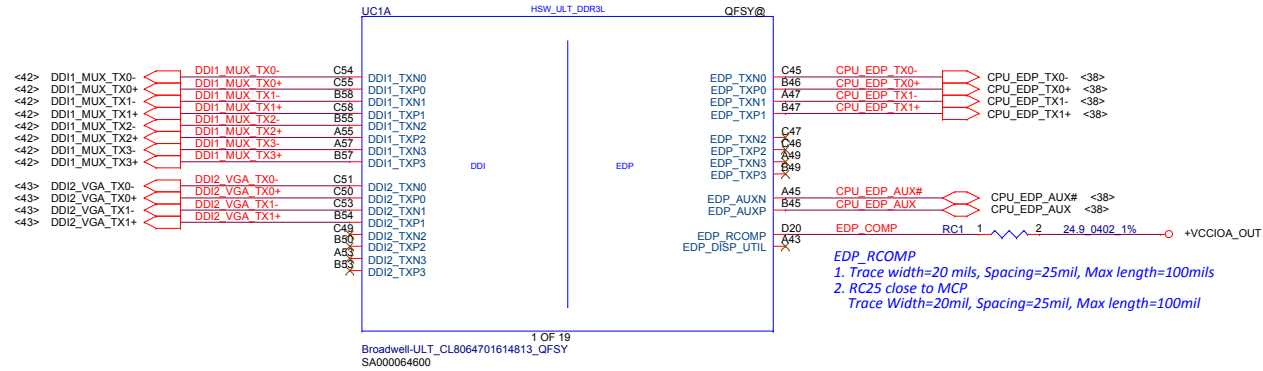
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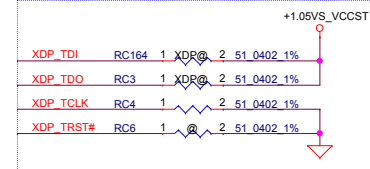


For 14" : DOCKING
For 15" : HDMI & DOCKING

For 14" : HDMI
For 15" : VGA

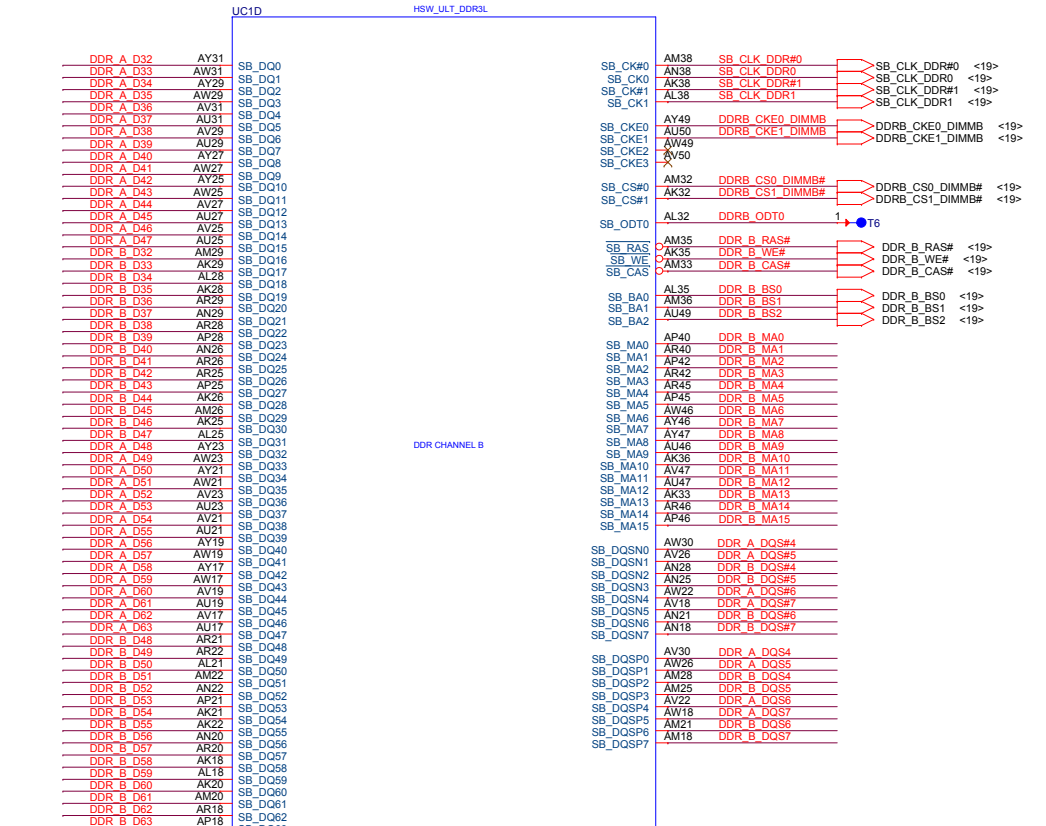
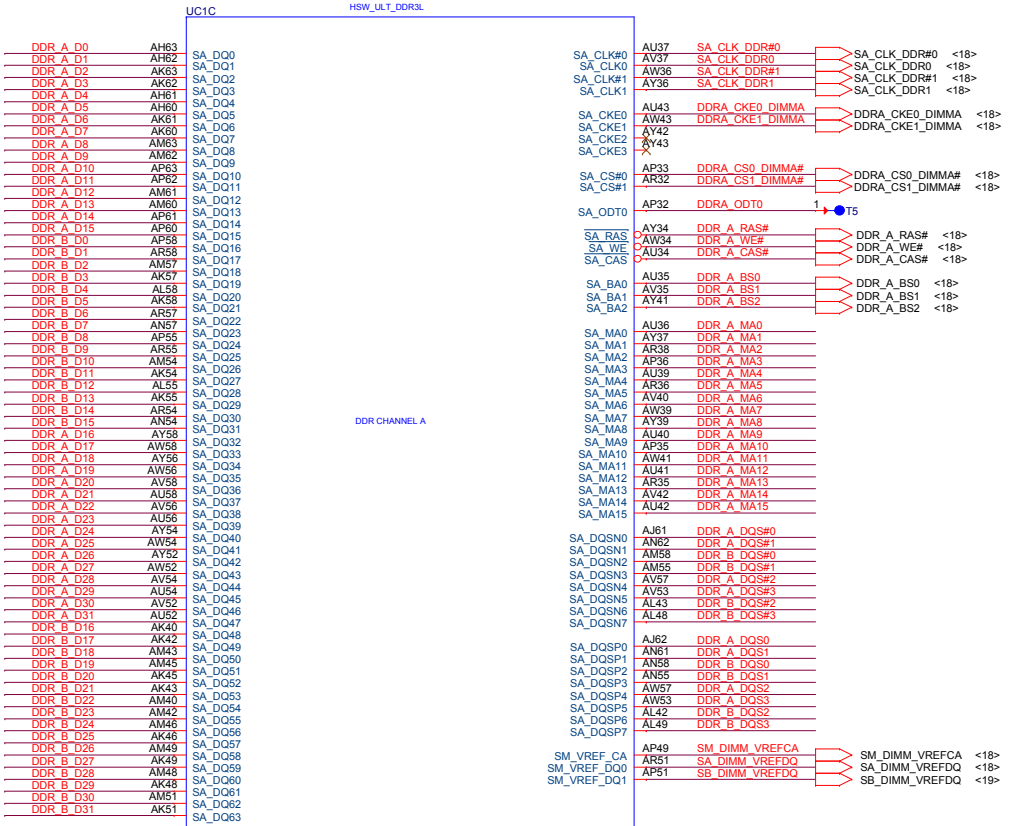
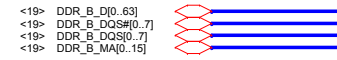
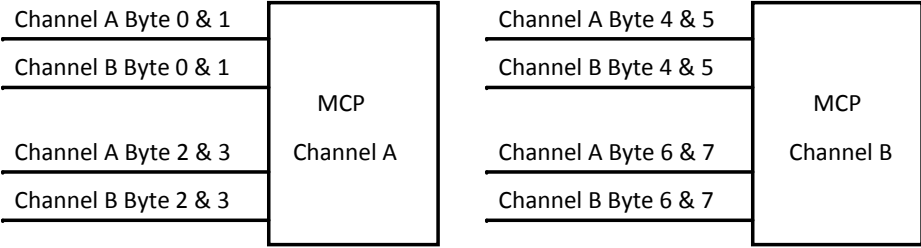


PU/PD Res. For CPU-XDP SIGNAL, Place R Closer to CPU



XDP PU/PD portion need to check again.

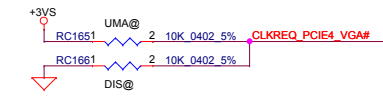
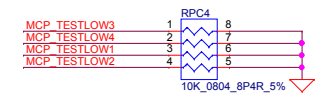
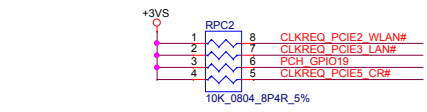
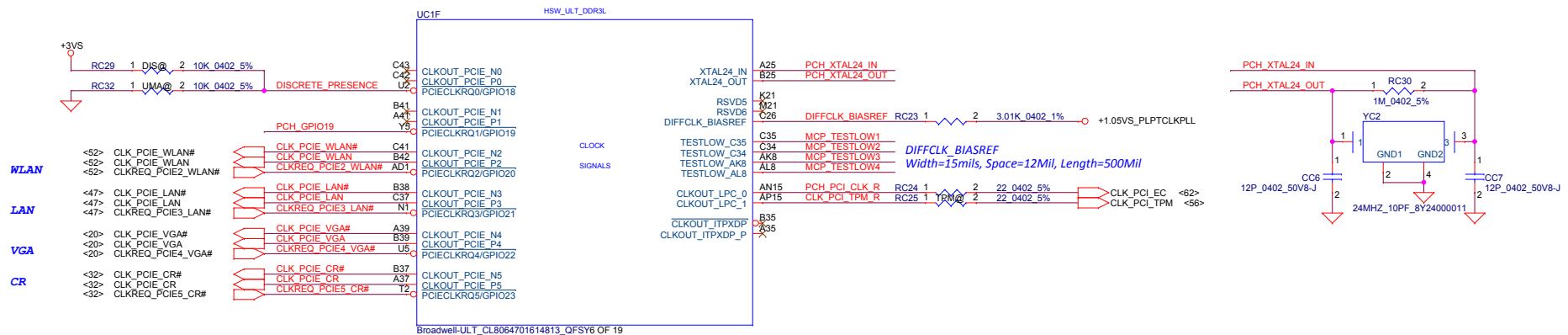
Interleaved (Butterfly Topology) Broadwell Platform System Memory Interface Document Number: 528378 BDW U DDR3L/DDR3L-RS SO-DIMM Interleaved Recommendations



Broadwell-ULT_CL8064701614813_QF0F 19

Broadwell-ULT_CL8064701614813_QF0F 19

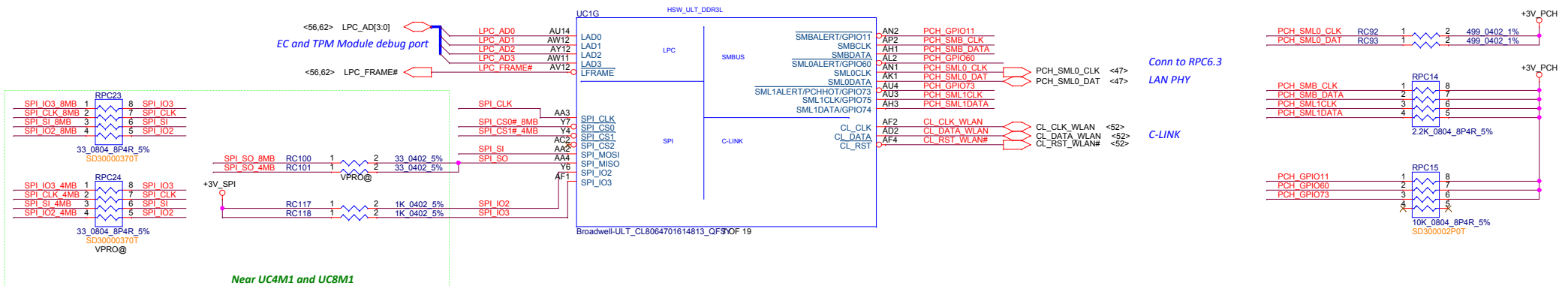
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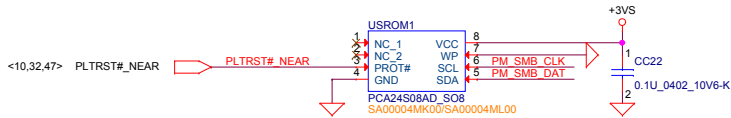
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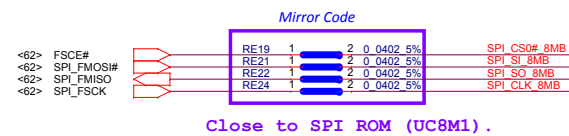
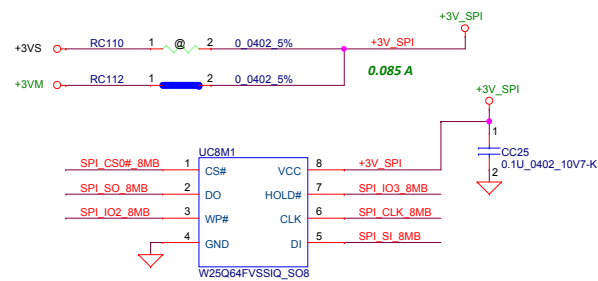
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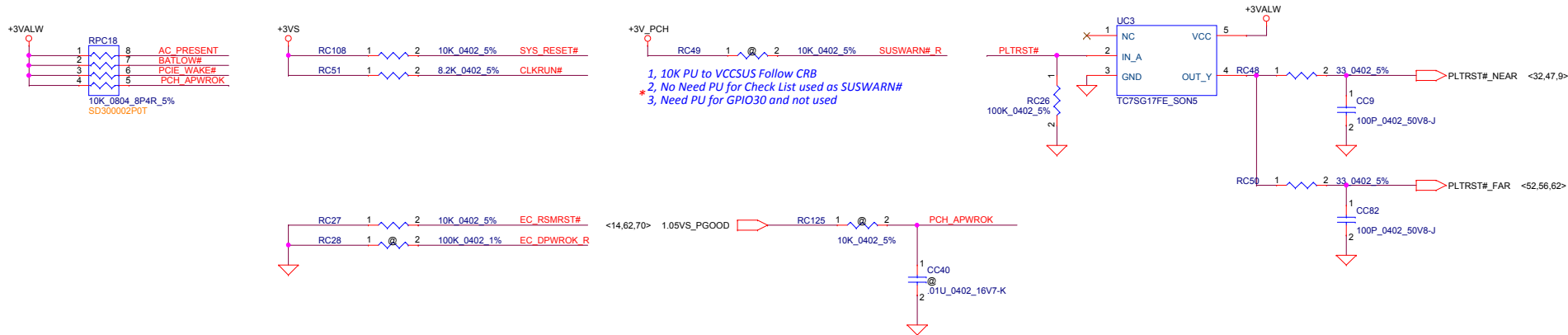
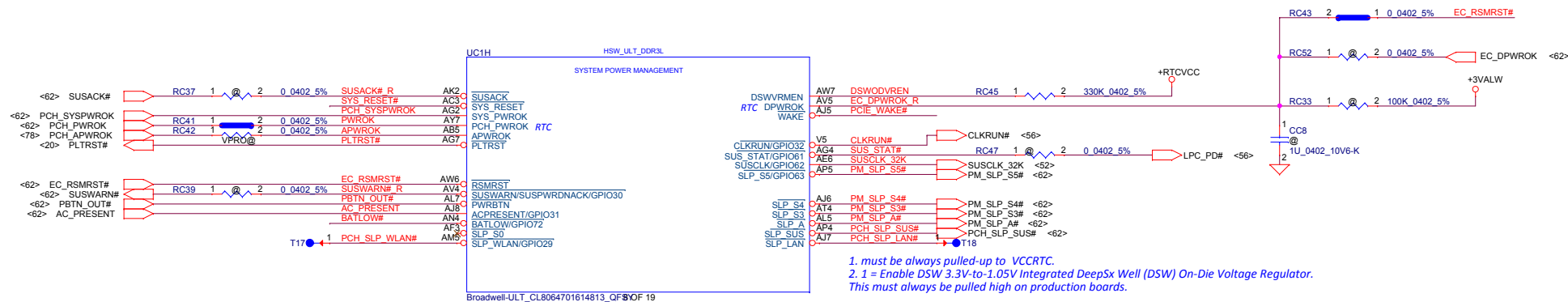
Security ROM



M3 Support + Intel LAN PHY / Wireless LAN Solution



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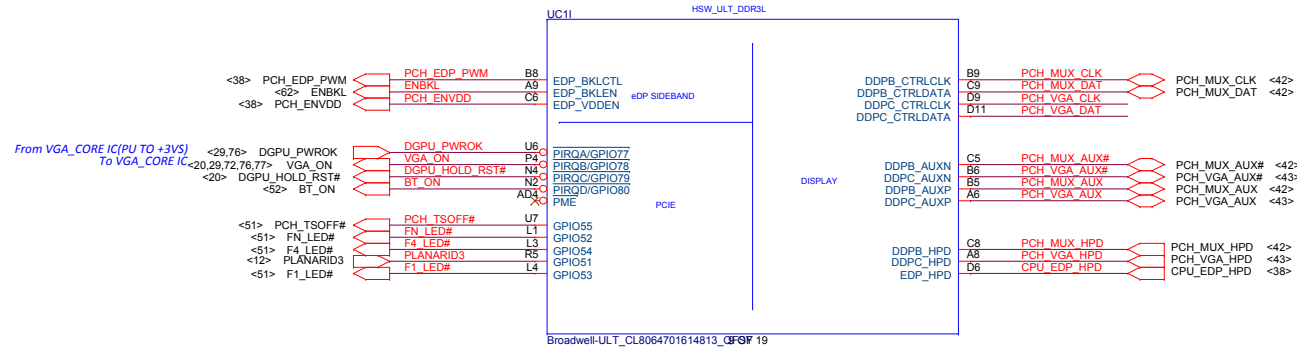


SUSWARN#_R 1 RC109 2 SUSACK#_R 0_0402_5% SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

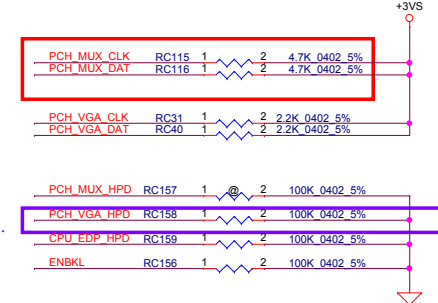
APWROK 1 RC111 2 PWROK 0_0402_5% For platforms not supporting IntelR AMT it can be connected to PWROK.

This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state.
 RSMRST# <-> DPWROK

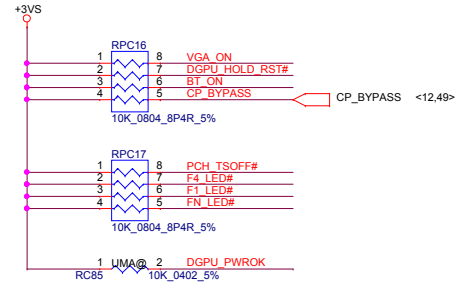
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1. 鐵VENDOR 鐵板PU , 鐵板Vih anf Vil Tmeet SPEC value.
2. Vender fine tune recommend value.(Pass Through Mode)
3. Vendor recommend use PU 4.7K ohm. (10/1) Intel Spec is PU 2.2K ohm



After testing, check if can un-stuff.

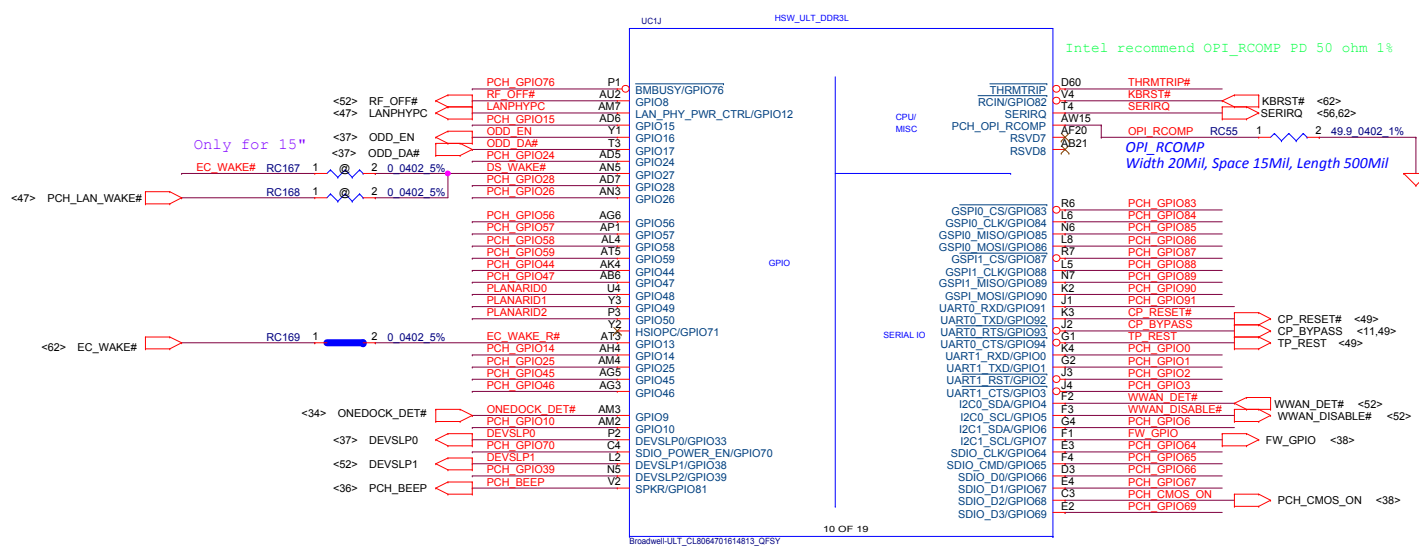


DDPB_CTRLDATA: Port B Detected
 DDPC_CTRLDATA: Port C Detected

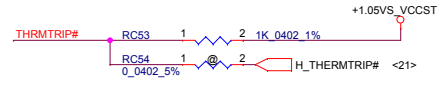
* 1: Port B or C is detected
 0: Port B or C is not detected

Internal PD 15K~40K, nominal 20K

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	SATA Port
DEVSLP0	SATA Port 0
DEVSLP1	SATA Port 1

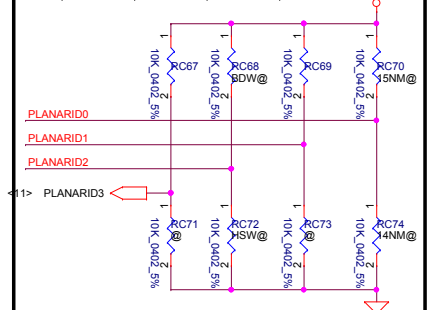


Intel recommend OPI_RCOMP PD 50 ohm 1%

OPI_RCOMP
Width 20Mil, Space 15Mil, Length 500Mil

Only for 15"

Planar ID			
PLANARID0 (GPIO48)	GPIO18	PLANARID2 (GPIO50)	PLANARID3 (GPIO51)
0	14"	UMA	HSW
1	15"	OPT	BDW



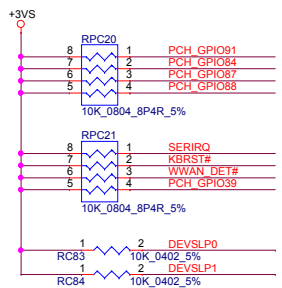
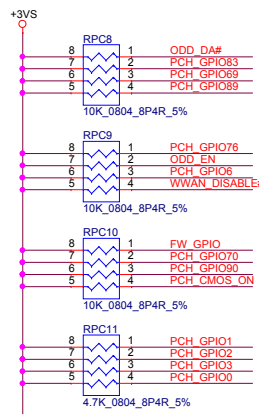
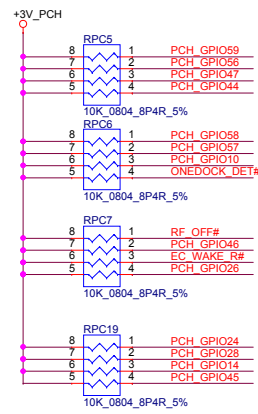
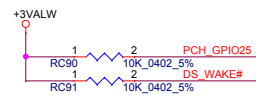
GPIO15, Internal PD
1: INTEL ME TLS W Confidentiality
0: INTEL ME TLS WO Confidentiality

GPIO66, Internal 20K PD
1: Top-Block Swap Override EN
*0: Disable

GPIO81, No Reboot, Internal PD
1: Enabled No Reboot Mode
*0: Disable No Reboot Mode

GPIO86, Internal PD
1: Enabled
*0: SPI ROM

2013/08/29 Set Nactive and Pull Down



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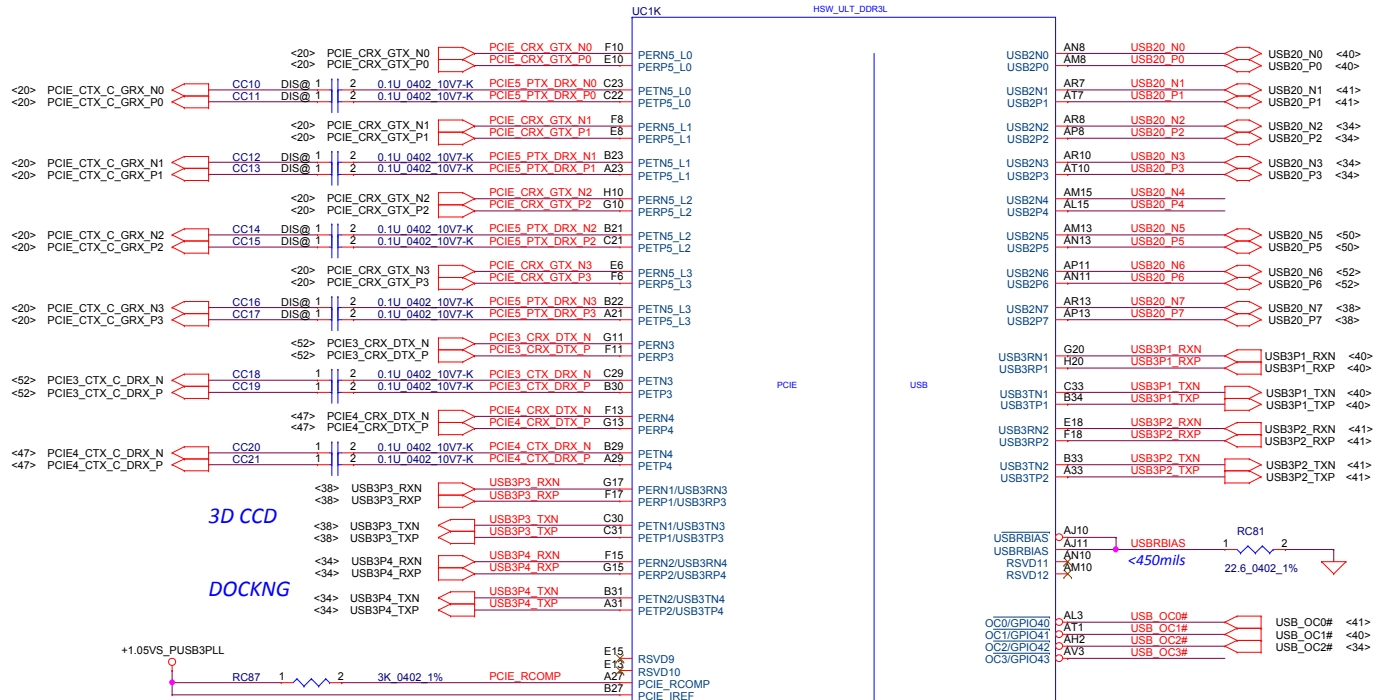
GPU

WLAN

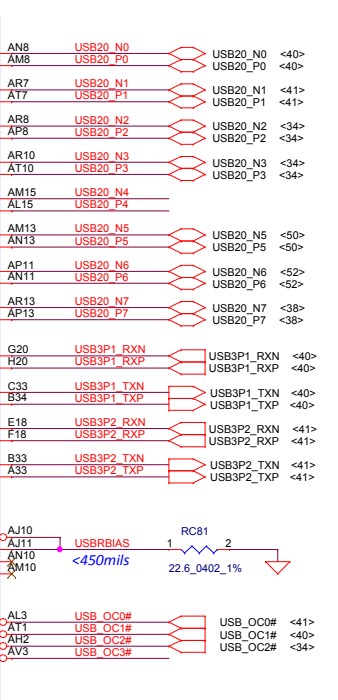
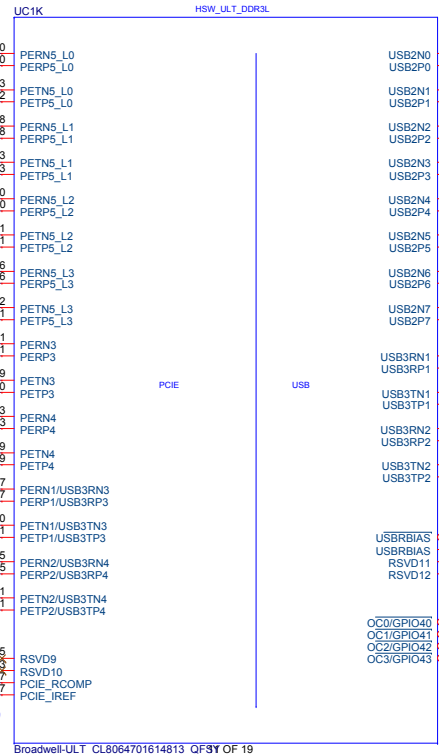
LAN

3D CCD

DOCKNG

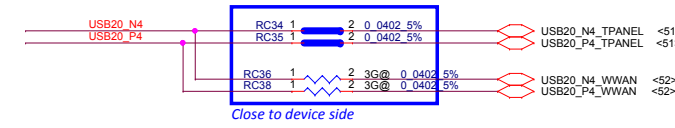
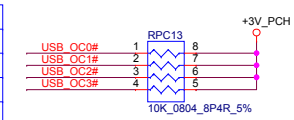


+1.05VS_PUSB3PLL
 RC87 1 2 3K 0402 1%
 PCIE_RCOMP
 PCIE_RCOMP&PCIE_IREF (Shared with DMI)
 Width 20Mil, Space 15Mil, Length 500Mil



On Board (Back)
 On Board /Charge Port (Front)
 Sub/B
 DOCKING
 TOUCH PANEL/WWAN
 FPR
 BT
 CAMERA
 On Board (Back)
 On Board (Front)
 USBRBIAS/USBRBIAS#
 1. trace length and no longer than 450 mils to resistor.
 2. Avoid routing next to clock pins or under stitching capacitors.
 Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

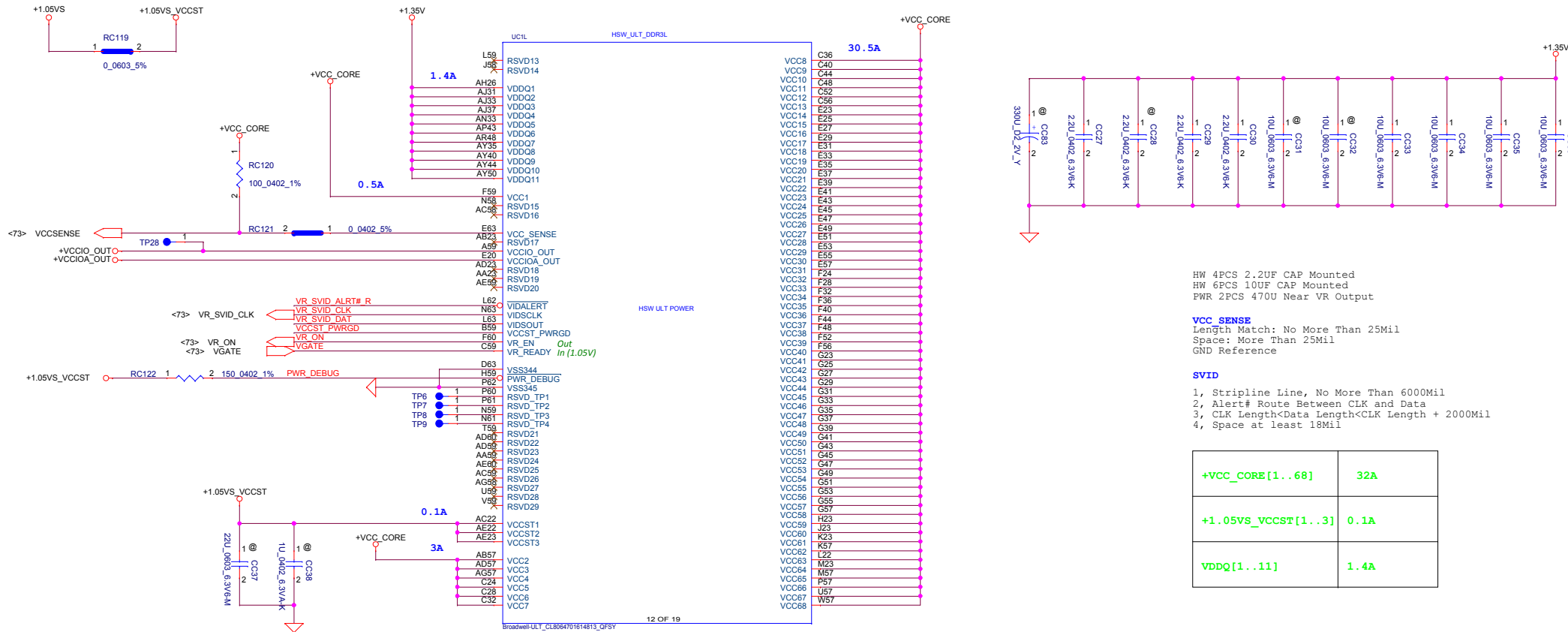
USB_OC#	USB3.0 Port NO.	USB2.0 Port NO.
USB_OC0#	Port 2	Port 1
USB_OC1#	Port 1	Port 0
USB_OC2#	Unused.	Port 2
USB_OC3#	Unused.	Unused.



Close to device side

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Haswell MCP (Power)



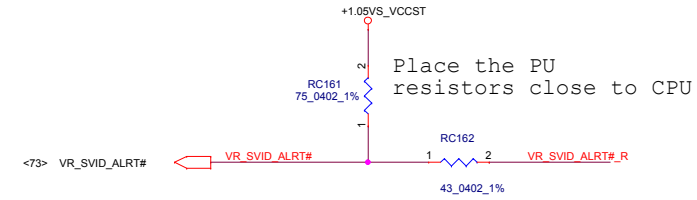
HW 4PCS 2.2UF CAP Mounted
 HW 6PCS 10UF CAP Mounted
 PWR 2PCS 470U Near VR Output

VCC SENSE
 Length Match: No More Than 25Mil
 Space: More Than 25Mil
 GND Reference

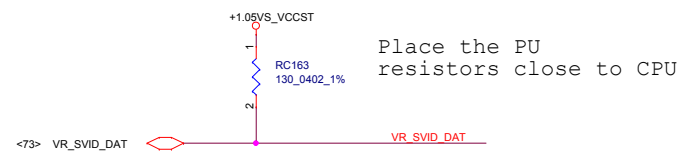
SVID
 1, Stripline Line, No More Than 6000Mil
 2, Alert# Route Between CLK and Data
 3, CLK Length < Data Length < CLK Length + 2000Mil
 4, Space at least 18Mil

+VCC_CORE[1..68]	32A
+1.05VS_VCCST[1..3]	0.1A
VDDQ[1..11]	1.4A

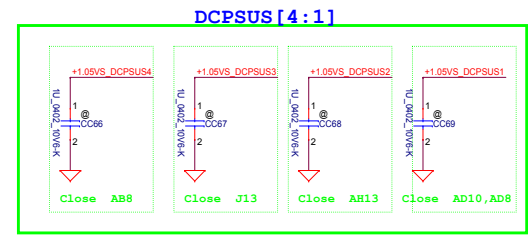
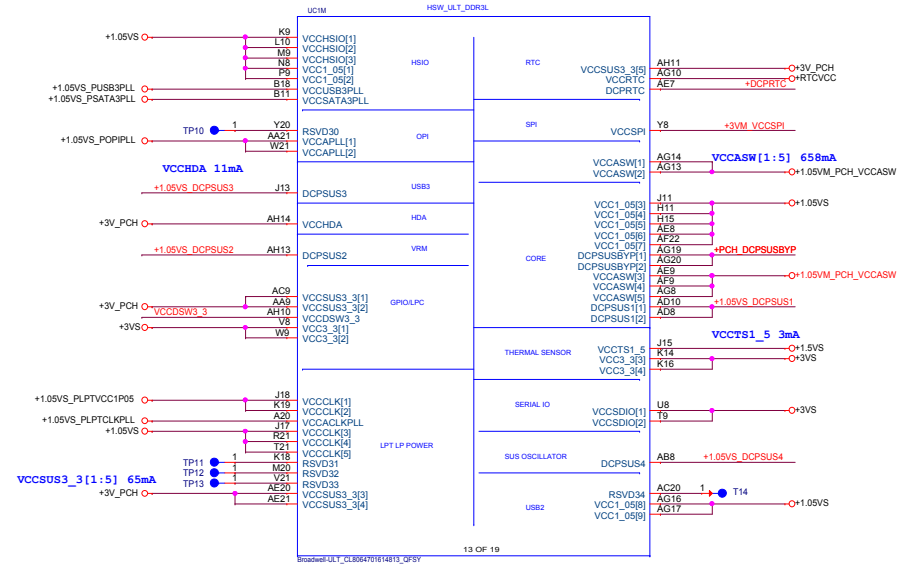
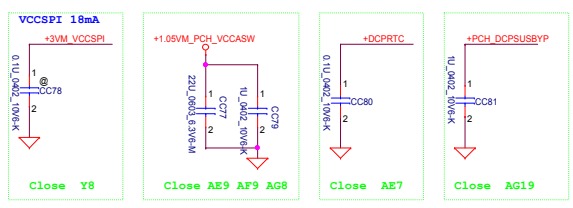
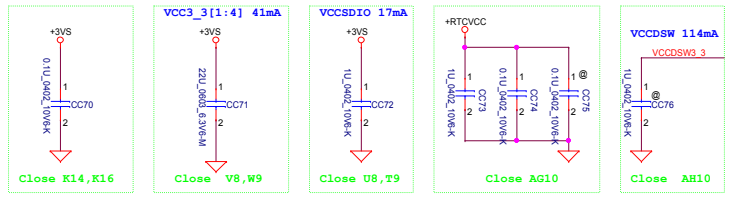
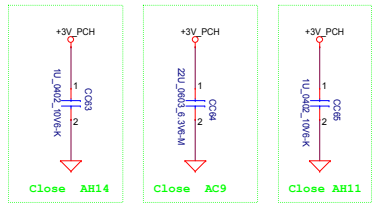
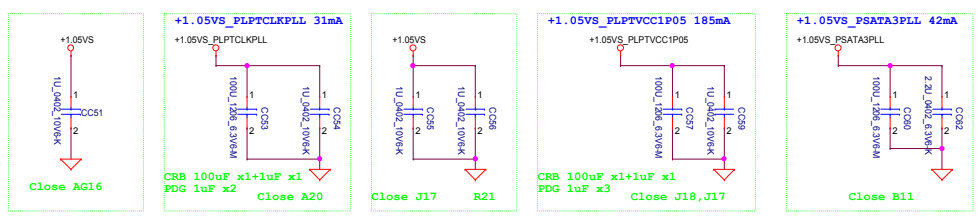
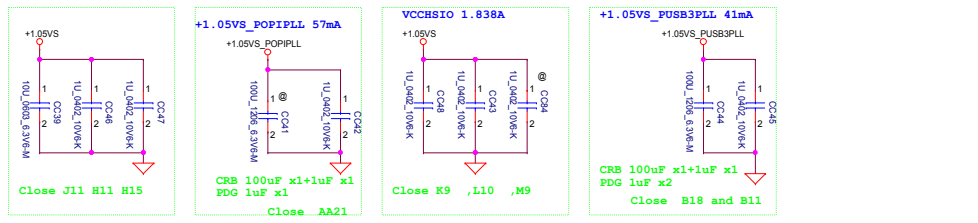
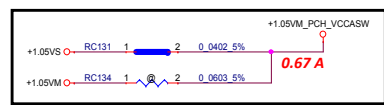
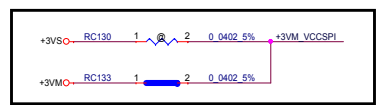
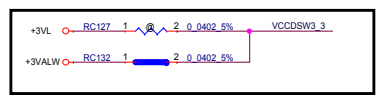
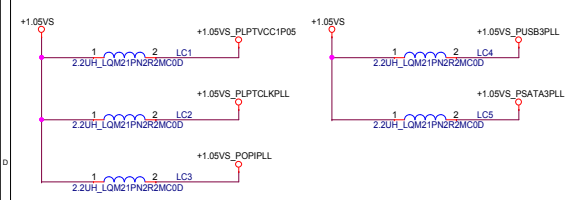
SVID ALERT



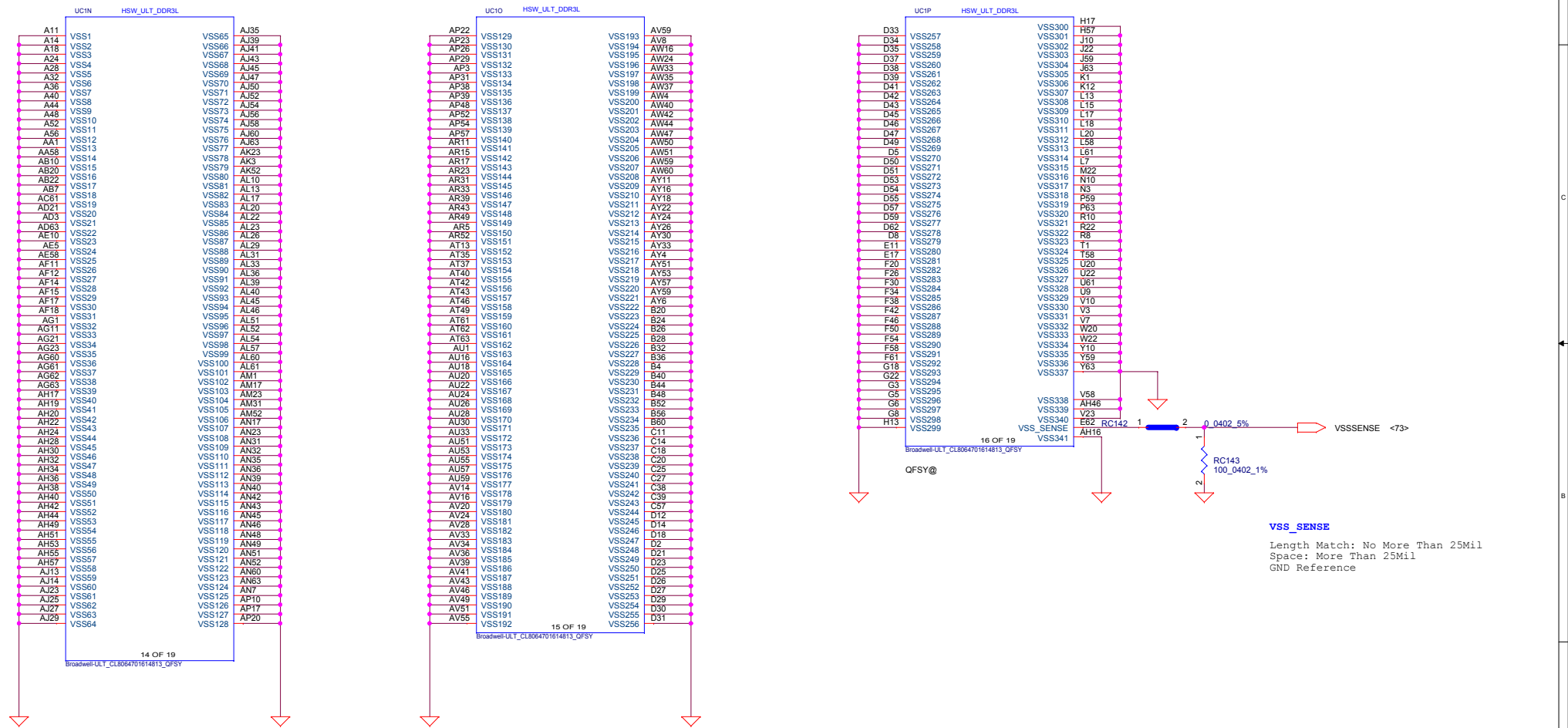
SVID DATA




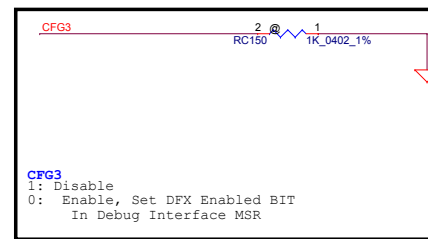
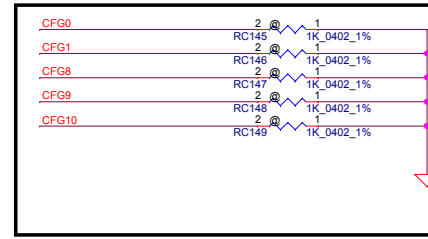
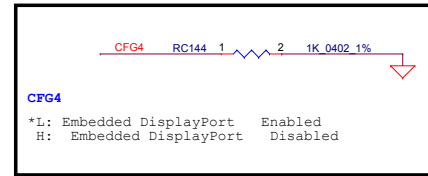
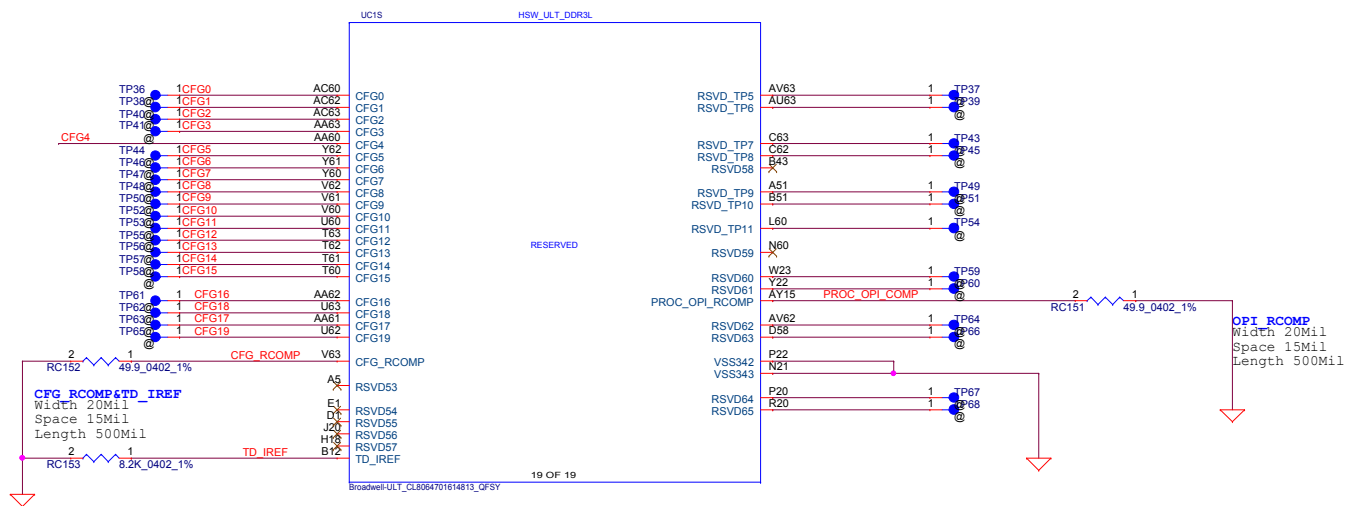
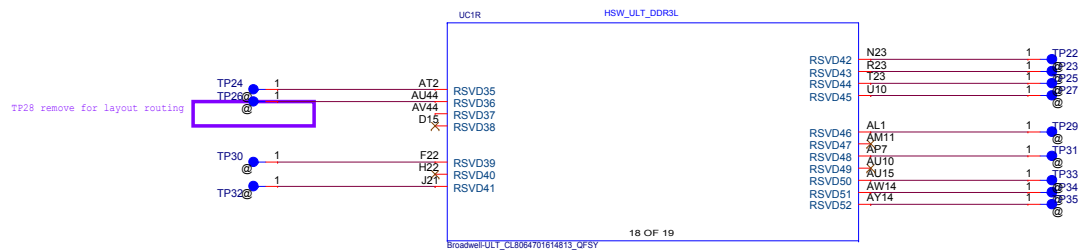
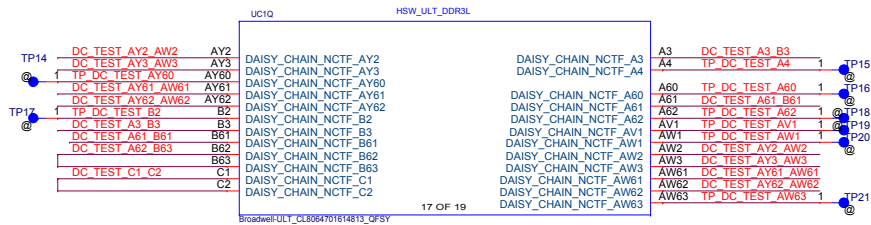
Haswell MCP (Power2)



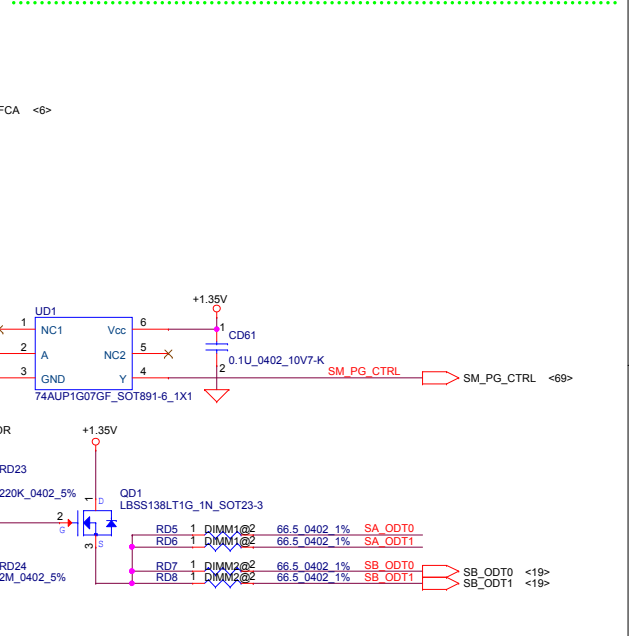
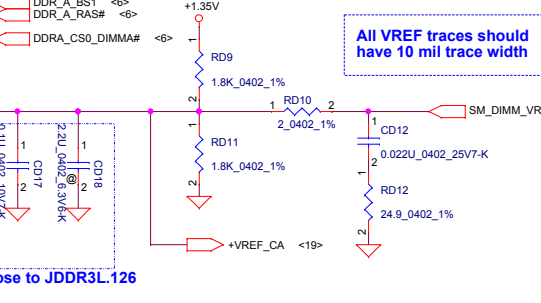
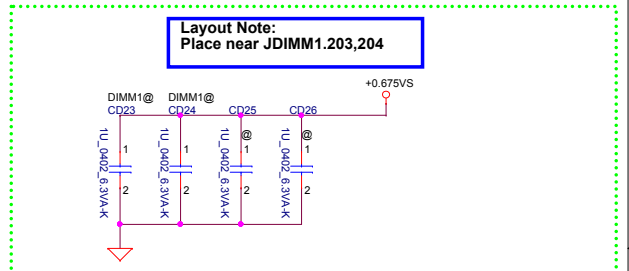
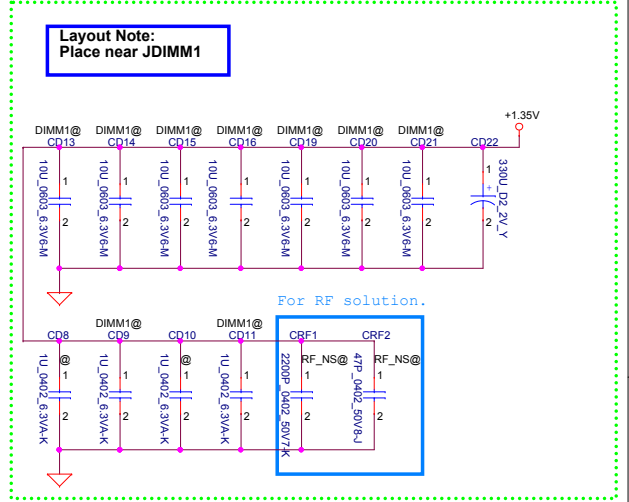
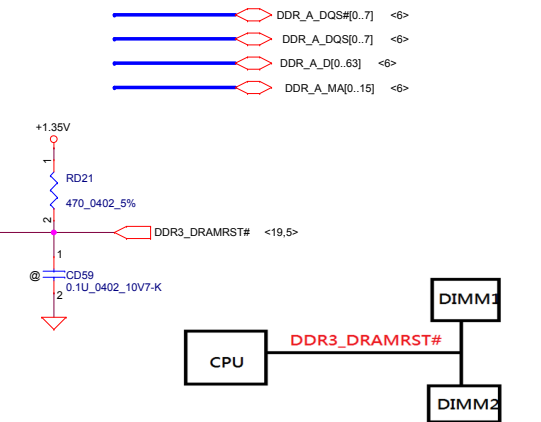
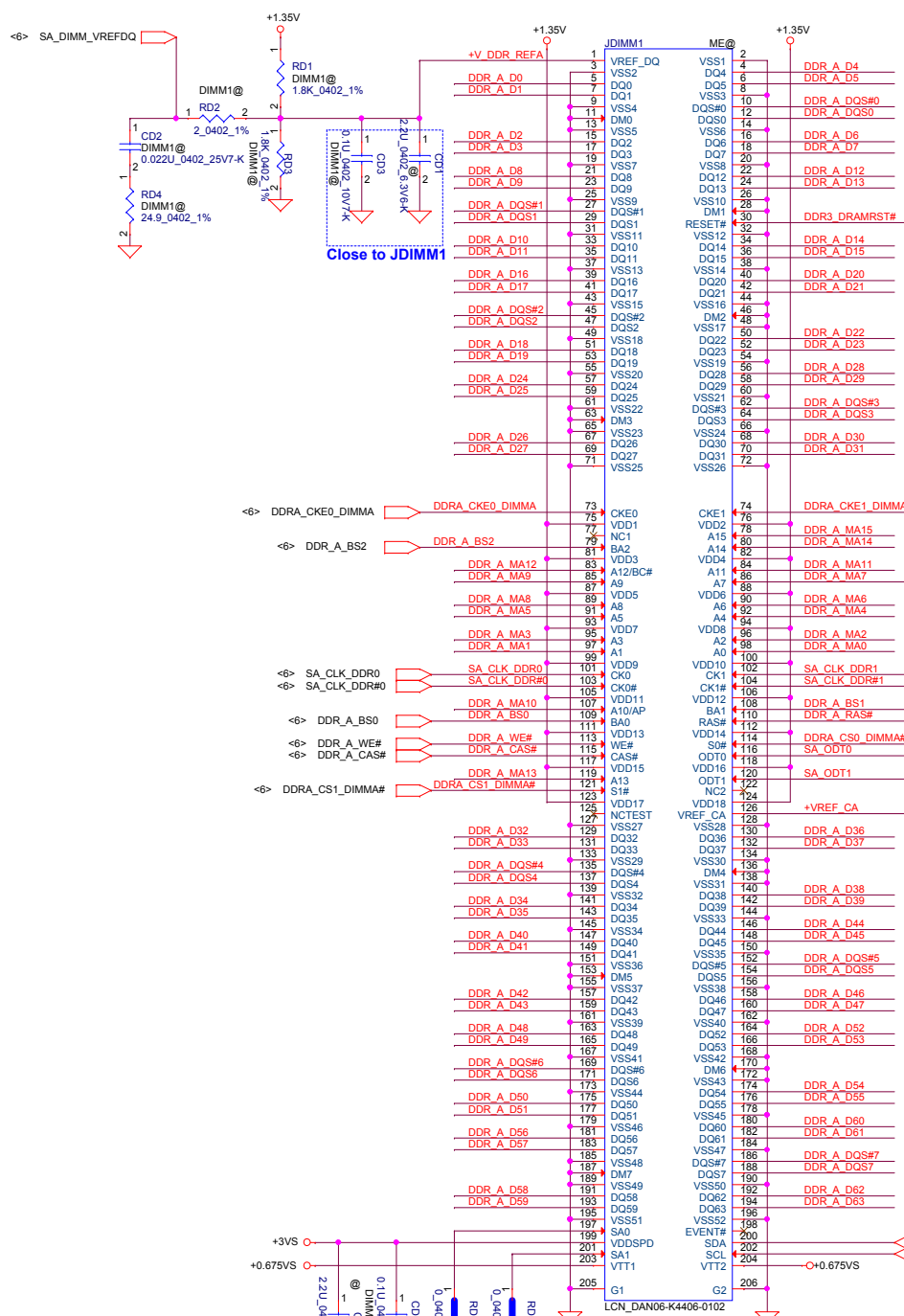
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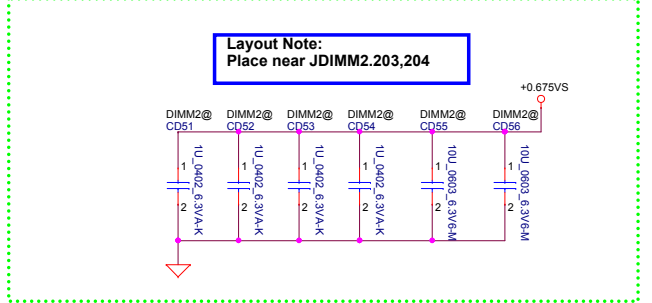
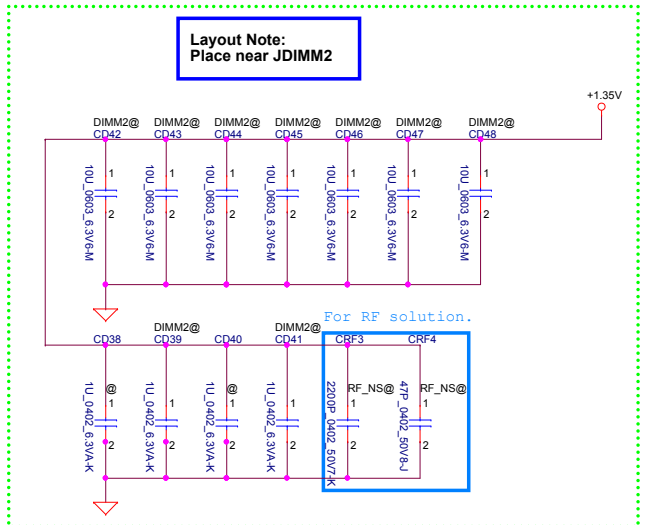
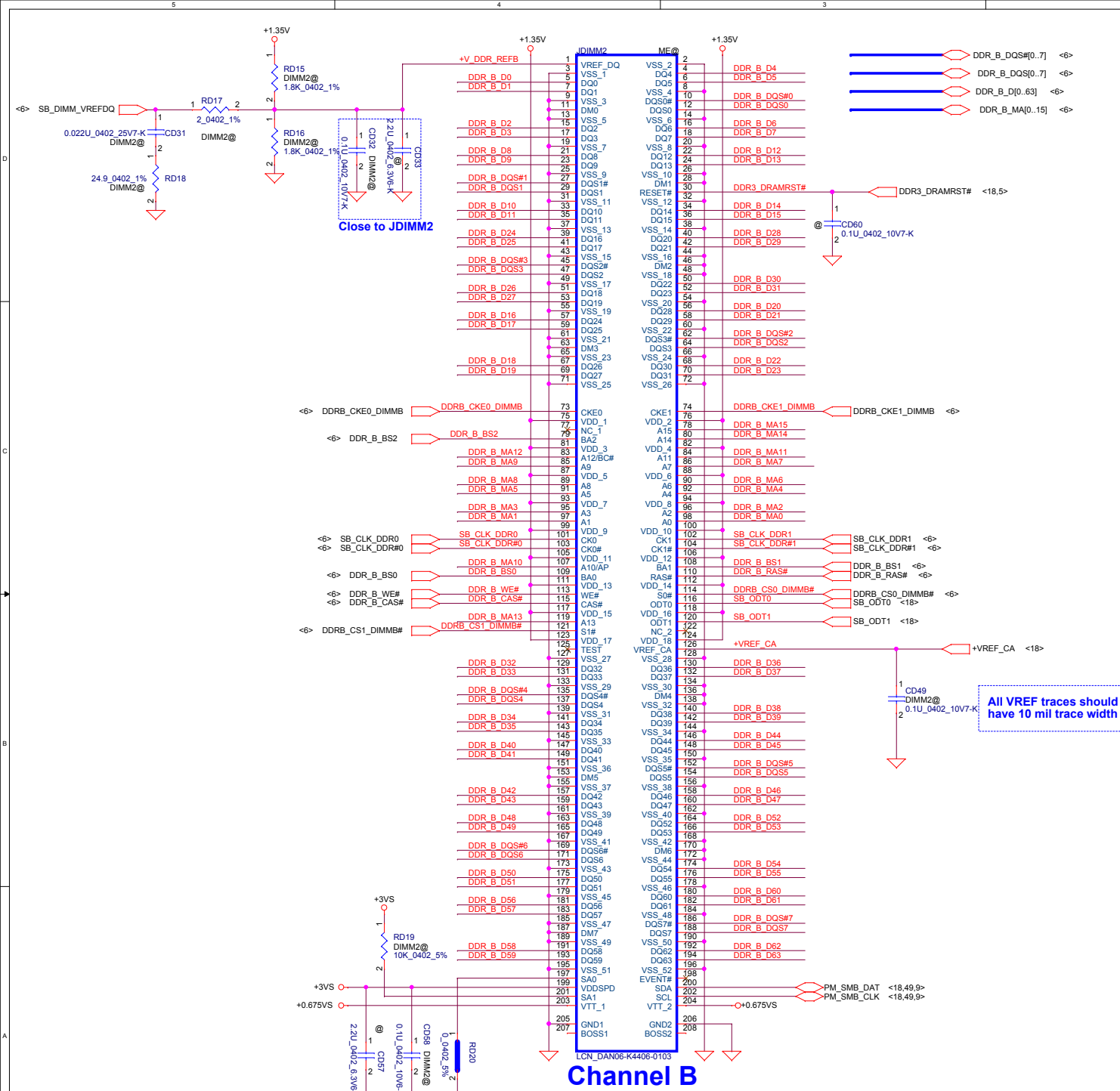
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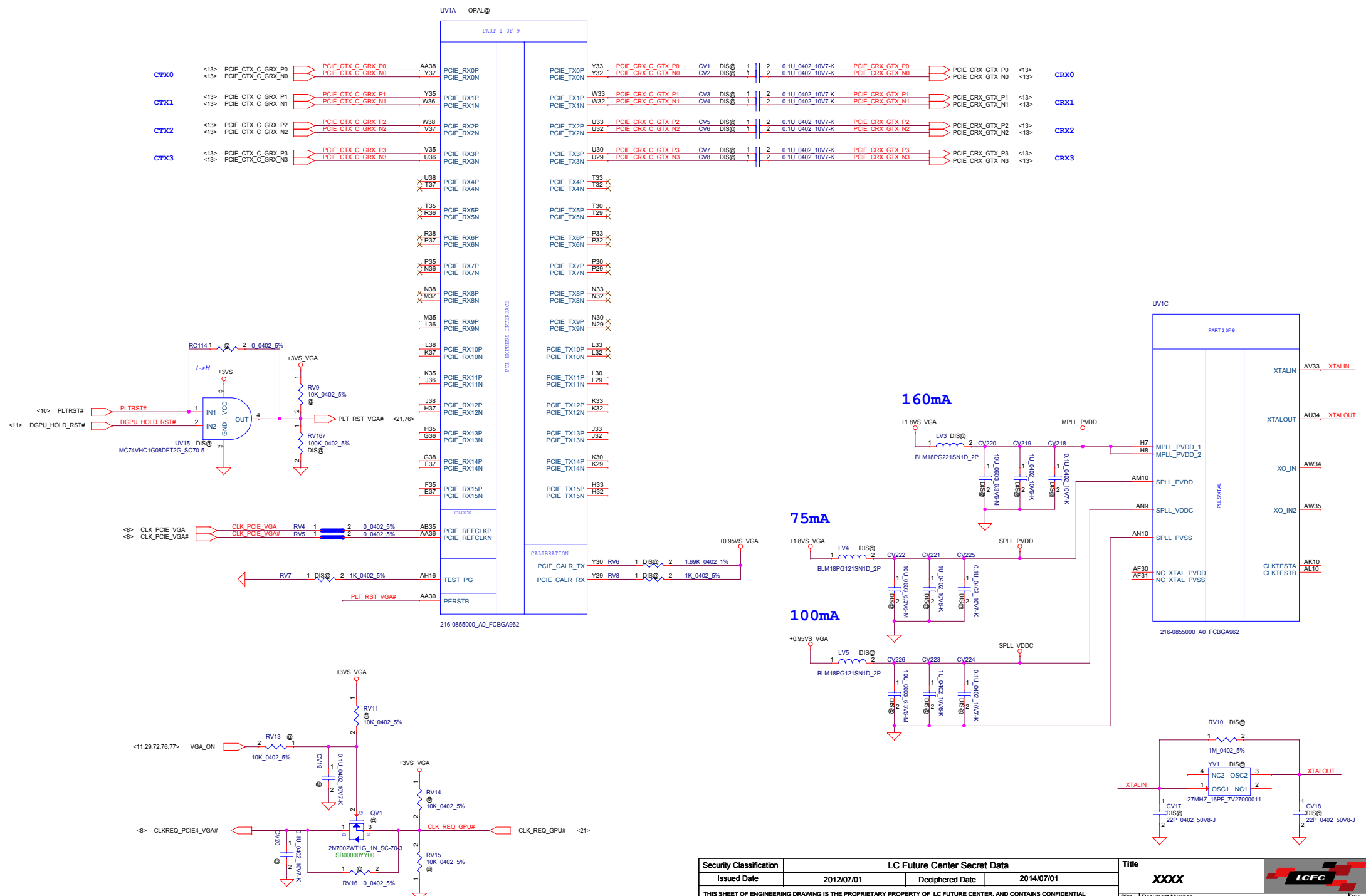
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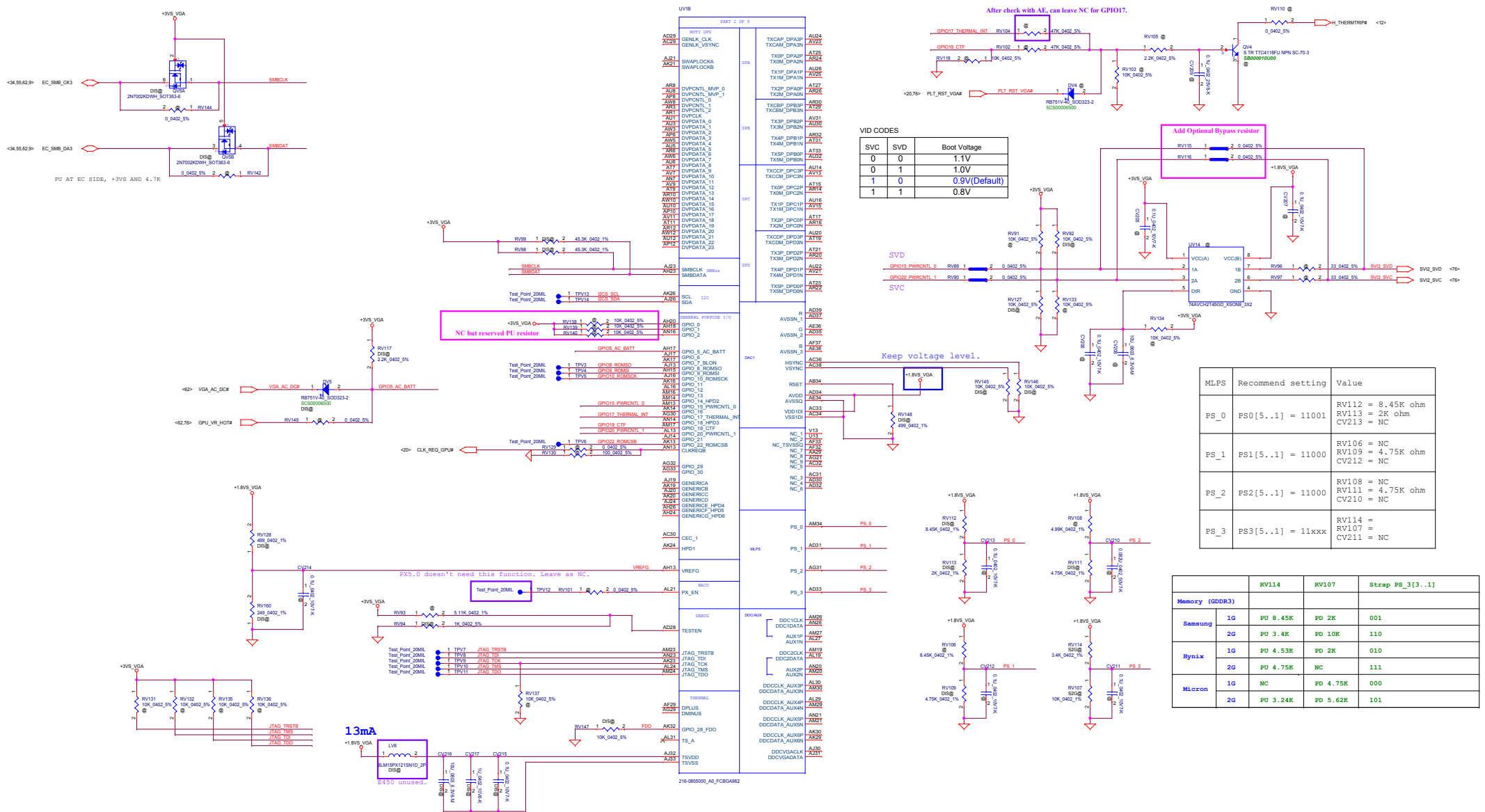
All VREF traces should have 10 mil trace width

<Address: SA1:SA0=10>
DIMM_2 STD H:4mm

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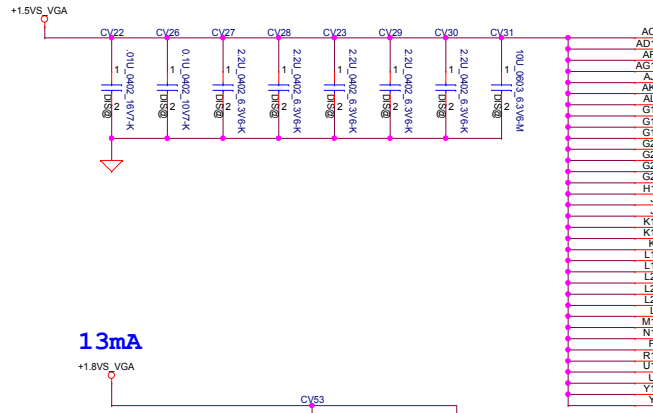
VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

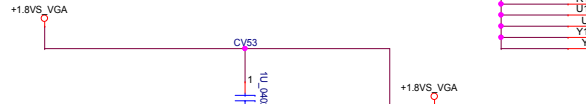
MLPS	Recommend setting	Value
PS_0	FS0[5..1] = 11001	RV112 = 8.45k ohm RV113 = 2K ohm CV213 = NC
PS_1	FS1[5..1] = 11000	RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2	FS2[5..1] = 11000	RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3	FS3[5..1] = 11xxx	RV114 = RV107 = CV211 = NC

	RV114	RV107	Strap PS_3[3..1]
Memory (GDDR3)			
Samsung	1G	PU 8.45K PD 2K	001
	2G	PU 3.4K PD 10K	110
Hynix	1G	PU 4.53K PD 2K	010
	2G	PU 4.75K NC	111
Micron	1G	NC PD 4.75K	000
	2G	PU 3.24K PD 5.62K	101

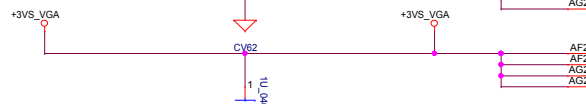
1.5A



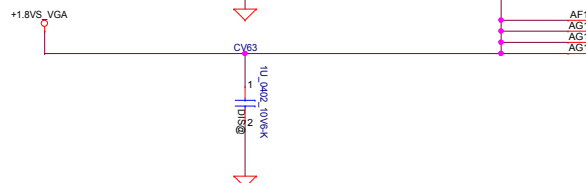
13mA



25mA



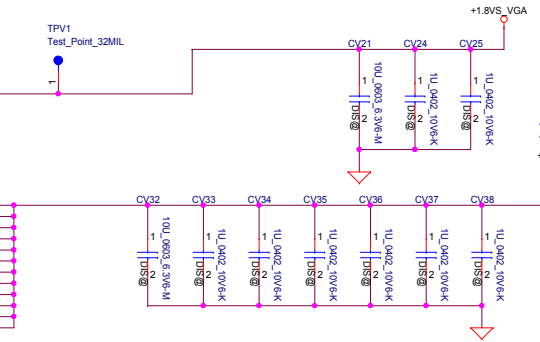
30mA



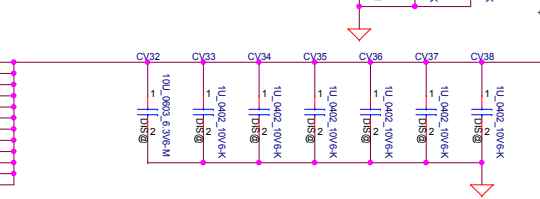
MEM I/O	MEM I/O	PCIE	BACO	CORE	I/O	DIF	VOLTAGE SENSE
AC7	VDDR1_1	AA31	N27	AA15	VDDR3_1	AD12	AF28
AD11	VDDR1_2	AA32	T27	AA17	VDDR3_2	AD11	AG28
AF7	VDDR1_3	AA33		AA20	VDDR3_3	AF11	
AG10	VDDR1_4	AA34		AA22	VDDR3_4	AG24	
AJ7	VDDR1_5	W30		AA24			
AK1	VDDR1_6	T31		AA27			
AL9	VDDR1_7	V28		AB18			
GI1	VDDR1_8	W29		AB21			
G14	VDDR1_9	AB37		AB23			
G17	VDDR1_10			AB28			
G20	VDDR1_11	G30		AC17			
G23	VDDR1_12	G31		AC20			
G26	VDDR1_13	H29		AC22			
G29	VDDR1_14	H30		AC24			
H10	VDDR1_15	J29		AD16			
J7	VDDR1_16	K31		AD21			
J9	VDDR1_17	L28		AD23			
K11	VDDR1_18	M28		AF17			
K13	VDDR1_19	N28		AF20			
K6	VDDR1_20	R28		AF22			
L12	VDDR1_21	T28		AG16			
L21	VDDR1_22	U28		AG18			
L23	VDDR1_23			AH22			
L26	VDDR1_24			AH27			
L7	VDDR1_25			AH28			
M11	VDDR1_26			M26			
N11	VDDR1_27			N24			
P7	VDDR1_28			R18			
RT1	VDDR1_29			R21			
U11	VDDR1_30			R23			
U7	VDDR1_31			R26			
Y11	VDDR1_32			T17			
Y7	VDDR1_33			T20			
	VDDR1_34			T22			
				T24			
				U18			
				U21			
				U23			
				U26			
				V17			
				V20			
				V22			
				V24			
				V27			
				Y16			
				Y18			
				Y21			
				Y23			
				Y26			
				Y28			
				Y13			

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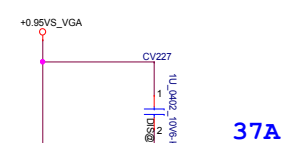
100mA



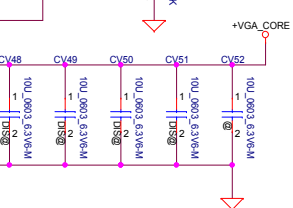
1A



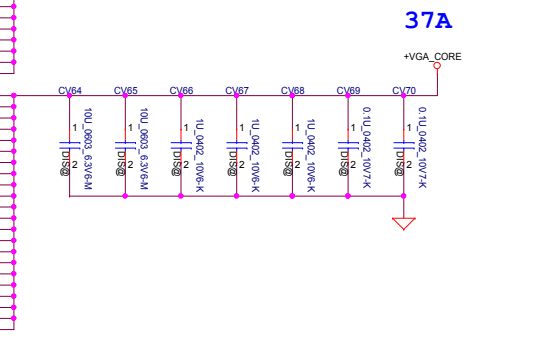
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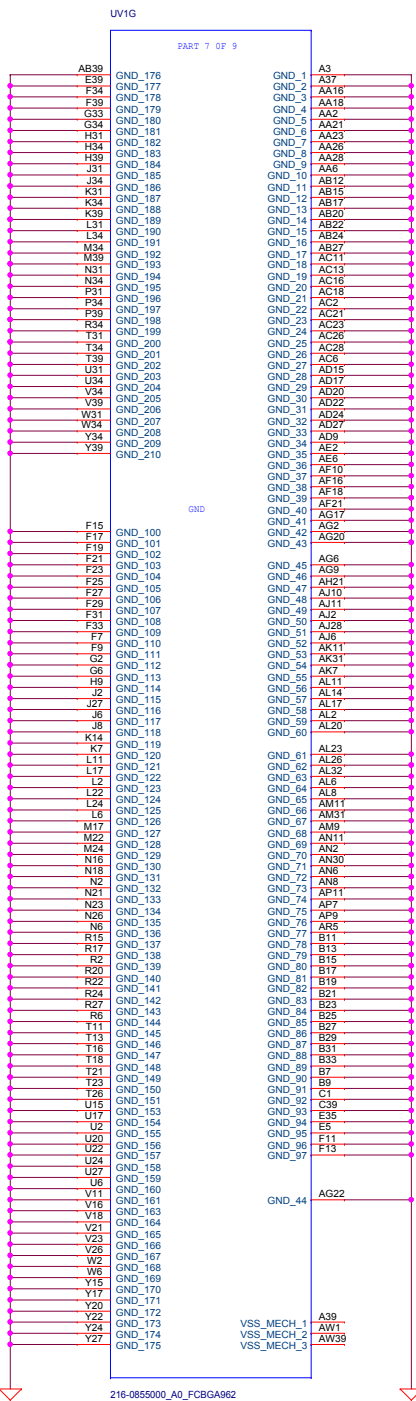


37A



37A





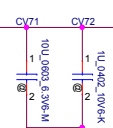
216-0855000_A0_FCBGA962

VSS_MECH_1
VSS_MECH_2
VSS_MECH_3

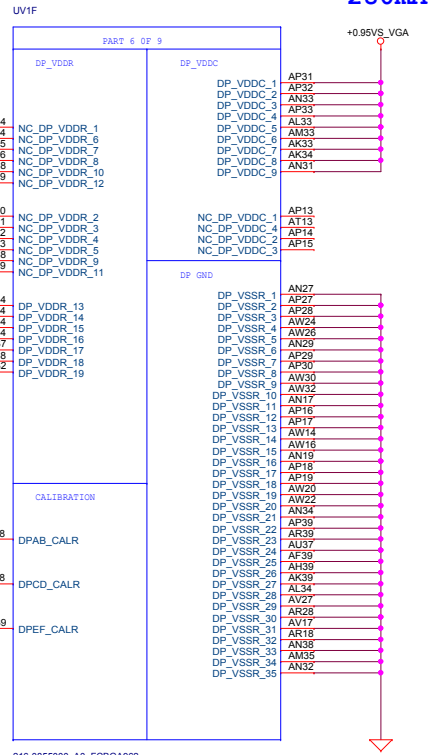
A39
AW1
AW39

237mA

+1.8VS_VGA



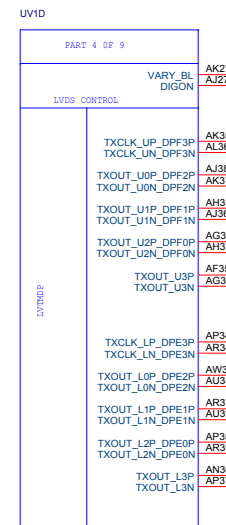
RV17 1 DIS 2 150.0402 1%



280mA

+0.85VS_VGA

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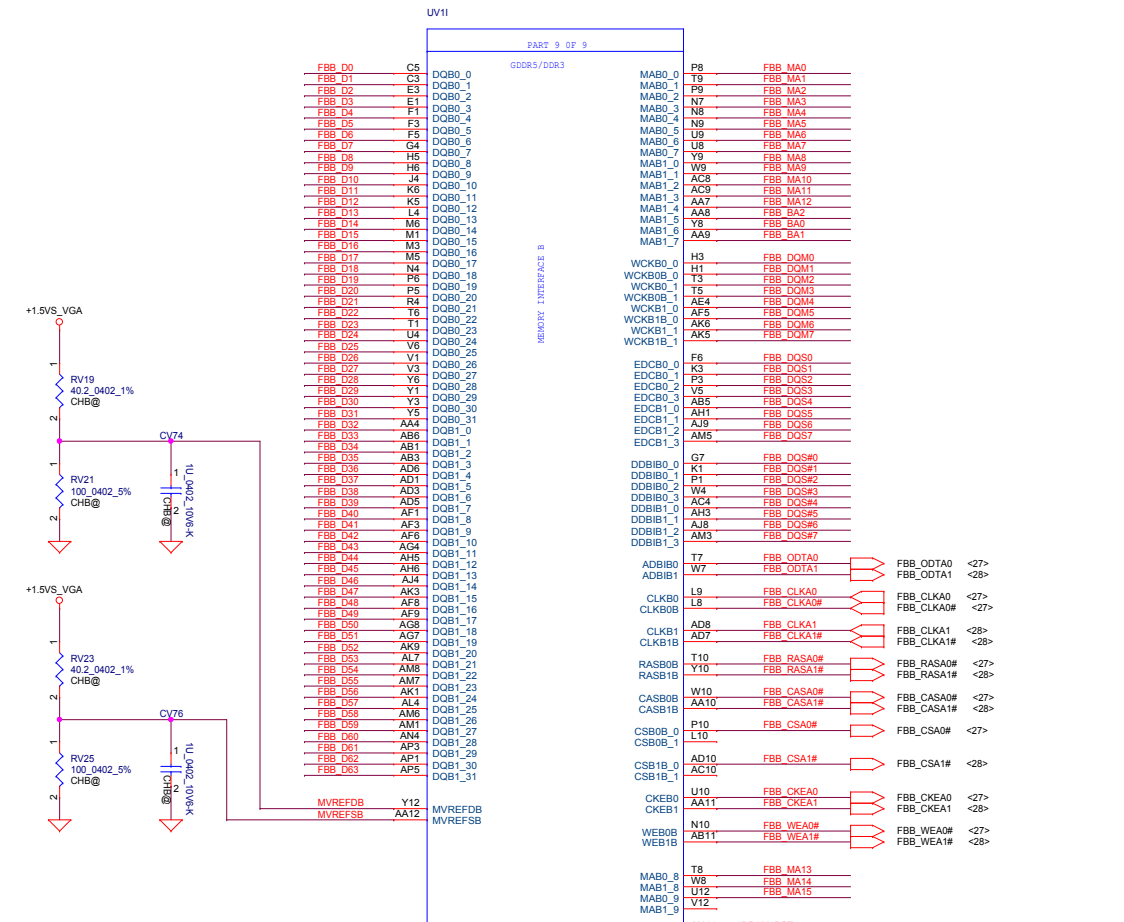
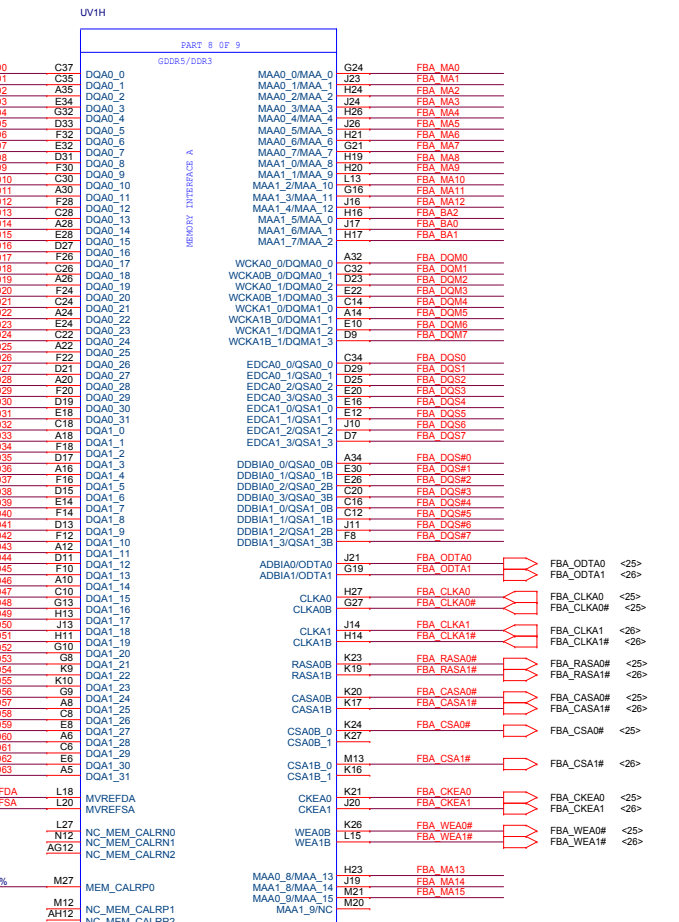
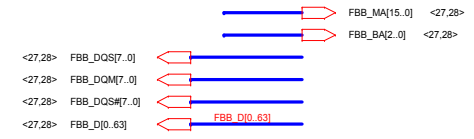
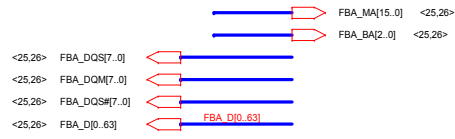


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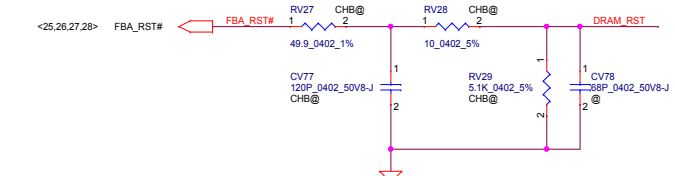


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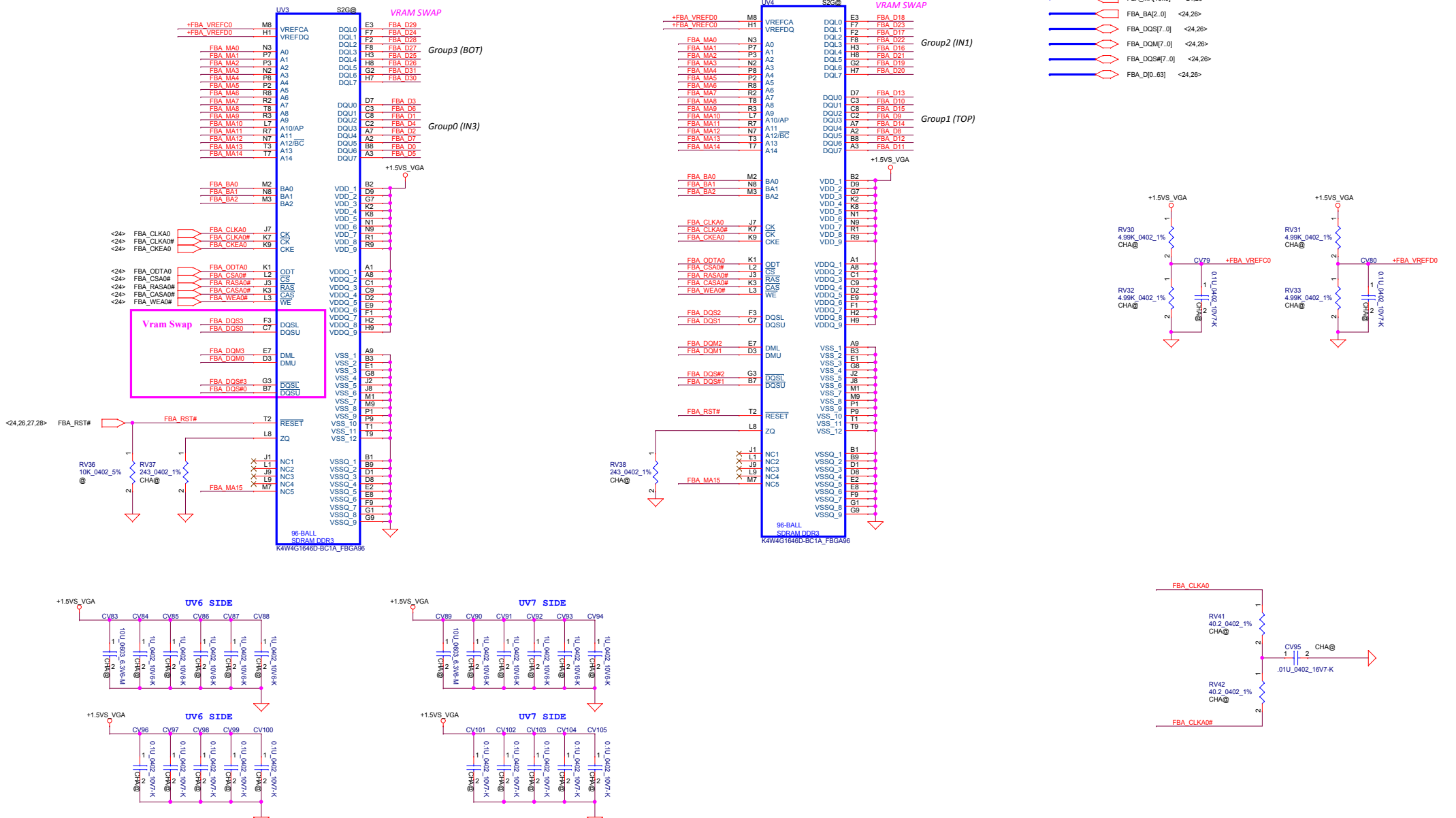
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216-0855000_A0_FCBGA962

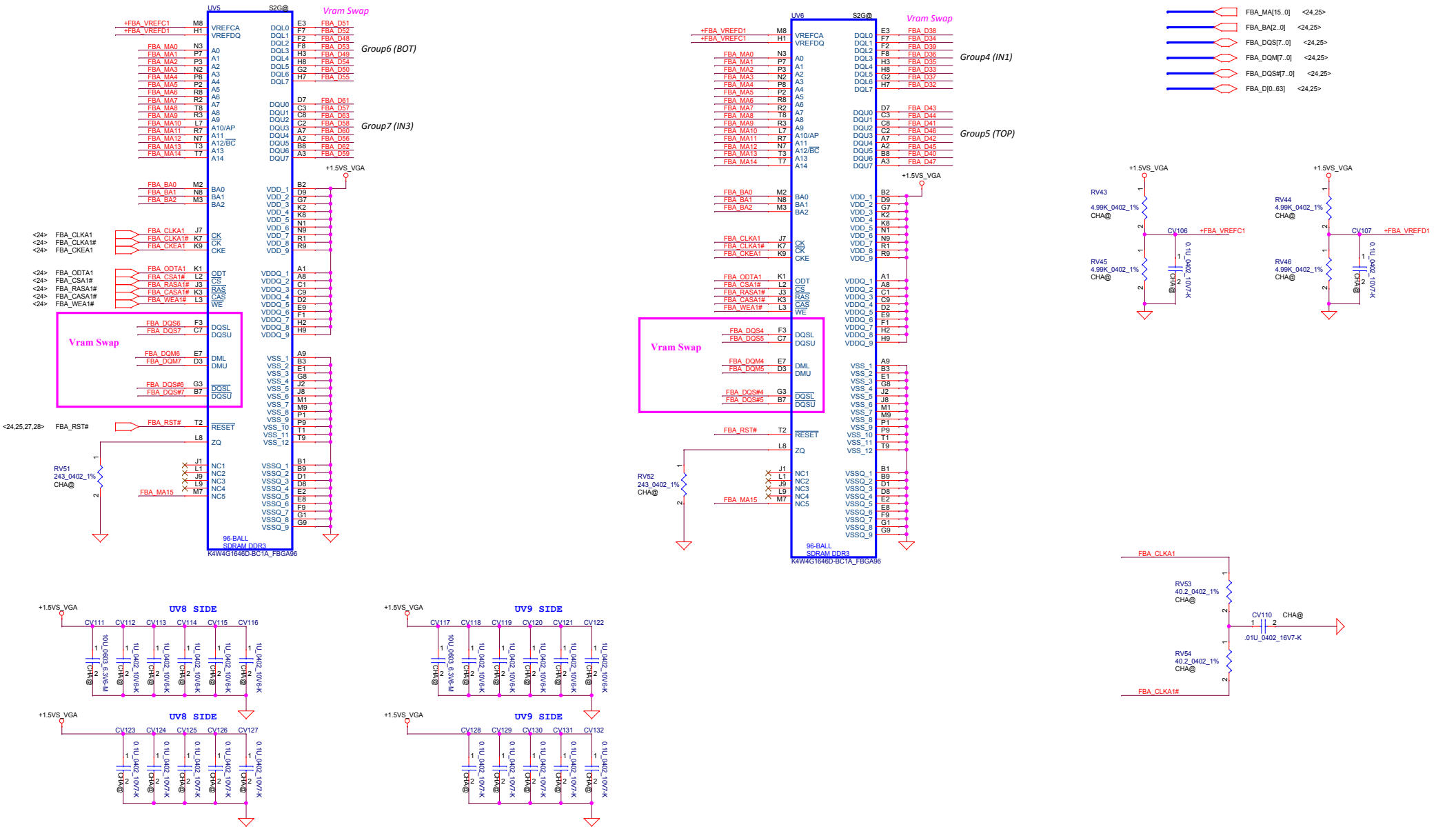


Memory Partition A - Lower 32 bits

Change all VRAM footprint to MT41K256M16HA107_FBGA96P-A39P

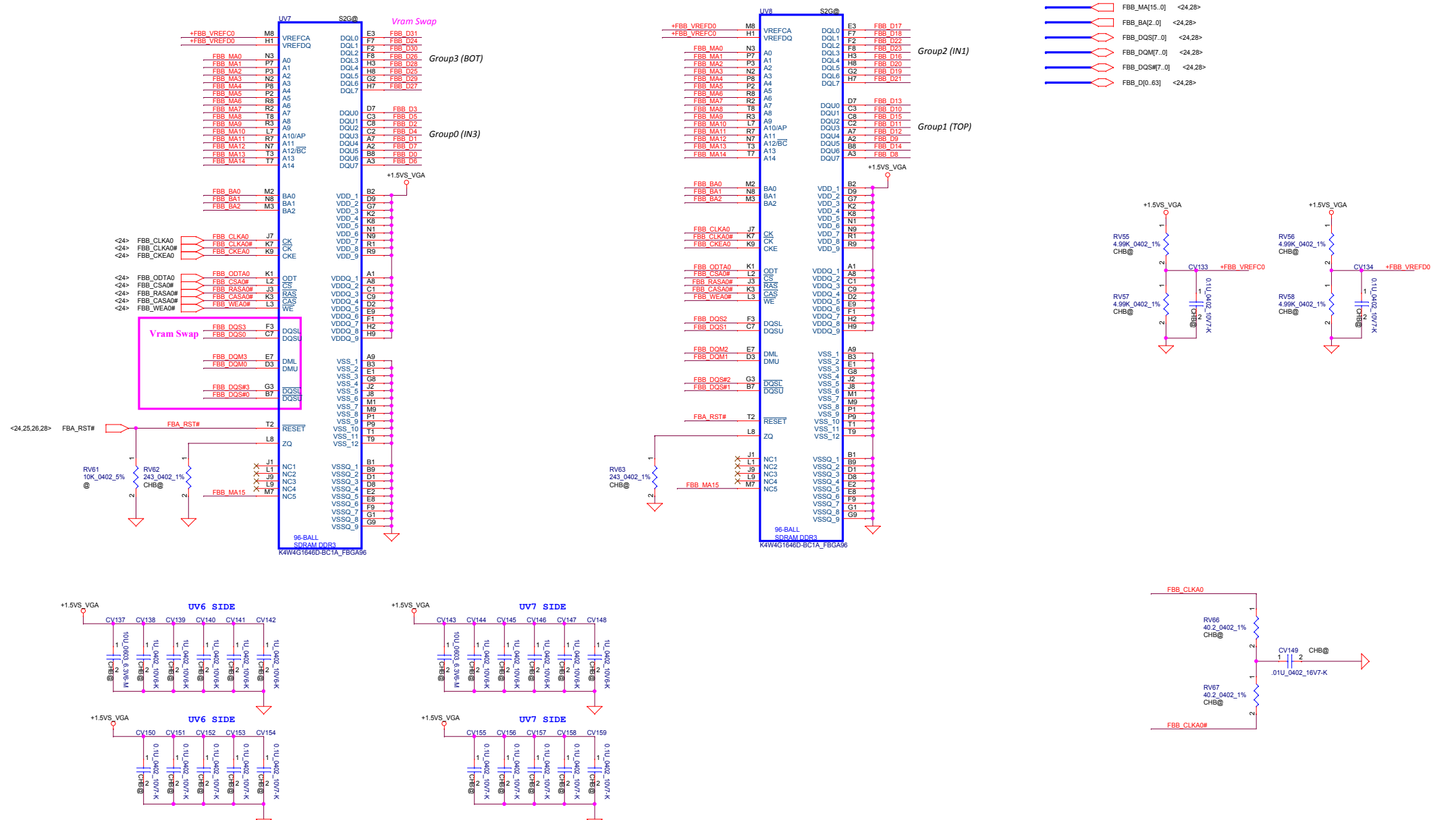


Memory Partition A - Upper 32 bits



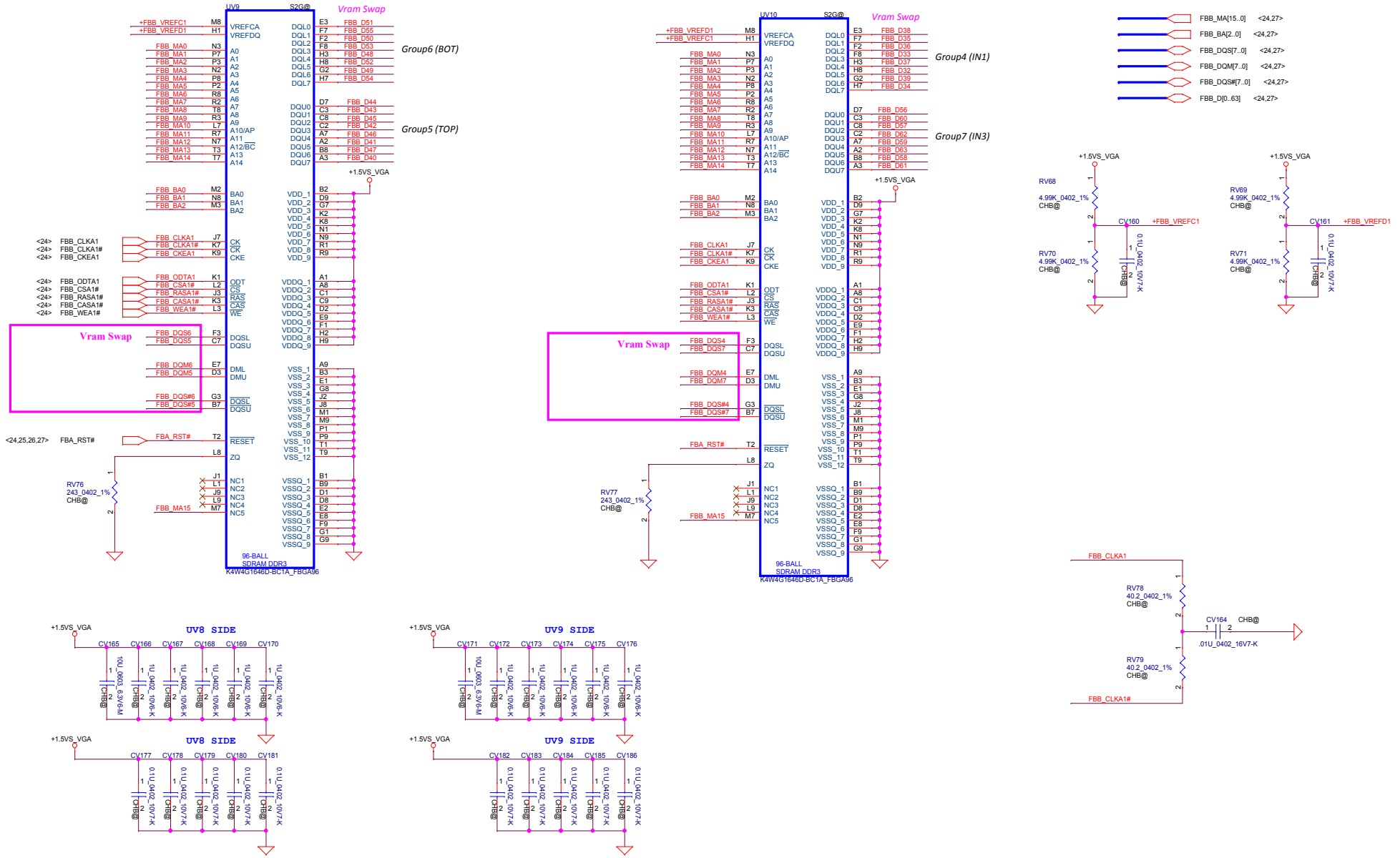
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	XXXX		
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Memory Partition A - Lower 32 bits

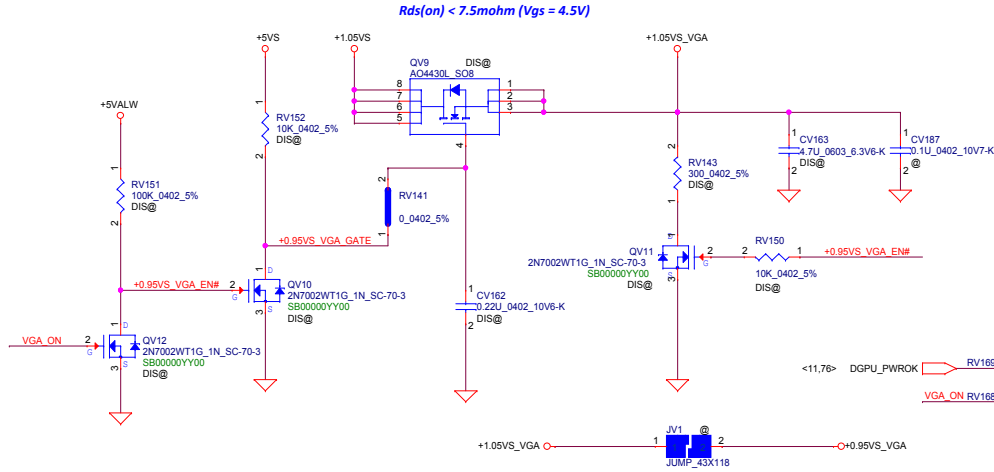


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Date:	Thursday, November 08, 2014	Sheet	27	of	81

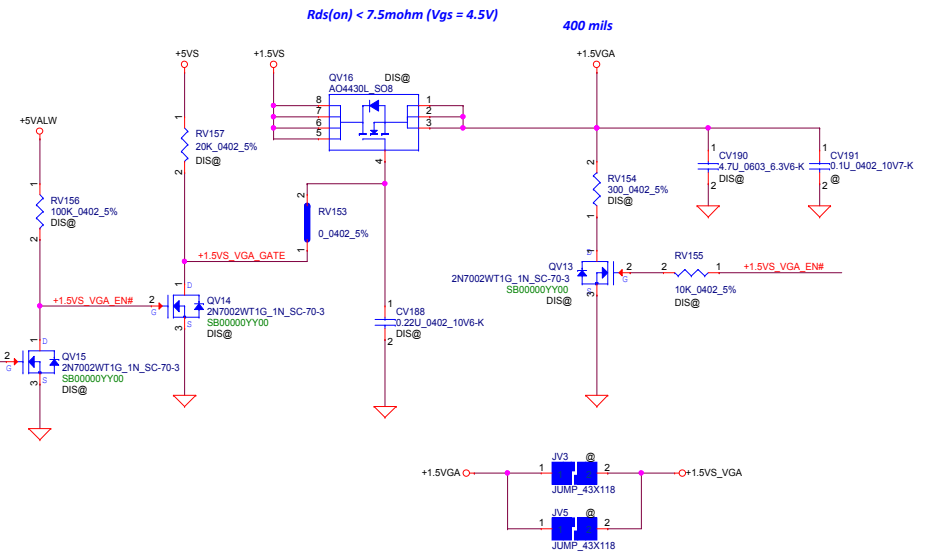
Memory Partition A - Upper 32 bits



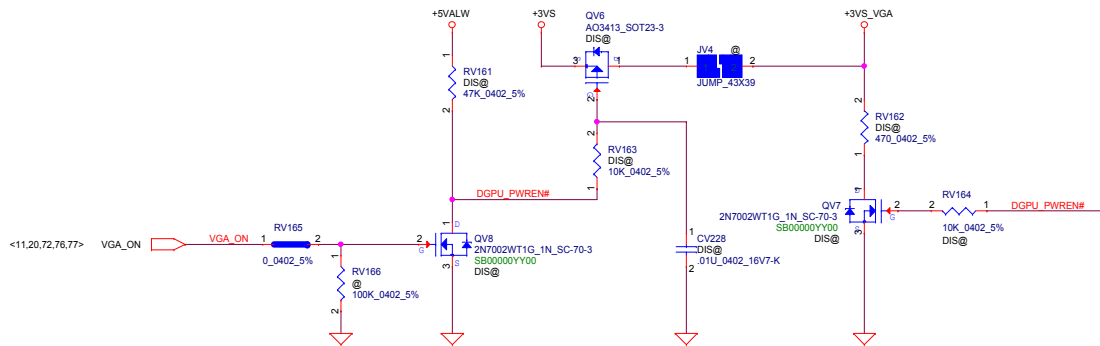
+1.05VS to +0.95VS_VGA



+1.5VS to +1.5VS_VGA




+3VS to +3VS_VGA




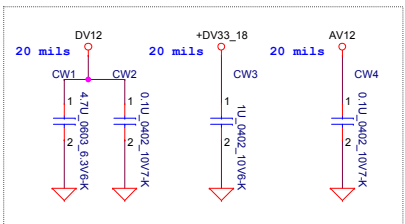
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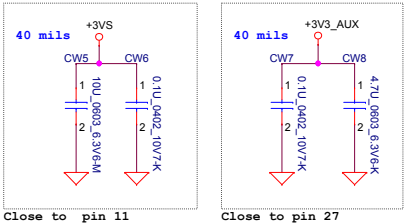
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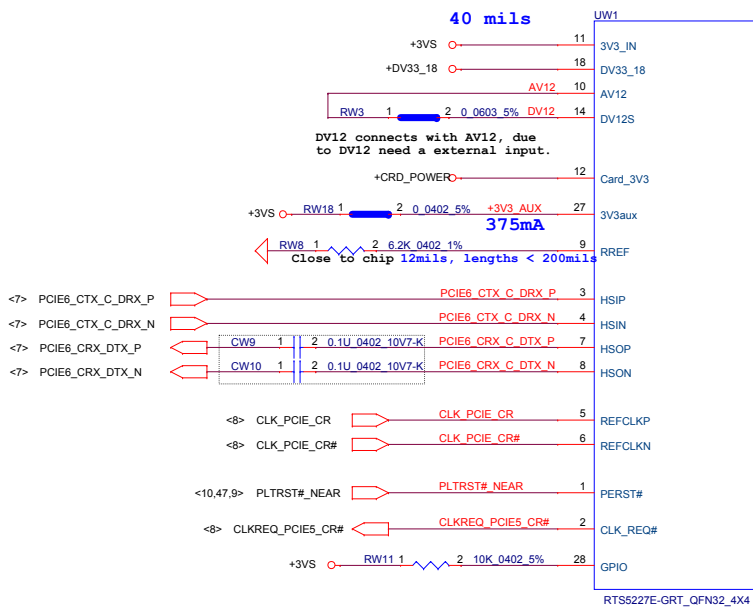


All of cap. close to chip

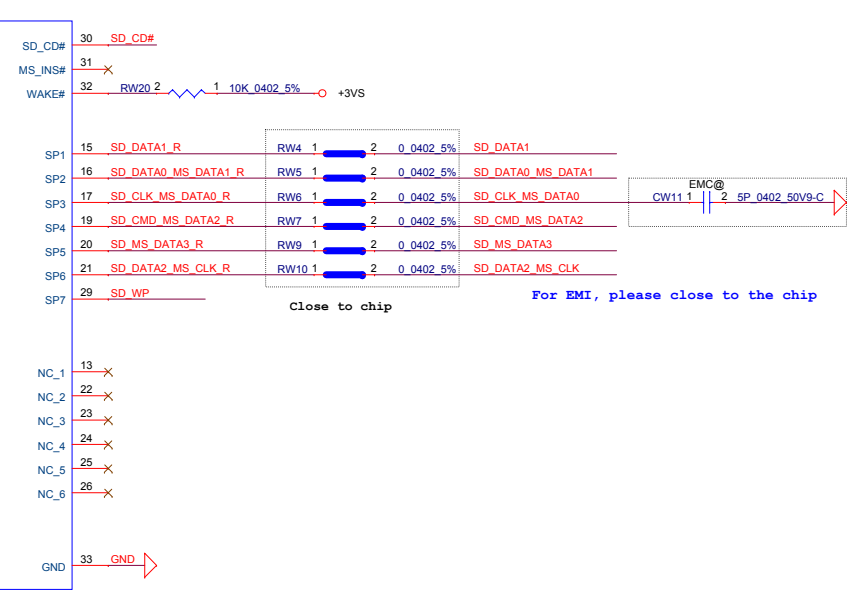


Close to pin 11

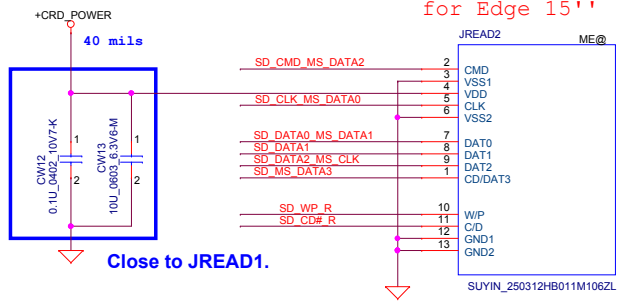
Close to pin 27



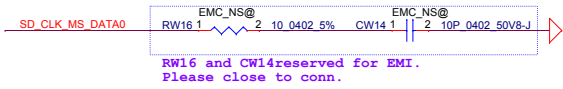
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- <7> PCIE6_CTX_C_DRX_N
- <7> PCIE6_CRX_DTX_P
- <7> PCIE6_CRX_DTX_N
- <8> CLK_PCIE_CR
- <8> CLK_PCIE_CR#
- <10,47,9> PLTRST#_NEAR
- <8> CLKREQ_PCIE5_CR#



Close to chip For EMI, please close to the chip




Close to JREAD1.

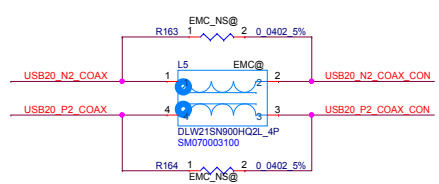


RW16 and CW14 reserved for EMI. Please close to conn.

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(Move to sub board)

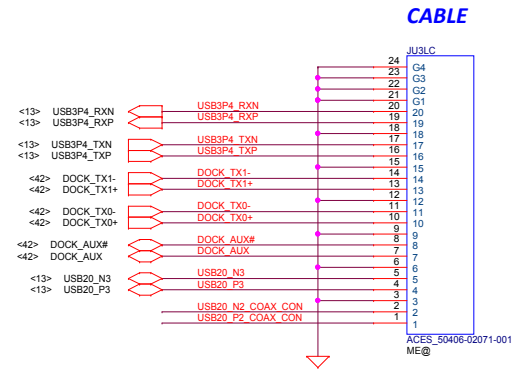
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DOCKING

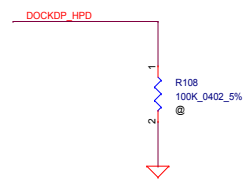
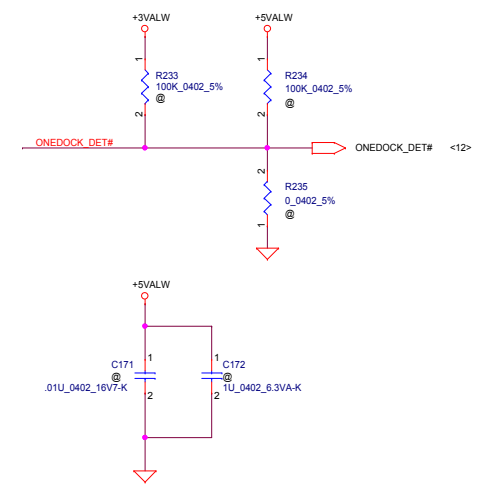
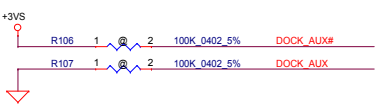
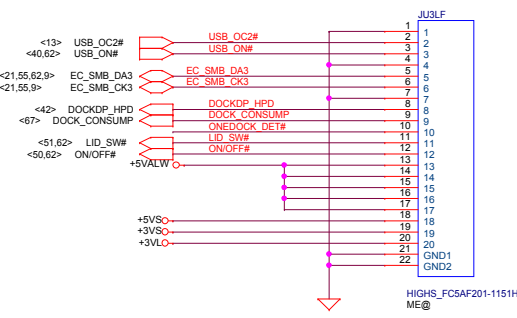
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SUB/B



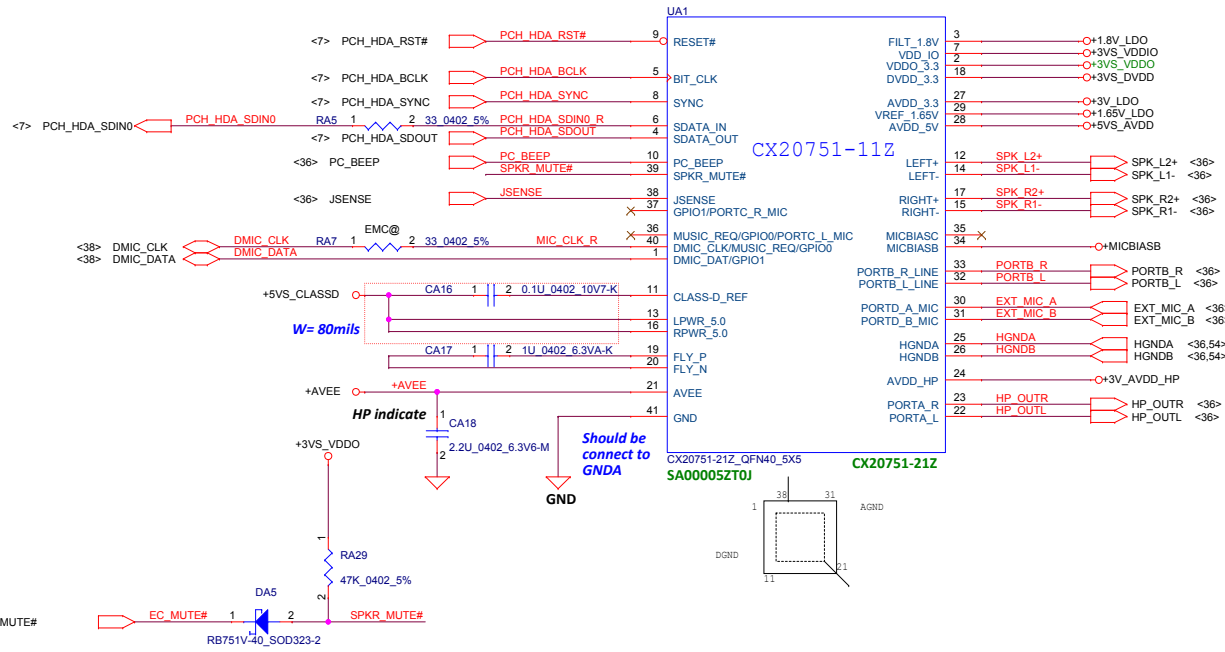
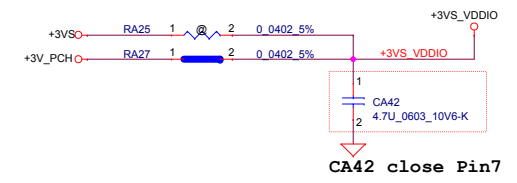
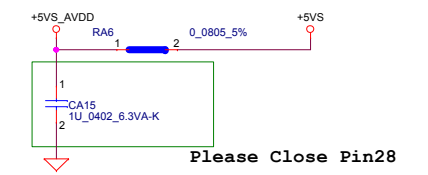
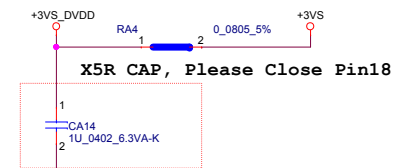
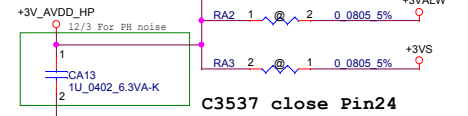
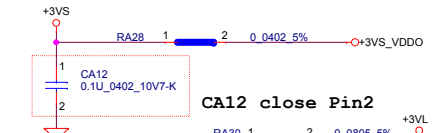
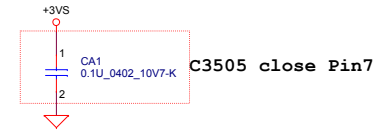
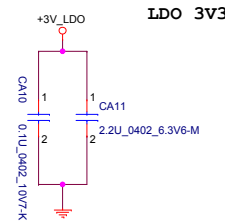
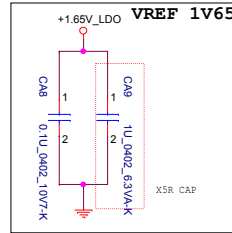
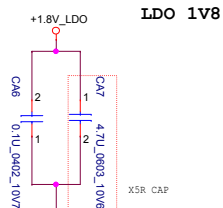
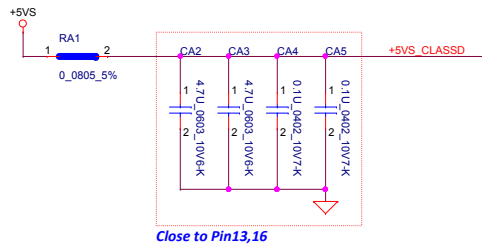
CABLE

FFC



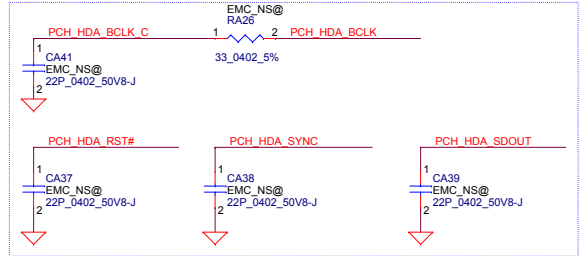
1. AC Capacitor place on Sub/B
2. Need to check with MUX IC vendor whether still need AC cap between MUX IC and device.

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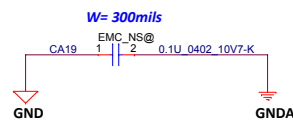
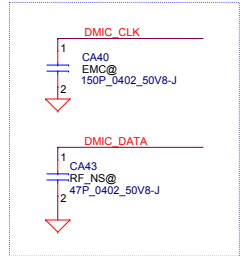


Apple -> EXT_MIC_A, HGND
 Nokia -> EXT_MIC_B, HGND

EMI, close to UA1



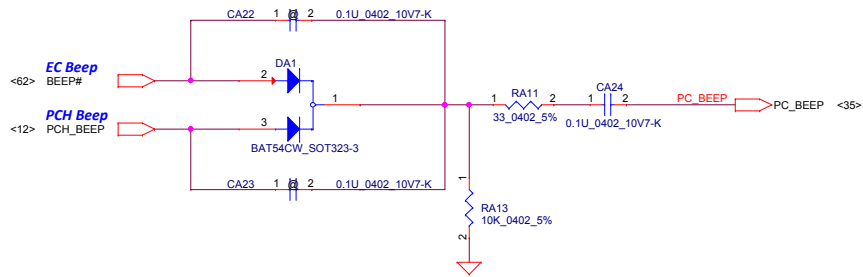
RF, close to RA7



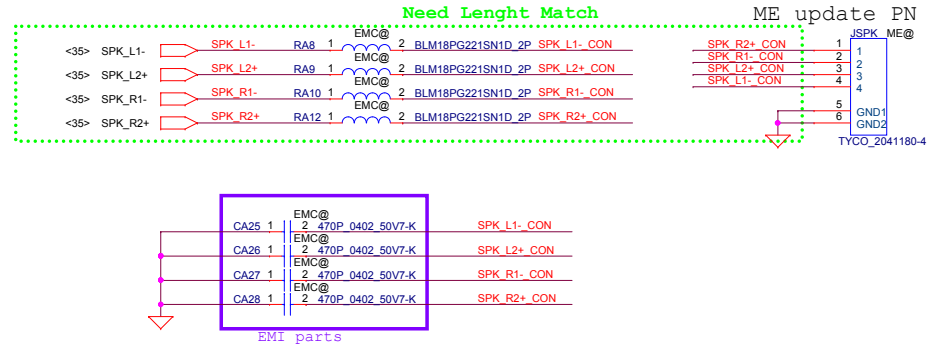
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PC Beep

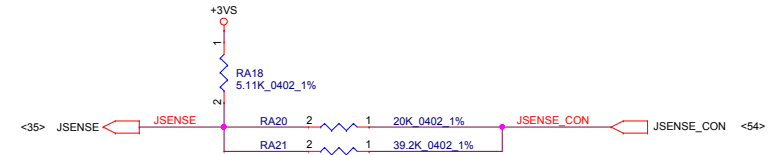
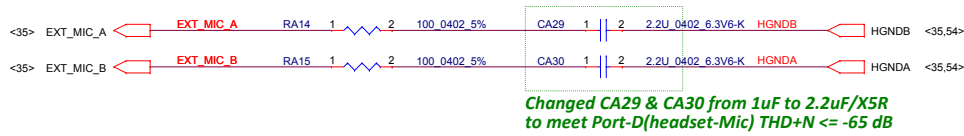


Speaker OUT

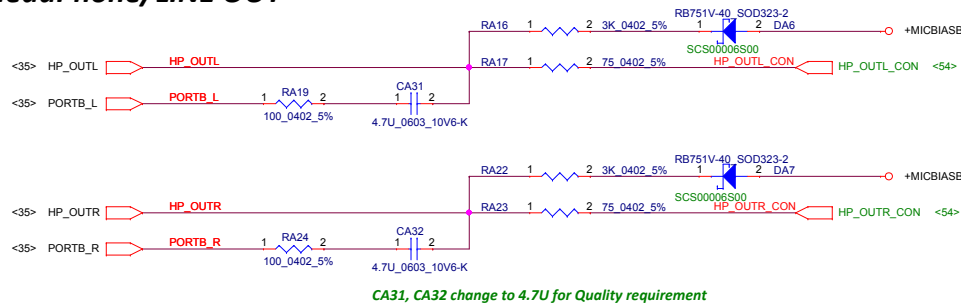


EXT. MIC/LINE IN

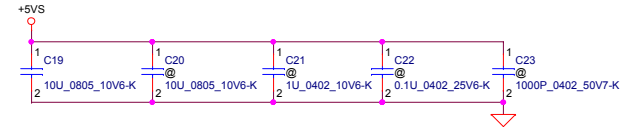
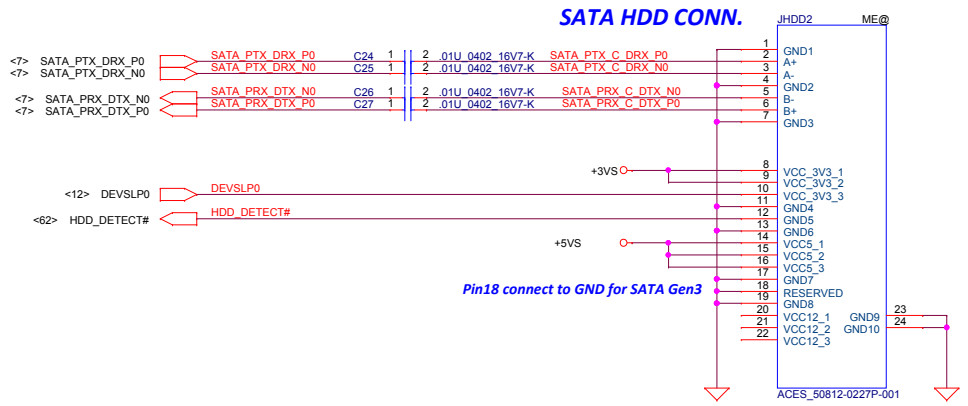
Apple --> EXT_MIC_A, HGND B
 Nokia --> EXT_MIC_B, HGND A



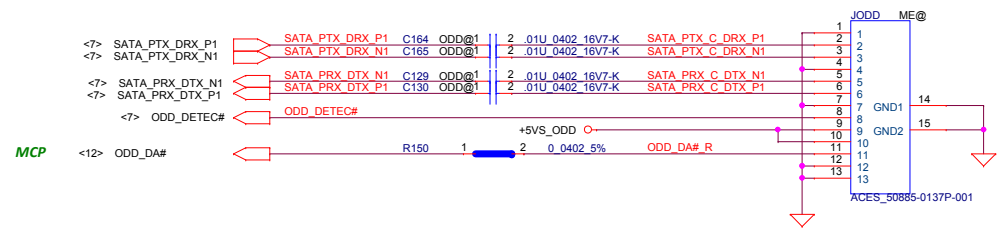
HeadPhone/LINE OUT



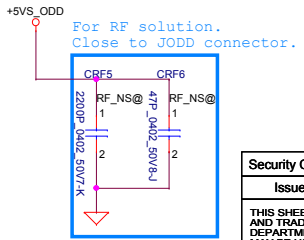
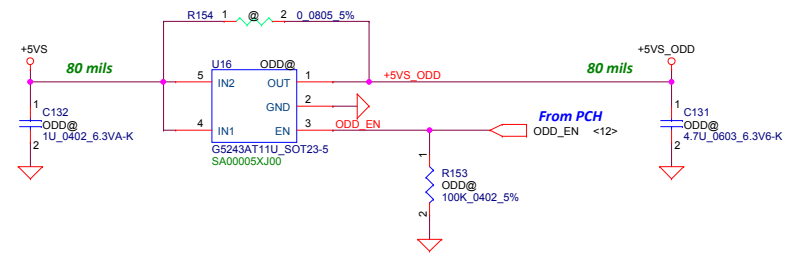
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SATA ODD CONN

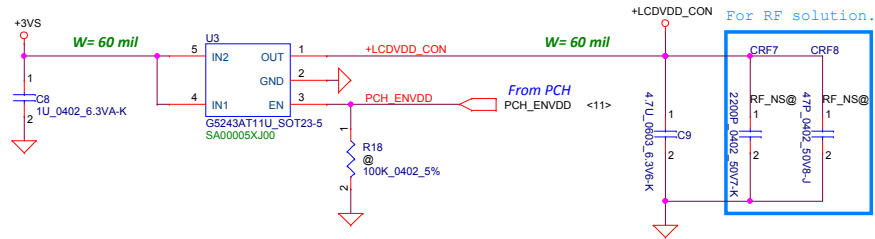


+5VS TO +5VS_ODD

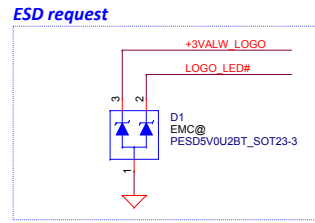
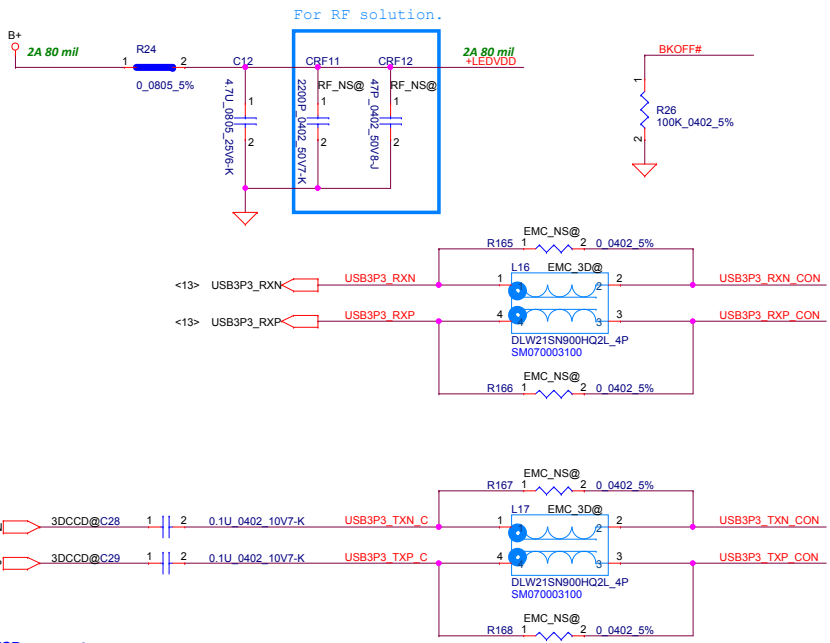
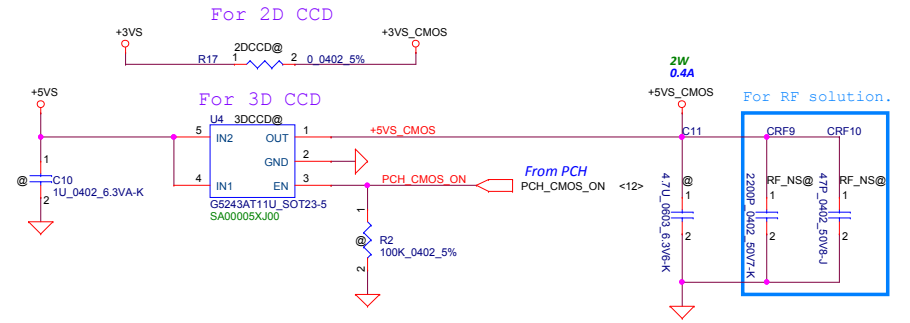


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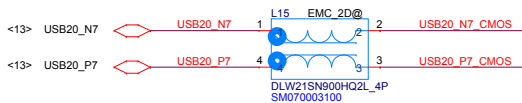
LCDVDD Circuit



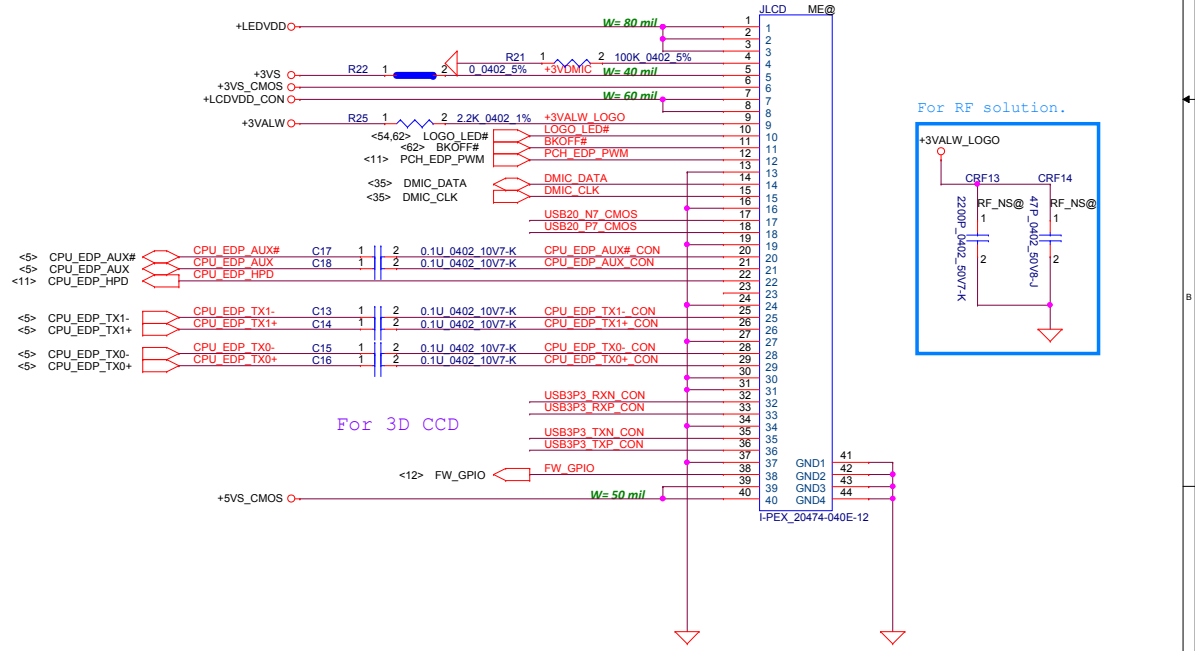
CMOS Camera



CMOS USB Port 2




eDP CONN.

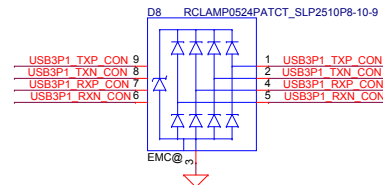
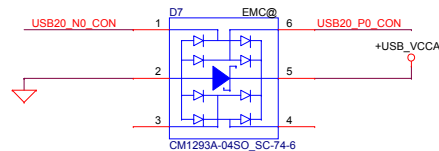
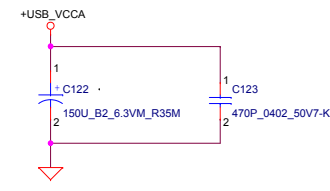
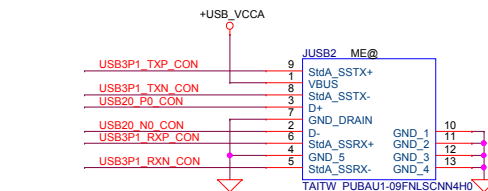
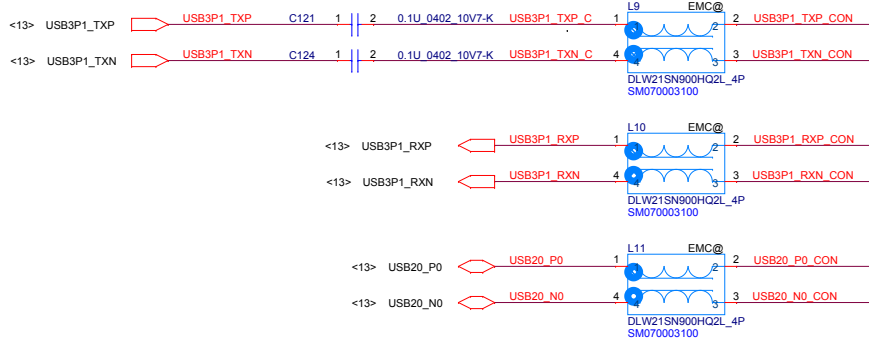
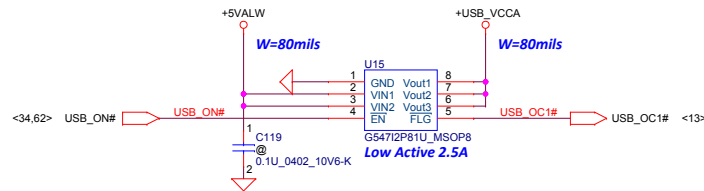


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				Date:	Thursday, November 06, 2014	Sheet	39	of	81

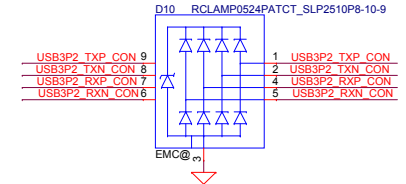
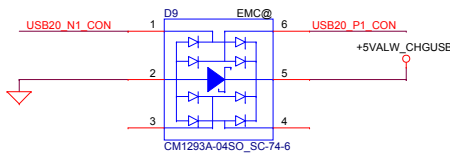
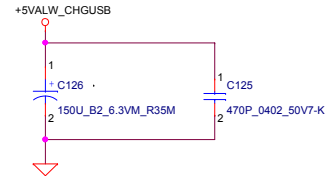
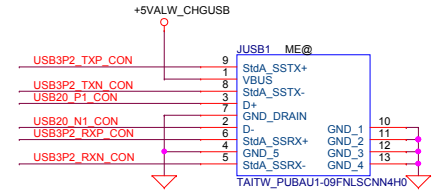
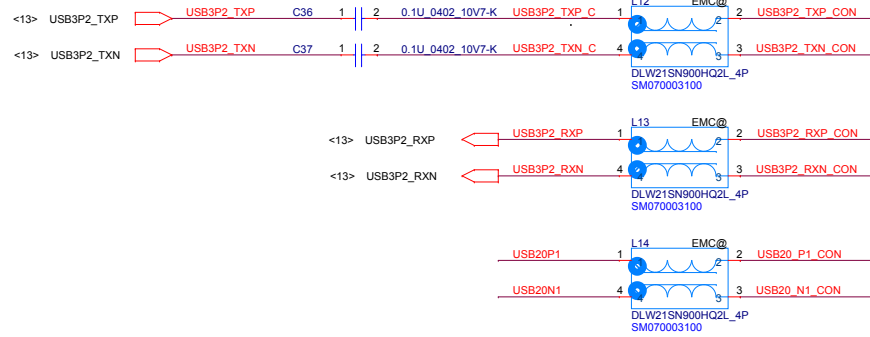
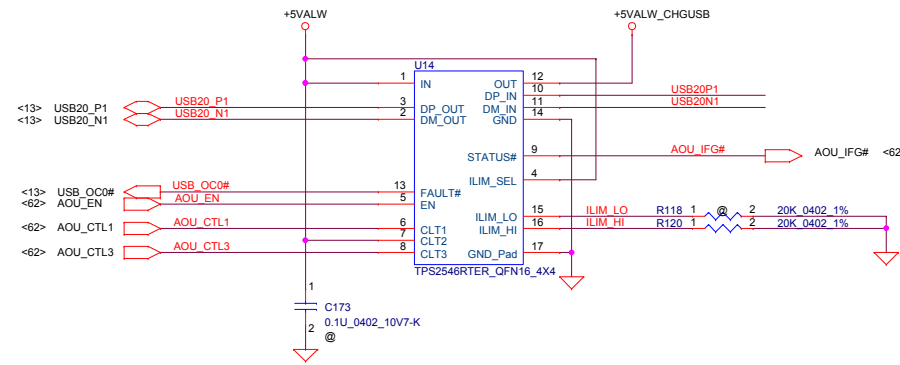
POWER SWITCH



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Title	USB3 PORT1-BACK
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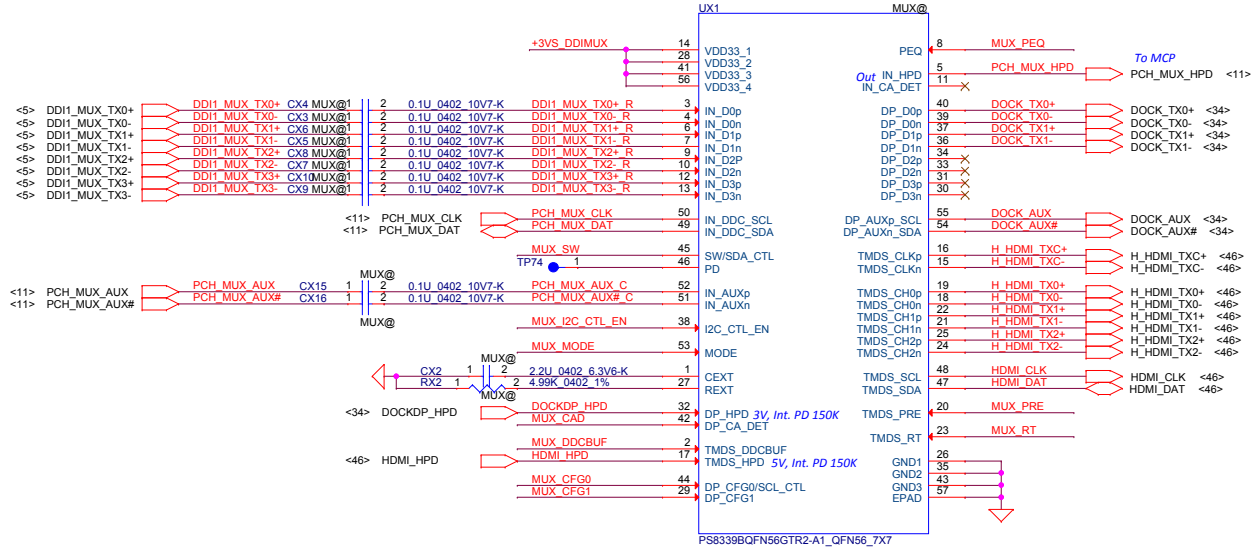
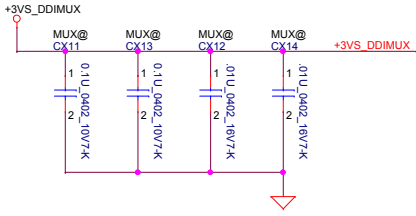
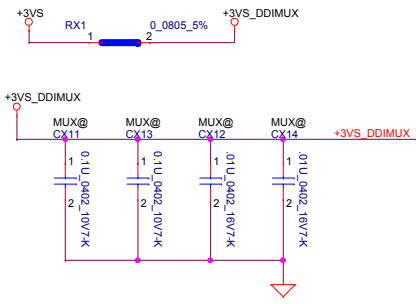




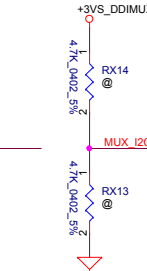
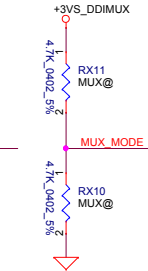
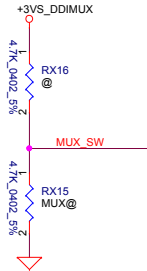
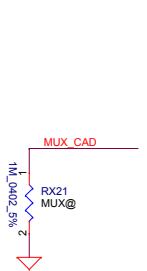
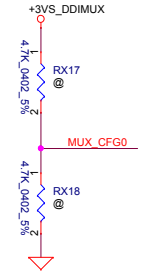
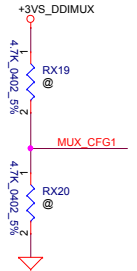
TI TPS2546

CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
* 1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
* 1	1	1	0	SDP2	Data Connected
* 1	1	0	X	SDP1	Data Connected
* 0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
* 0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

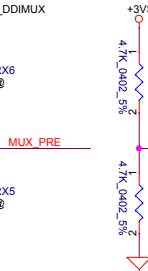
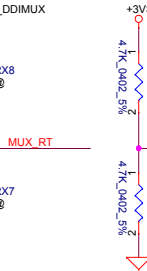
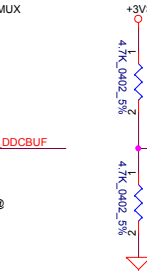
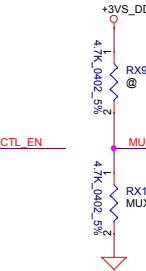
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**Auto Mode
DP Higher Priority**

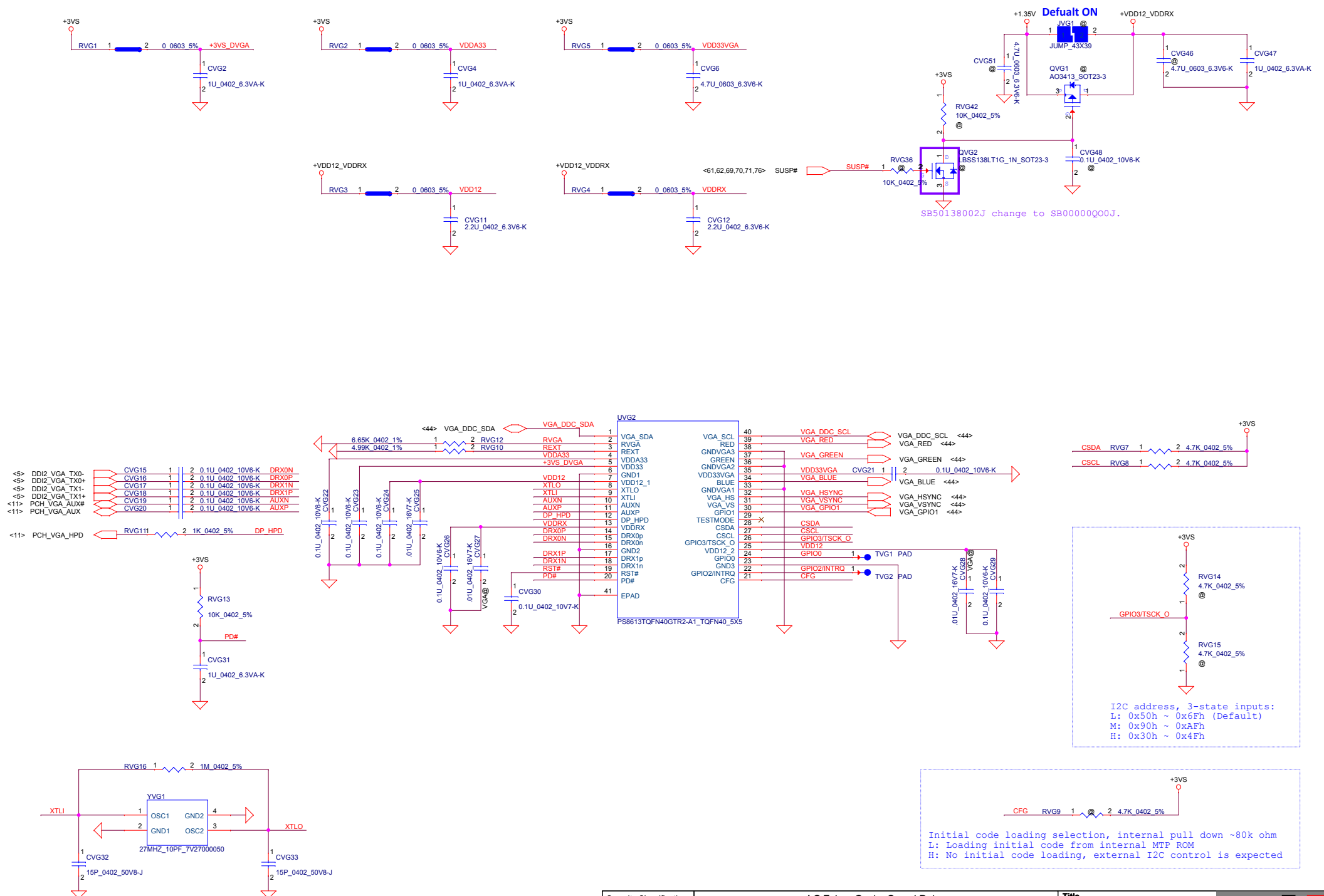


Pass Through Mode



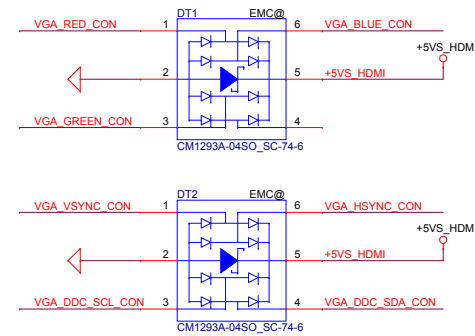
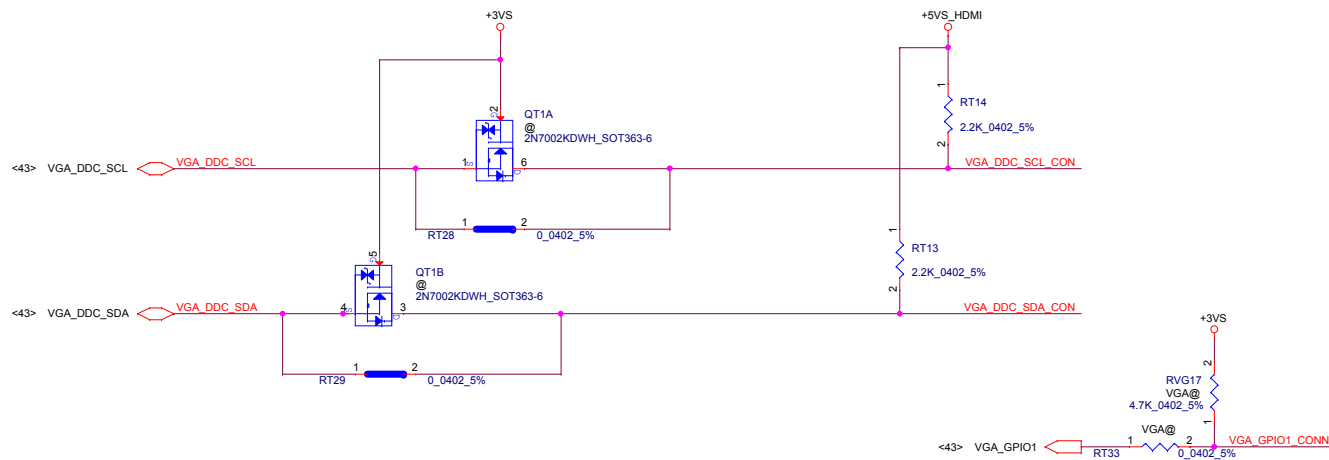
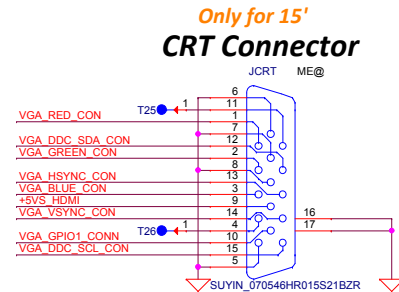
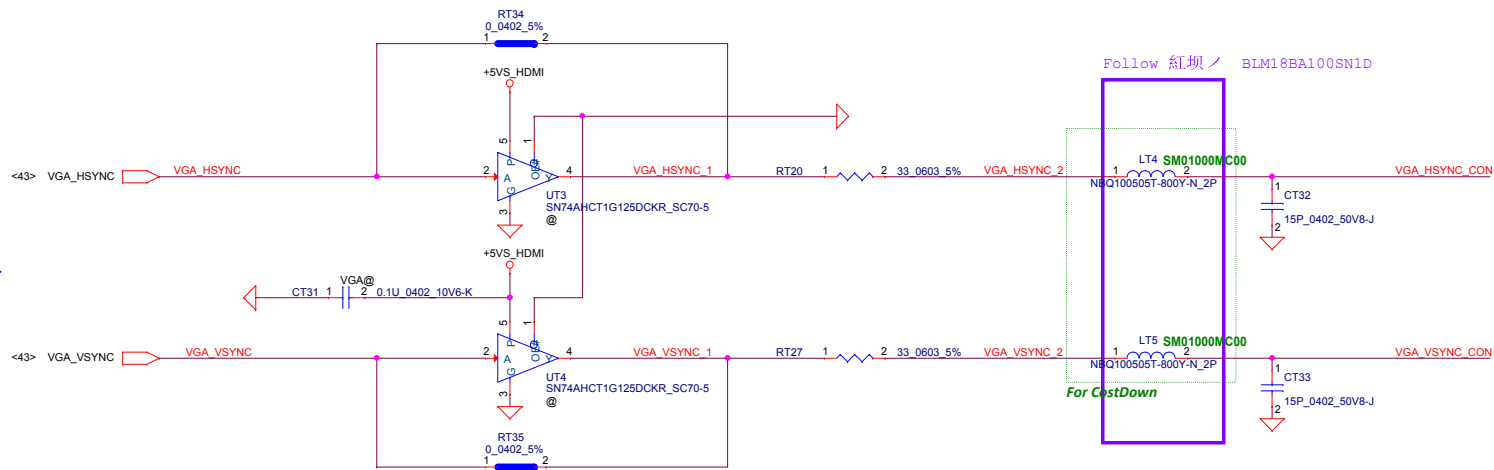
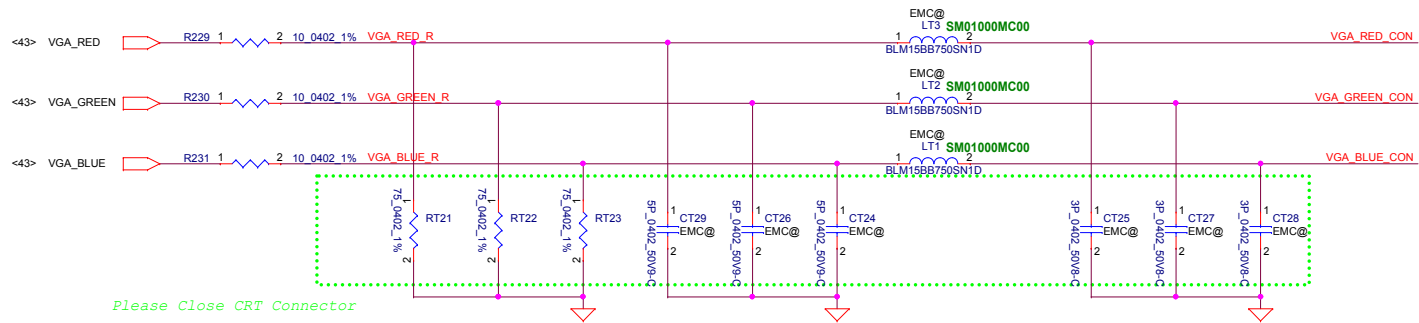
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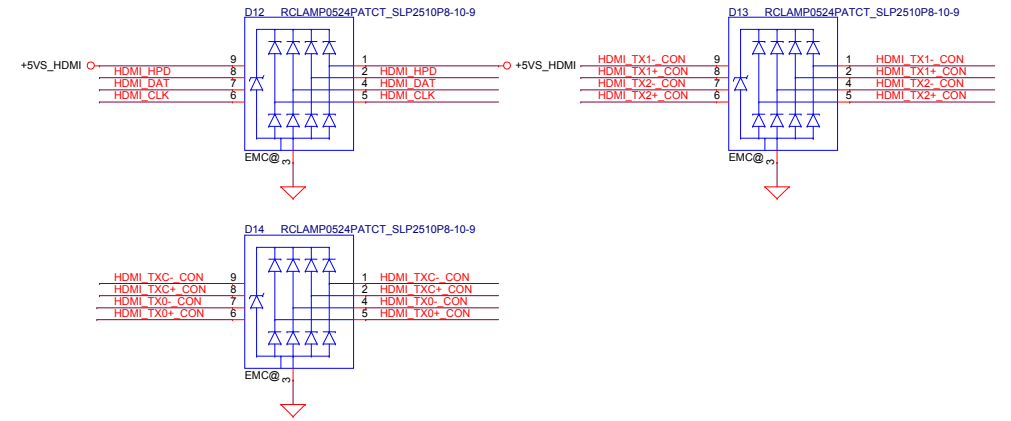
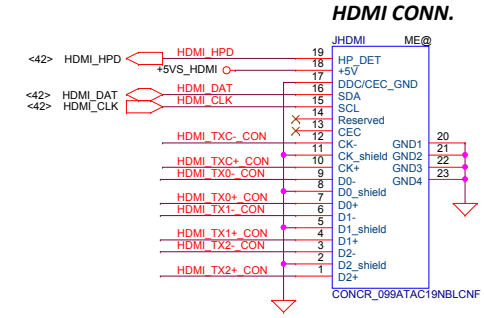
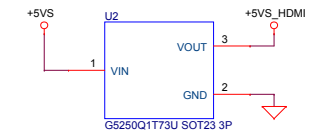
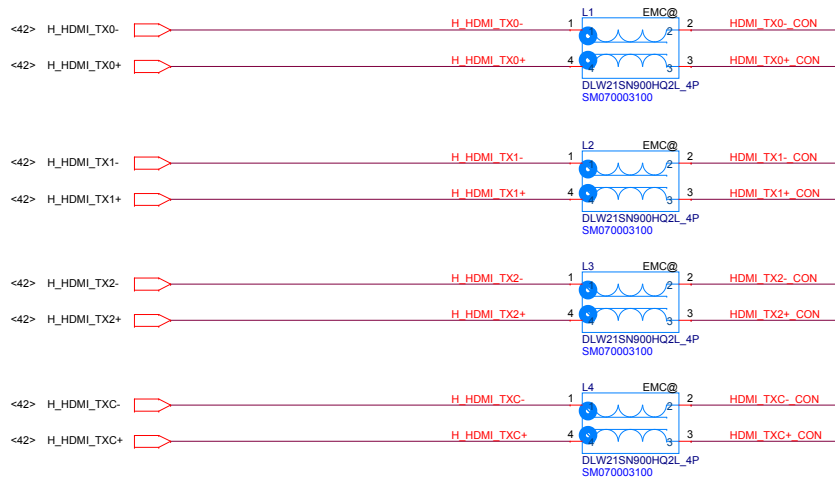
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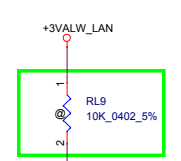
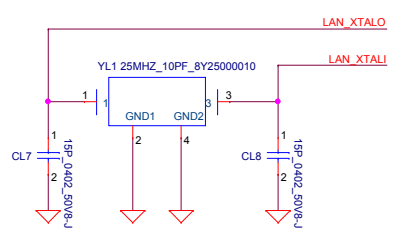
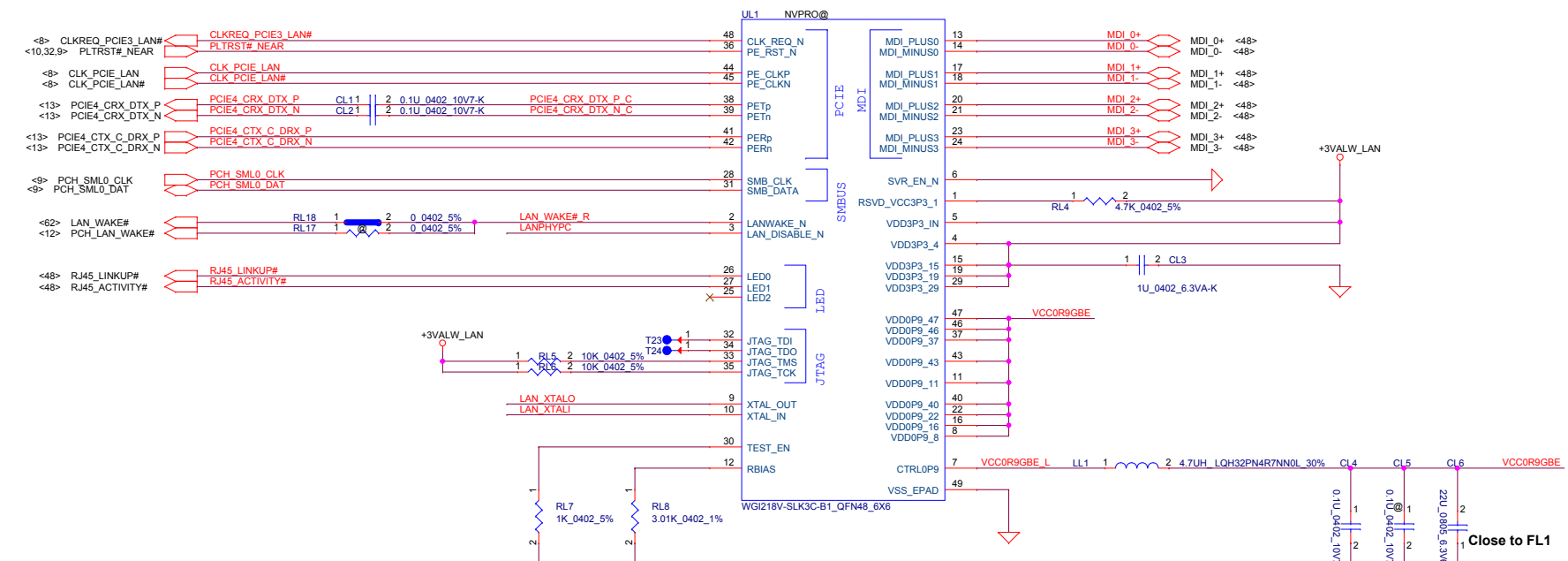
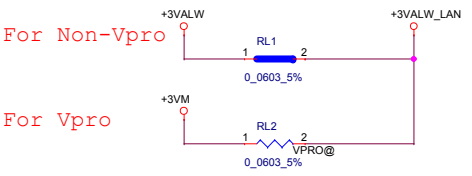
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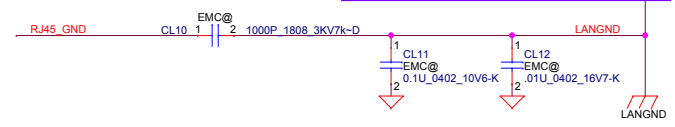
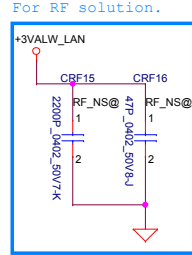
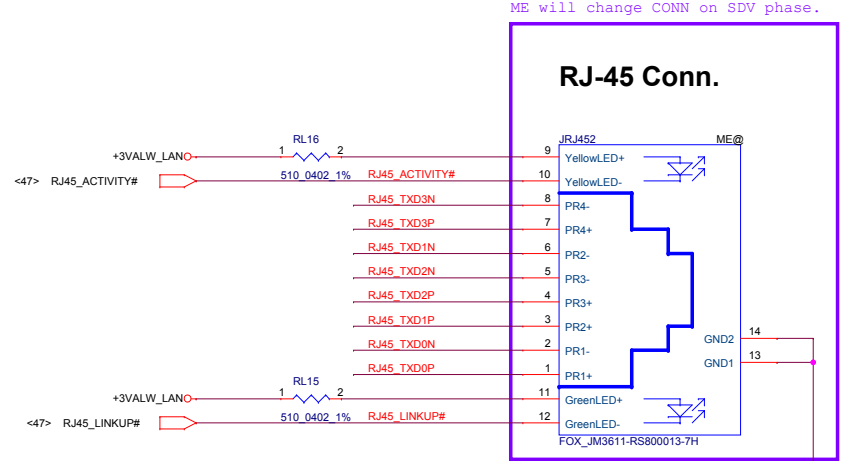
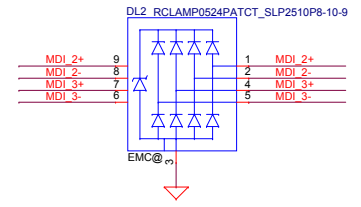
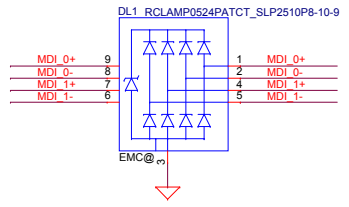
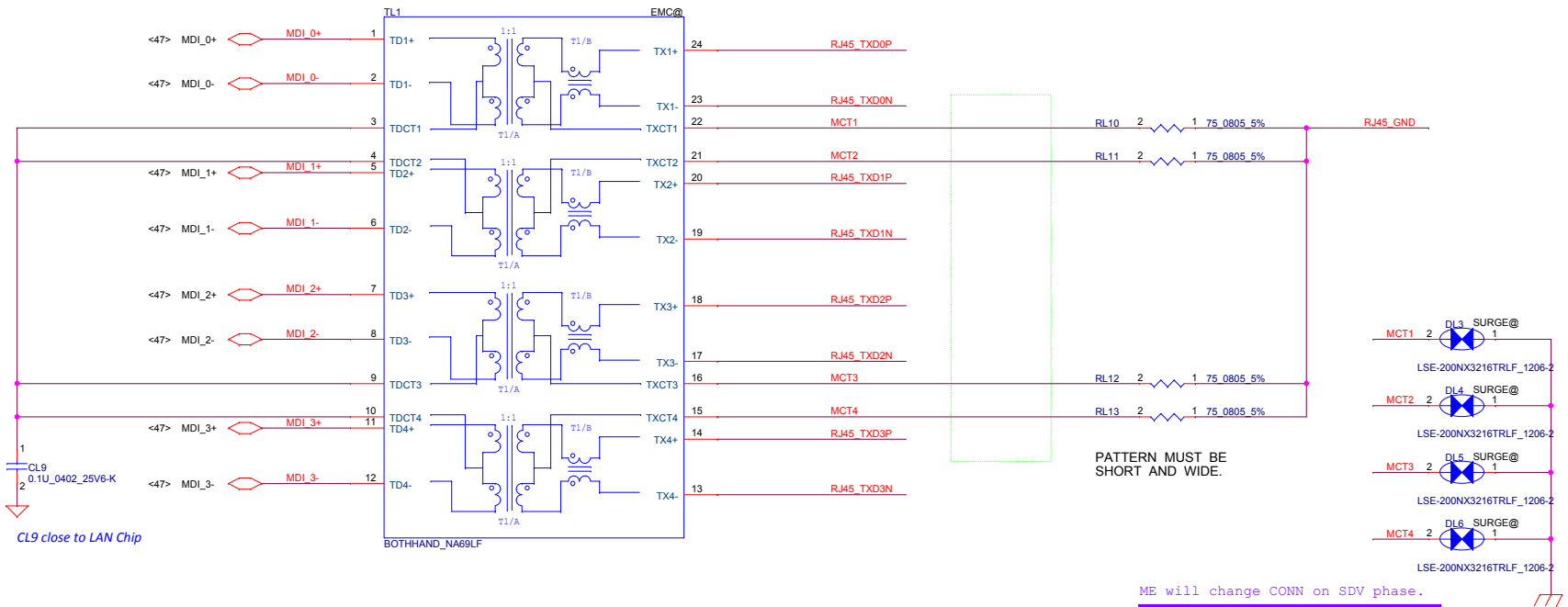


When use Native function, intel recommend pull high 10K ohm
 This part is un-mount in Sting.

UL1 GBE PHY

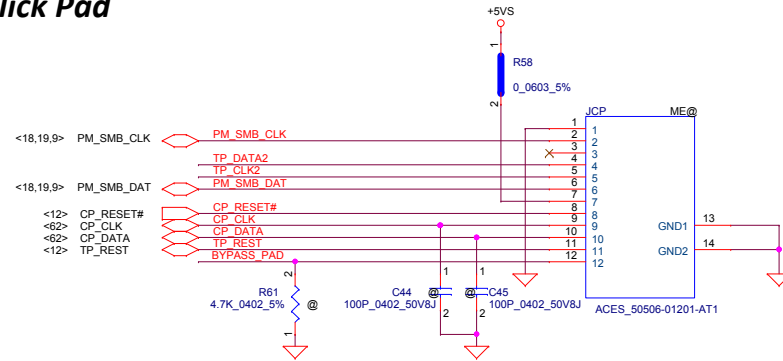
vPro Model	Non-vPro Model
I218LM	I218V

ST-1_SWG_SDV-SWG_EC062
 Add vPro/Non-vPro table.

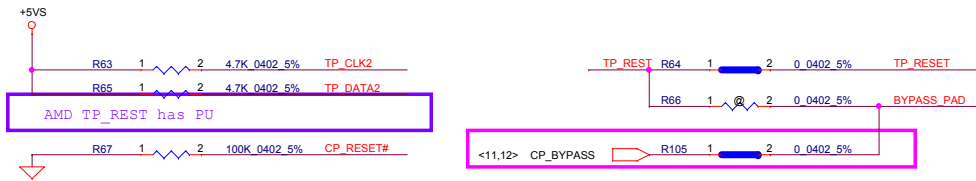
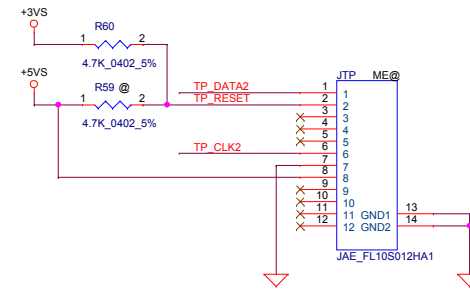


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Click Pad



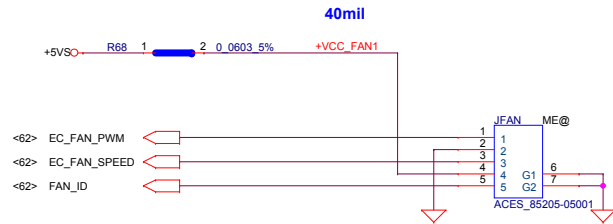
Track point



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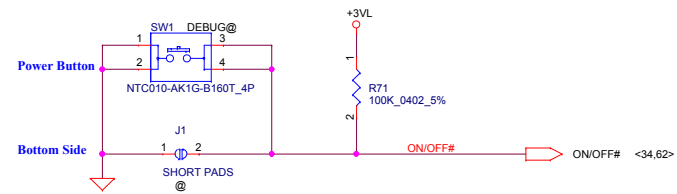
FAN CONN.



PWR BTN/LID SW CONN.

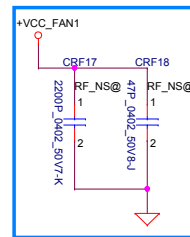
For 14" on board
For 15" on Sub/B

ON/OFF Switch --> 薄 'Sub/B

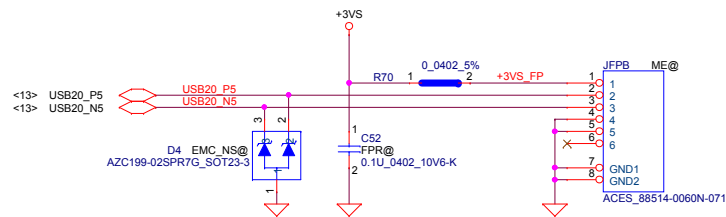


惠璣鐵AMD鐵THERMAL絨板PIN define

For RF solution.

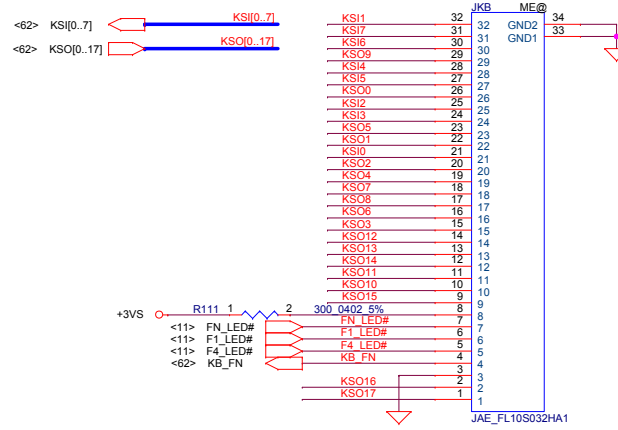


FingerPrint CONN.

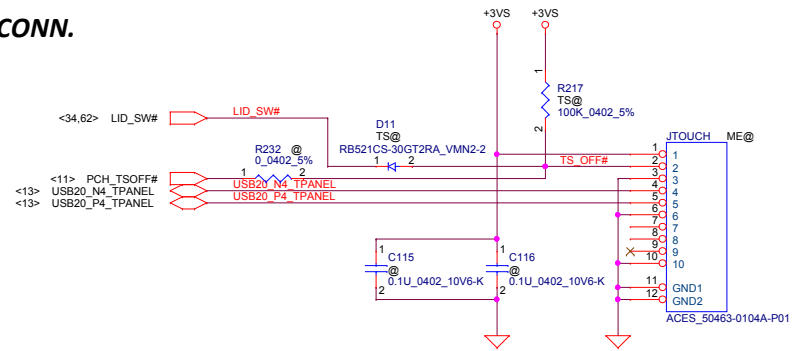


Lid Switch --> 薄 'Sub/B

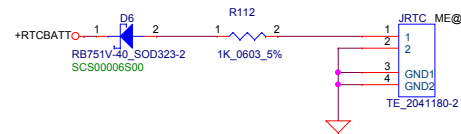
KB CONN




TOUCH PANEL CONN.

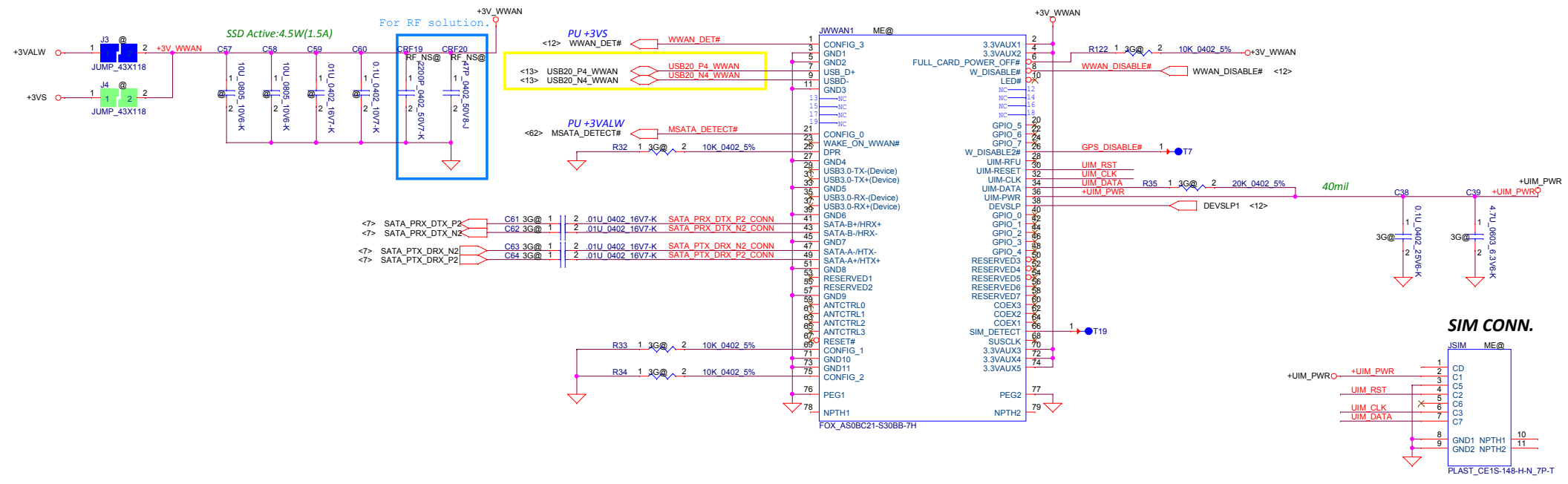


RTC CONN.

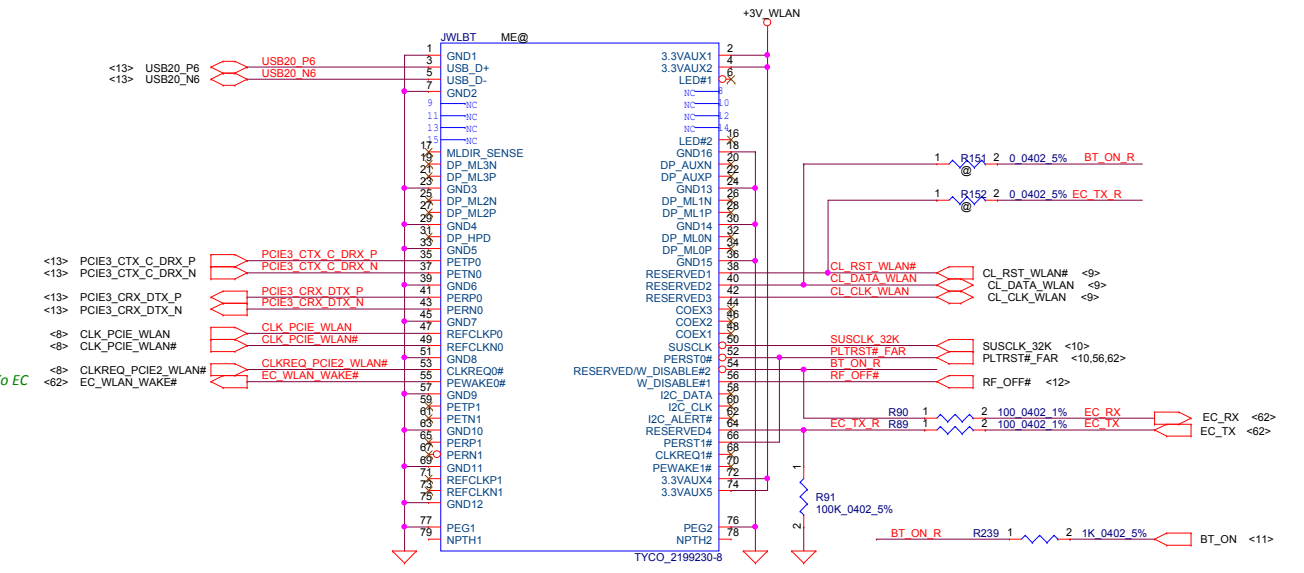
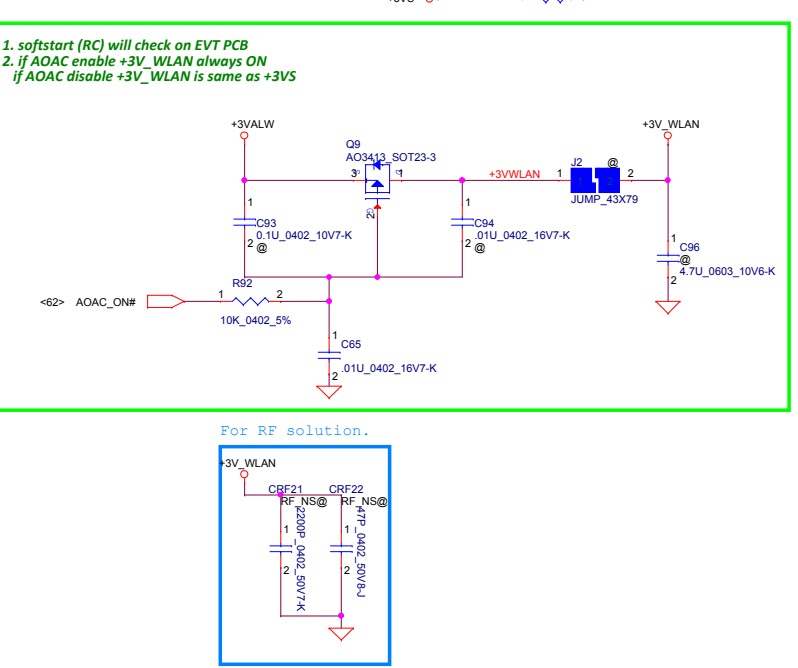


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TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR




TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR

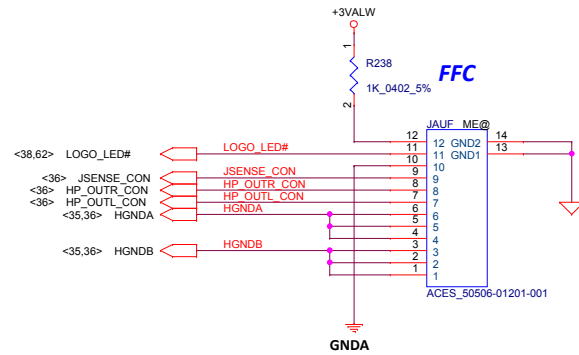



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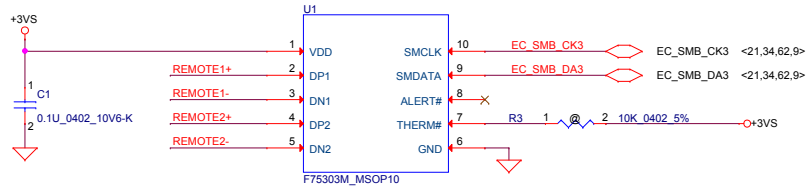
For Edge 15" Audio board CONNECTOR



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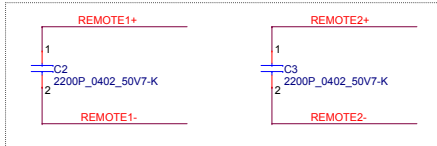
Thermal Sensor

**Thermal Sensor
placed near by VRAM**

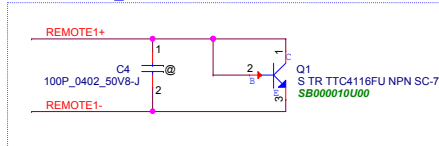


Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

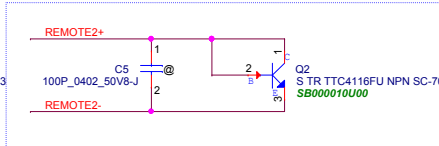
Close to U1



Close to +VCC_CORE



Close JDIMM1&JDIMM2



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

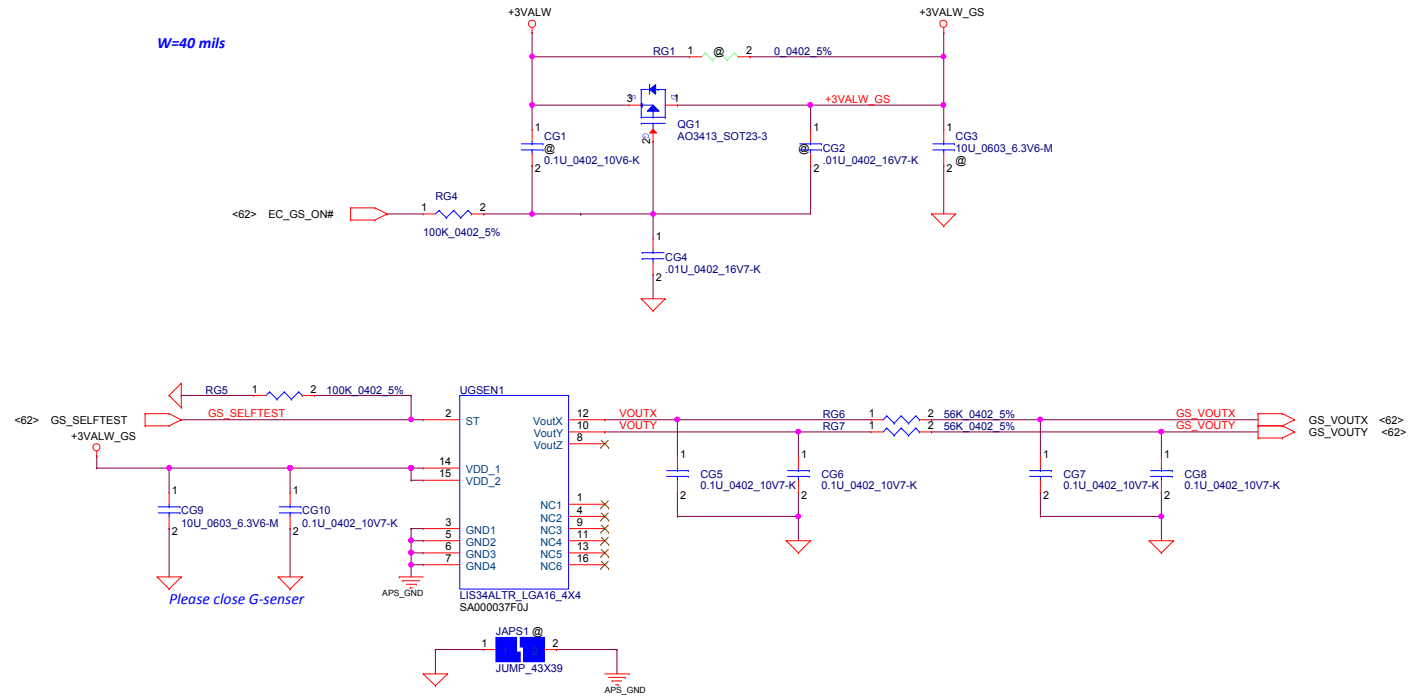
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				Custom	1.0
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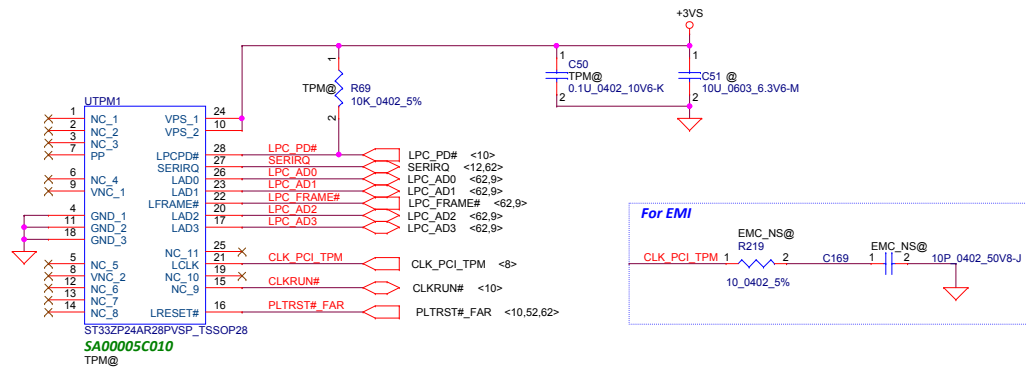
AITE1 NM-A221

APS G-Sensor

W=40 mils




TPM IC




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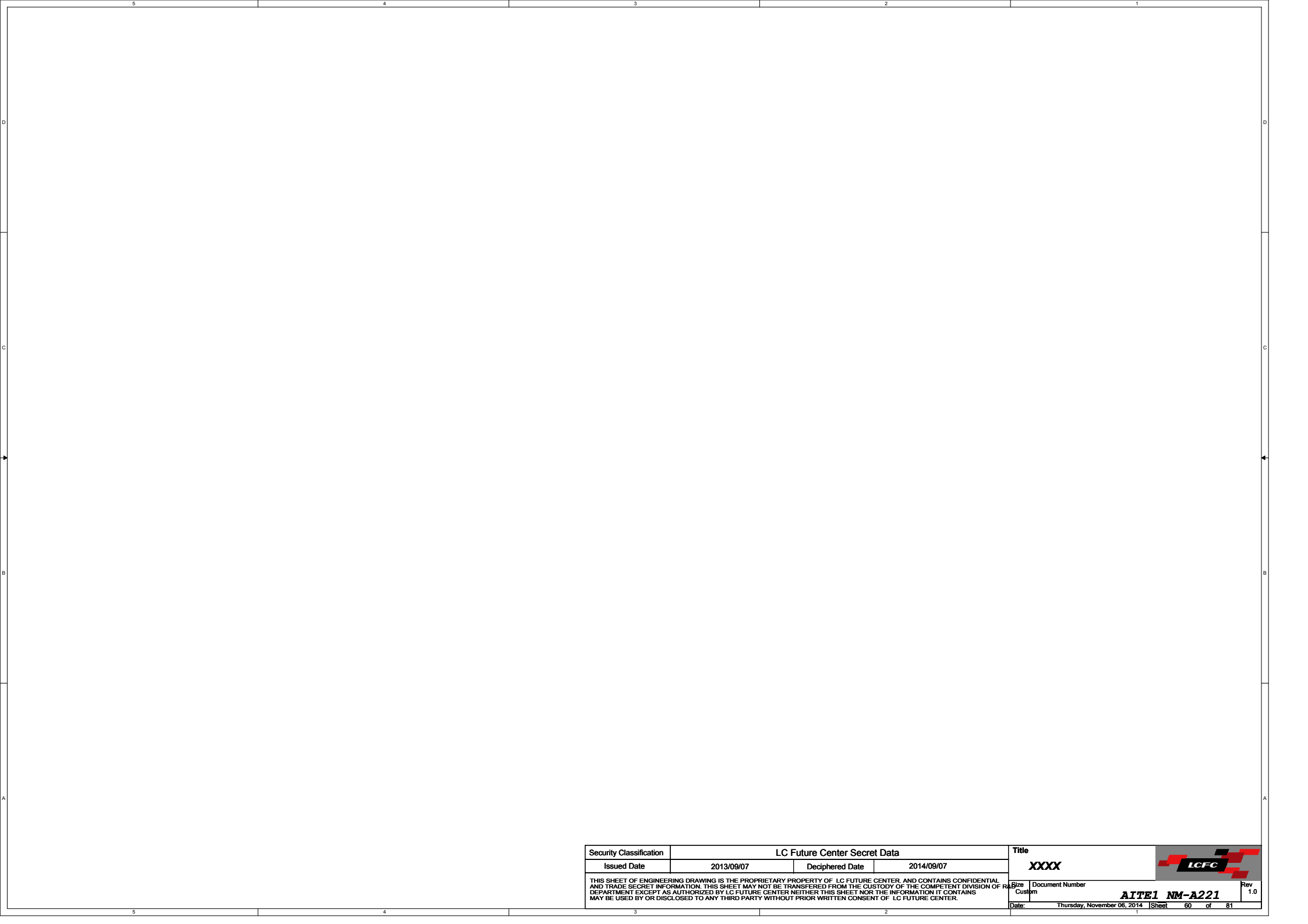
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					Custom	AITE1 NM-A221	1.0
					Date:	Thursday, November 06, 2014	Sheet 58 of 81

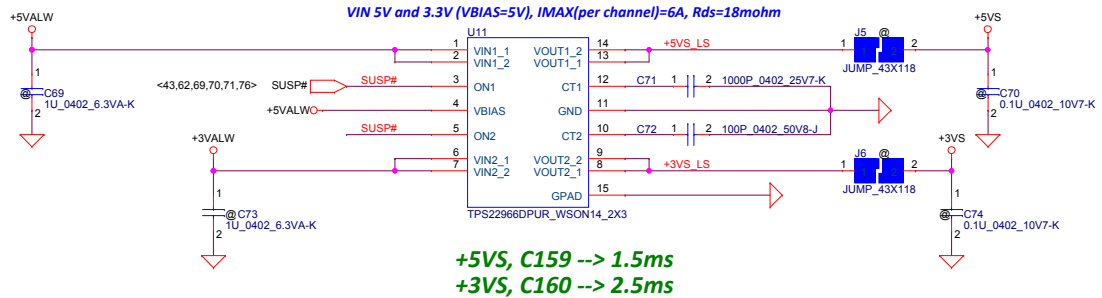
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				Size	Document Number	Rev
				Custom	AITE1 NM-A221	1.0
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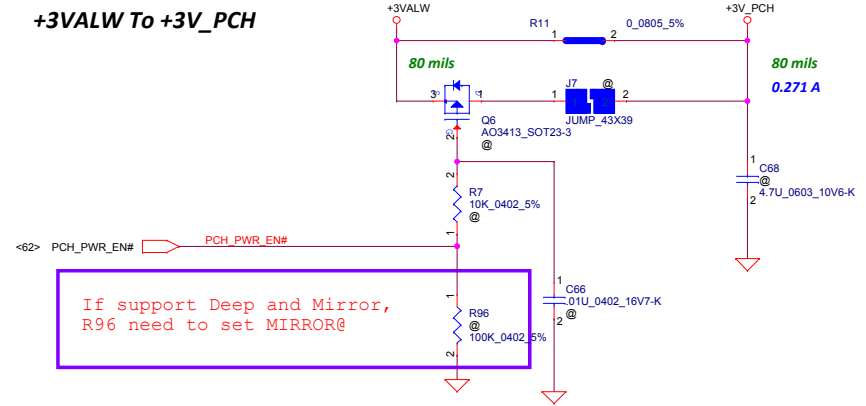


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				<small>Date:</small> Thursday, November 08, 2014	<small>Sheet</small> 60	<small>of</small> 81

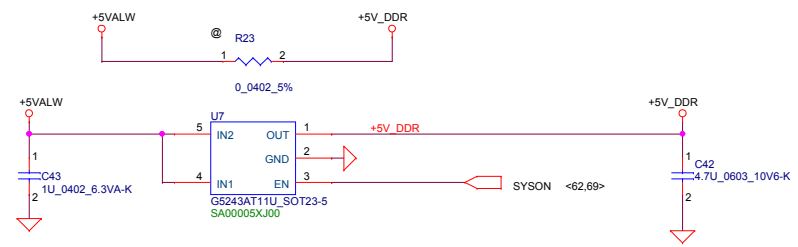
Load Switch
+5VALW To +5VS
+3VALW To +3VS



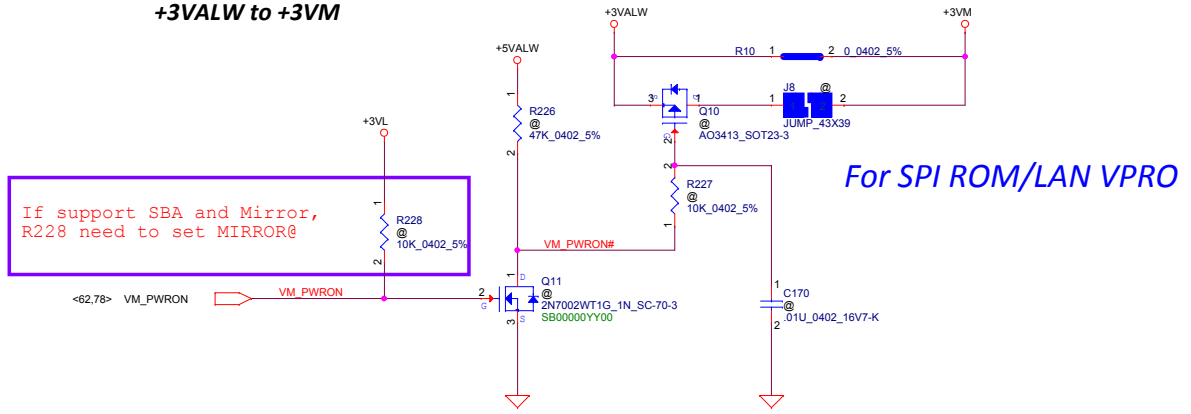
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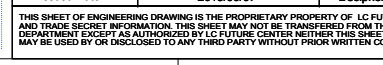
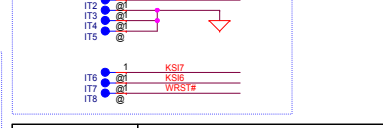
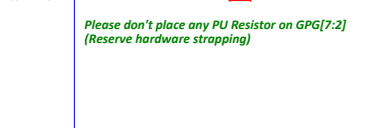
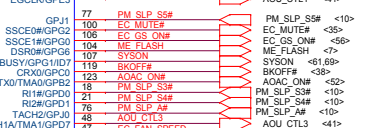
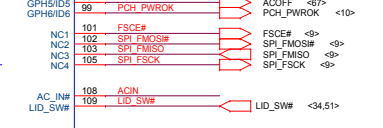
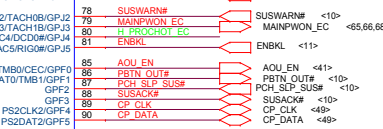
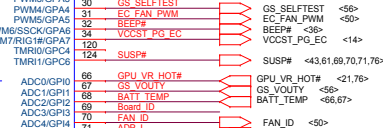
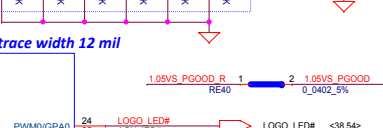
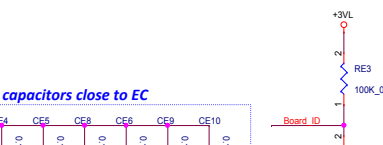
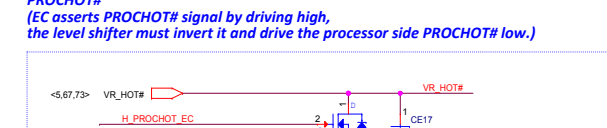
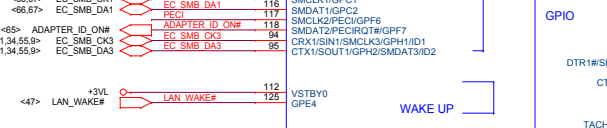
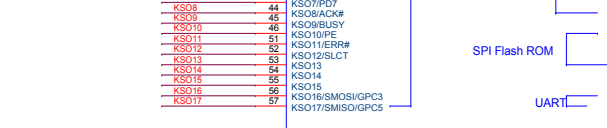
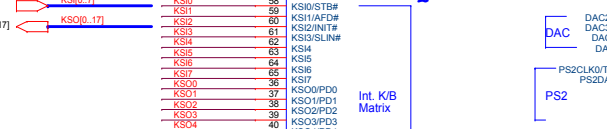
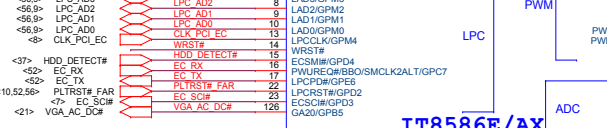
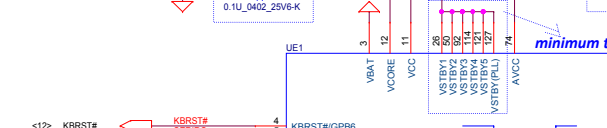
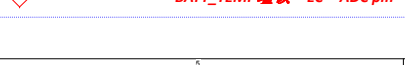
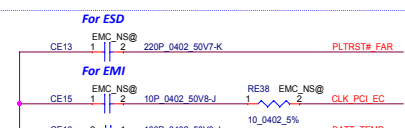
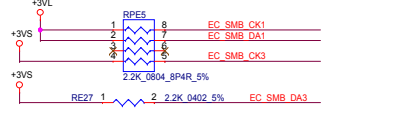
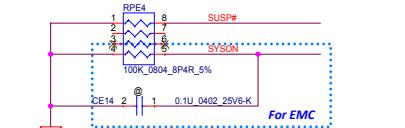
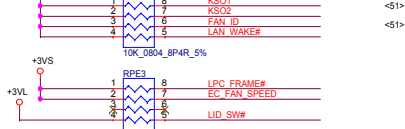
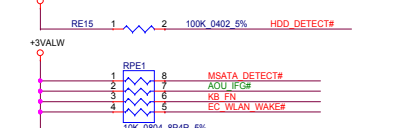
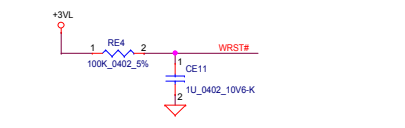
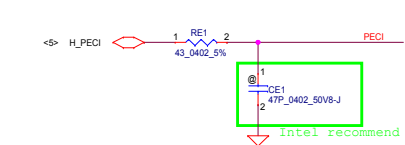
+5VALW To +5V_DDR



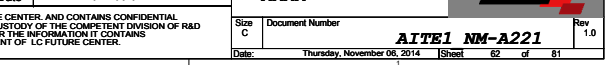
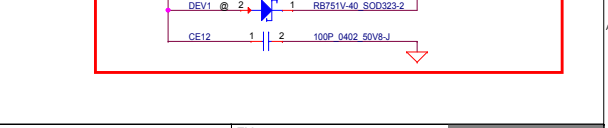
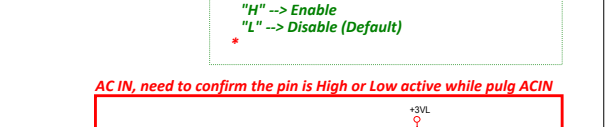
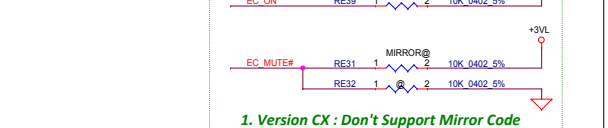
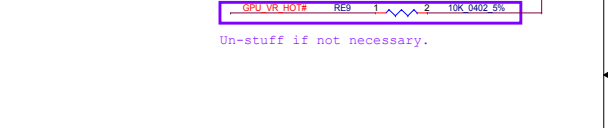
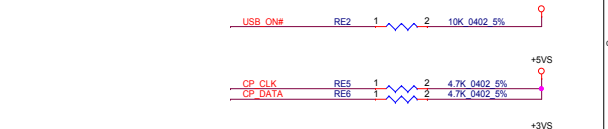
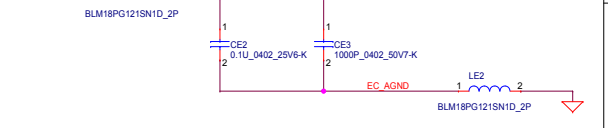
+3VALW to +3VM



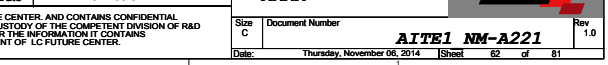
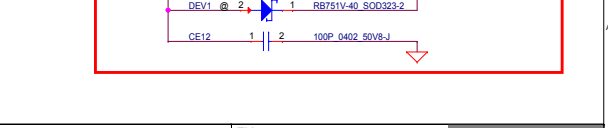
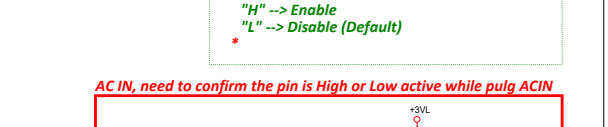
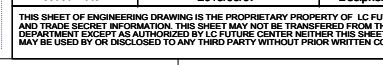
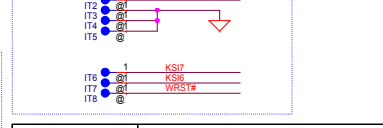
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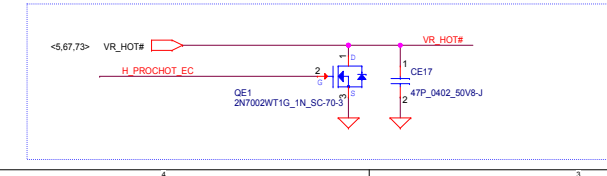
Board ID	RE7	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	Pre-SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SVT
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



Pin	Signal	Component	Value
1	KBRST#	RE1	43.0402_5%
2	WRST#	RE4	100K_0402_5%
3	HDD_DETECT#	RE15	100K_0402_5%
4	MSATA_DETECT#	RPE1	10K_0804_8P4R_5%
5	LAN_WAKE#	RPE2	10K_0804_8P4R_5%
6	LPC_FRAME#	RPE3	10K_0804_8P4R_5%
7	EC_FAN_SPEED	RPE4	10K_0804_8P4R_5%
8	LID_SW#	RPE5	10K_0804_8P4R_5%
9	EC_SMB_CK1	RPE6	10K_0804_8P4R_5%
10	EC_SMB_DAT1	RPE6	10K_0804_8P4R_5%
11	EC_SMB_CK3	RPE6	10K_0804_8P4R_5%
12	EC_SMB_DAT3	RPE6	10K_0804_8P4R_5%
13	LAN_WAKE#	RE27	2.2K_0402_5%
14	USB_ON#	RE2	10K_0402_5%
15	MSATA_DETECT#	RE3	10K_0402_5%
16	EC_WAKE#	RE3	10K_0402_5%
17	AC_PRESENT	RE4	10K_0402_5%
18	BATT_TEMP	RE3	10K_0402_5%
19	EC_ADC pin	RE3	10K_0402_5%
20	H_PECI	RE1	43.0402_5%
21	VR_HOT#	RE11	100P_0402_50V8-J
22	H_PROCHOT_EC	RE11	100P_0402_50V8-J
23	EC_WAKE#	RE3	10K_0402_5%
24	AC_PRESENT	RE4	10K_0402_5%
25	BATT_TEMP	RE3	10K_0402_5%
26	EC_ADC pin	RE3	10K_0402_5%
27	VR_HOT#	RE11	100P_0402_50V8-J
28	H_PROCHOT_EC	RE11	100P_0402_50V8-J
29	EC_WAKE#	RE3	10K_0402_5%
30	AC_PRESENT	RE4	10K_0402_5%
31	BATT_TEMP	RE3	10K_0402_5%
32	EC_ADC pin	RE3	10K_0402_5%
33	VR_HOT#	RE11	100P_0402_50V8-J
34	H_PROCHOT_EC	RE11	100P_0402_50V8-J
35	EC_WAKE#	RE3	10K_0402_5%
36	AC_PRESENT	RE4	10K_0402_5%
37	BATT_TEMP	RE3	10K_0402_5%
38	EC_ADC pin	RE3	10K_0402_5%
39	VR_HOT#	RE11	100P_0402_50V8-J
40	H_PROCHOT_EC	RE11	100P_0402_50V8-J
41	EC_WAKE#	RE3	10K_0402_5%
42	AC_PRESENT	RE4	10K_0402_5%
43	BATT_TEMP	RE3	10K_0402_5%
44	EC_ADC pin	RE3	10K_0402_5%
45	VR_HOT#	RE11	100P_0402_50V8-J
46	H_PROCHOT_EC	RE11	100P_0402_50V8-J
47	EC_WAKE#	RE3	10K_0402_5%
48	AC_PRESENT	RE4	10K_0402_5%
49	BATT_TEMP	RE3	10K_0402_5%
50	EC_ADC pin	RE3	10K_0402_5%
51	VR_HOT#	RE11	100P_0402_50V8-J
52	H_PROCHOT_EC	RE11	100P_0402_50V8-J
53	EC_WAKE#	RE3	10K_0402_5%
54	AC_PRESENT	RE4	10K_0402_5%
55	BATT_TEMP	RE3	10K_0402_5%
56	EC_ADC pin	RE3	10K_0402_5%
57	VR_HOT#	RE11	100P_0402_50V8-J
58	H_PROCHOT_EC	RE11	100P_0402_50V8-J
59	EC_WAKE#	RE3	10K_0402_5%
60	AC_PRESENT	RE4	10K_0402_5%
61	BATT_TEMP	RE3	10K_0402_5%
62	EC_ADC pin	RE3	10K_0402_5%
63	VR_HOT#	RE11	100P_0402_50V8-J
64	H_PROCHOT_EC	RE11	100P_0402_50V8-J
65	EC_WAKE#	RE3	10K_0402_5%
66	AC_PRESENT	RE4	10K_0402_5%
67	BATT_TEMP	RE3	10K_0402_5%
68	EC_ADC pin	RE3	10K_0402_5%
69	VR_HOT#	RE11	100P_0402_50V8-J
70	H_PROCHOT_EC	RE11	100P_0402_50V8-J
71	EC_WAKE#	RE3	10K_0402_5%
72	AC_PRESENT	RE4	10K_0402_5%
73	BATT_TEMP	RE3	10K_0402_5%
74	EC_ADC pin	RE3	10K_0402_5%
75	VR_HOT#	RE11	100P_0402_50V8-J
76	H_PROCHOT_EC	RE11	100P_0402_50V8-J
77	EC_WAKE#	RE3	10K_0402_5%
78	AC_PRESENT	RE4	10K_0402_5%
79	BATT_TEMP	RE3	10K_0402_5%
80	EC_ADC pin	RE3	10K_0402_5%
81	VR_HOT#	RE11	100P_0402_50V8-J
82	H_PROCHOT_EC	RE11	100P_0402_50V8-J
83	EC_WAKE#	RE3	10K_0402_5%
84	AC_PRESENT	RE4	10K_0402_5%
85	BATT_TEMP	RE3	10K_0402_5%
86	EC_ADC pin	RE3	10K_0402_5%
87	VR_HOT#	RE11	100P_0402_50V8-J
88	H_PROCHOT_EC	RE11	100P_0402_50V8-J
89	EC_WAKE#	RE3	10K_0402_5%
90	AC_PRESENT	RE4	10K_0402_5%
91	BATT_TEMP	RE3	10K_0402_5%
92	EC_ADC pin	RE3	10K_0402_5%
93	VR_HOT#	RE11	100P_0402_50V8-J
94	H_PROCHOT_EC	RE11	100P_0402_50V8-J
95	EC_WAKE#	RE3	10K_0402_5%
96	AC_PRESENT	RE4	10K_0402_5%
97	BATT_TEMP	RE3	10K_0402_5%
98	EC_ADC pin	RE3	10K_0402_5%
99	VR_HOT#	RE11	100P_0402_50V8-J
100	H_PROCHOT_EC	RE11	100P_0402_50V8-J



PROCHOT#
 (EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)



Please don't place any PU Resistor on GPIO[7:2]
 (Reserve hardware strapping)

1. Version CX : Don't Support Mirror Code
 Version DX/EX/FX : Support Mirror Code
 "H" --> Enable
 "L" --> Disable (Default)

AC IN, need to confirm the pin is High or Low active while pulg ACIN

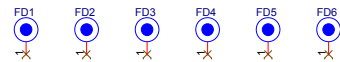
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Screw Hole




Center Zero

PCB Fedcal Mark PAD

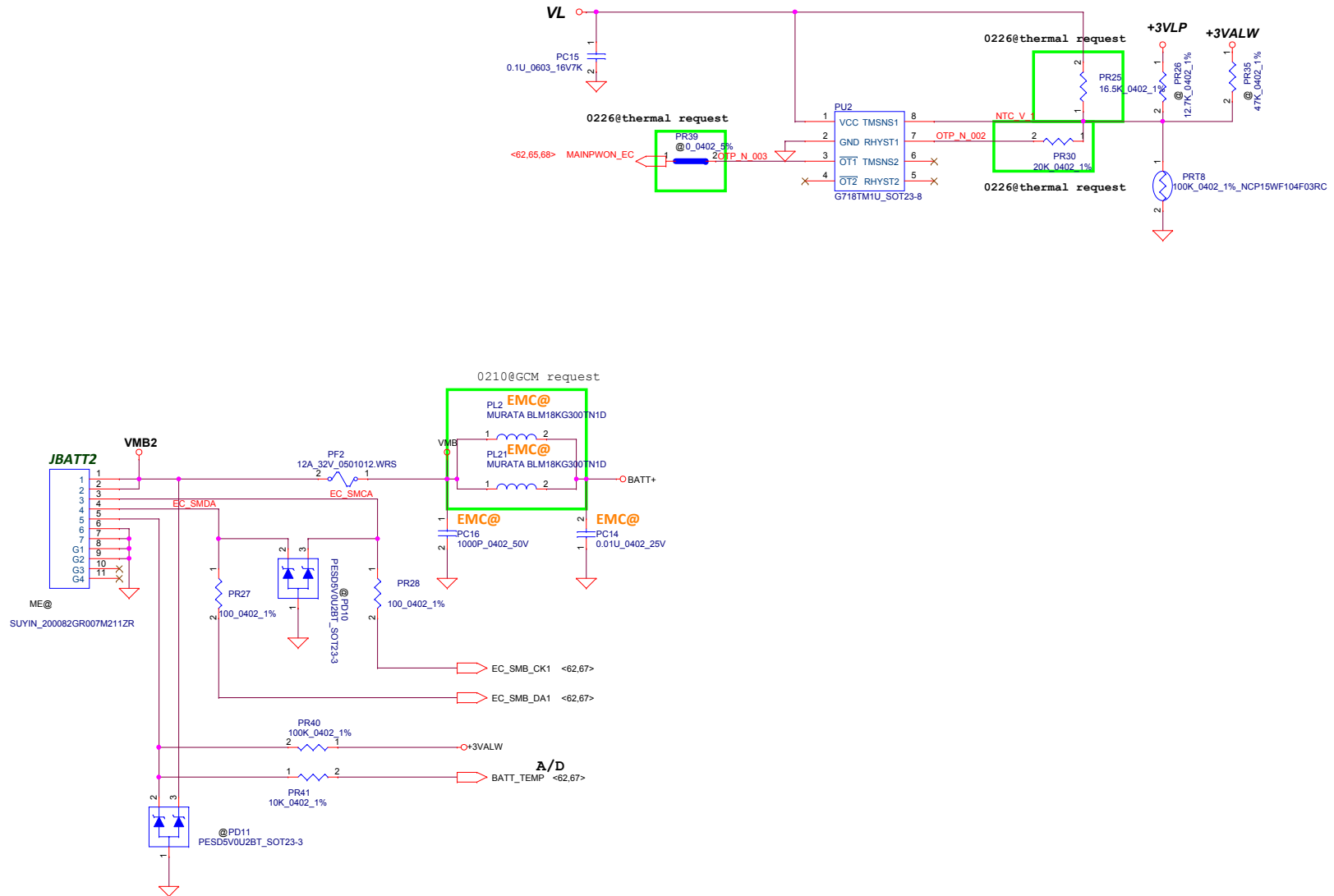


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				<small>Date:</small> Thursday, November 08, 2014	<small>Sheet</small> 63 <small>of</small> 81

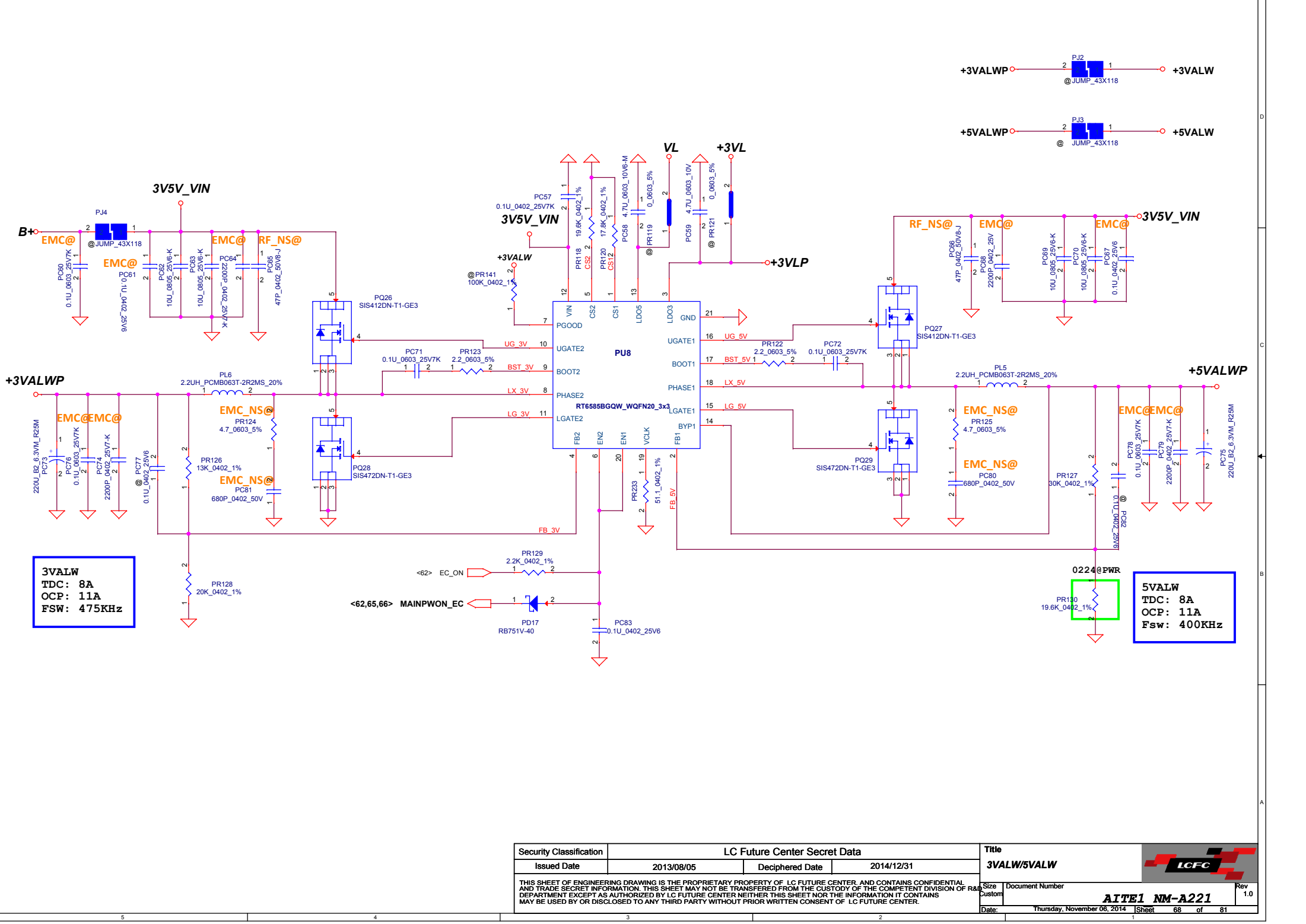
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PRT8 under CPU bottom side :
 CPU thermal protection at 93 +/-3 degree C
 Recovery at 56 +/-3 degree C




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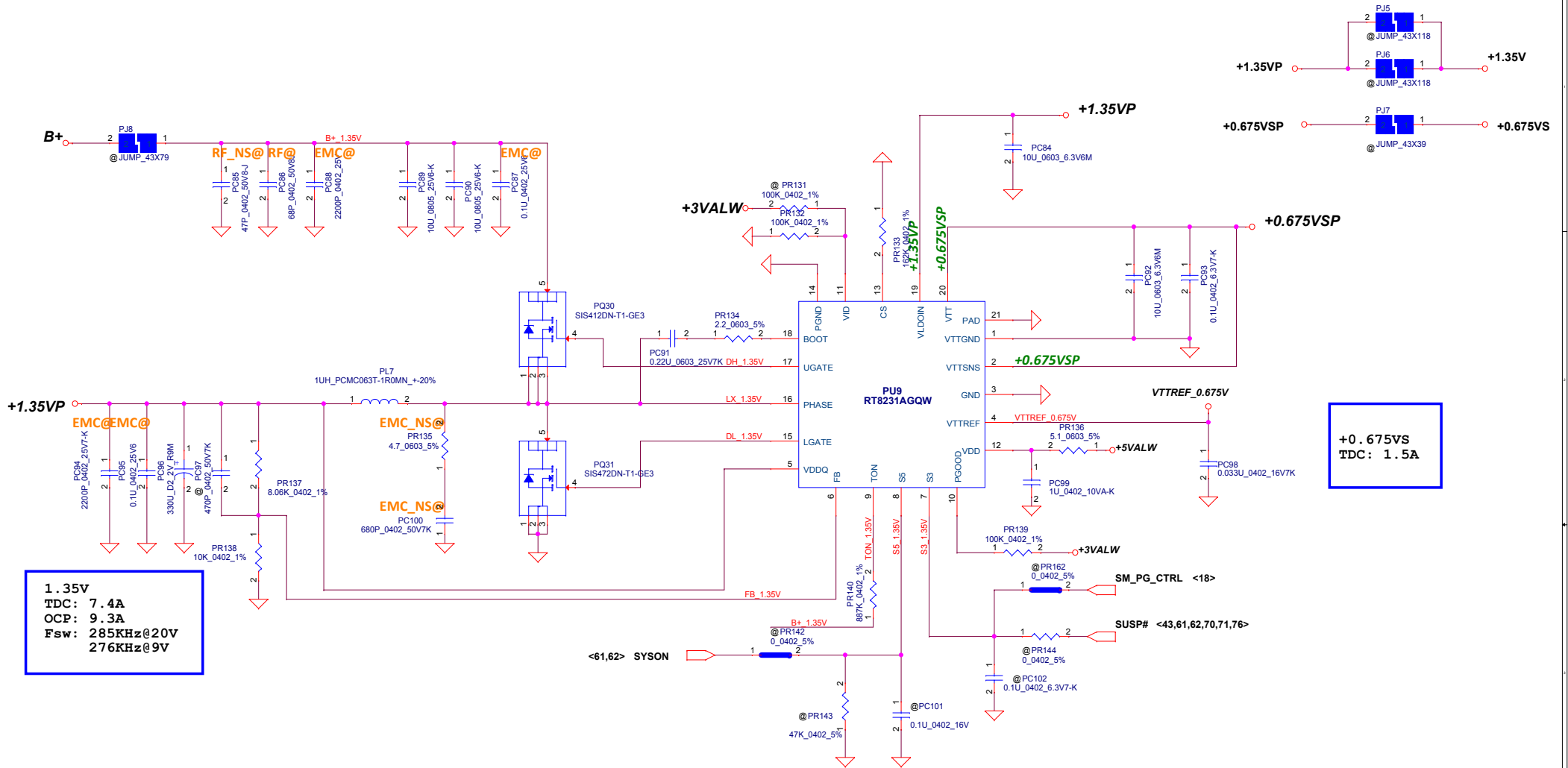


3VALW
 TDC: 8A
 OCP: 11A
 FSW: 475KHz

5VALW
 TDC: 8A
 OCP: 11A
 Fsw: 400KHz

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Title		
3VALW/5VALW		
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Custom		
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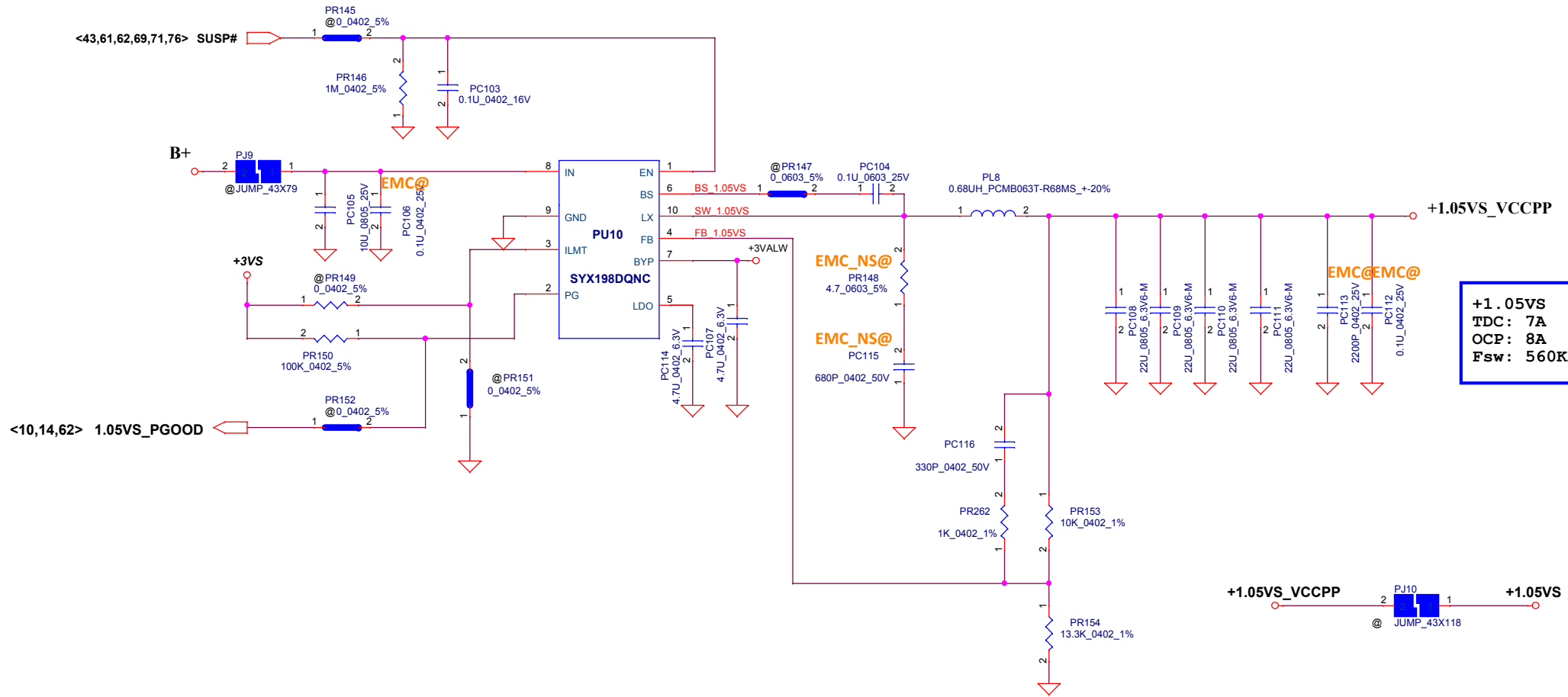


1.35V
TDC: 7.4A
OCP: 9.3A
Fsw: 285KHz@20V
276KHz@9V

+0.675VS
TDC: 1.5A

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+1.35V/+0.675VS		Size Custom	Document Number
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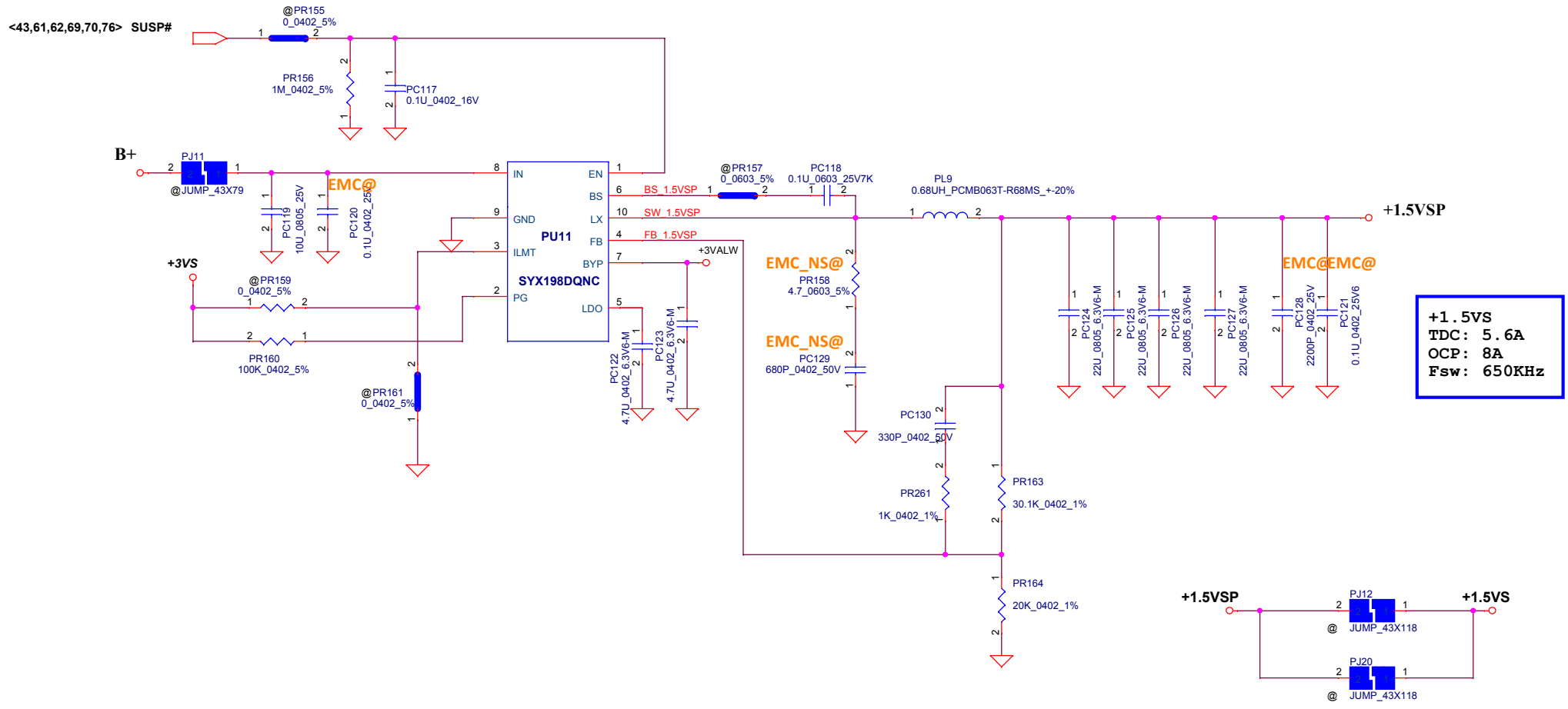


+1.05VS
TDC: 7A
OCP: 8A
Fsw: 560KHz


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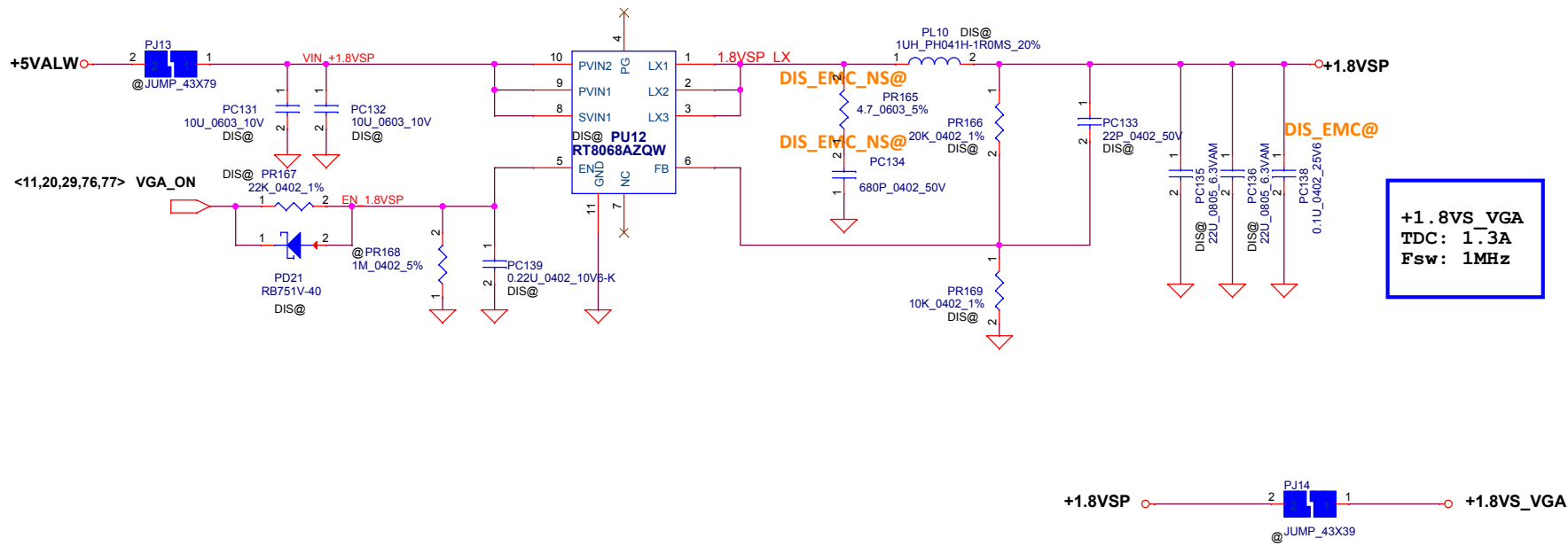
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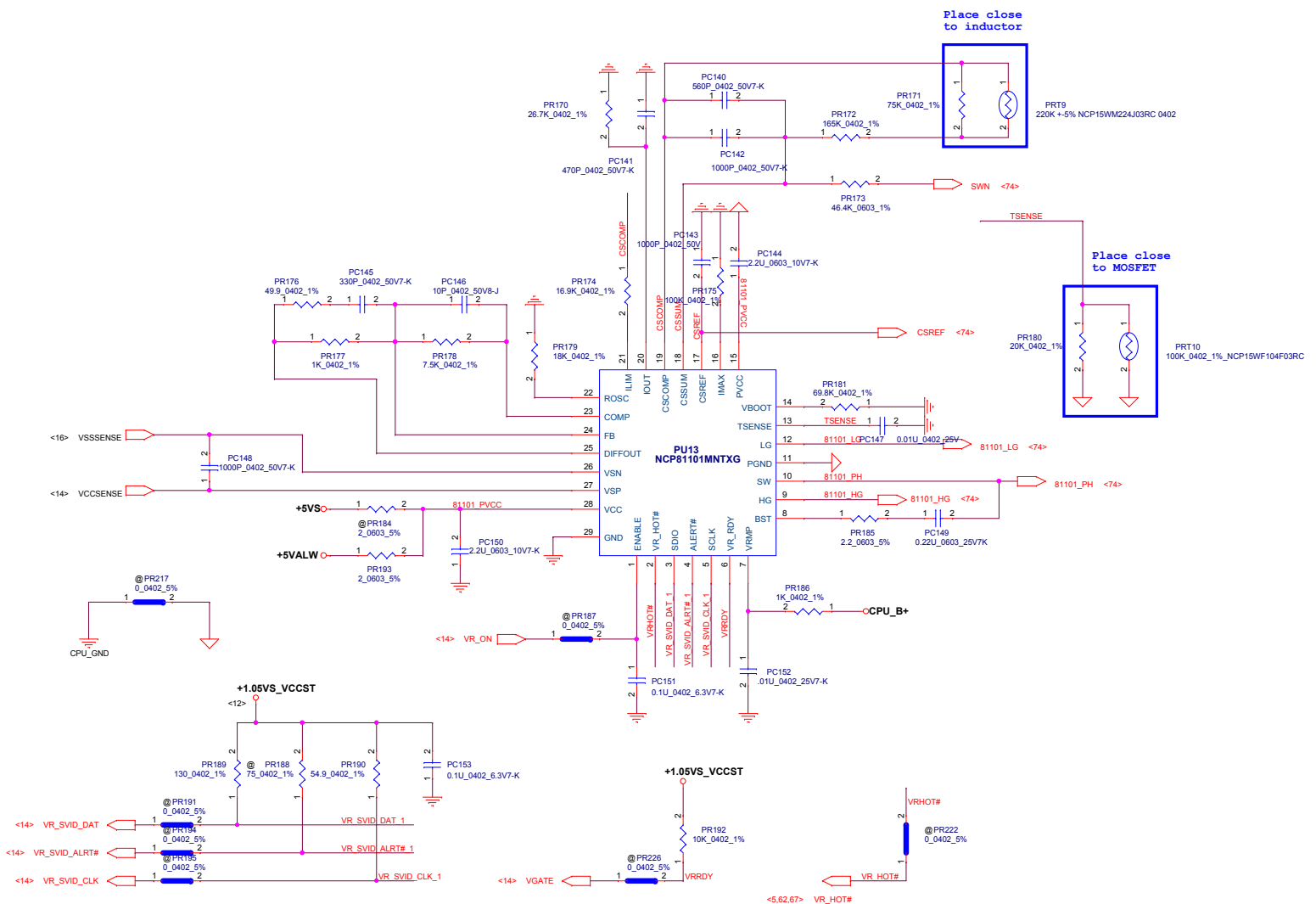


+1.5VS
TDC: 5.6A
OCP: 8A
Fsw: 650KHz

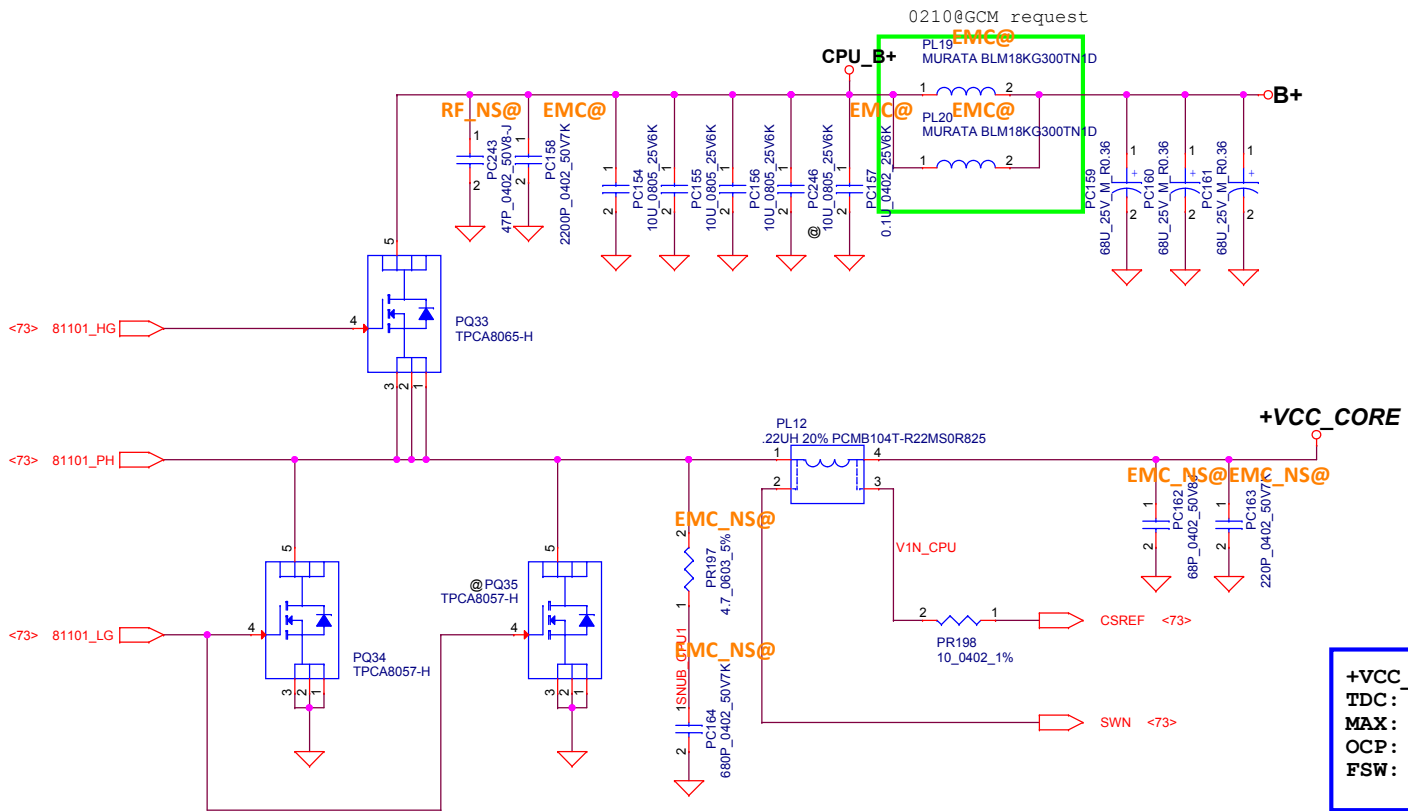
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+VCC_CORE
TDC: 10A
MAX: 32A
OCP: 42A
FSW: 560KHz@20V
670KHz@9V

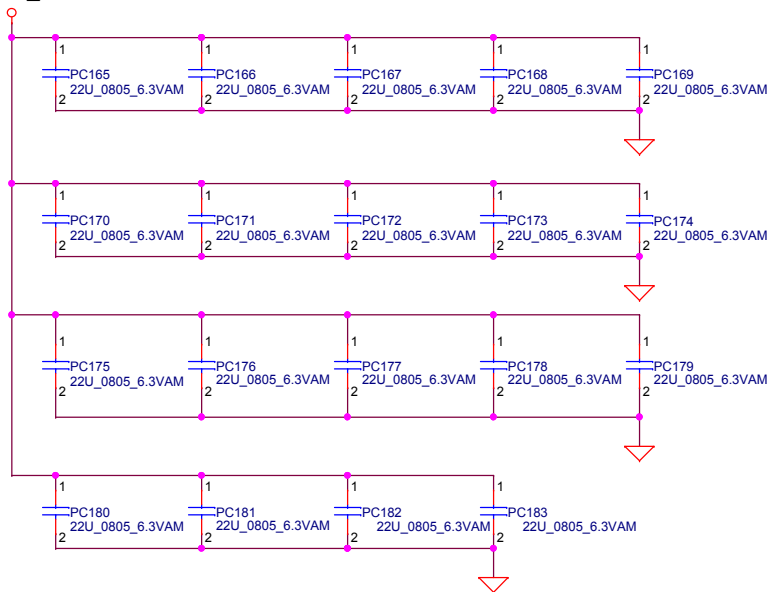
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Title	+CPU_CORE2	
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Based on PDDG rev 0.7 Table 5-1.

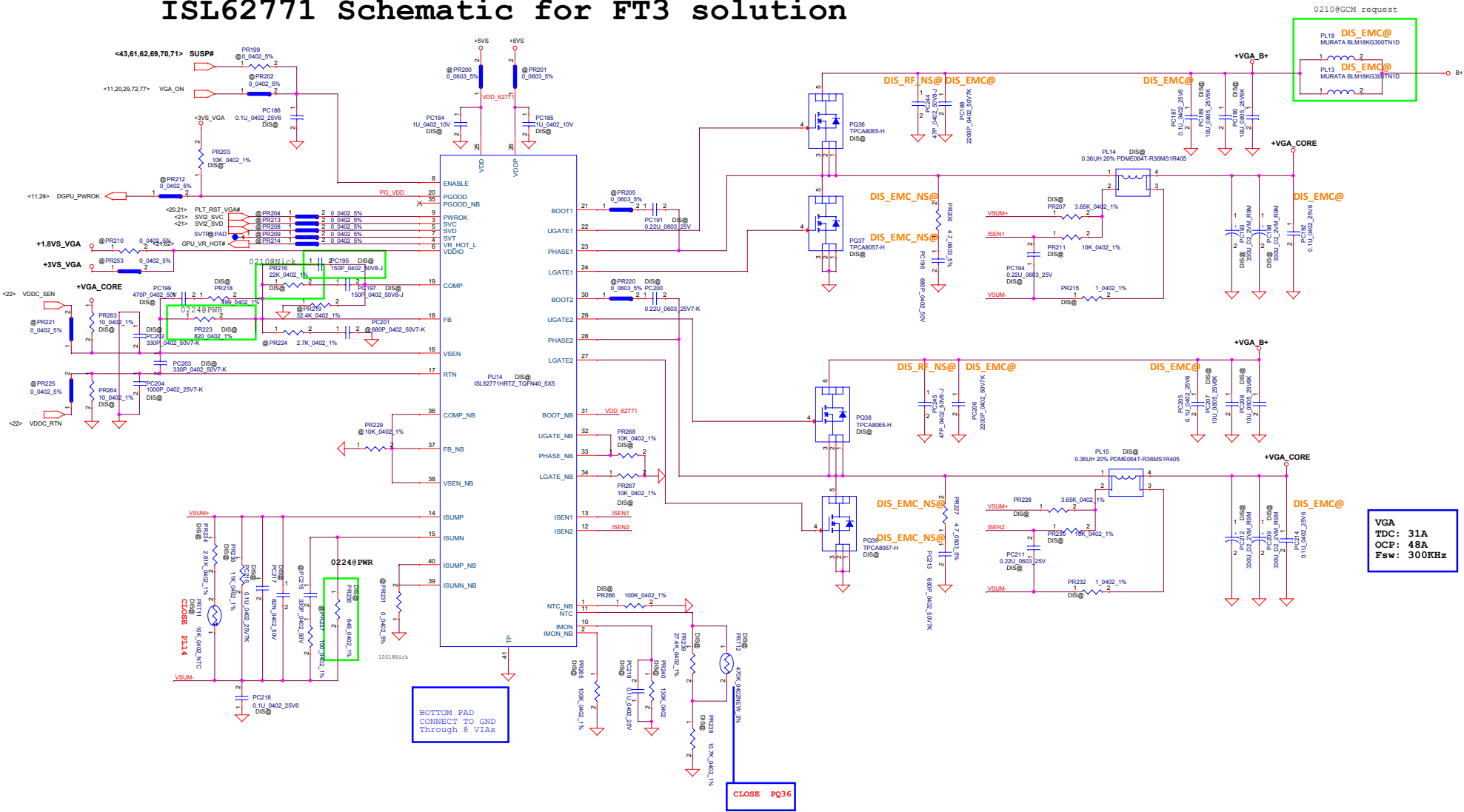
+VCC_CORE



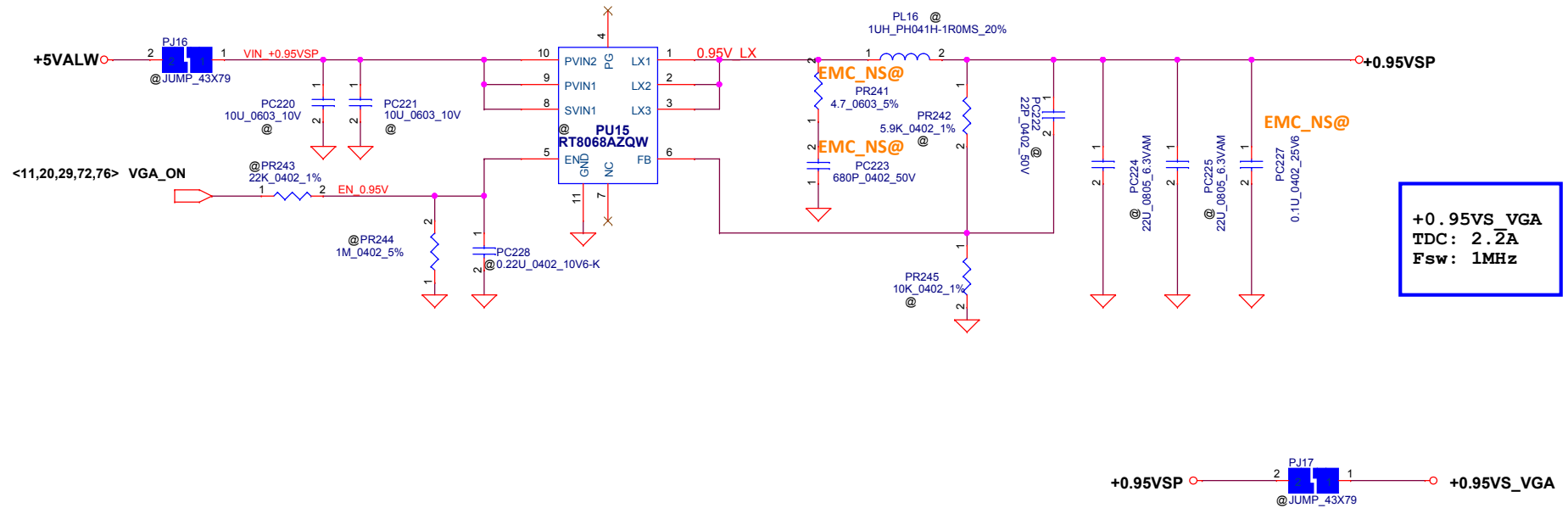
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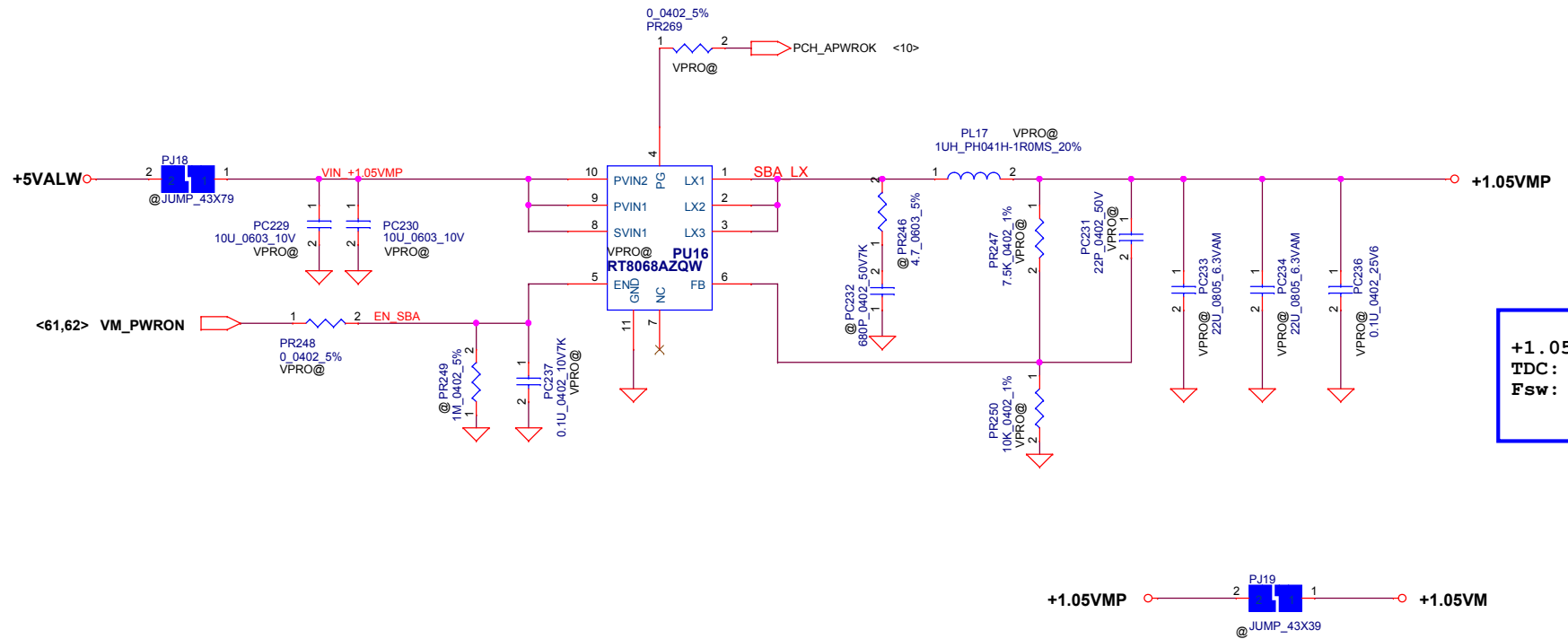
ISL62771 Schematic for FT3 solution




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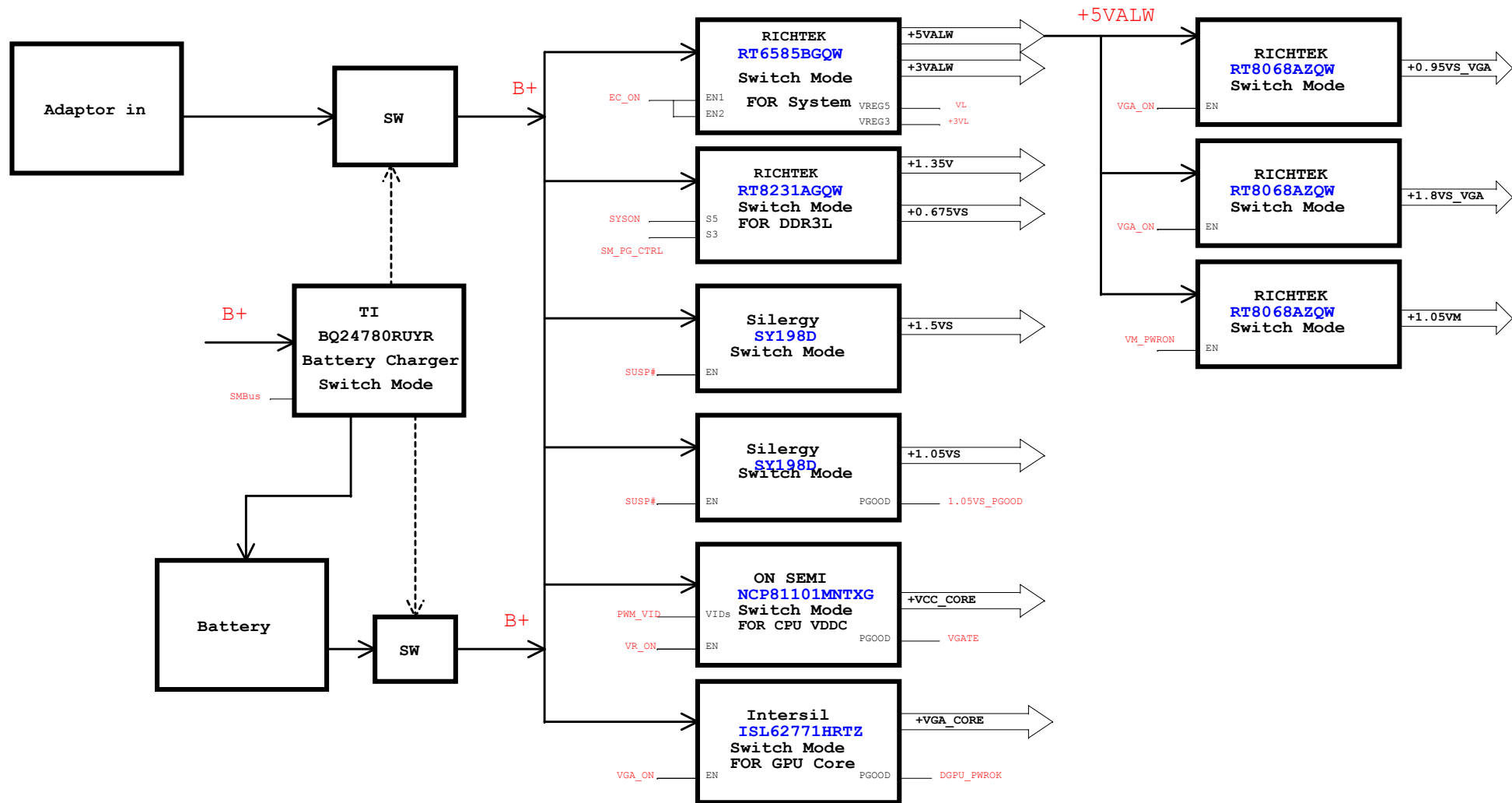
+1.05VMP
TDC: 1A
Fsw: 1MHz


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POWER PIR (Product Improve Record)

AIIE1 NM-A151 SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1
 GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE




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HW PIR (Product Improve Record)

AIVE1 NM-XXXX SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1
 GERBER-OUT DATE: 2013/10/15

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Gordon SDV LOGIC SCHEMATICS

NMA-221
VER 0.1
Nov/13/2013

1.COVER PAGE
2.BLOCK DIAGRAM
3.NOTE LIST
4.VGA NOTE
5.BDW_DDI/EDP/XDP
6.BDW_DDR3L INT
7.BDW_RTC/HDA/SATA/PCIe/JTAG
8.BDW_CLOCK/PM
9.BDW_LPC/SPI/SM BUS
10.BDW_SYS PM
11.BDW_eDP SBAND/DDPx
12.BDW_GPIO/SIO
13.BDW_PCIE/USB BUS
14.BDW (Power)
15.BDW (Power2)
16.BDW (VSS)
17.BDW (OTHER)
18.DDR3L DIMM1
19.DDR3L DIMM2
20.Opal & Jet PCIE
21.Opal & Jet GPIO
22.Opal & Jet Core Power
23.Opal & Jet DP Power/GND
24.Opal & Jet MEM Interface
25.Opal & Jet DDR3 VRAM U
26.Opal & Jet DDR3 VRAM L
27.Opal 22 TO 24 VRAM U2
28.Opal 23 TO 25 VRAM L2
29.Opal & Jet swich power
30.BLANK
31.BLANK
32.CARDREADER IC/CONN.
33.DP RP --> BLANK
34.DOCKING/ DCIN CONN
35.CX20751

36.HP/MIC JACK/Speaker
37.SATA HDD/ODD CONN.
38.eDP/CMOS CONN.
39.USB30 RP --> BLANK
40.USB3 PORT1-BACK
41.USB3 PORT2-FRONT(AOU)
42.MUX IC
43.DP TO VGA
44.VGA CONN.
45.HDMI RP --> BLANK
46.HDMI CONN.
47.GBE LAN PHY
48.RJ45 CONN.
49.CP/TPOINTCONN.
50.PBTN/LID/FP/FAN CONN.
51.KB/RTC/TOUCH PAN CONN.
52.WWAN/WLAN NGFF CONN.
53.SUB CONN. --> BLANK
54.SUB-AUDIO JACK CONN.
55.THERMAL SENSOR
56.G SENSOR/TPM
57.BLANK
58.BLANK
59.BLANK
60.BLANK
61.DC V TO VS/ V-PCH/VM
62.EC_IT8586E/FX
63.PLM/SCREW HOLE
64.BLANK
65.DCIN / Vin Detector
66.BATTERY CONN/OTP
67.CHARGER(BQ24780)
68.3V/5VALW(RT6585B)
69.+1.35V/+0.675V(RT8231A)
70.+1.05VS(SYX198DQNC)

71.+1.5VS(SYX198DQNC)
72.+1.8VS_VGA(RT8068A)
73.+VCC_CORE(NCP81101MNTXG)
74.+VCC_CORE2
75.PROCESSOR DECOUPLING
76.+VGA_CORE(ISL62771)
77.+0.95VS_VGA(RT8068A)
78.+1.05VM(RT8068A)
79.PWR-PIR
80.HW PIR

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