

# Foxconn Precision Co. Inc.

## G41M05 Schematic

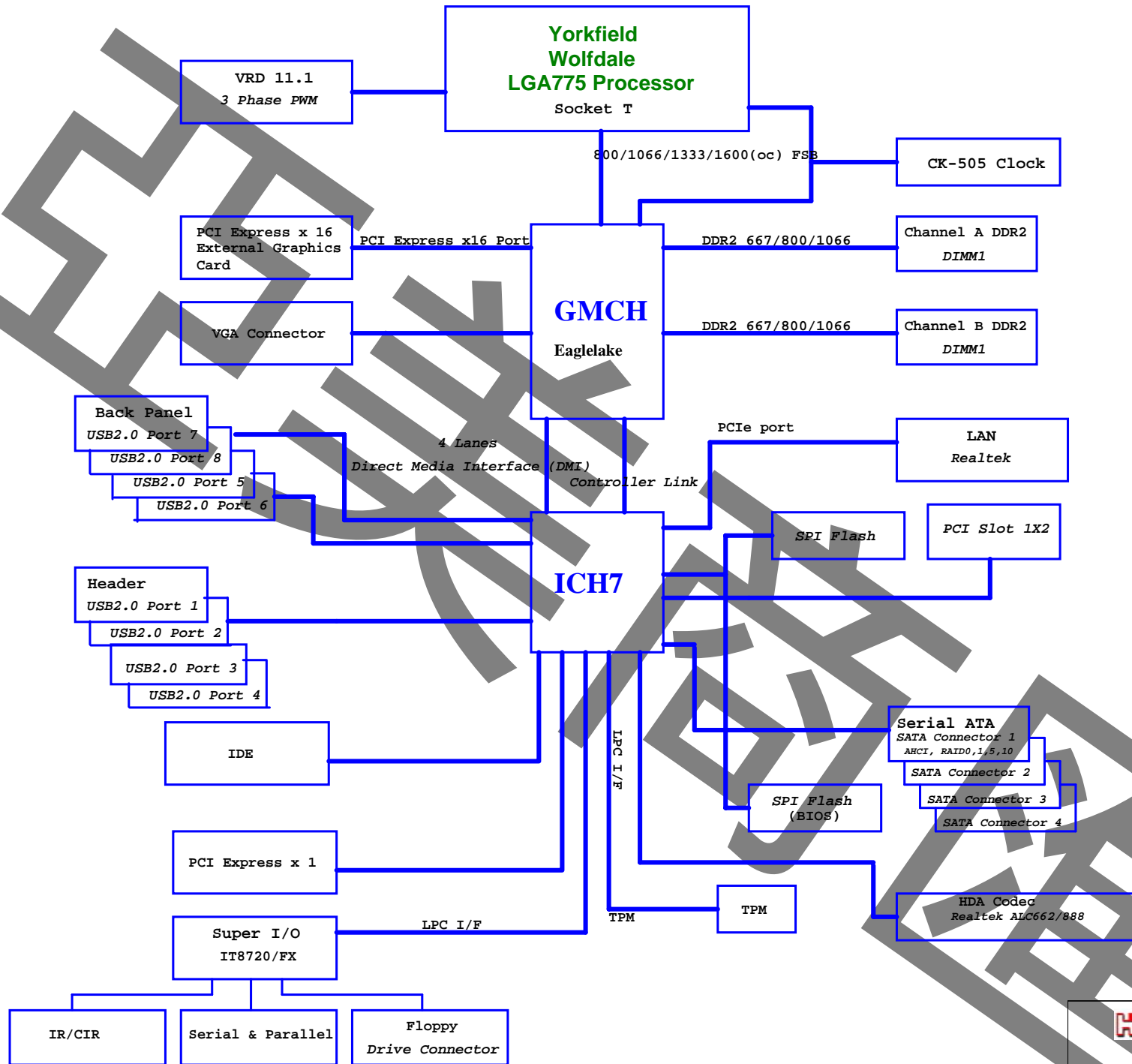
Fab.A  
Data: 2008/7/30

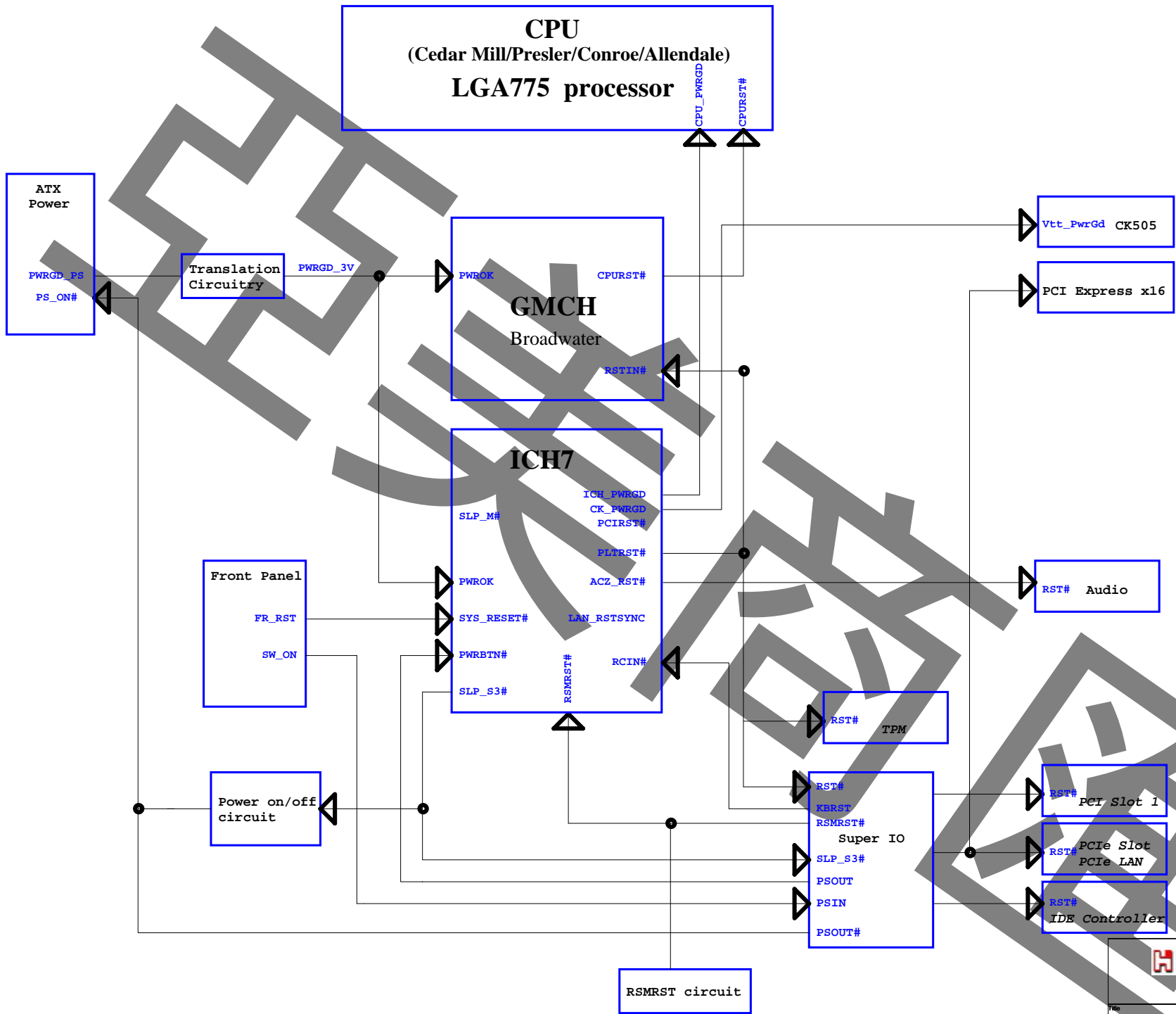
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14.318MHz

CPU

CPU 200/266/333 MHz Diff Pair

MCH 200/266/333 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCI Express x16 Gfx

G41

Channel A DDR2 DIMM1

Channel B DDR2 DIMM1

DOT 96 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

ICH 33 MHz

REF 14 MHz

ICH7

SPI Clock

SPI

Azalia Bit Clock

HD Audio

PCI 33 MHz

PCI Slot 1

TPM 33 MHz

TPM

32.768KHz

Super I/O

SIO 33 MHz

SATA 100 MHz Diff Pair

PCI Express 100 Mhz Diff Pair

ICS91PRS908DGLF



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File: Clock Distribution		
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ATX P/S

**DDR2 Channel A**

Vdd (Core)=1.8V  
Ivdd(Max)=TBD(per channel)

Vtt (Core)  
0.9V  
Ivterm(Max)=200mA  
(per channel)

**DDR2 Channel B**

Vdd (Core)=1.8V  
Ivdd(Max)=TBD(per channel)

Vtt (Core)  
0.9V  
Ivterm(Max)=200mA  
(per channel)

**HDA Codec**

Vcc  
5V  
Icc(Max)=200mA

Vcc  
3.3V  
Icc(Max)=40mA

**Nineveh GbE Lan**

3.3V STBY  
IO LED 15.5mA

1.8V ANALOG 418.2mA

1.0V Internal 1.8  
to 1.0 VR core  
277.2mA

**CK505**

Vdd (Core)  
3.3V  
Ivdd(Max)=250mA

5V  
5VSB

5VDUAL  
Icc(Max)=10A

Single Phase Switch  
5V to 1.8V  
Ivdd(Max)=TBD  
LDO  
1.8V to 0.9V  
Ivterm(Max)=1.2A

12V

VRD 11  
Switching  
Three Phase

3.3V

GMCH 1.25 V  
21.34A  
Switching

Linear 1.25V  
to 1.05V  
V\_1P05V\_ICH  
2A

Linear 1.8V  
to 1.5V  
V\_1P5V\_ICH  
2.2A

RTC  
Battery

5V STBY to 3.3SB  
1.5A

**Processor**  
Vccp (CPU Vcore)  
Voltage=1.15-1.5V  
Icc(Max)=125A  
3-Phases Switching

1.2V FSB  
Vtt=5.3A

**Broadwater GMCH**

FSB\_Vtt  
1.2V FSB Vtt  
Icc(Max)=1.3A

1.8V VCCSM  
1.8V VCC\_SMCLK

Vcore (Core Logic)  
1.25V  
Icc(Max)=18.8A(Integrated)  
\*1.25V (DMI&PCIe)  
VCCA\_EXP 2.5A  
1.25V  
VCC\_CL 3.8A

3.3V VCCA\_DAC 70mA  
3.3V VCC3\_3 15.8mA

**ICH7**

1.25V VCCDMI 40mA

1.2V VCC\_CPU\_IO 14mA

1.05V (Core) VCC1\_05  
1.17A

1.5V (USB & SATA) VCC1\_5A  
1.12A

1.5V (PCIe) VCC1\_5B  
0.77A

1.5V VCCGLAN1\_5  
74mA

RTC=5uA

3.3V VccCL3\_3 12mA  
3.3V VccSUS3\_3 141mA  
3.3V VccLAN (10/100) 12mA  
3.3V VccSUSHDA 4mA  
3.3V VCC3\_3 310mA

3.3V VccGLAN3\_3 1mA  
3.3V VccHDA 4mA

**Super I/O**

3.3V  
Icc(Max)=50mA

3.3SBV  
Icc(Max)=50mA(S0)

3.3SBV  
Icc(Max)=38mA(S3)

5V  
5VSB

5VDUAL  
Icc(Max)=  
4.345A(S0,S1)  
22mA(S3)

**USB2.0 10 Ports**  
+5V DUAL=5A(S0, S1)  
+5V DUAL=20mA(S3)

**PS2**  
+5V DUAL=345mA(S0, S1)  
+5V DUAL=2mA(S3)

**FWH**  
3.3V=107mA(S0, S1)

**PCI Express X16 slot (1)**  
+12V=5.5A

3.3VSB  
Icc(Max)=0.375A(wake)  
Icc(Max)=0.02A(no wake)

+3.3V=3A

12V

**PCI Express X1 Per slot (1)**  
+12V=0.5A

3.3VSB  
Icc(Max)=0.375A(wake)  
Icc(Max)=0.02A(no wake)

+3.3V=3A

**PCI Per Slot (X2)**

-12V  
Icc(Max)=0.1A

5V  
Icc(Max)=5A

3.3V  
Icc(Max)=7.6A

12V  
Icc(Max)=0.5A

3.3VSB  
Icc(Max)=0.375A(wake)  
Icc(Max)=0.02A(no wake)

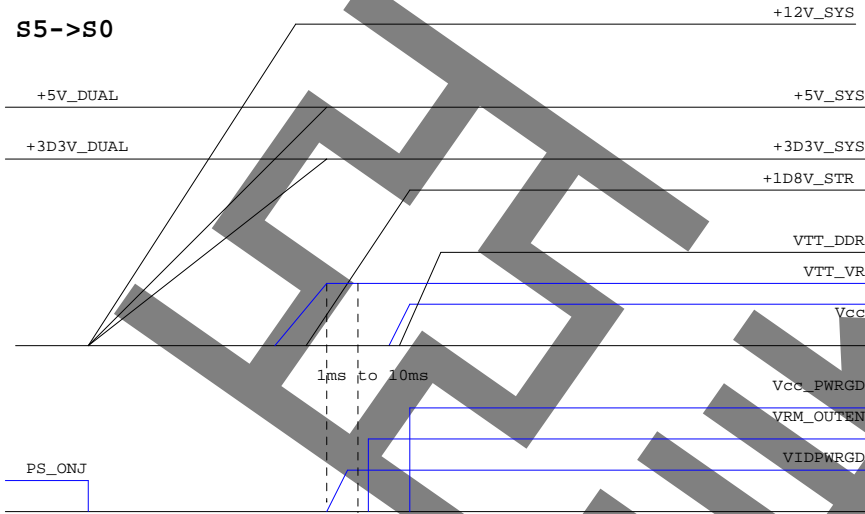
-12V

5V

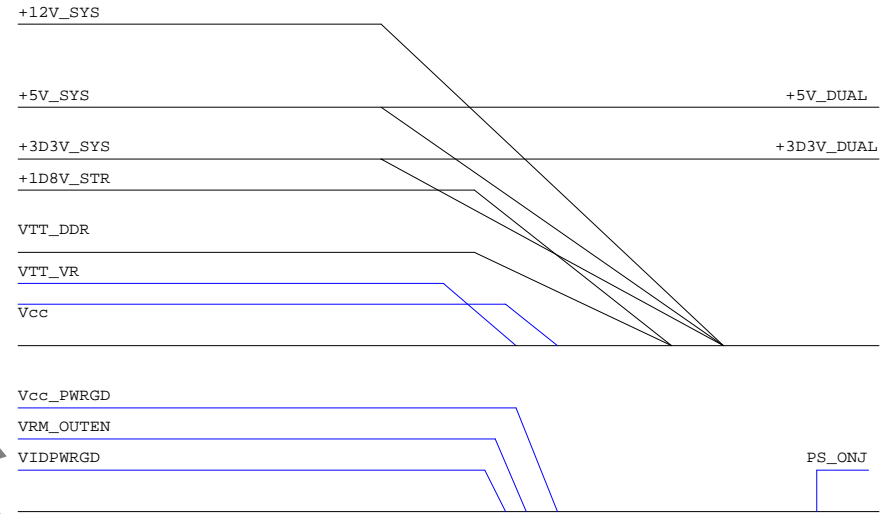
3.3V



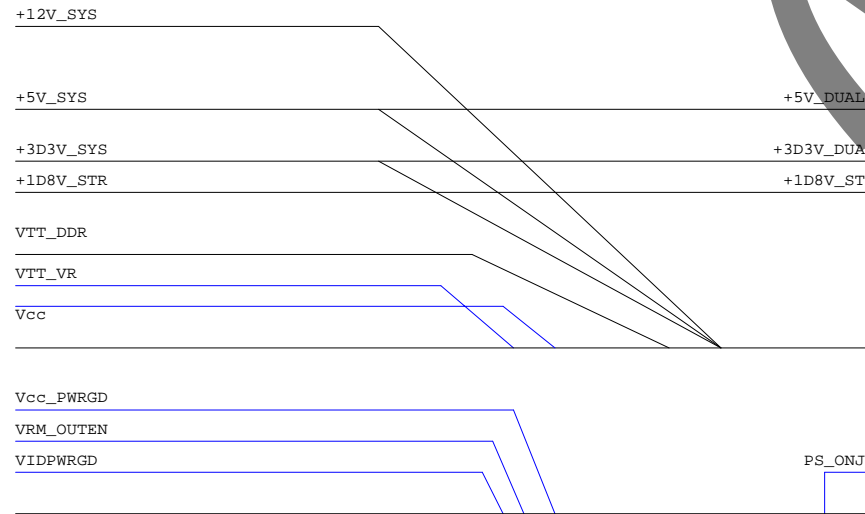
### S5->S0



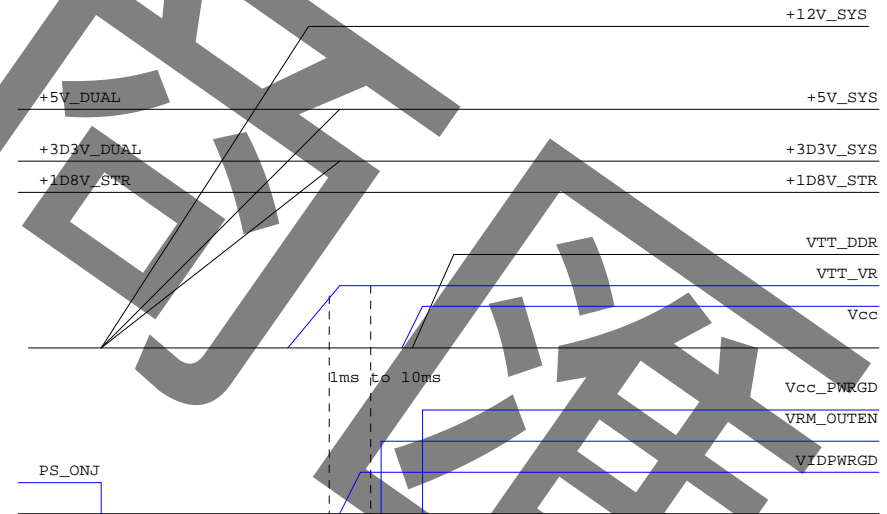
### S0->S5



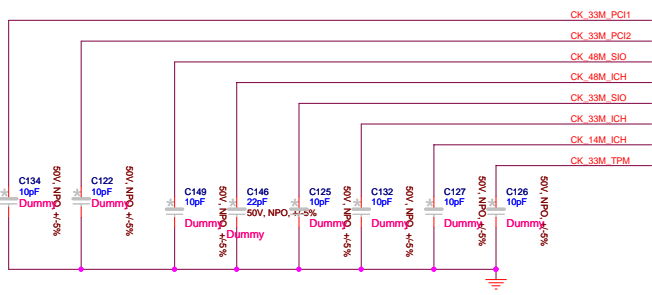
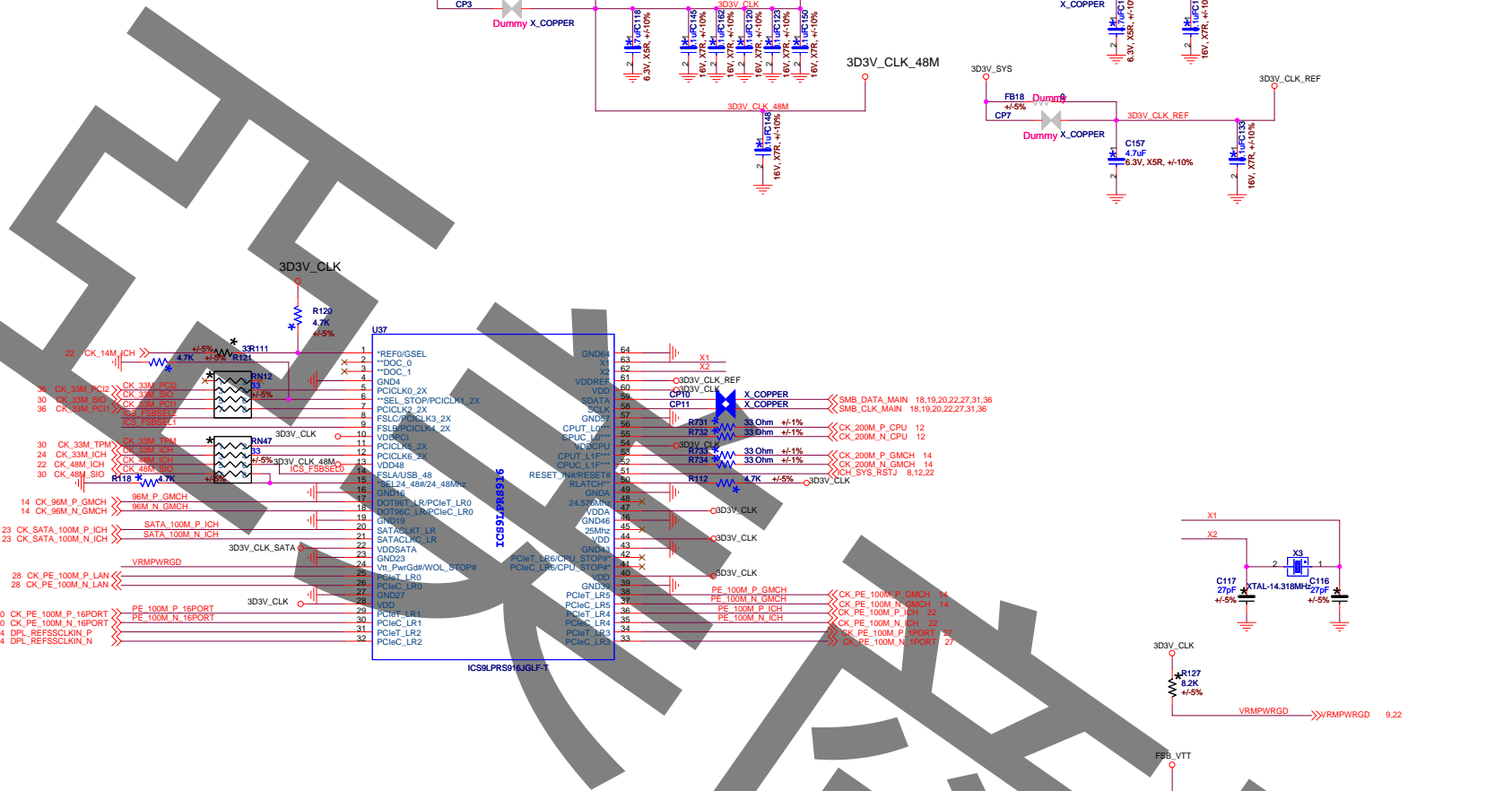
### S0->S3



### S3->S0



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**BSEL TABLE**

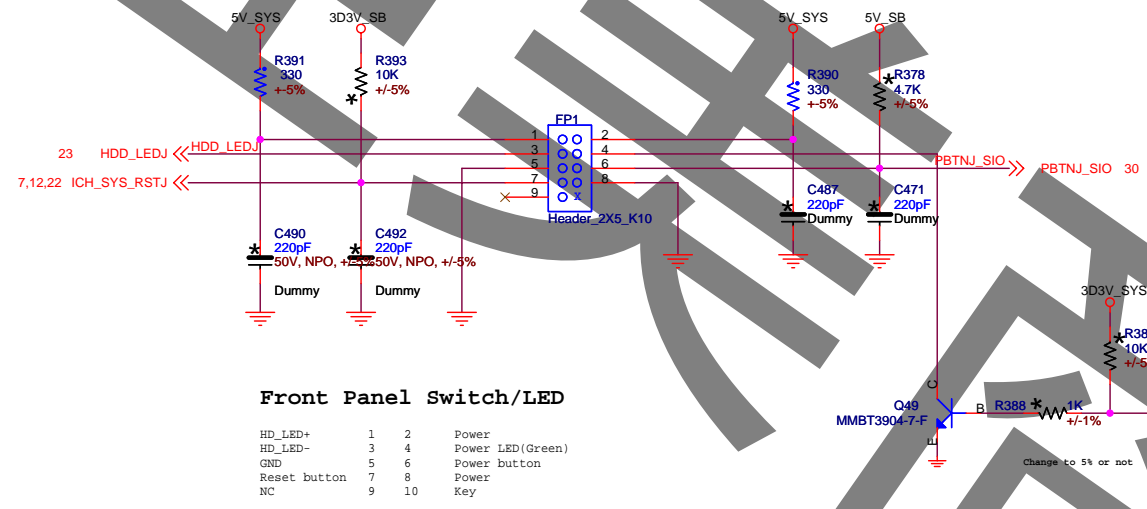
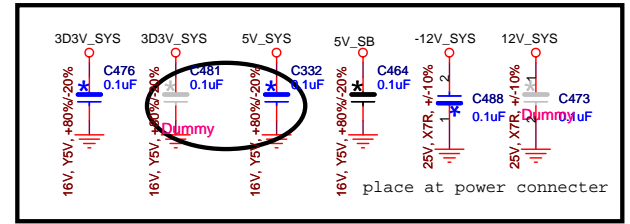
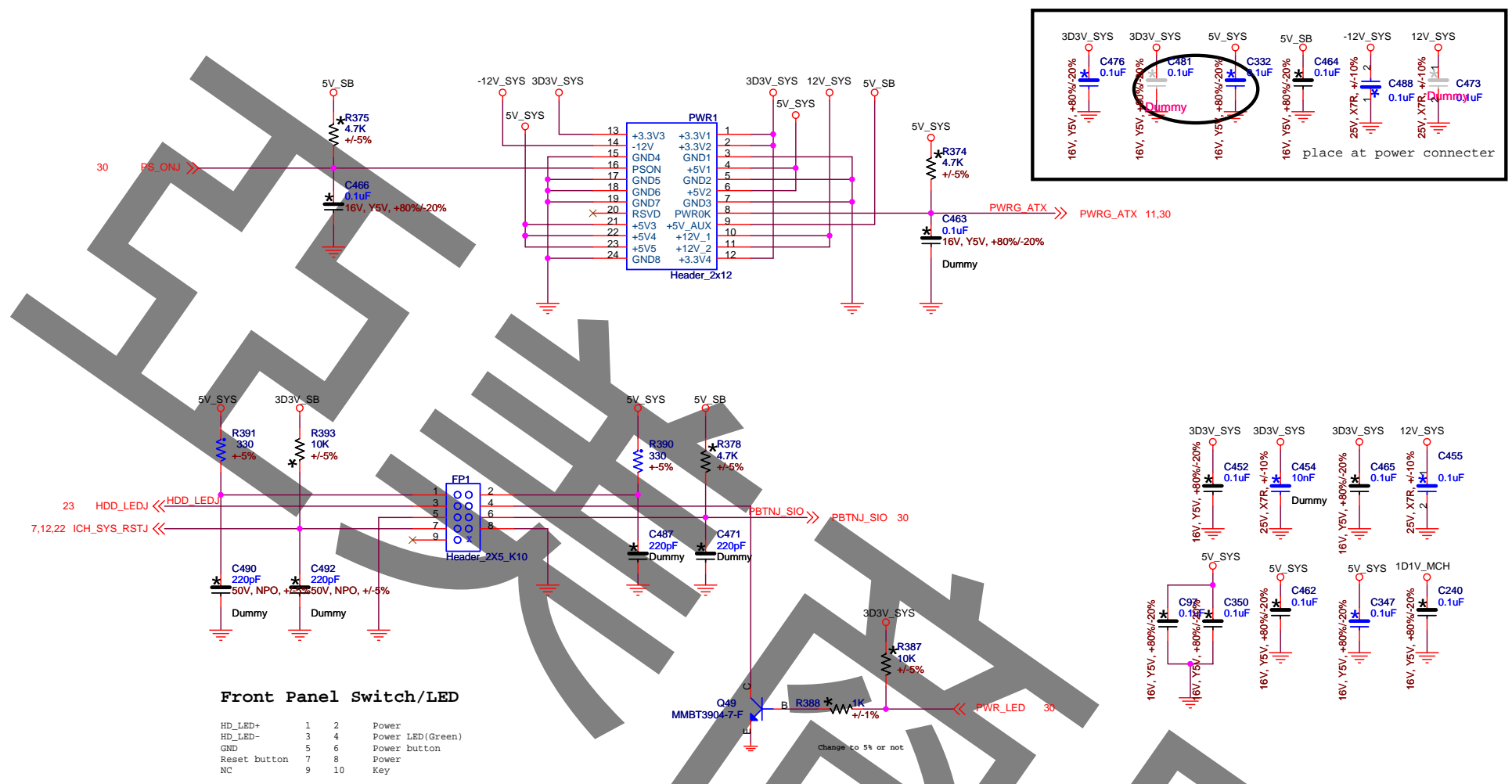
FS_C	FS_B	FS_A	FSB Frequency
0	0	1	133MHz (533)
0	1	0	200MHz (800)
0	0	0	266MHz (1066)
1	0	0	333MHz (1333)
1	1	0	400MHz (1600)

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File: **CLOCKGEN**

Size: C Document Number: **G41M05** Rev: A

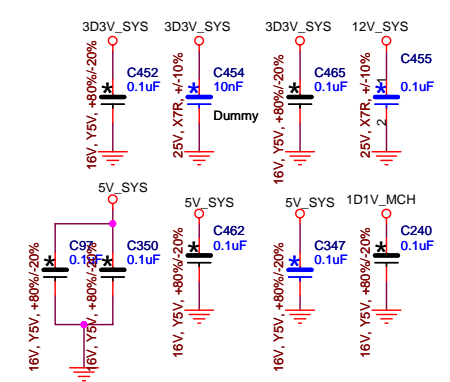
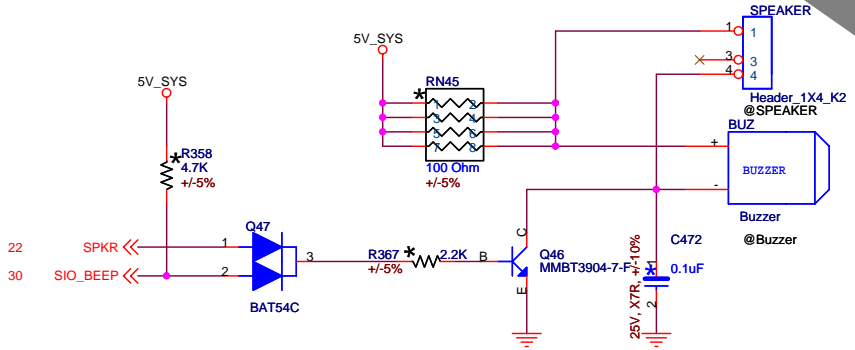
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**Front Panel Switch/LED**

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Power
NC	9	10	Key

**SPEAKER HEADER**



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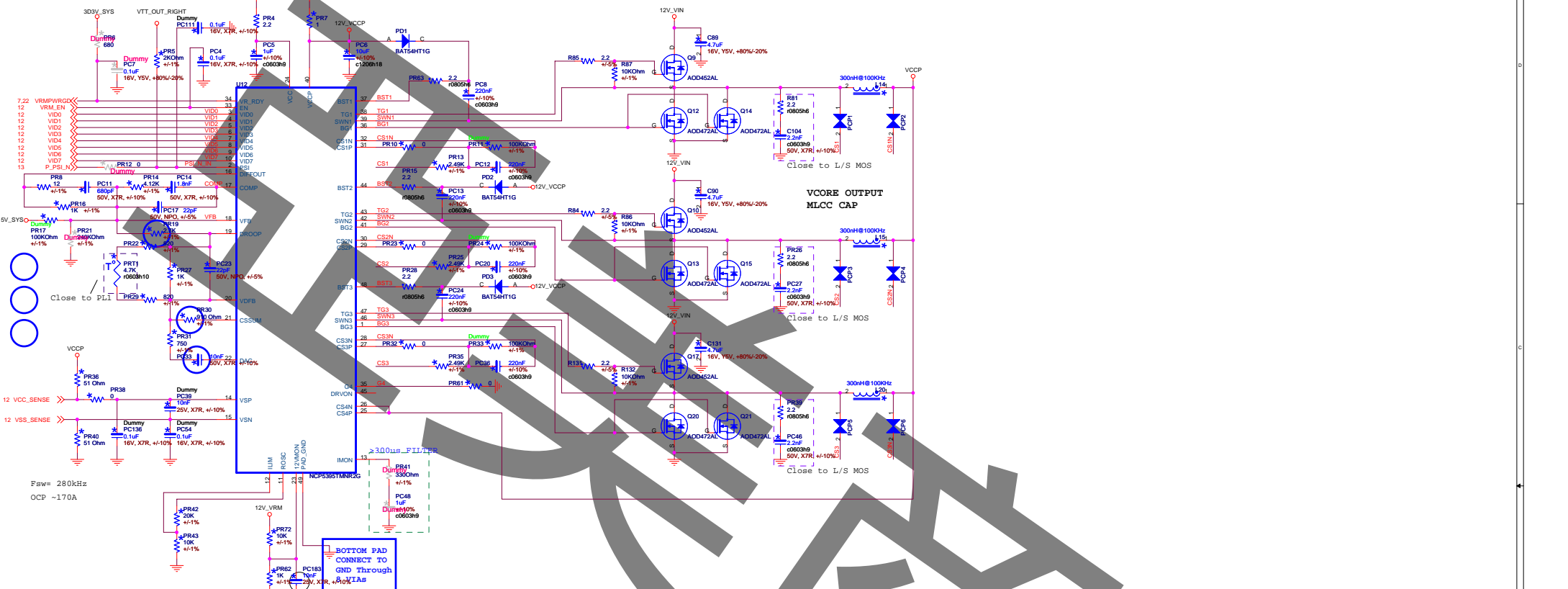
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Size: Custom	Document Number: <b>G4IM05</b>	Rev: A
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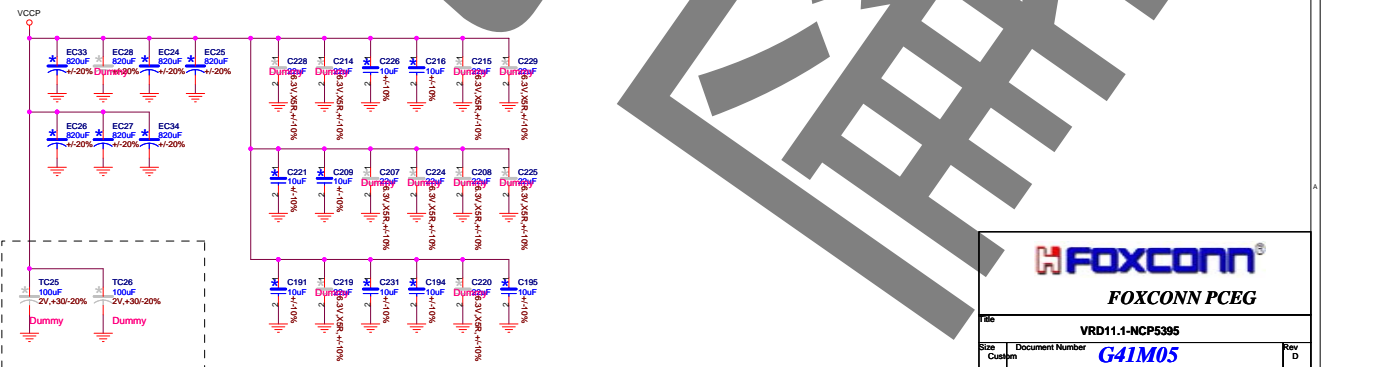
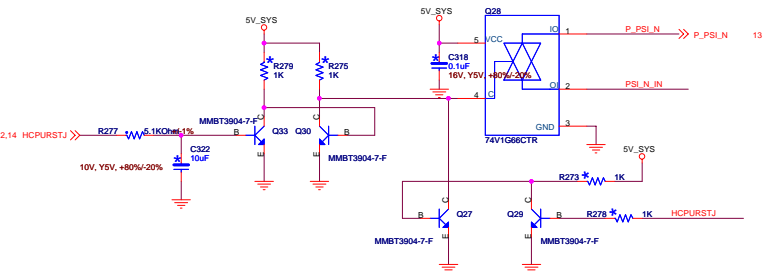
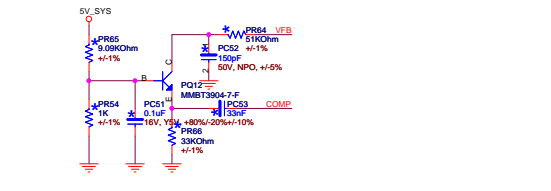
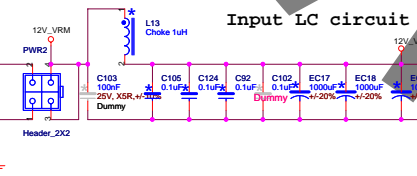
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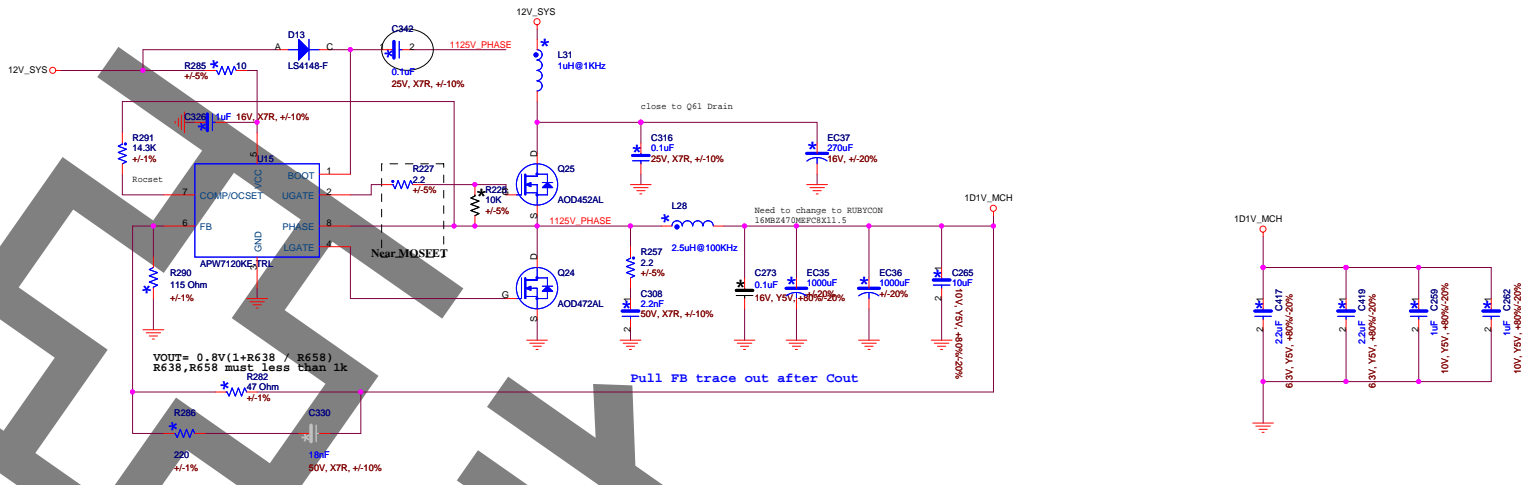


VCCP

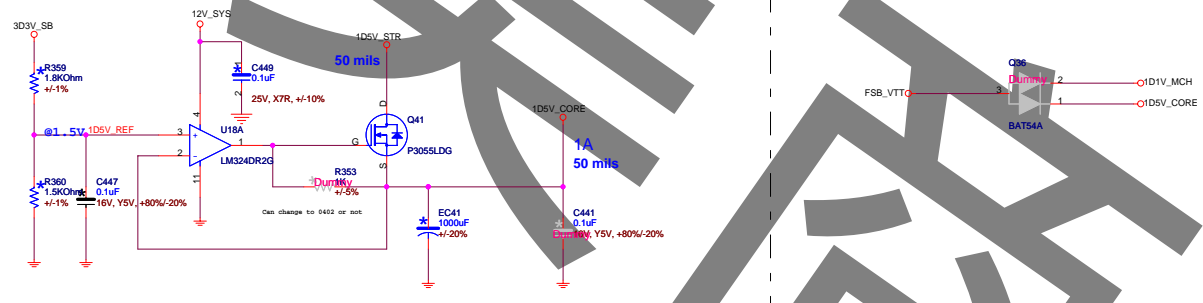


Input LC circuit

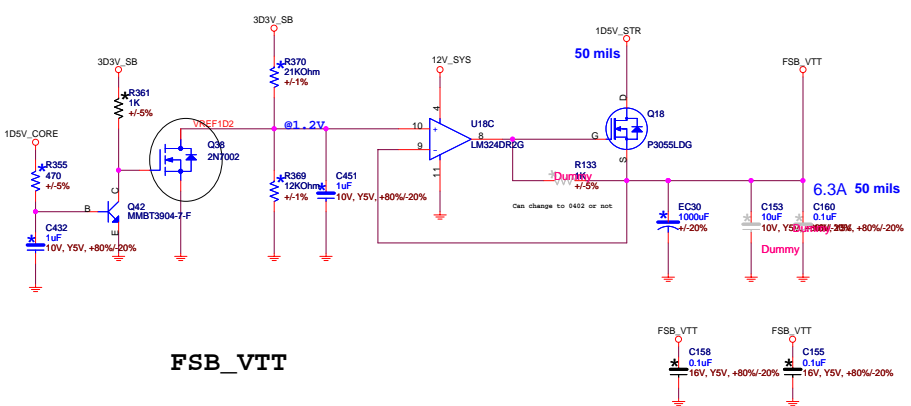




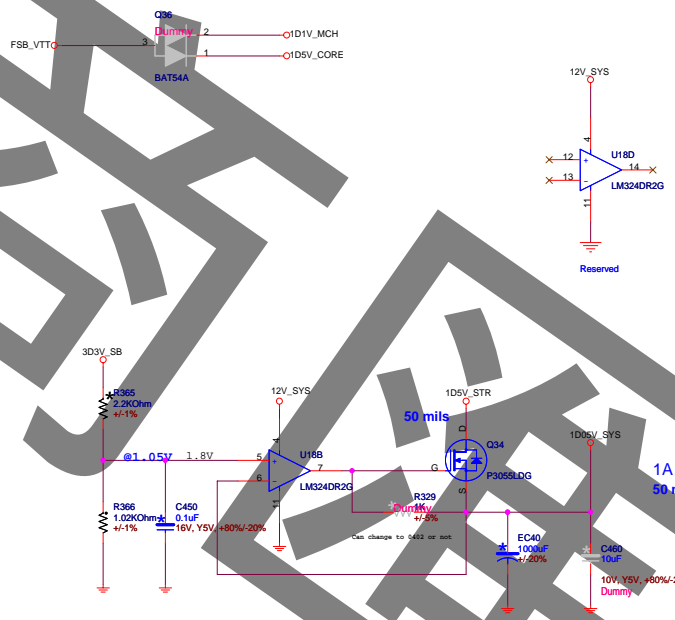
1D125V FOR CHIP



1D5V\_SYS



FSB\_VTT

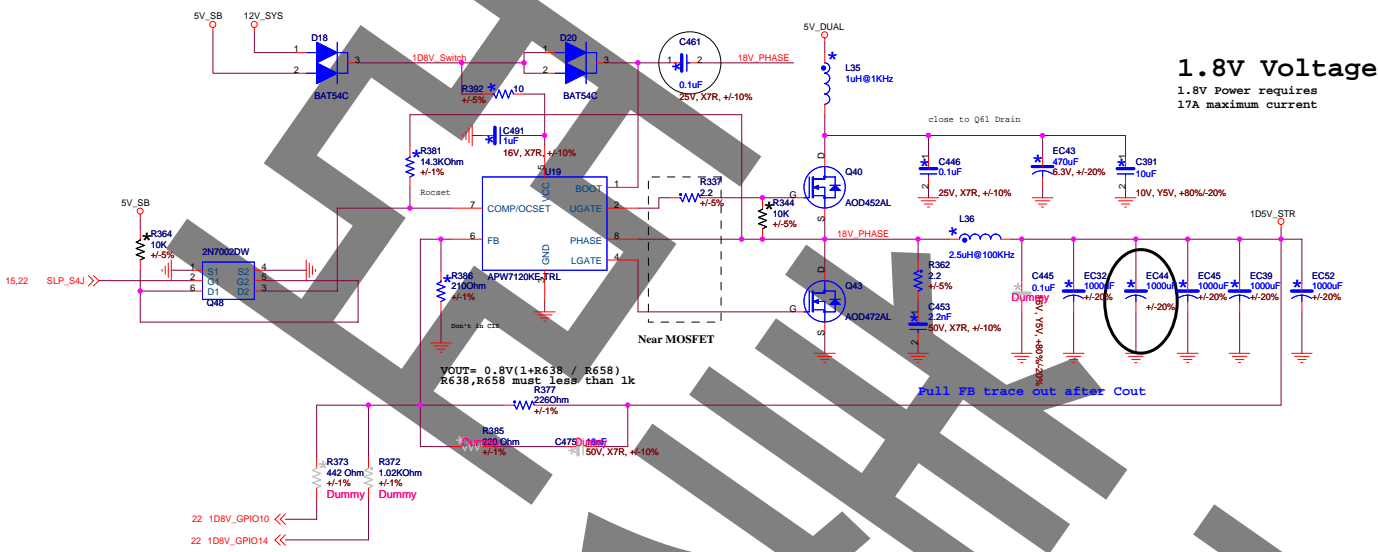


1D05V\_SYS

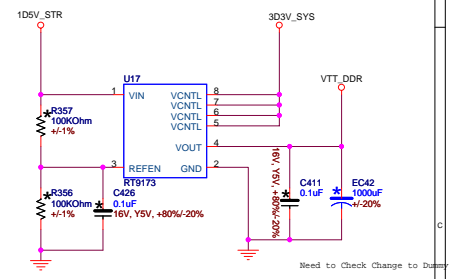


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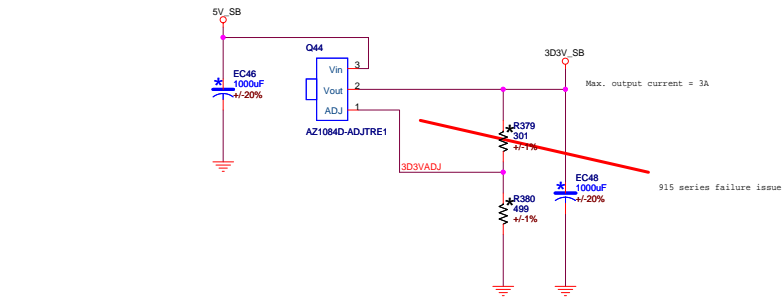
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**DDR\_VTT**

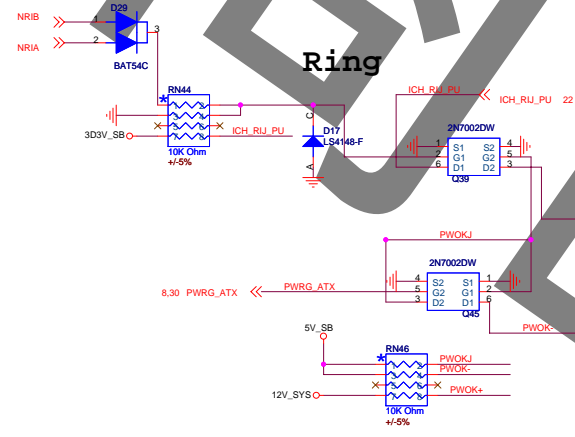


**1D8V\_STR**



$V_{out} = V_{ref}(1 + R_2/R_1) + I_{adj}R_2$   
R1 is Up Resistor.  
Iadj=50uA  
Vref=1.25V

**3D3V\_DUAL**

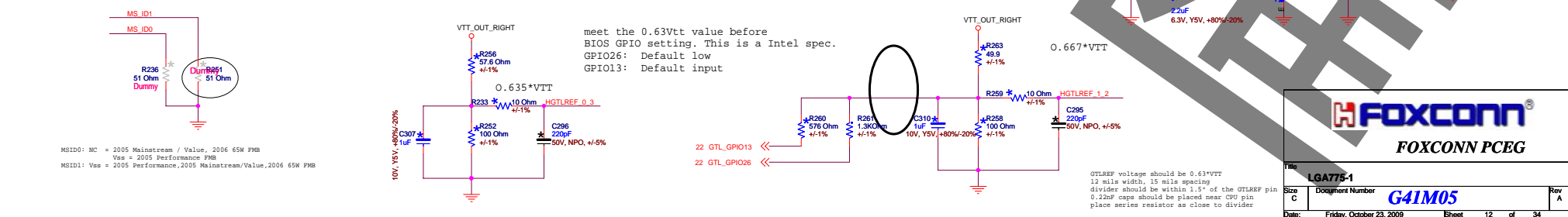
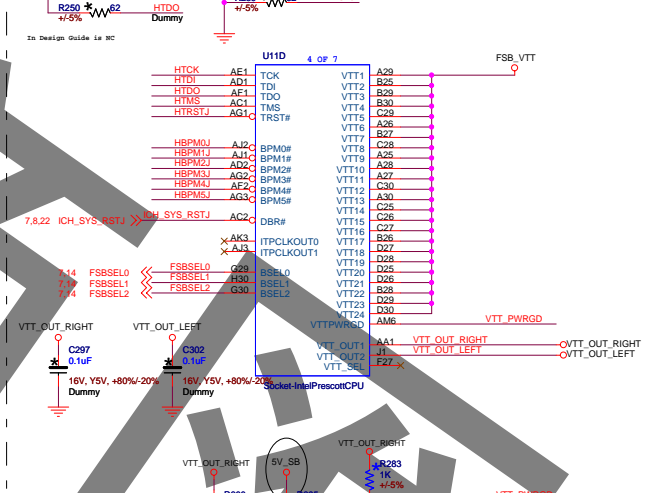
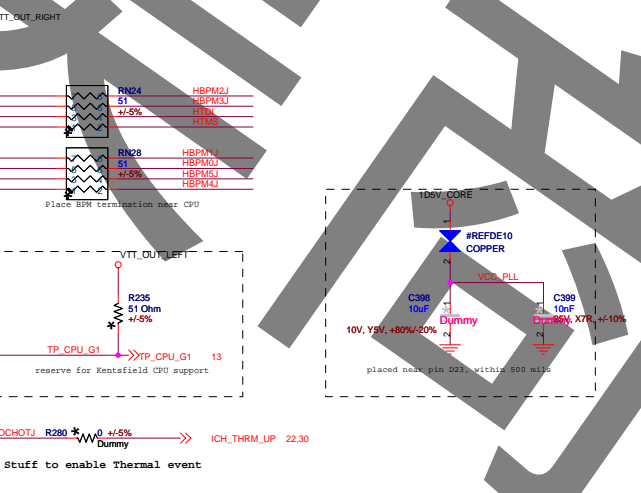
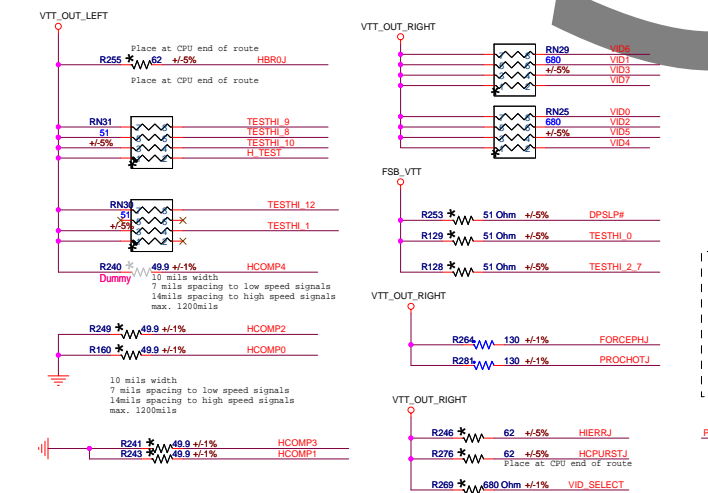
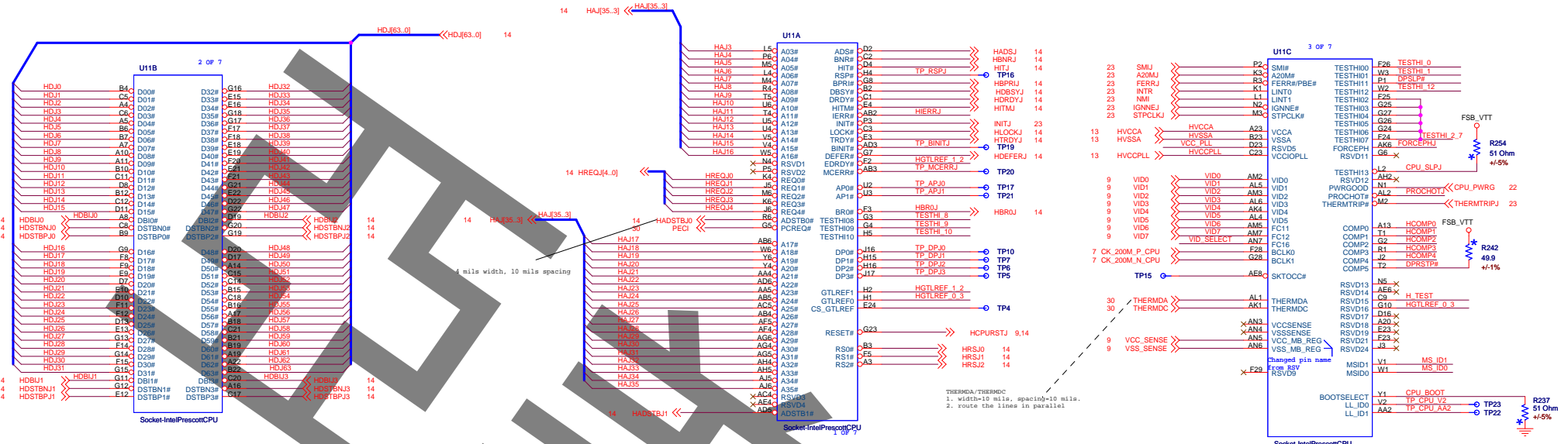


**5V\_DUAL**



FOXCONN PCEG

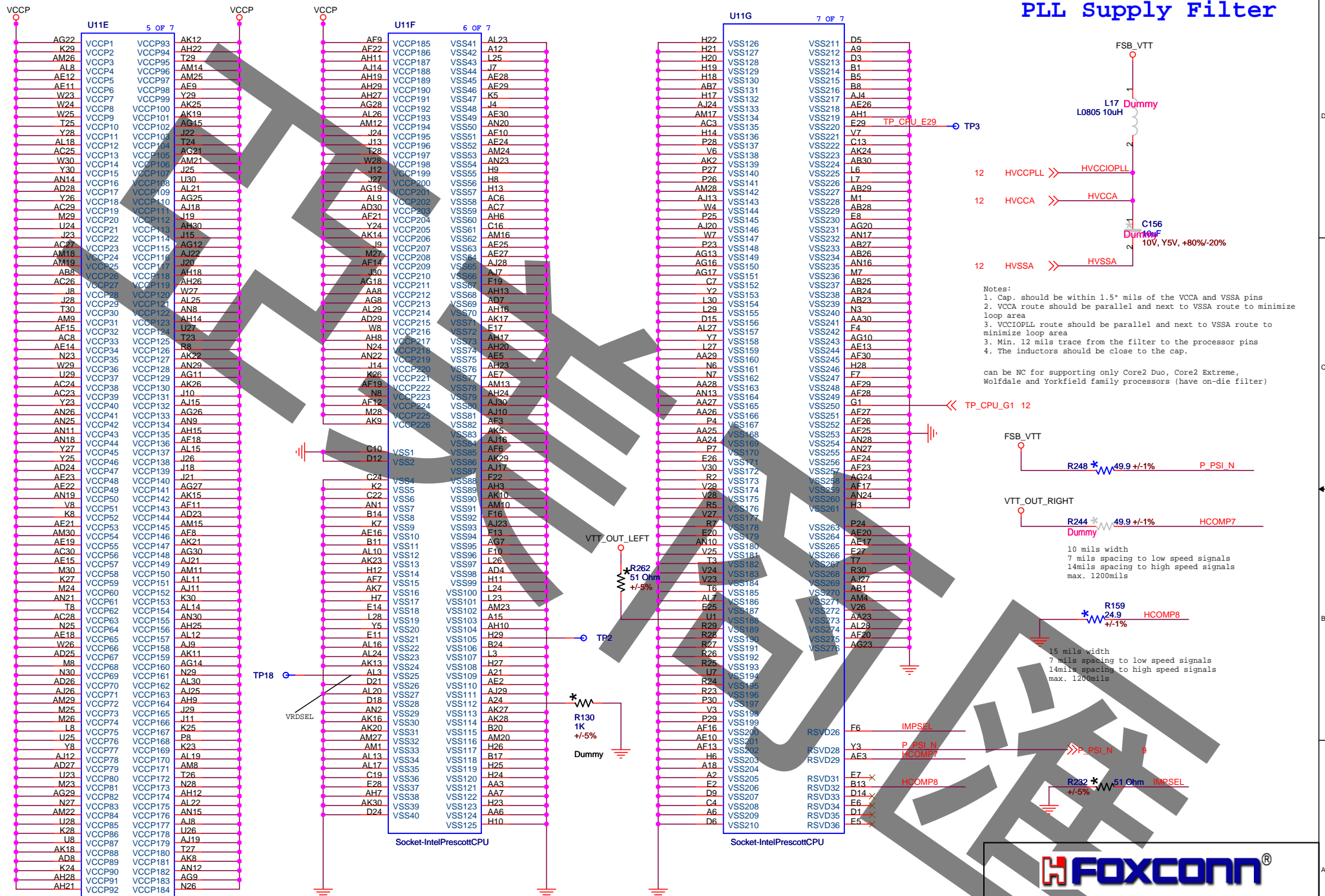
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MSID0: VC = 2005 Mainstream / Value, 2006 65W PFM  
 Vss = 2005 Performance PFM  
 MSID1: Vss = 2005 Performance, 2005 Mainstream/Value, 2006 65W PFM

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 Rev A

# PLL Supply Filter



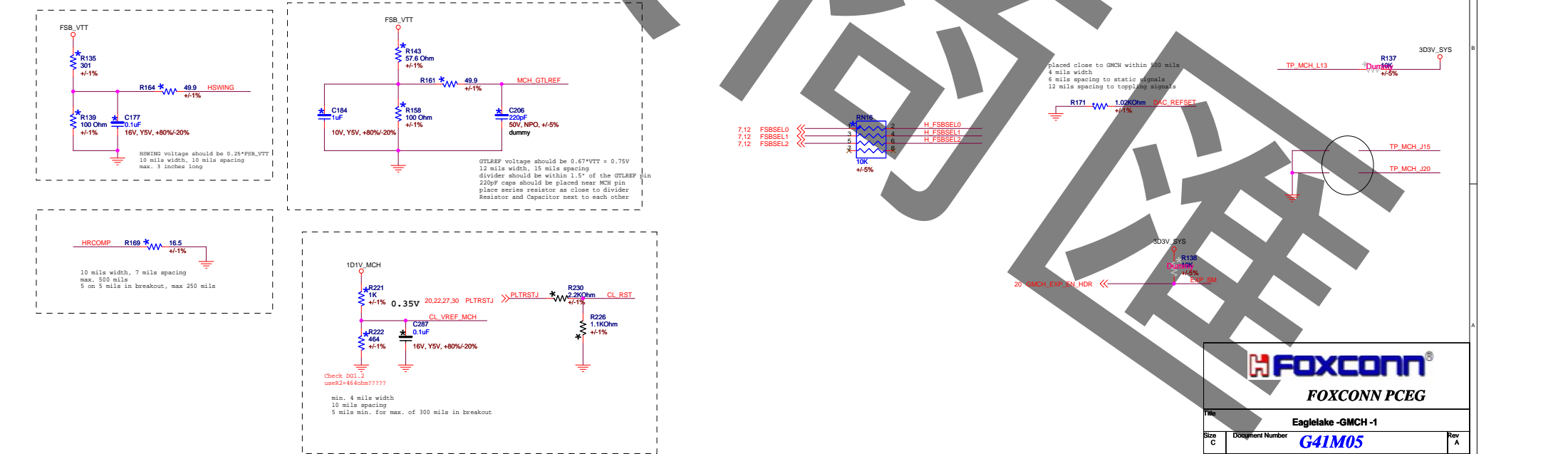
- Notes:
1. Cap. should be within 1.5" mils of the VCCA and VSSA pins
  2. VCCA route should be parallel and next to VSSA route to minimize loop area
  3. VCCIOPLL route should be parallel and next to VSSA route to minimize loop area
  3. Min. 12 mils trace from the filter to the processor pins
  4. The inductors should be close to the cap.

can be NC for supporting only Core2 Duo, Core2 Extreme, Wolfdale and Yorkfield family processors (Have on-die filter)

10 mils width  
7 mils spacing to low speed signals  
14mils spacing to high speed signals  
max. 1200mils

15 mils width  
7 mils spacing to low speed signals  
14mils spacing to high speed signals  
max. 1200mils





**FOXCONN**

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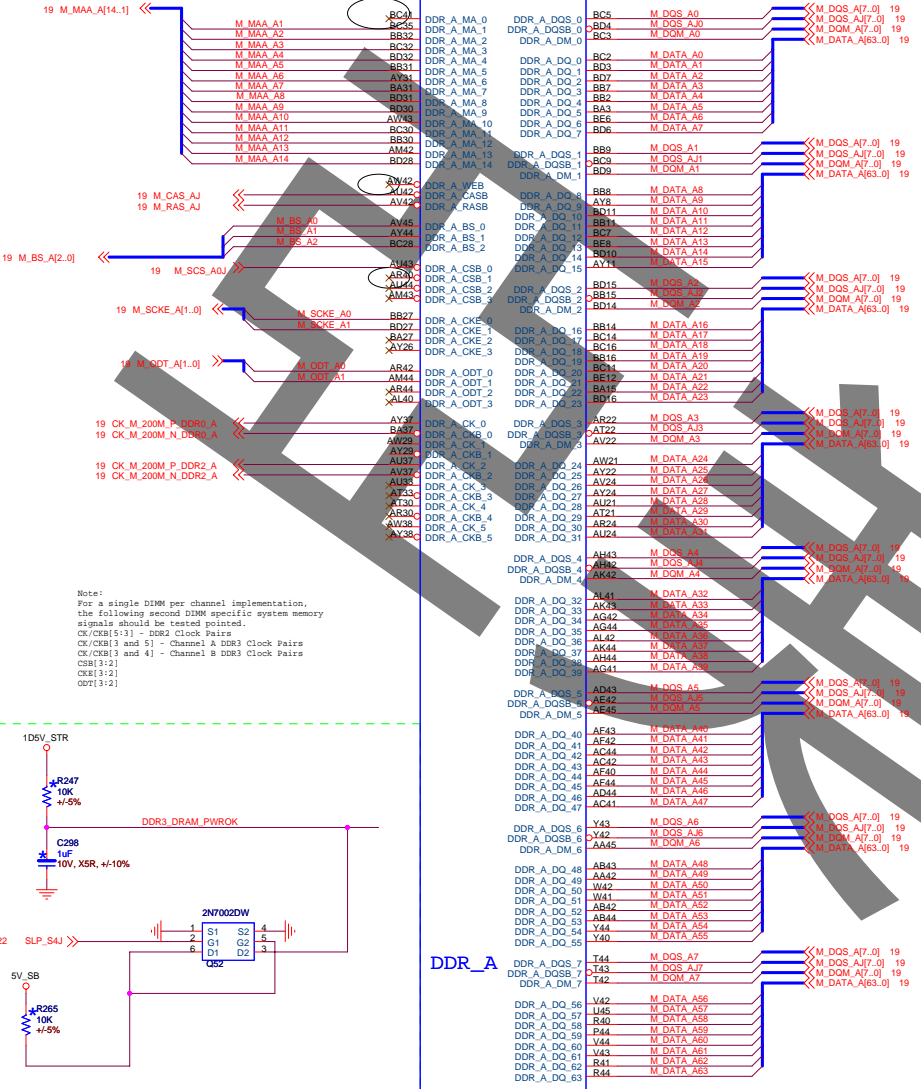
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Size C Document Number 641M05 Rev A

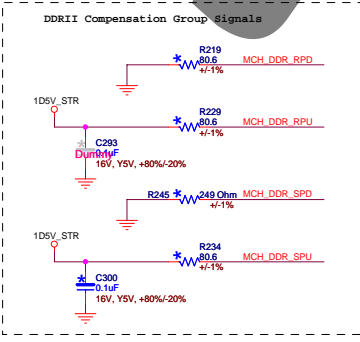
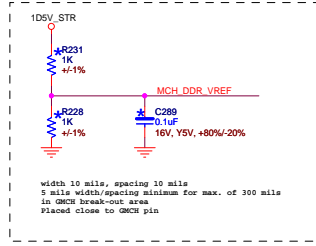
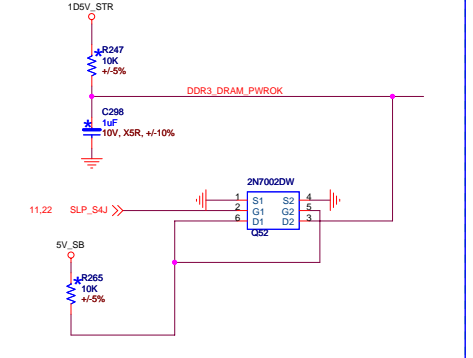
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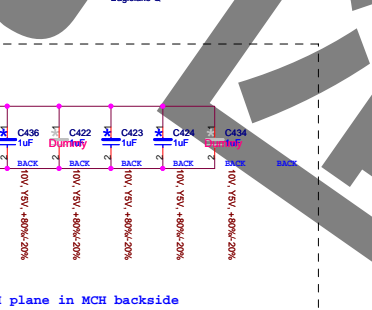
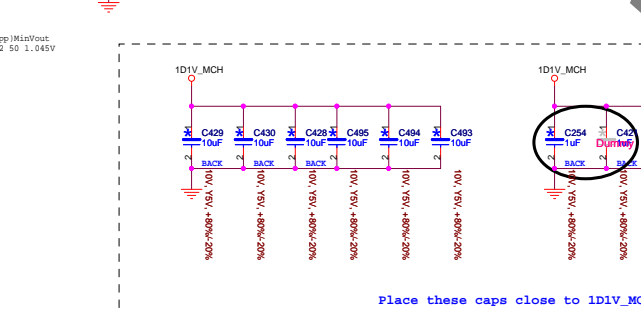
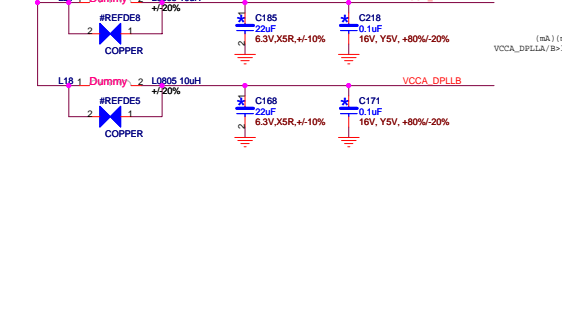
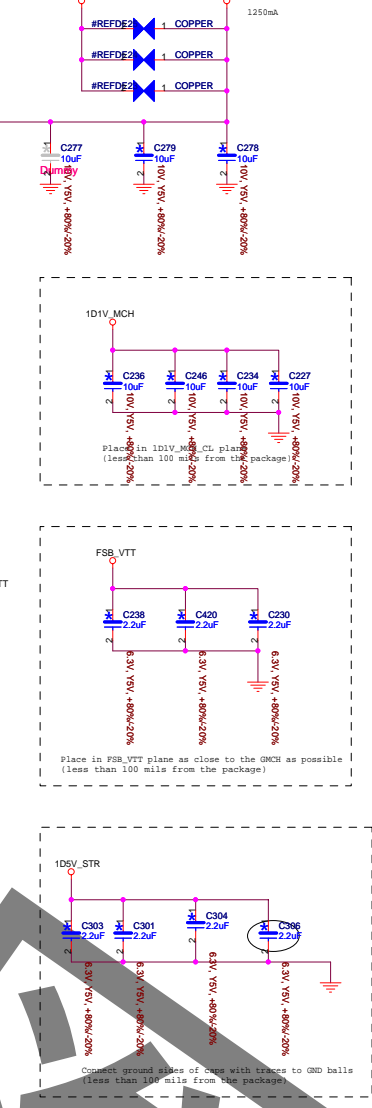
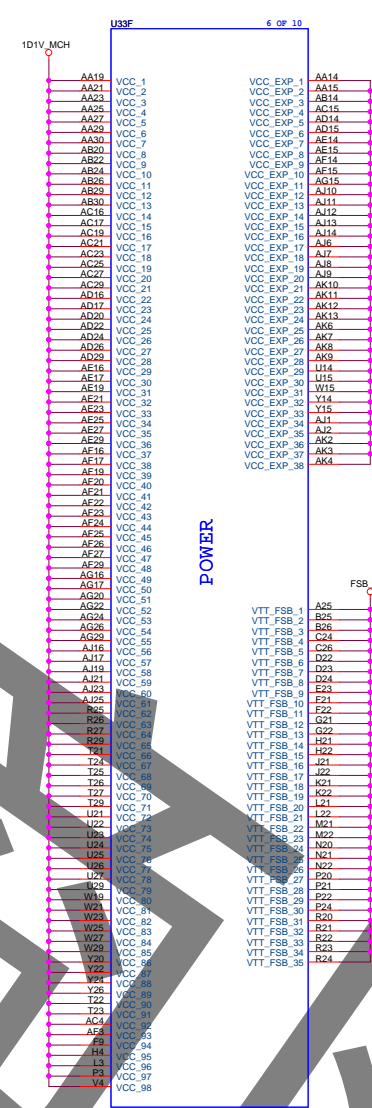
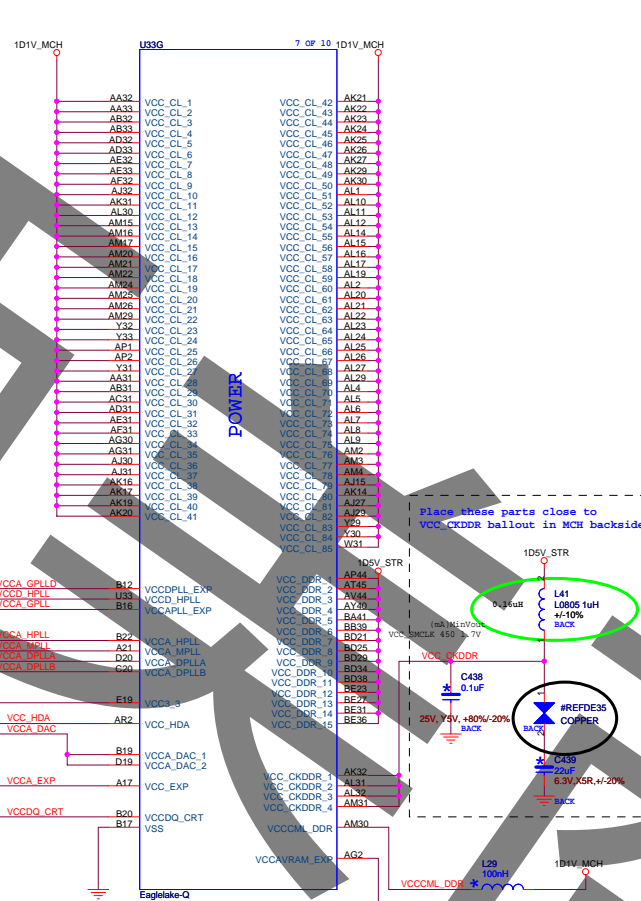
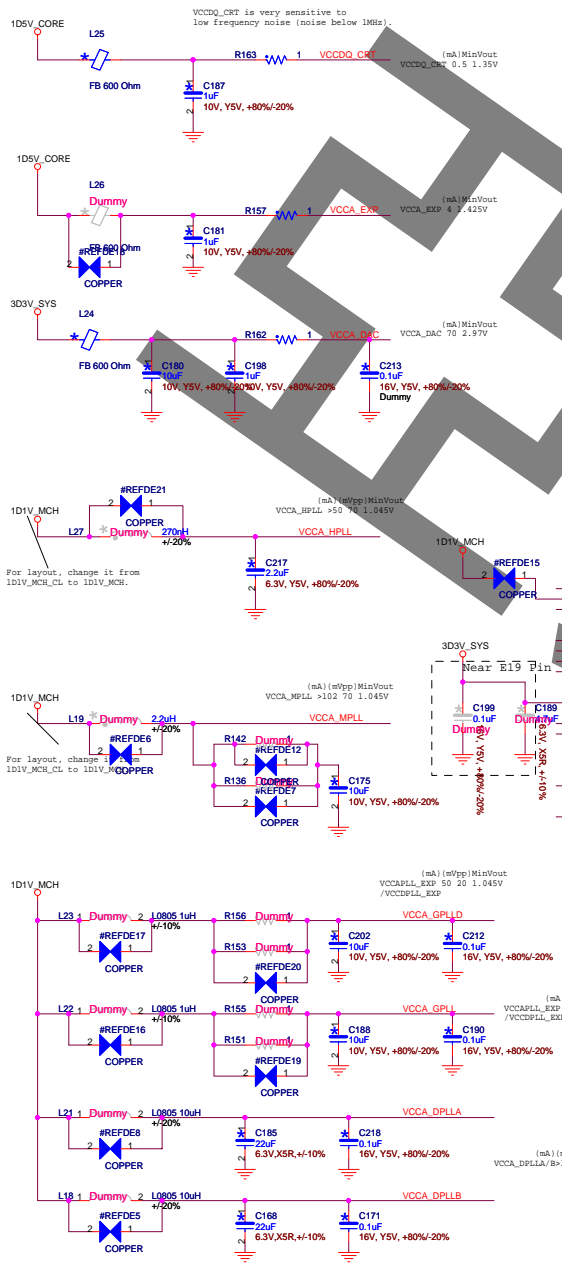
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Note:  
For a single DIMM per channel implementation,  
the following second DIMM specific system memory  
signals should be tested pointed.  
CK/CDB[5:3] - DDB2 Clock Pairs  
CK/CDB[7 and 5] - Channel B DDB3 Clock Pairs  
CK/CDB[3 and 4] - Channel B DDB3 Clock Pairs  
CSB[3:2]  
CSB[1:2]  
ODT[3:2]



Title: Eaglelake-GMCH-2  
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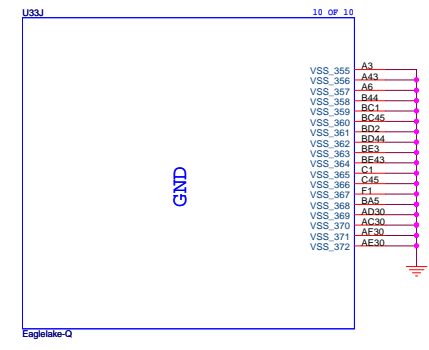
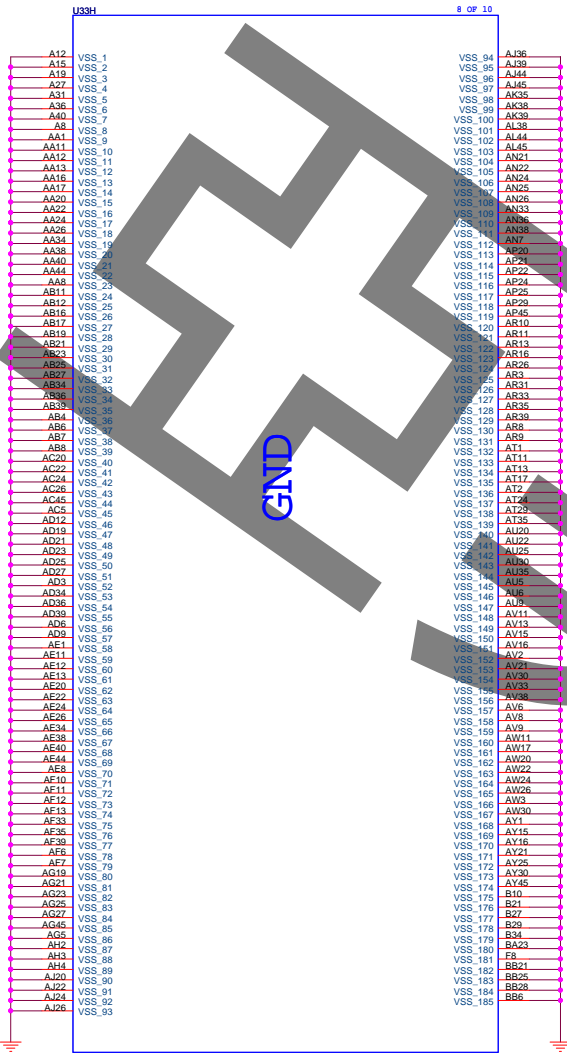


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Title: Eaglelake-GMCH-3

Size: C	Document Number: G41M05	Rev: A
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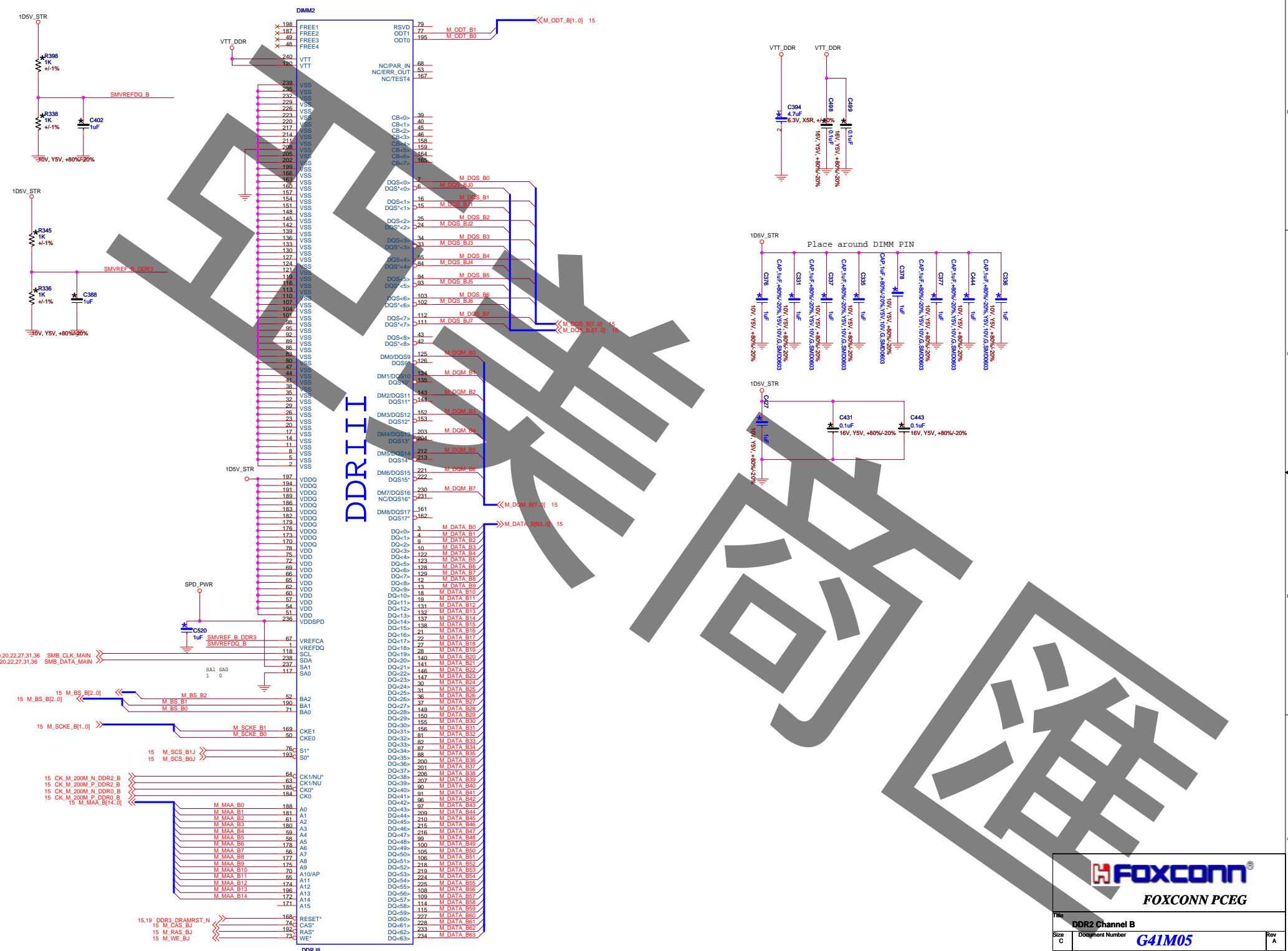




**FOXCONN**  
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Size: C	Document Number: G41M05	Rev: A
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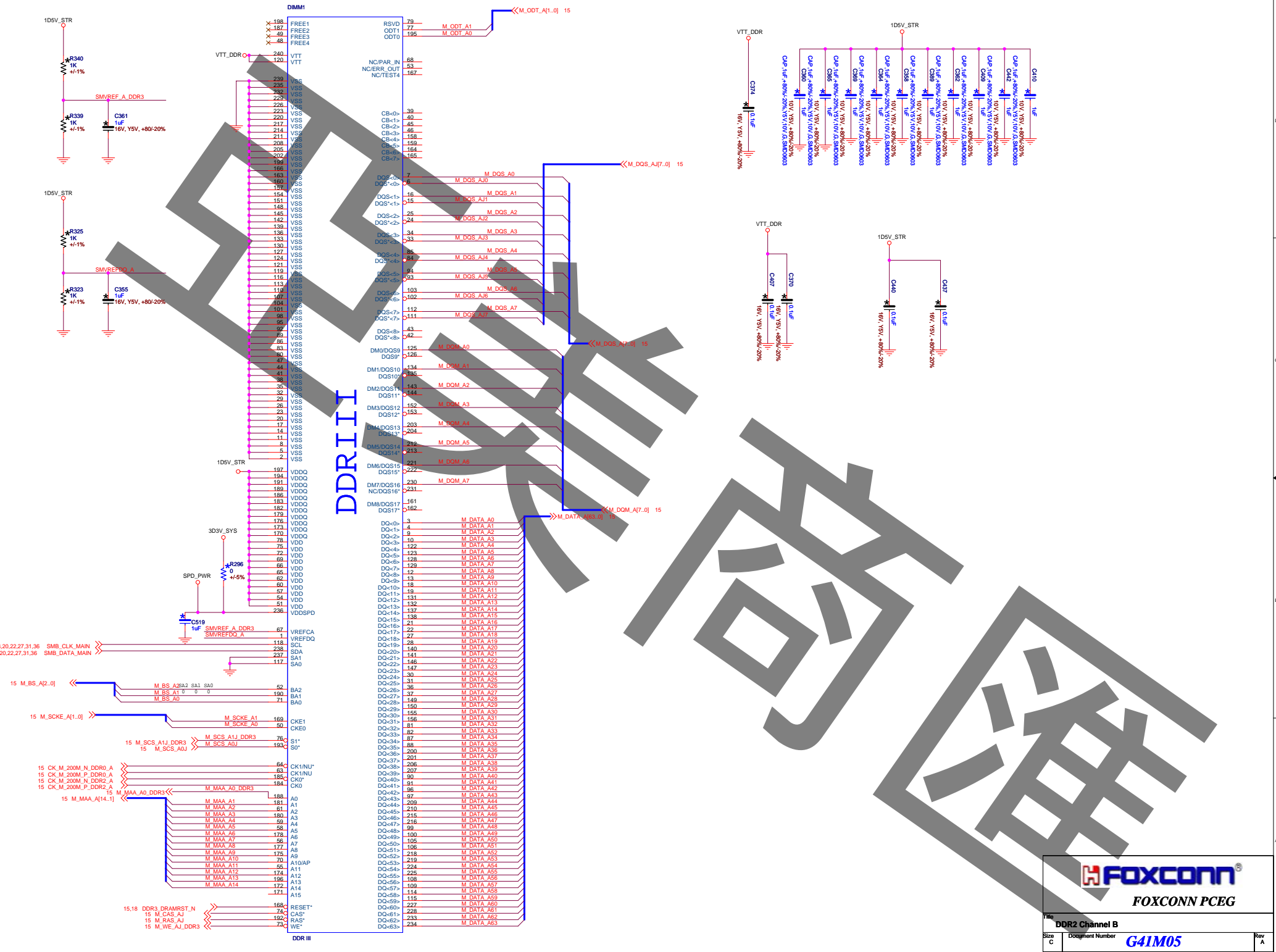


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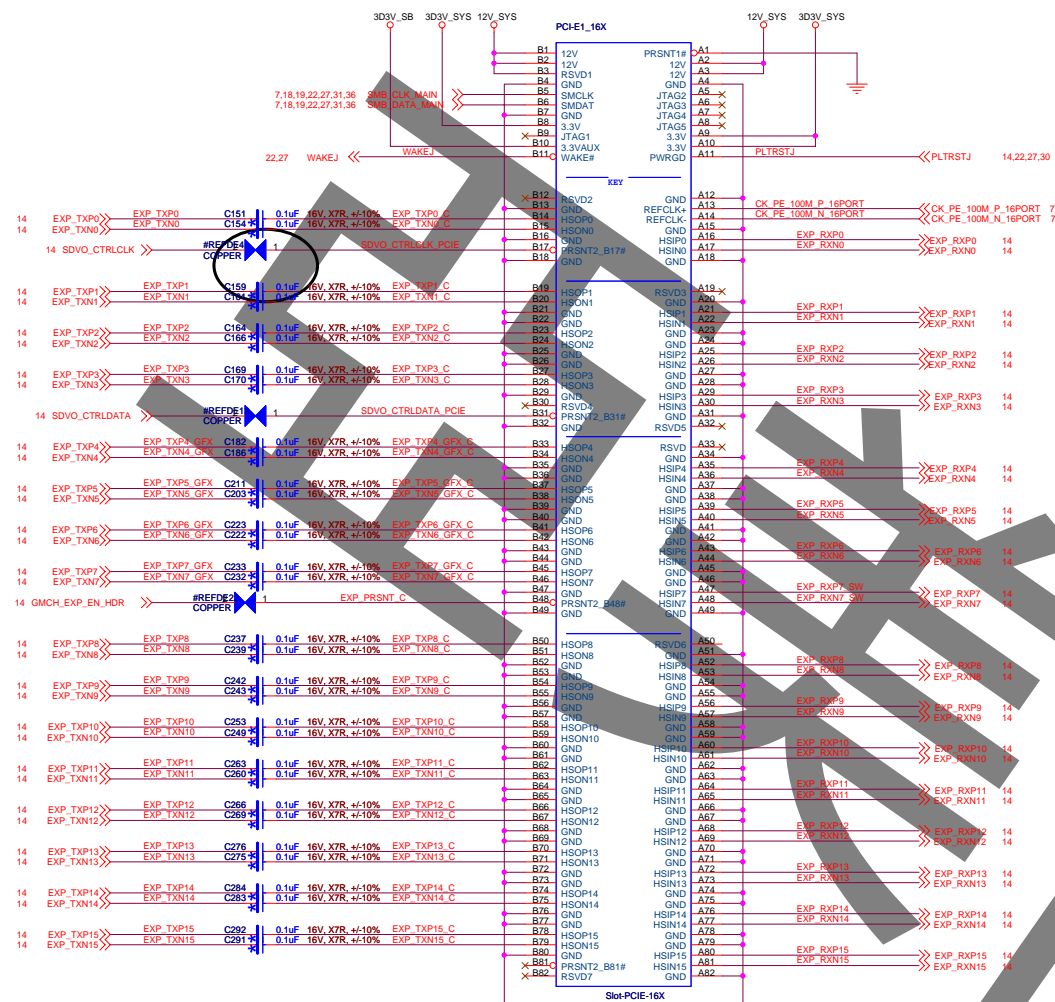
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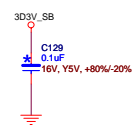
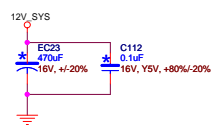
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File: **DDR2 Channel B**

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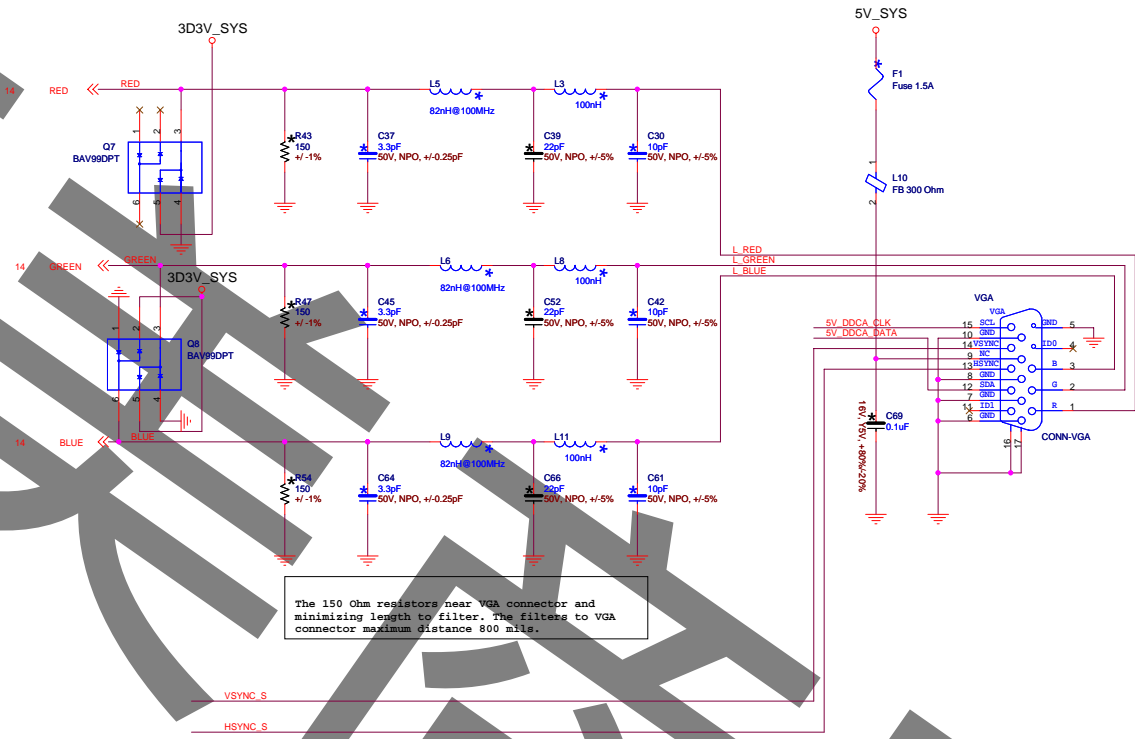
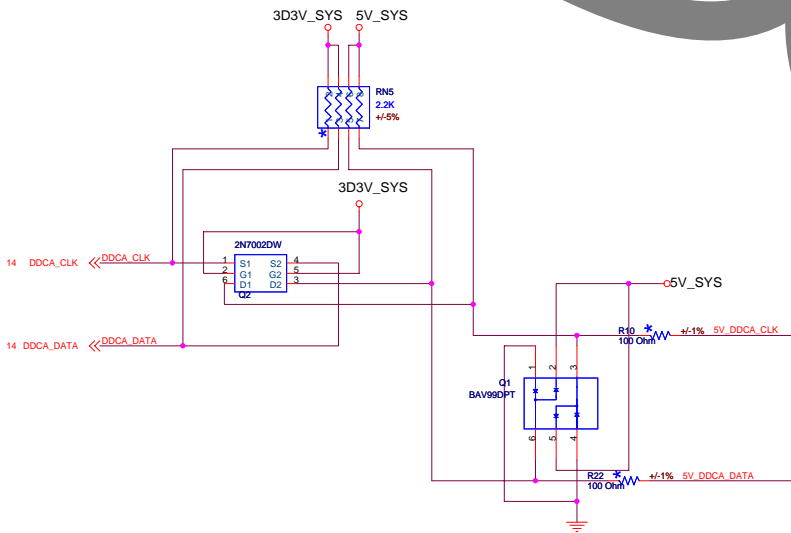
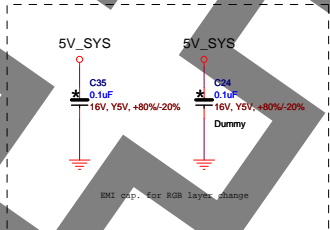


Change to another part.  
050608

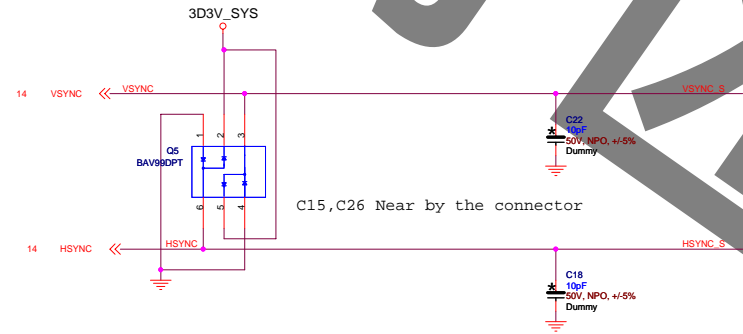


RGB routing

1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced



The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.



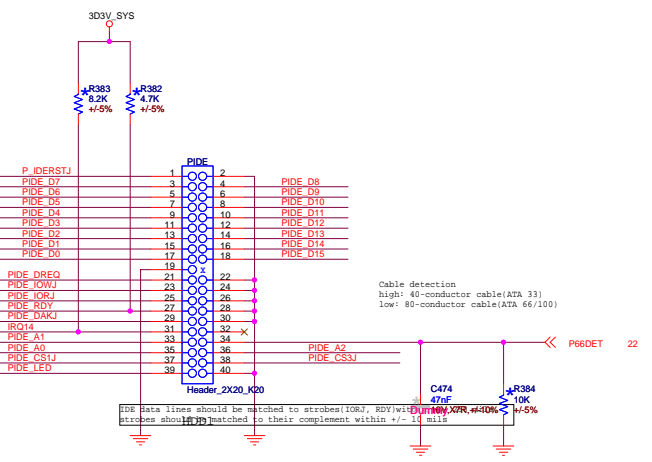
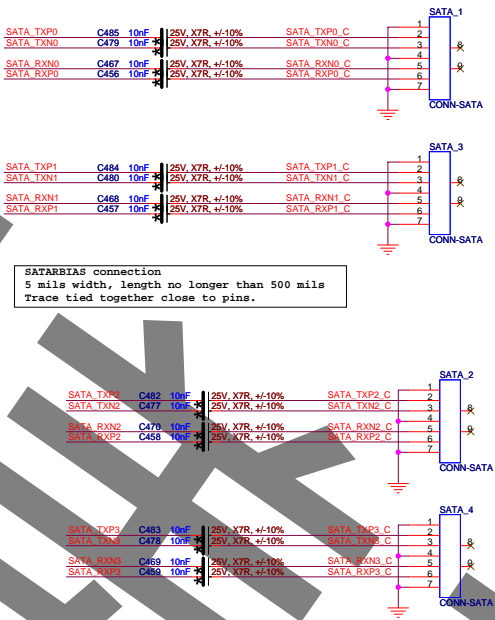
C15,C26 Near by the connector

**FOXCONN**  
FOXCONN PCEG

File: **VGA**

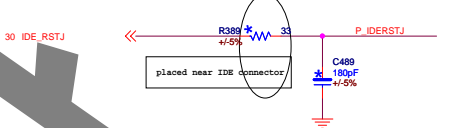
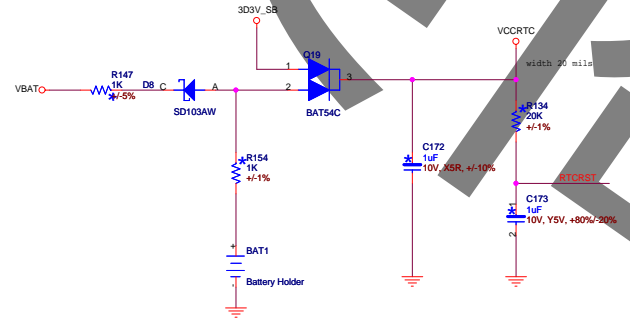
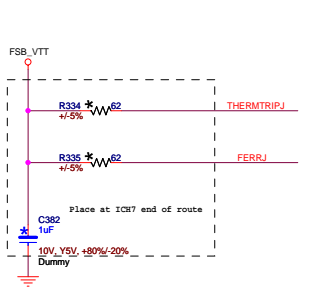
Size: C	Document Number: <b>G41M05</b>	Rev: A
Date: Friday, August 28, 2009	Sheet: 21 of 34	





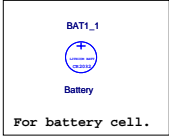
SATARBIAS connection  
5 mils width, length no longer than 500 mils  
Trace tied together close to pins.

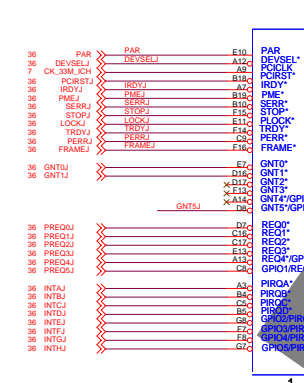
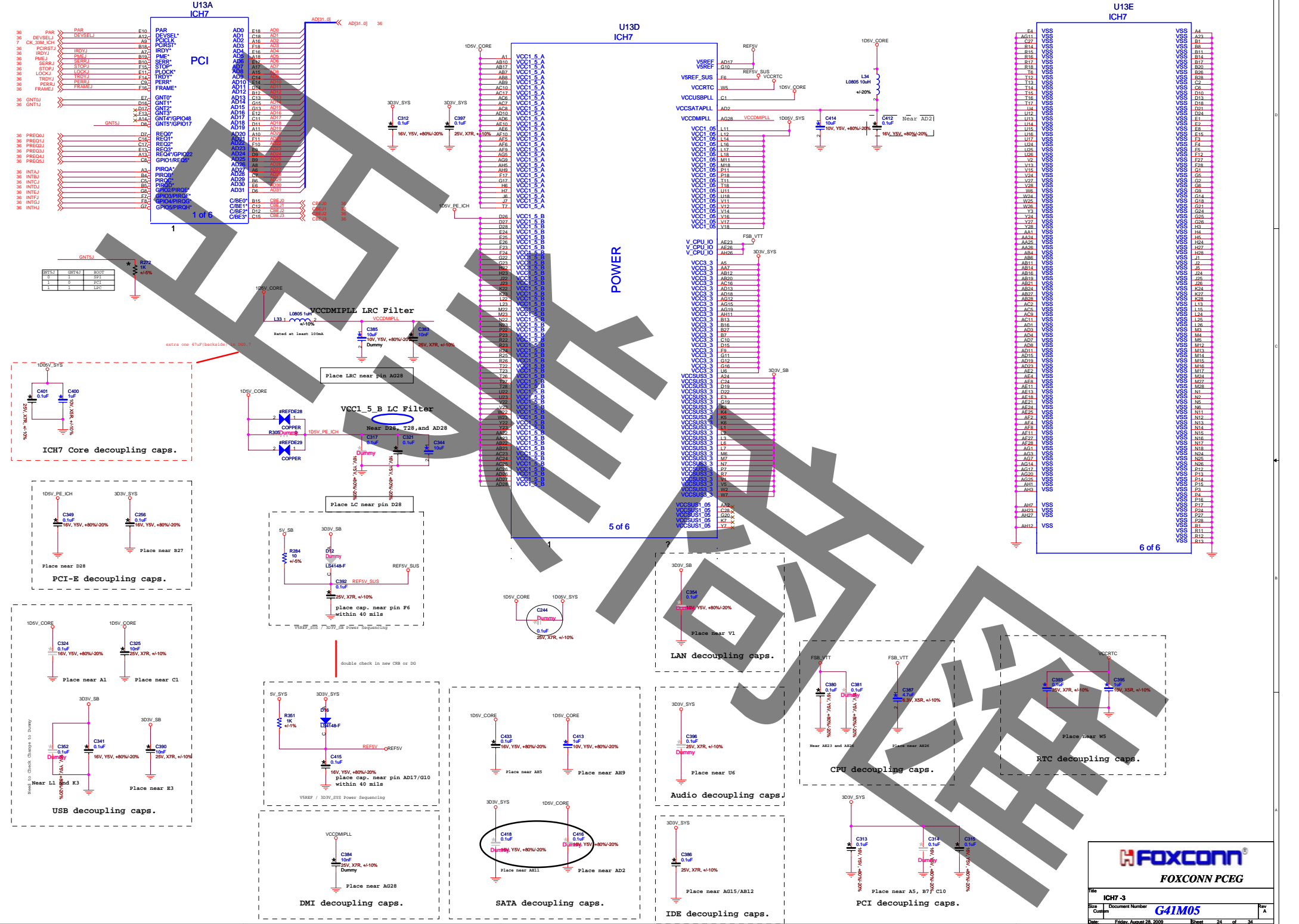
IDE data lines should be matched to strobes (IORJ, RDVW) with 100 pF capacitors. Strobes should be matched to their complement within +/- 10 mils.



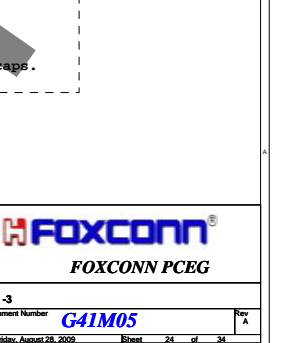
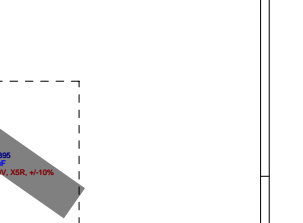
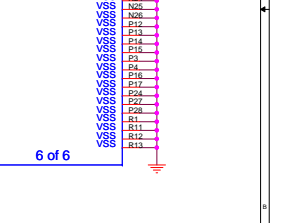
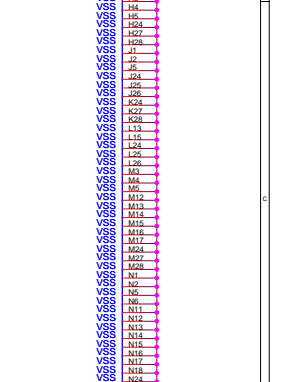
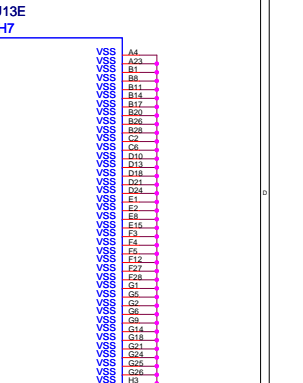
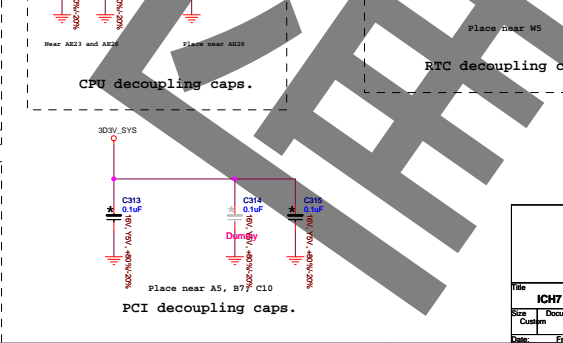
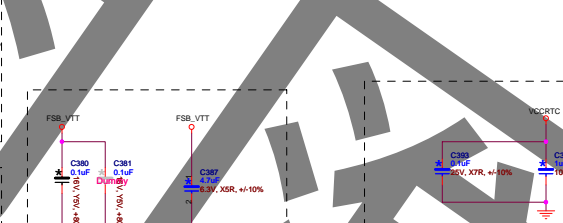
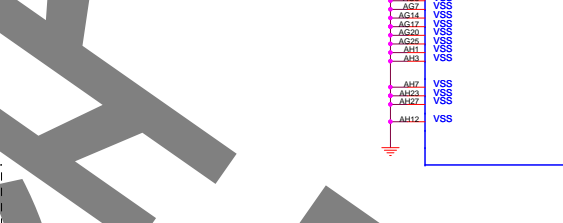
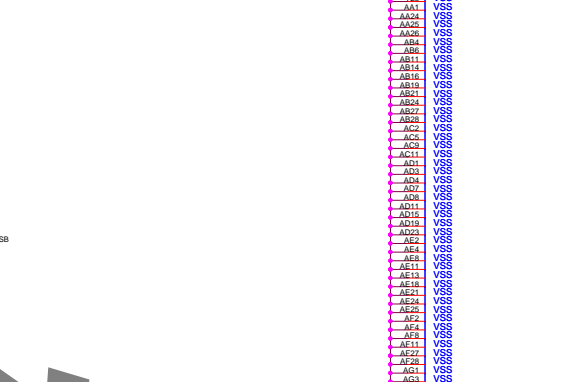
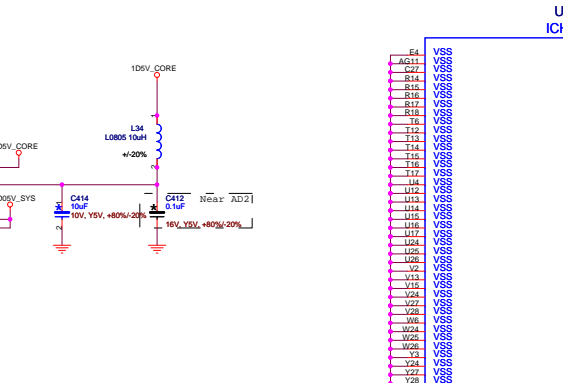
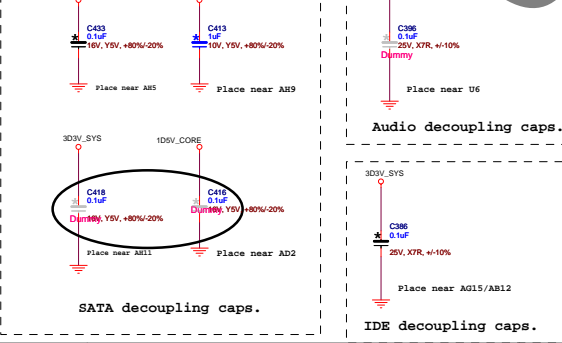
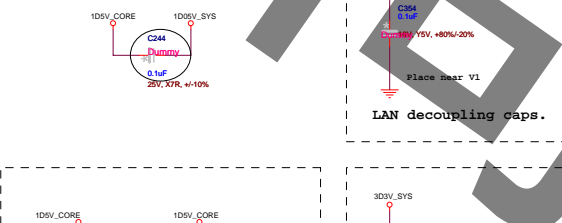
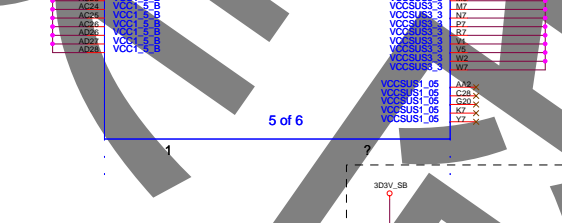
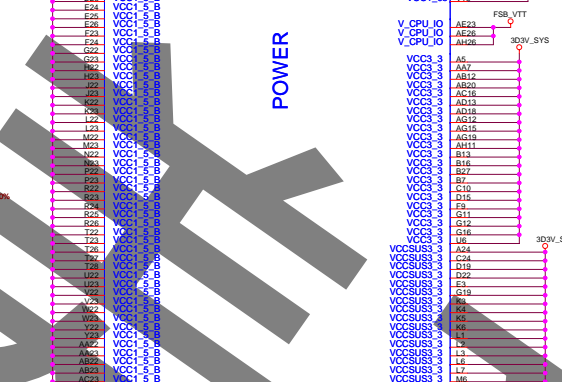
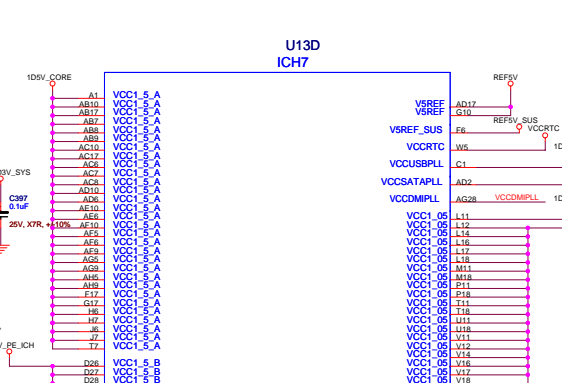
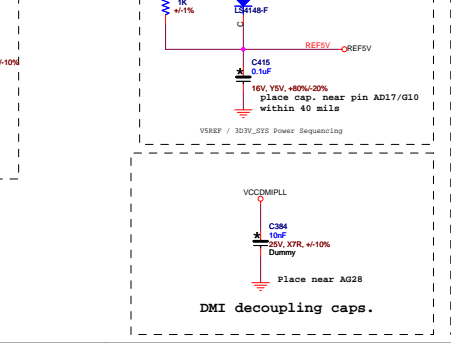
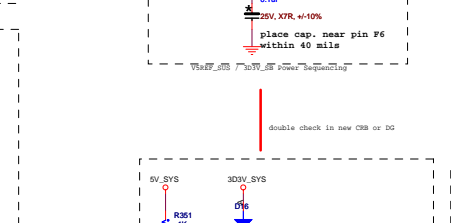
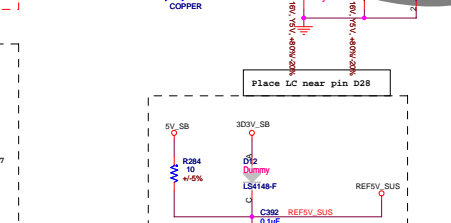
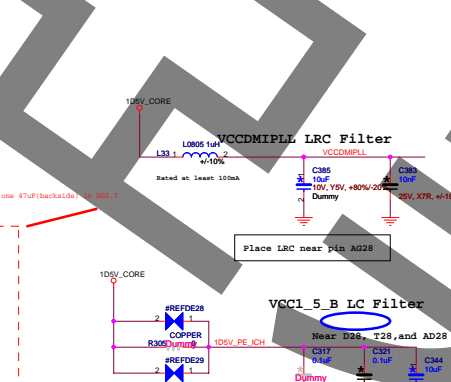
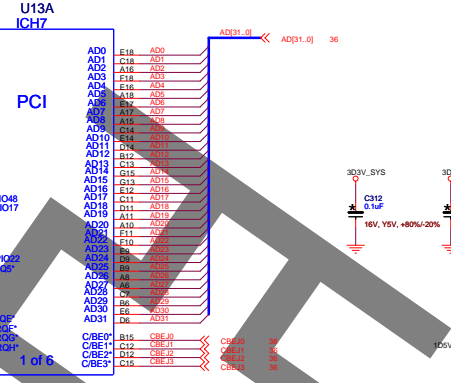
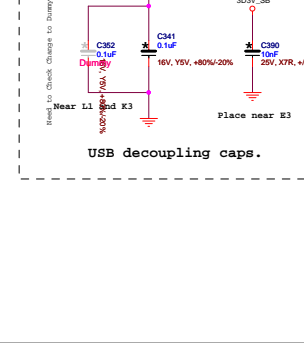
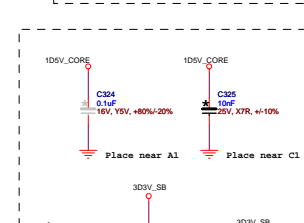
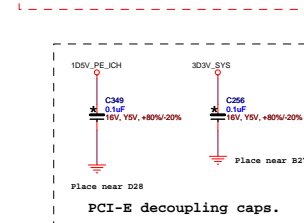
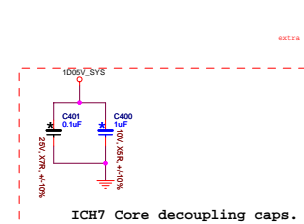
Clear CMOS

CLR_CMOS	CMOS
Clear	(1-2)
Normal	(2-3) <b>Default</b>





REFS1	GNTJ1	BOOT
0	1	SP1
1	1	SP2

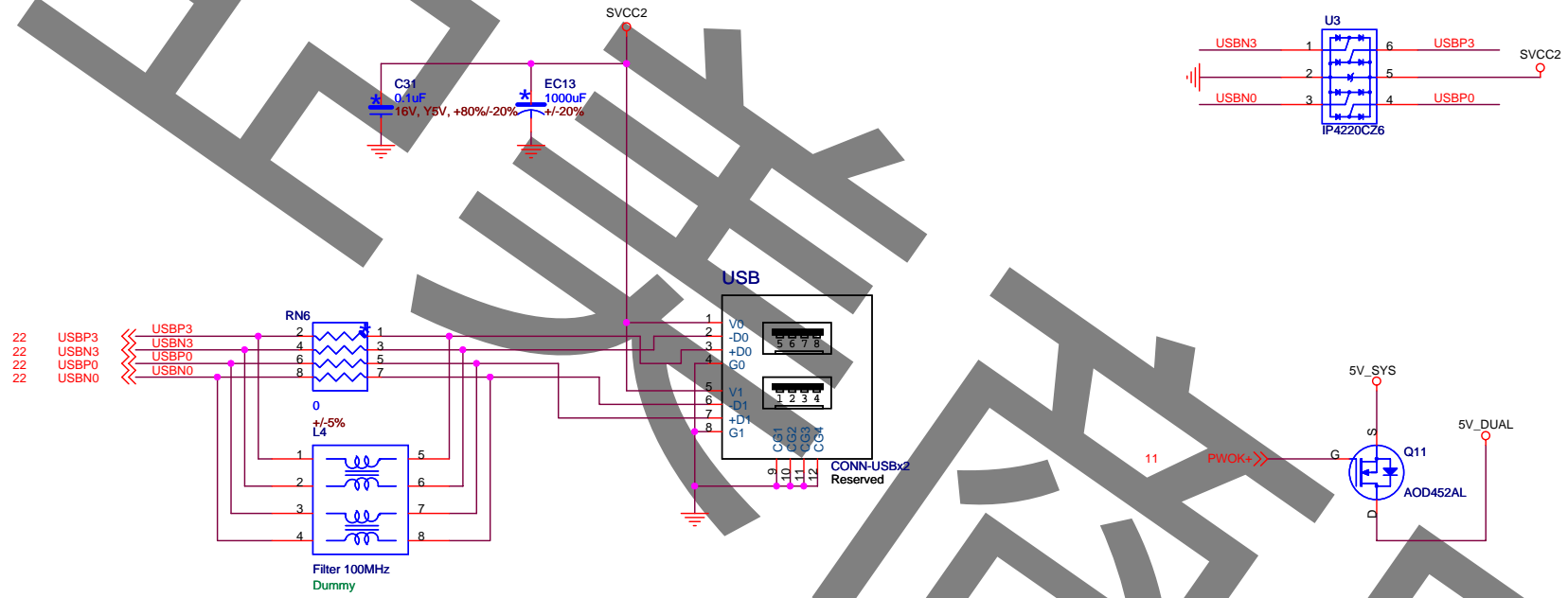


**FOXCONN**  
FOXCONN PCBG

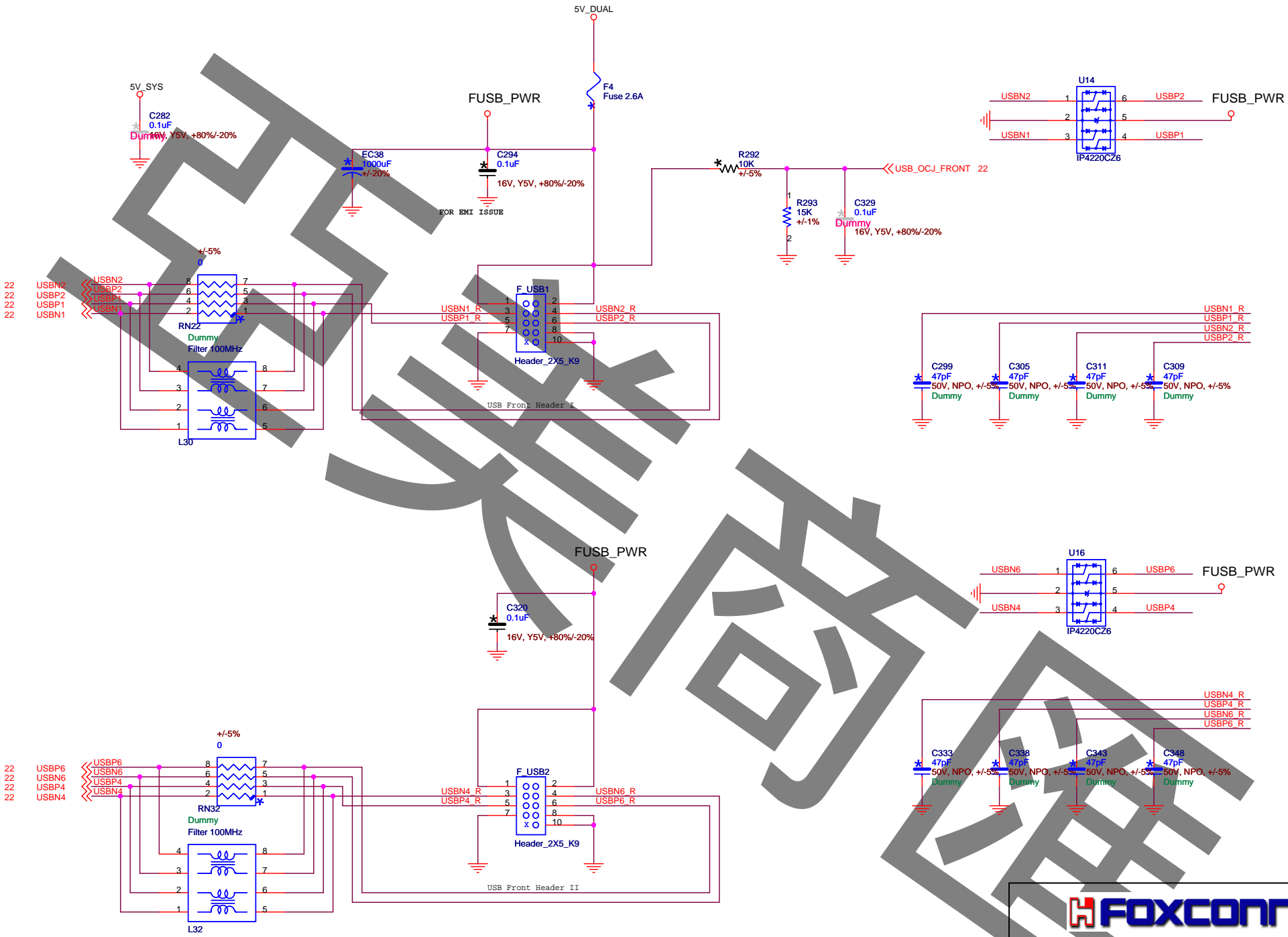
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 Size: Document Number: G41M05  
 Date: Friday, August 28, 2009 Sheet: 21 of 34 Rev: A



# Rear Dual USB Connector

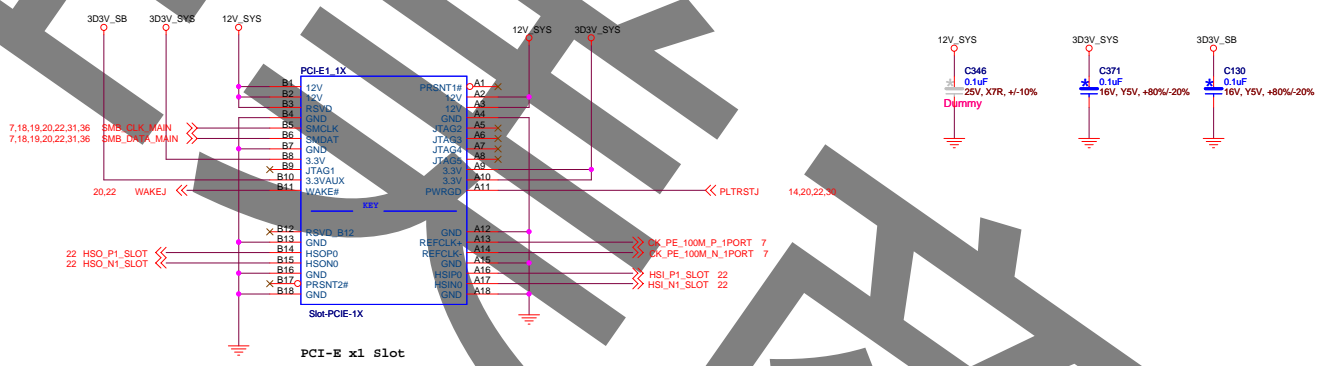


Title			REAR USB
Size	Document Number	G4IM05	
Custom			Rev A
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**FOXCONN**  
FOXCONN PCEG

Title <b>FRONT USB</b>		
Size Custom	Document Number <b>G4IM05</b>	Rev A
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FOXCONN PCEG

File: PCI Express x1Slot		
Size: C	Document Number: G41M05	Rev: A
Date: Friday, August 28, 2009	Sheet: 27	of 34

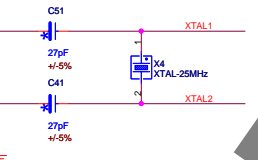
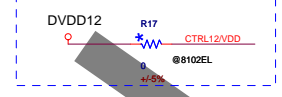
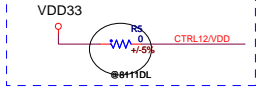
For RTL8111DL, use this block

For RTL8102EL/8103EL, use this block.

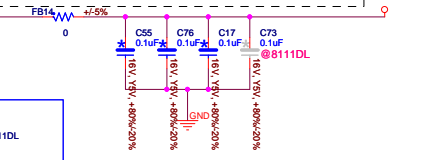
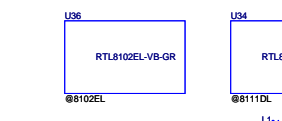
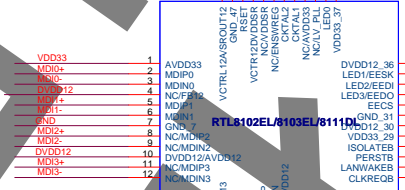
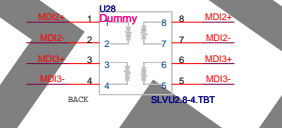
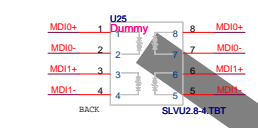
EC1 is only for RTL8111DL.

R5 and R6 are used in the RTL8111DL application. Remove R6 if switching regulator is enabled. Remove R5 if external power 1.2V is used.

C1 to C4 are for 8111DL VDD33 pins-- 1, 29, 37, 40. \* C1 to C3 are for 8102EL/8103EL VDD33 pins-- 1, 29, 37.

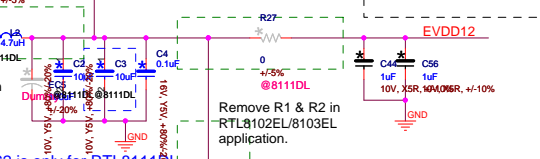


R7 value should be 2.49K (1%) for all application.



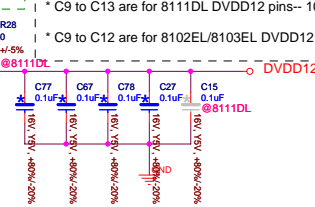
\* C6 and C7 are for U2 EVDD12 pin 19.

Change L1 to 0 ohm in RTL8102EL/8103EL application.



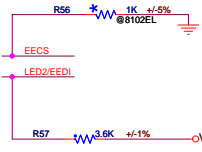
Remove R1 & R2 in RTL8102EL/8103EL application.

\* C9 to C13 are for 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.



U20 and U21 are ESD protection array Reserve for cable discharge.

R13 is only required by RTL8102EL and RTL8103EL.



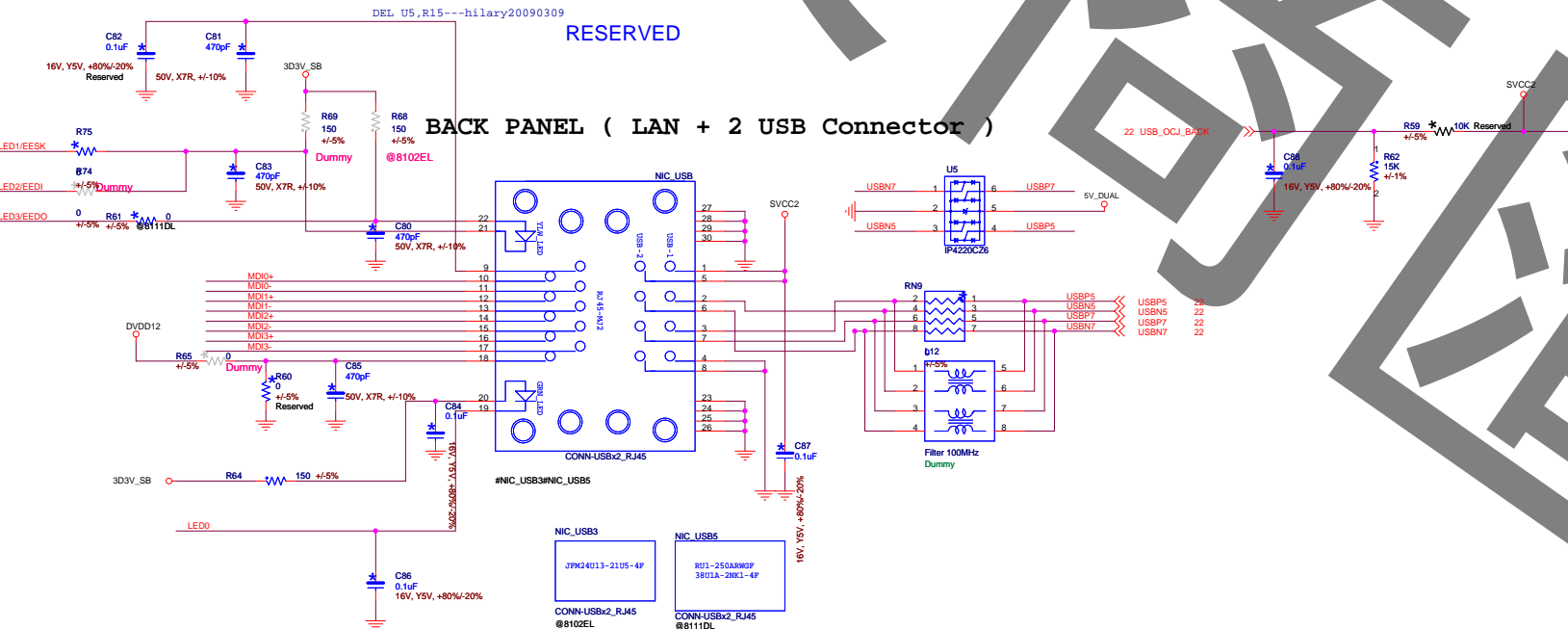
U5, R15 are only used as an independent power source for DVDD12 when switching regulator is disabled. For RTL8102EL/8103EL, remove R15 and U5.

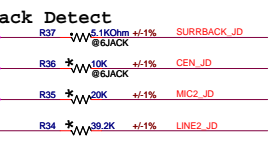
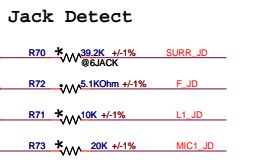
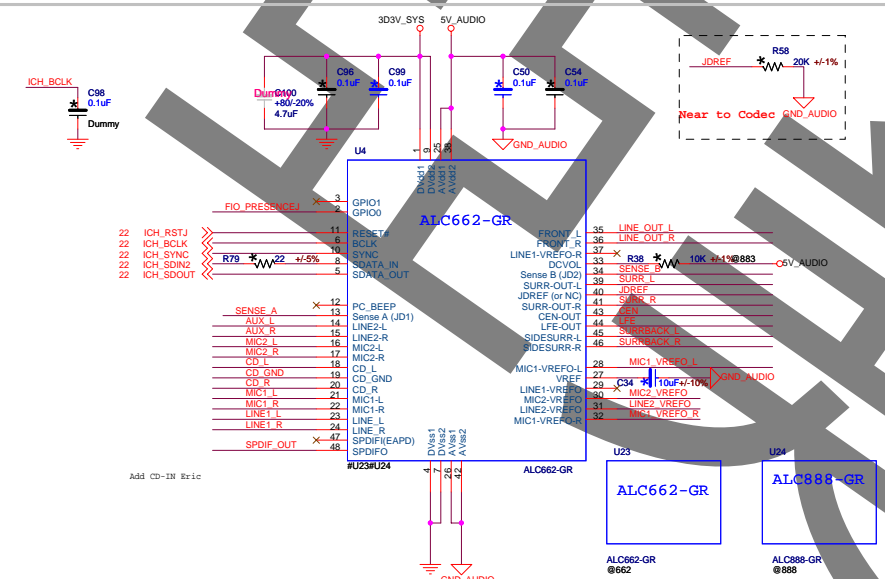
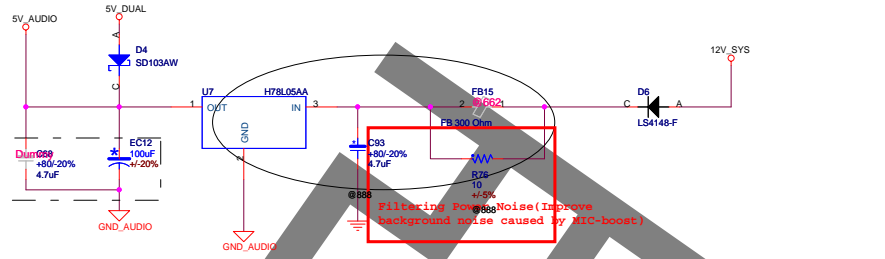
Pin 23 is GPO pin for 8111DL. It is used for DSM function.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

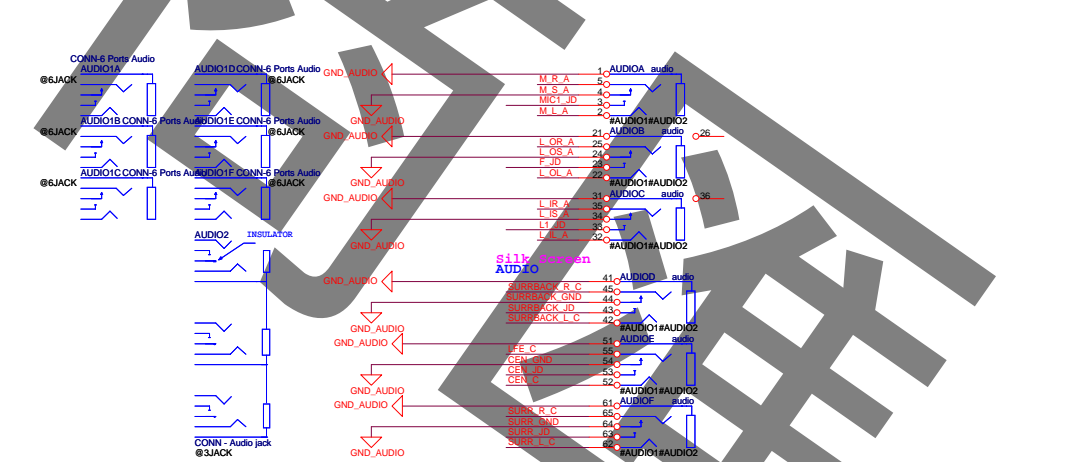
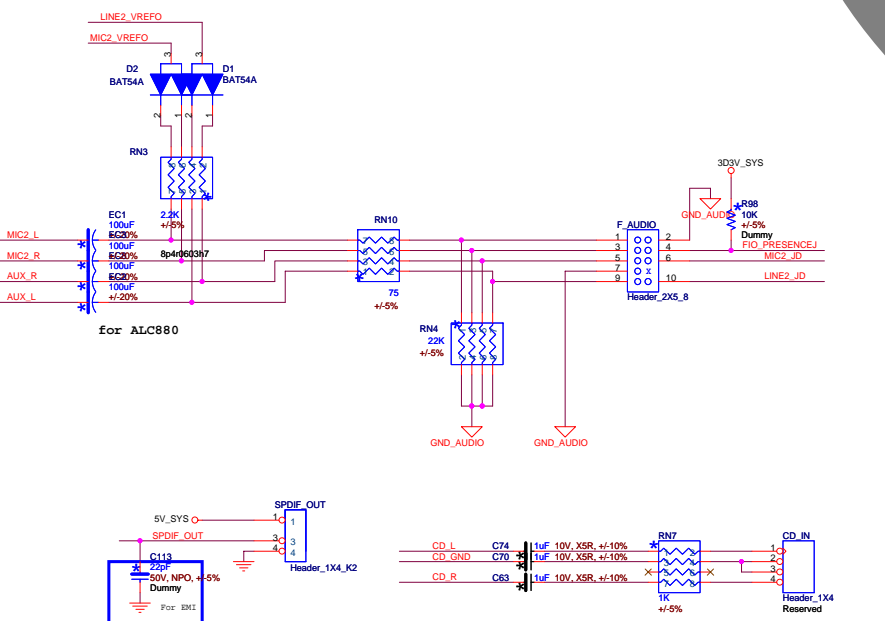
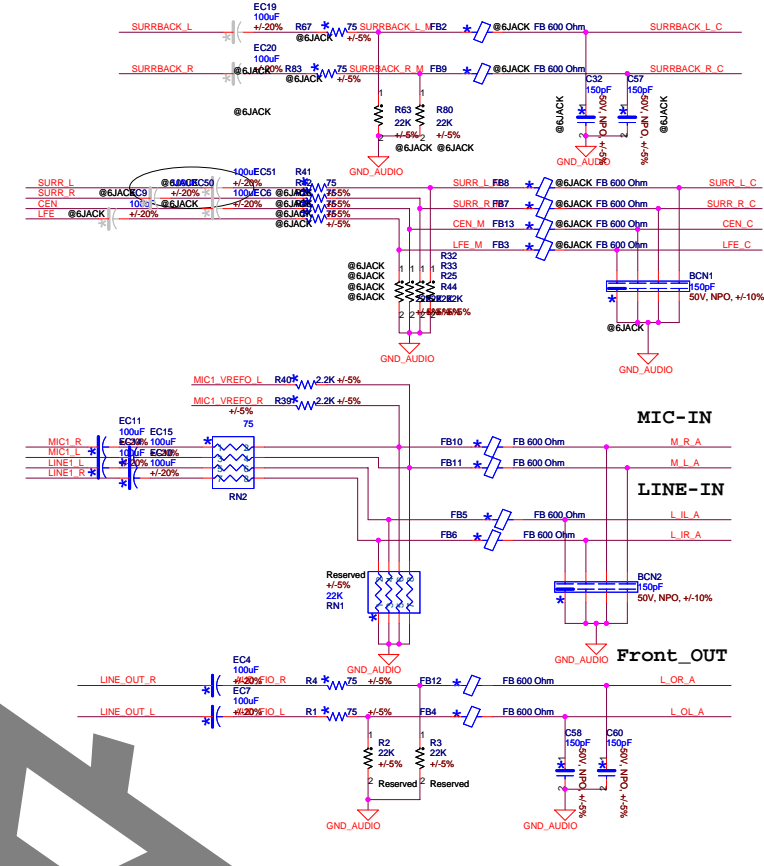
RESERVED

BACK PANEL ( LAN + 2 USB Connector )





All of JD resistors should be placed as close as possible to Codec.



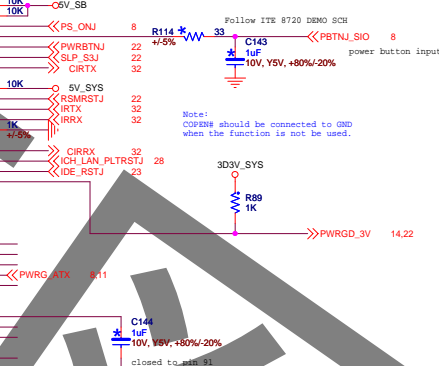
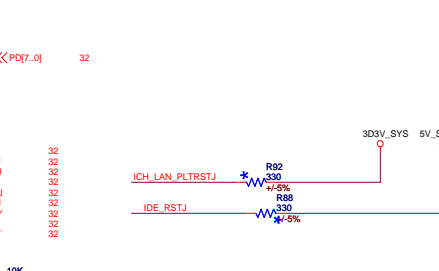
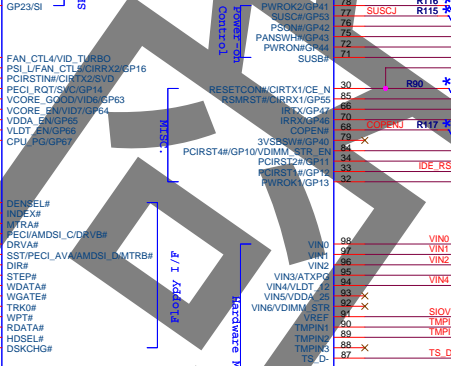
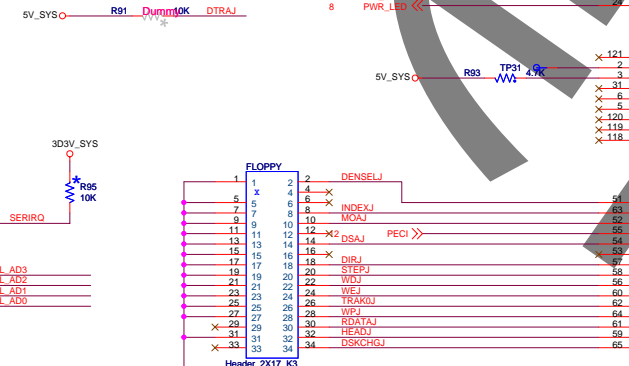
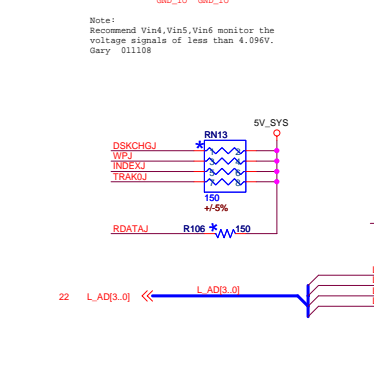
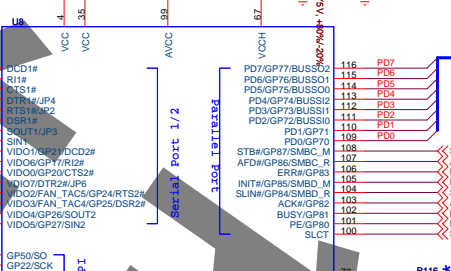
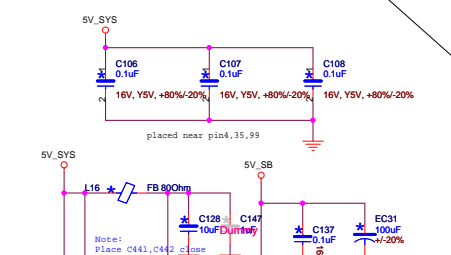
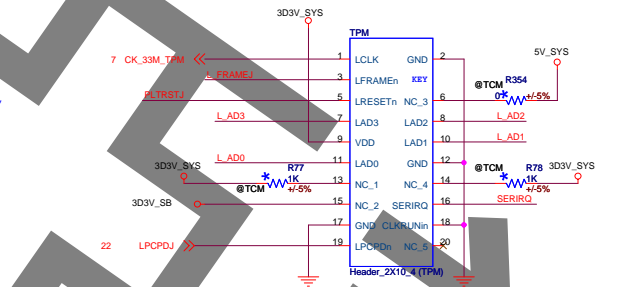
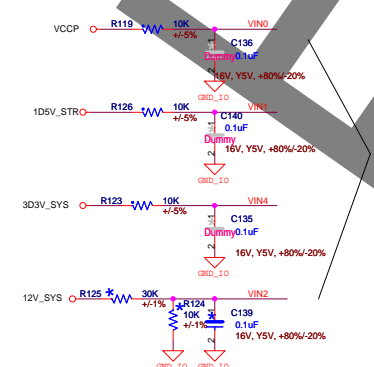
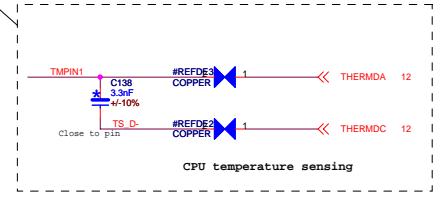
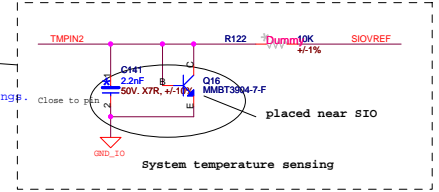
**FOXCONN**  
FOXCONN PCEG

Title: **AUDIO 655/861**  
Size: C  
Date: Friday, August 28, 2008  
Revision: **G41M05**  
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If without use these pins, Please pull-up to VCC.  
 Don't let it floating

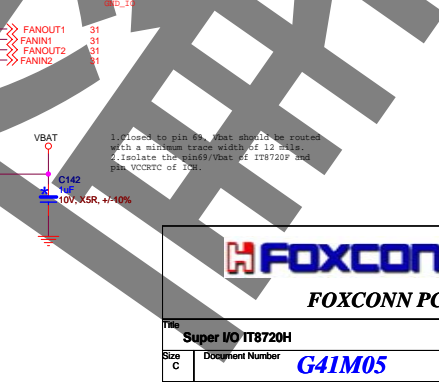
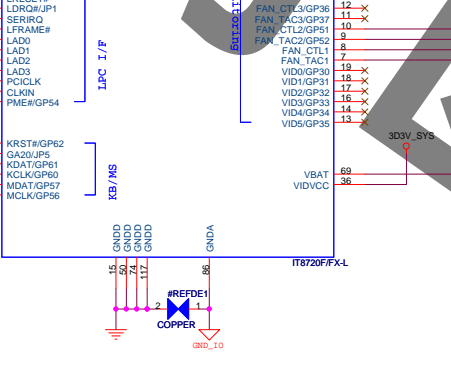
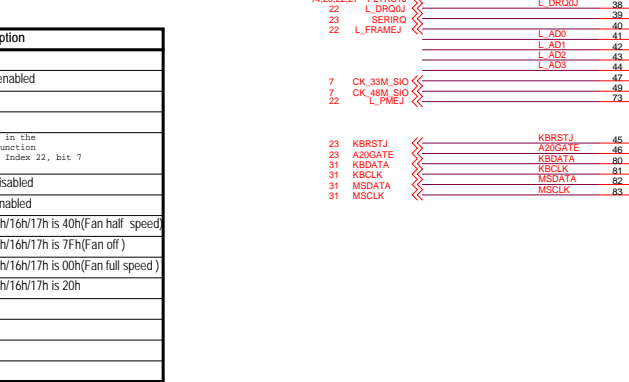
- 1.Pin 30:RESETCON#
- 2.Pin 95:VIN3/ATXPG
- 3.Pin 71:SUSB#
- 4..Power On Strapping Options pin
- 5.Please don't remove the pull-up resistor (R108) of pin38/LDRQ#.
- 6.Please don't remove any components in the VINx circuits and the FANx control circuits.
- 7.Please don't change the sequence of VIN0-VIN6.
- 8.If without use these pins,please pull-up to VCC, Don't let it floating ,pin 3, pin 30, pin 38, pin 46, pin 95, pin 122, pin 124, pin 129.

For the temperature sensor circuits,  
 1)Please don't remove the 1uF capacitor(C620) between Vref and AGND.  
 2)Place R568 close to IT8720P.  
 3)Keep the trace away from +12V, fast data bus, and CRTS.  
 4)Recommended trace 10mils widths and 12 mils spacing.  
 5)Isolate AGND and DGND.



**IT8720 Power On Strapping Options**

JP1	Symbol	value	Description
Pin 38	Flashseg1_EN	1	Disabled.
JP2	VIDO_EN	1	Disable VID output pins
Pin 122	VIDO_EN	0	Enable VID output pins
JP3	CHIP_SEL		Use for chip 1 when two 178718P exist in the same system. Chip is selected in conjunction with Global Configuration Register - Index 22, bit 7
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 126	K8PWR_EN	0	K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
Pin 124 & 46	FAN_CTL_SEL	10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
	FAN_CTL_SEL	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
	FAN_CTL_SEL	00	The default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1	Disable WDT to rest PWROK
Pin46	WDT_EN	0	Enable WDT to rest PWROK
JP6	SVID_EN	1	Disable SVID Function
Pin29	SVID_EN	0	Enable SVID Function



**FOXCONN**  
 FOXCONN PCEG

Super I/O IT8720H

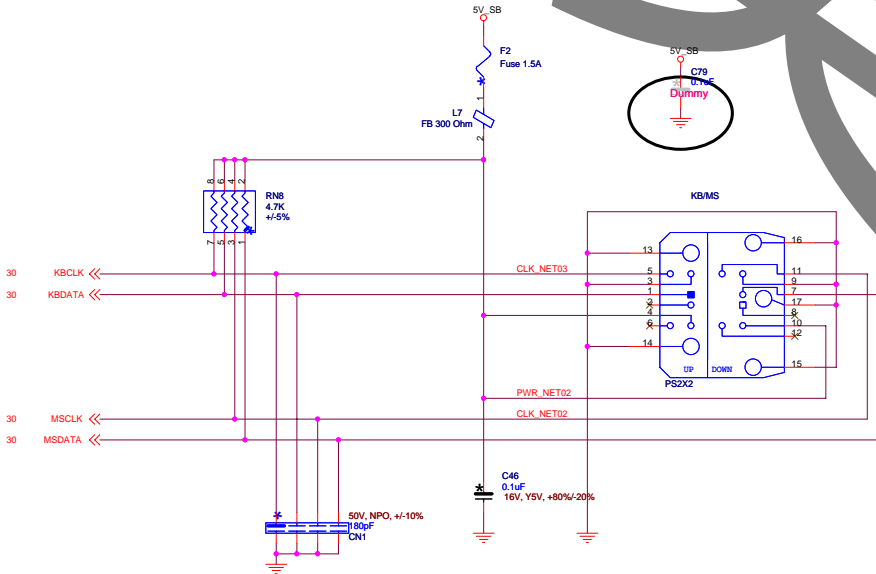
Size C Document Number **G41M05** Rev A

Date: Friday, August 28, 2008 Sheet 30 of 34

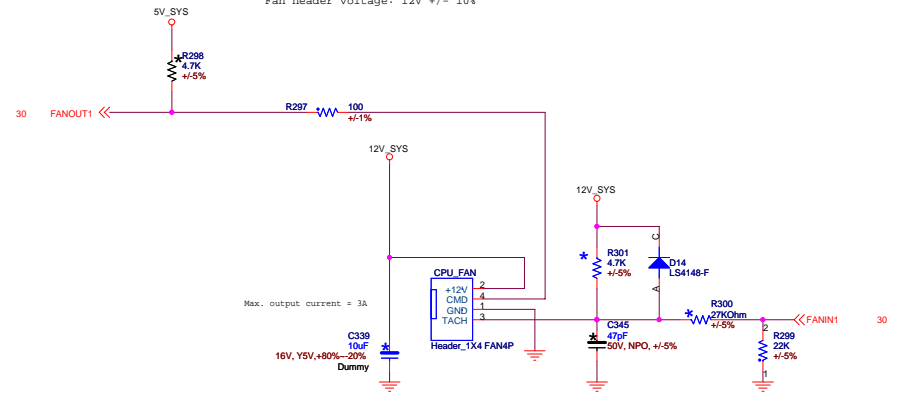
# SM Bus Bridge



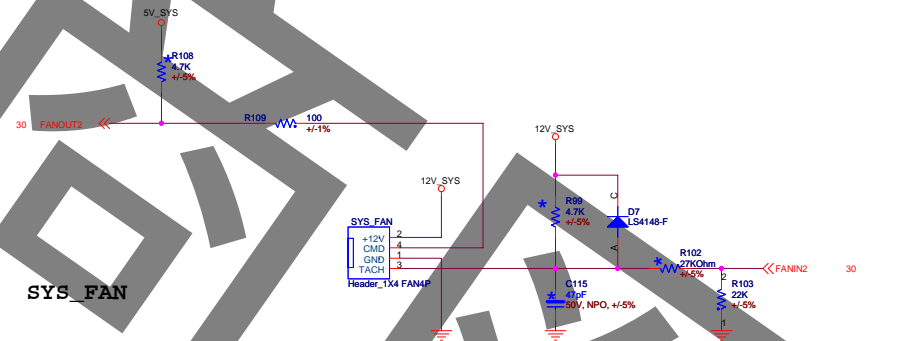
# KB\MS



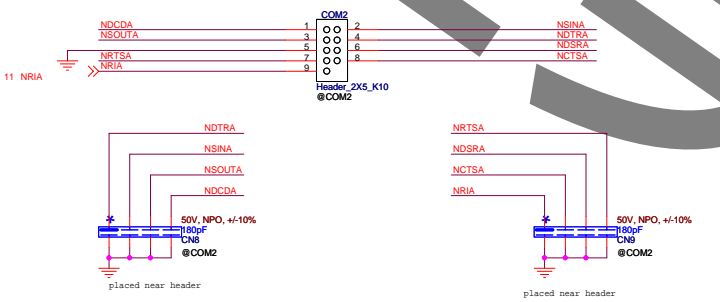
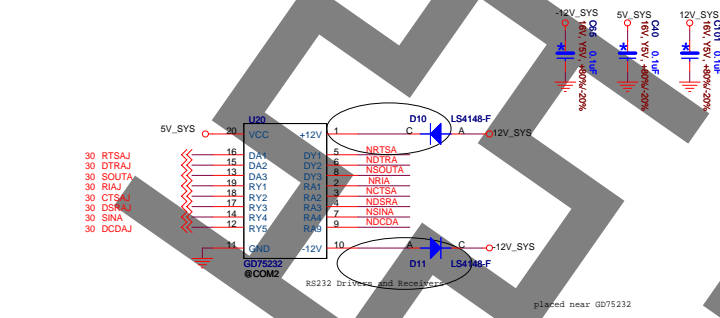
# CPU FAN



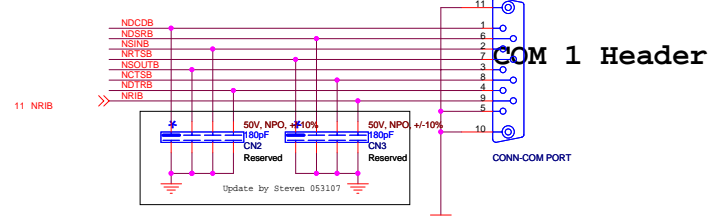
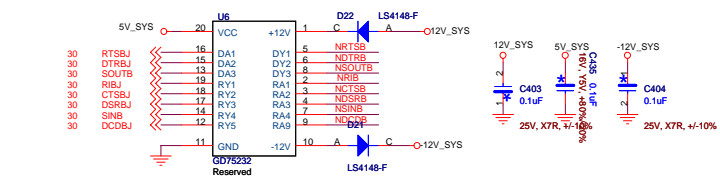
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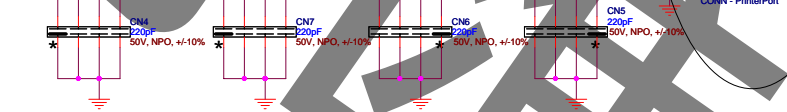
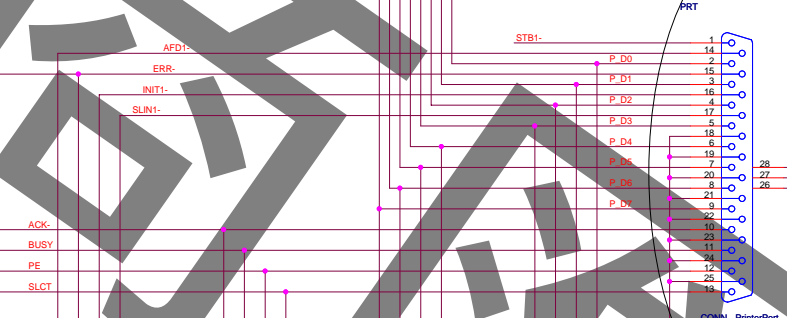
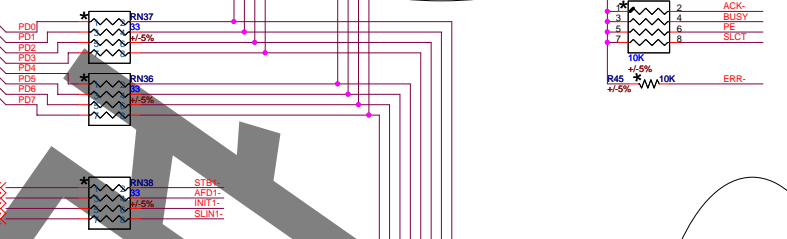
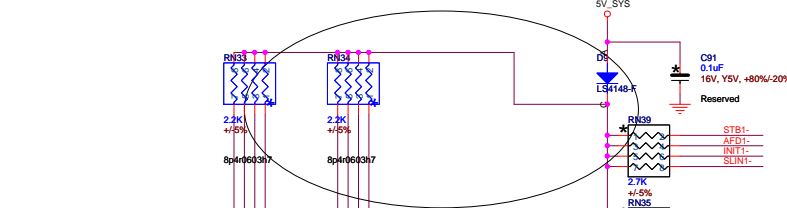
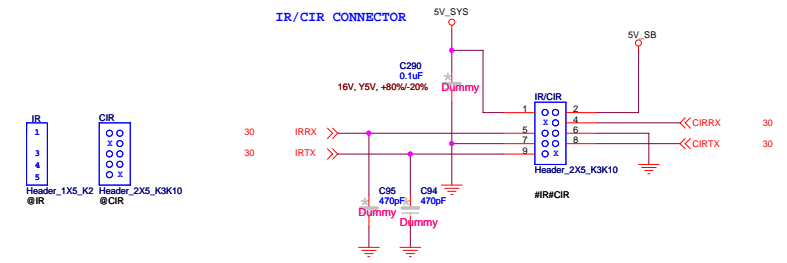
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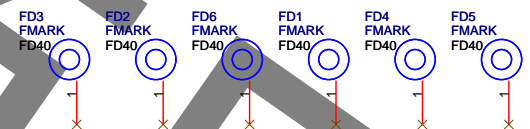
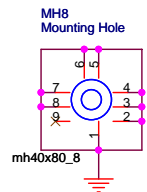
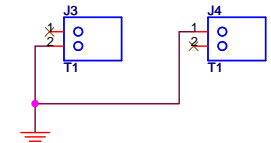
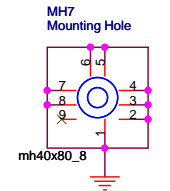
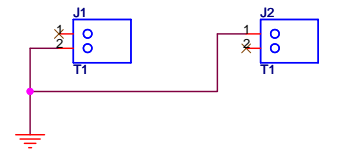
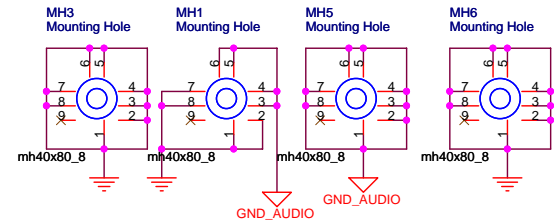
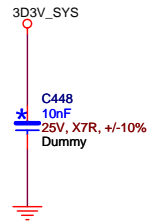
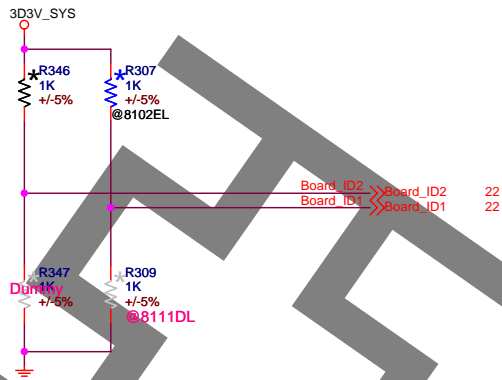
COM 2 Header



COM 1 Header







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change C23 to 10uF follow Realtek advice. 11/28  
change EC5,EC12,EC14 to 6.3v/1000uF. 11/28

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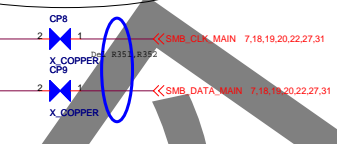
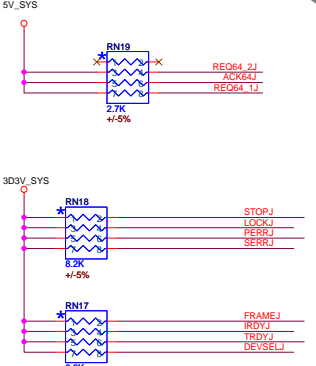
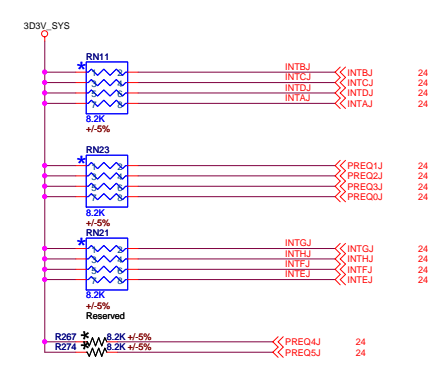
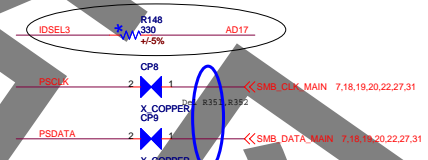
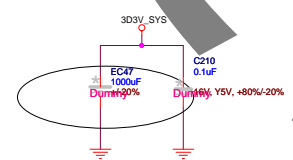
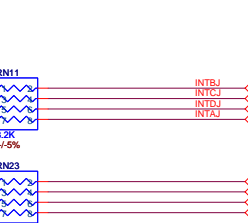
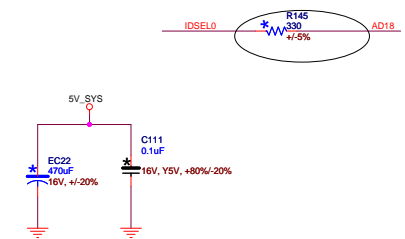
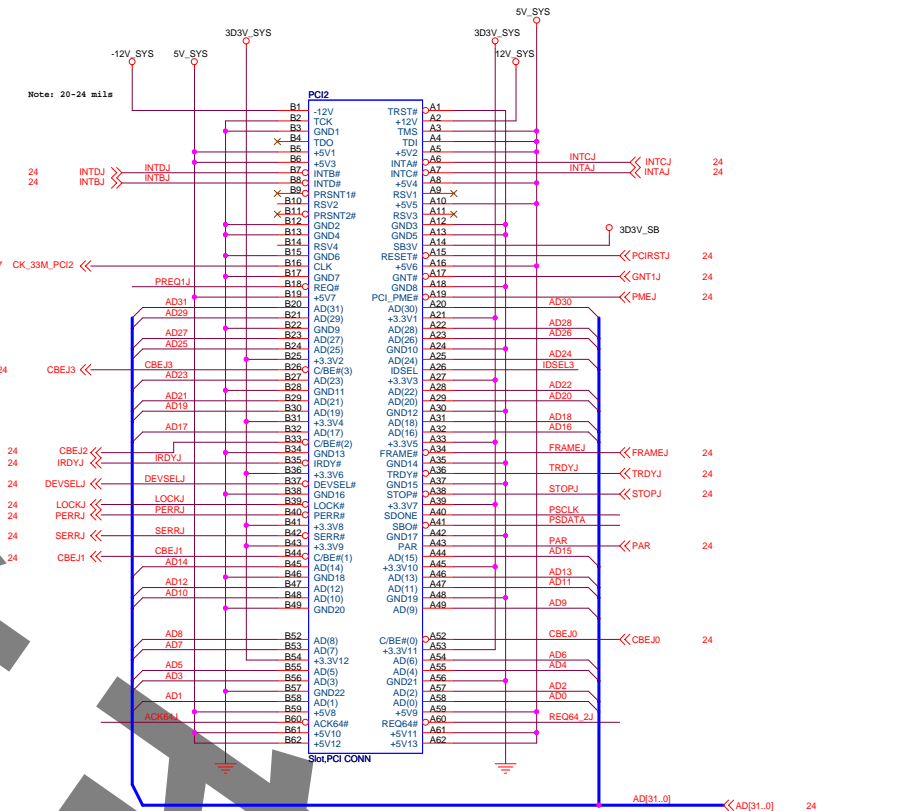
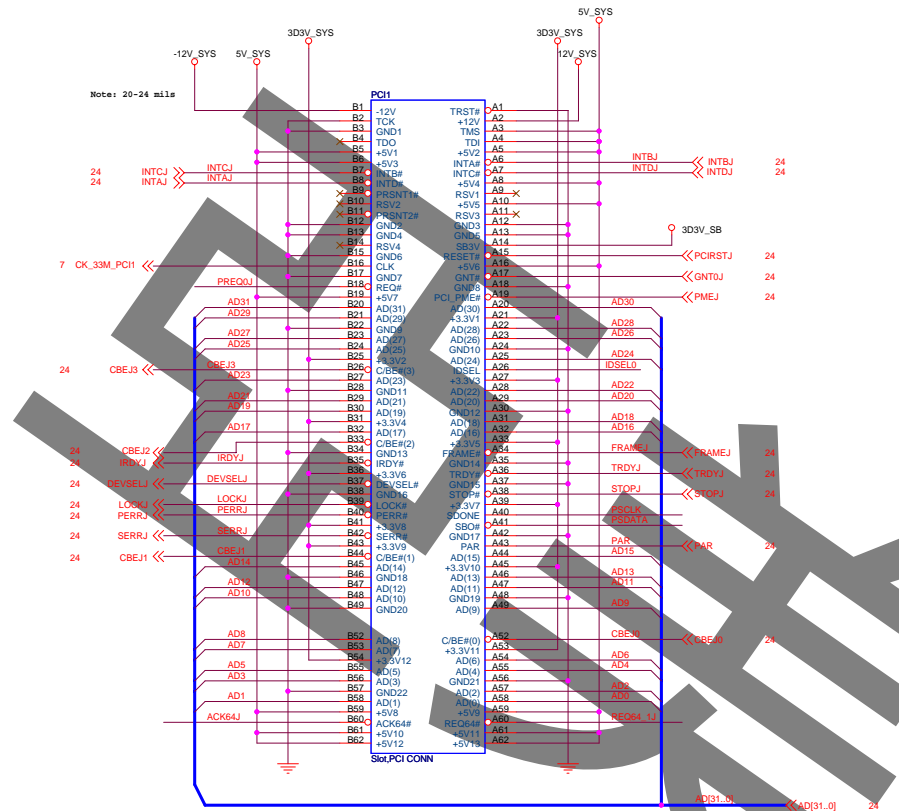
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