LV3D-14" Block Diagram -- Intel Chief River ULV

01

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

POWER

DC/DC 3VPCU, 5VPCU, +15V	Page 37
REGULATOR (DDR3) 1.5VSUS, +0.75V_DDR_VTT	Page 38
REGULATOR +1.05V&+1.8V	Page 39,40
REGULATOR +VCCSA	Page 41
CPU Core +VCC_CORE & +VCC_GFX	Page 45
Charger VIN	Page 36
RUN POWER SW/Discharge 3VSUS,5VSUS, 3V_S5, 5V_S5, +3V, +5V	Page 46
dGPU Core GFX_CORE	Page 44

DDR3 SO-DIMM 1 (STD) Page 13

DDR3 SO-DIMM 1 (RVS) Page 14

Intel Chief River
Ivy Bridge
(Sandy Bridge)
31mmX24mm, BGA
Duo Core, 17W, ULV
Page 3,4,5,6

GPU
nVIDIA
N13M-GS
6B2-64
23mmX23mm
15W-20W
Page 15,16,17,18

27MHz

1GB VRAM
DDR3 2Gb x 4
FBGA96
Page 19

CPU Thermal Sensor

GPU Thermal Sensor

UM77 only

LVDS

eDP/LVDS Converter Page 20

eDP

14" HD (1366x768) LCD Page 21

FDI

X4 DMI

LVDS

PCH
Panther Point
HM77/UM77
25mmX25mm, BGA
Page 7,8,9,10,11,12

mDP Page 22

DP

HDMI Page 23

DP

HP/Mic Audio Jack Page 24

HDA CODEC ALC3203-GR Page 24

HD Audio

Internal MIC Page 24

Internal SPK Page 24

SPI Flash (8MB) x 2
(One for BIOS, one for Intel SBA)
Page 8,49

PCI-e

Card Reader Conn
Realtek RSS5209-GR Page 32

4 in 1 Socket
SD/SDHC/SDXC/MMC

PCI-e/USB

Mini PCIe Slot Page 28

WLAN+BT Module

PCI-e

1G Ethernet
RTL8111F-CG Page 25

RJ-45 Page 25

25MHz

SATA

2.5" HDD /SSD Module
(Option) Page 26

SATA HDD Re-driver
SN75LVCP600DRF Page 26

SATA

USB2.0

Mini PCIe Slot Page 29

mSATA SSD

WWAN module

SIM Page 29

either one

USB3.0

USB 3.0 PORT X 2 Page 27

USB2.0

Camera Conn Page 32

Camera Module

USB2.0

Bluetooth(Reserved) Page 32

USB2.0

FingerPrint
TCS5DA6C0 Page 31

32.768KHz

LPC BUS

SPI Flash (512K) Page 34

IT8518 Page 34

TPM Page 30

Accelerometer (APS) Page 30

Int. KB Page 31

T/P Page 31

Battery (Polymer) Page 56

Charger Page 36

Quanta Computer Inc.
PROJECT : LV3D
Size | Document Number: System Block Diagram | Rev 1A
Date: Monday, March 12, 2012 | Sheet 1 of 56

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07-12	Panther/Cougar Point-PCH
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15-18	N13M-GS
19	N13M VRAM
20	PS8622 LVDS converter
21	LCD CONN
22	MIni DisPlay Port
23	HDMI CONN
24	AUDIO (ALC3202-VC3-GR)
25	LAN_RTL8111F-CG
26	SATA HDD
27	USB3.0 x 2
28	WLAN/BT
29	WWAN(SSD)
30	G-SENSOR/TPM/RFID
31	KB/TP/FP
32	BB CON/LED/CCD
33	FAN & THERMAL
34	KBC IT8518/19
35	Screw Hole/EMI/ESD
36	CHARGER (BQ24737)
37	SYSTEM 5V/3V (TPS51123)
38	1.5V_SUS/VTT (TPS51216)
39	+1.05V(TPS51219)
40	+1.8V (UP0104SSW8)
41	VCCSA (RT8241DZQW)
42	+1.5VGPU/+1.05V_GPU
43	+3V_GPU
44	VGA (ISL62882C) 1 PHASE
45	VCC_CORE (ISL95837)
46	POWER_Discharge
47	SBA Block
48	SBA M3 Power(RT8068A)
49	Circuit for Intel SBA
50	

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	21,36,37,38,39,41,44,45,46	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0~S5
3VPCU	+3.3V	7,8,21,25,28,32,34,36,37,39,40,46,48,49	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	21,36,37,38,39,40,41,42,43,44,46,48	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	21,30,32,37,38,42,43,46,48	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	25,46	LAN POWER	LAN_ON	
5V_S5	+5V	11,27,46	PCH SUS POWER	S5_ON(AC only)	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,28,30,32,34,46 .	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON(AC only)	S0~S3
1.5V_SUS	+1.5V	3,11,13,14,38,42,46	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,38,46	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,21,22,23,24,26,31,32,33,45,46	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,20,21,22,23,24,25,26 28,29,30,31,32,33,34,37,38,39,41,43,45,46 49	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX	+0.65V~+1.25V	5,45,46	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,41,46	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,40,46	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,20,39,42,45,46,49	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,45,46	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	21	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	36	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,38,46	DDR3 1.5V Rails	PS_S3CNTRL	S0

Quanta Computer Inc.

PROJECT : LV3D

Size	Document Number	Rev
	FRONTPAGE	1A

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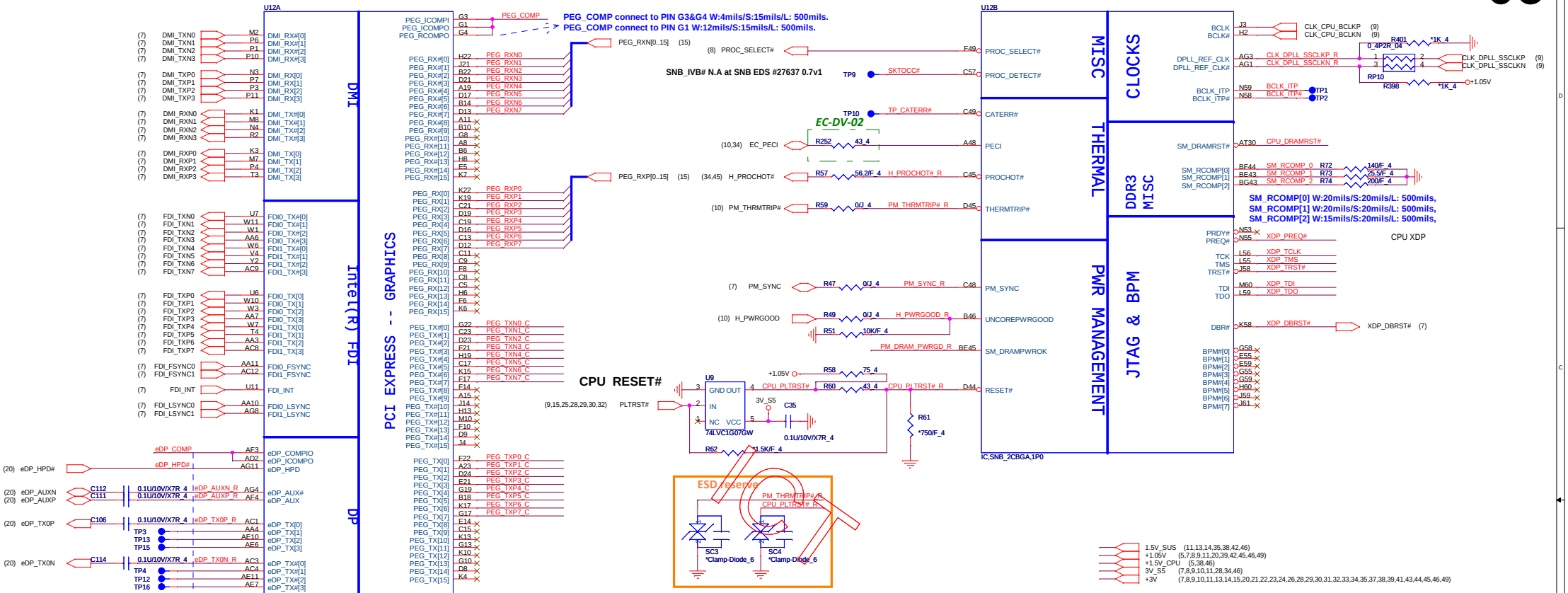
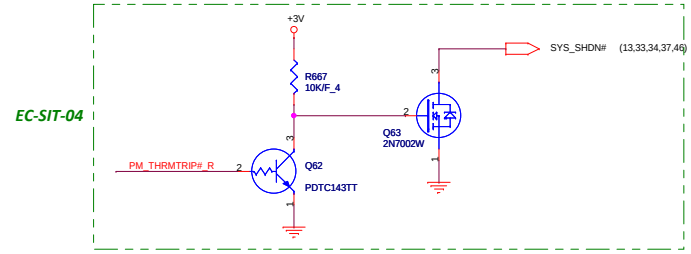
Ivy/Sandy Bridge Processor (DMI,PEG,FDI)

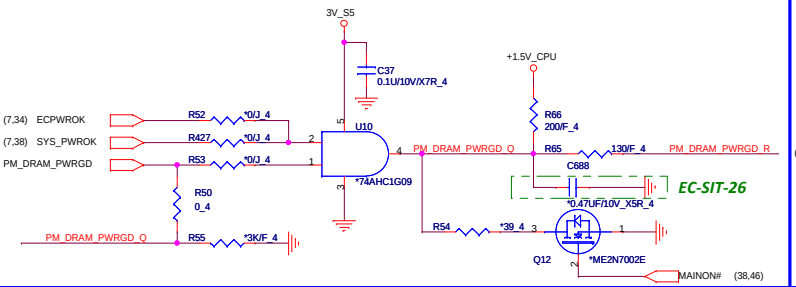
Ivy/Sandy Bridge Processor (CLK,MISC,JTAG)

03

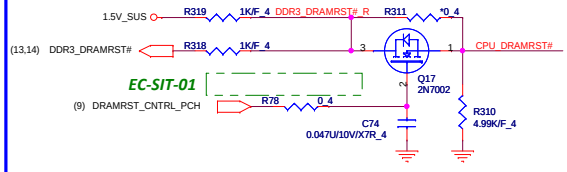




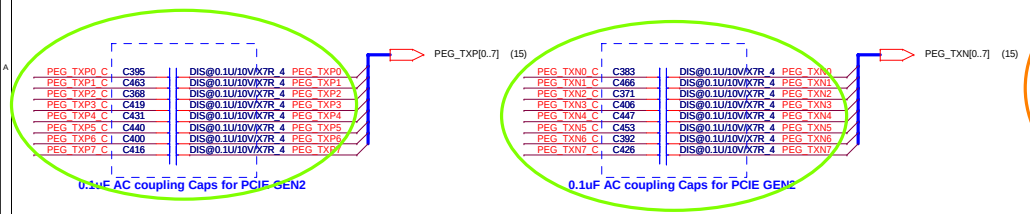
SM_DRAMPWROK Processor Input.

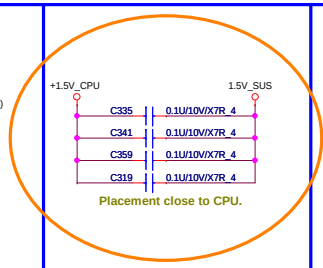


DDR3 DRAM RESET



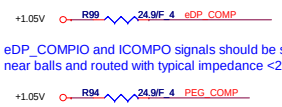
PEG x16 (UMA Non-stuff)





DP & PEG Compensation

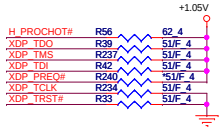
EC-DV-27



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



Quanta Computer Inc.

PROJECT : LV3D

Size	Document Number	Rev
	IVY 1/4 (PCIE&DMI&FDI)	1A
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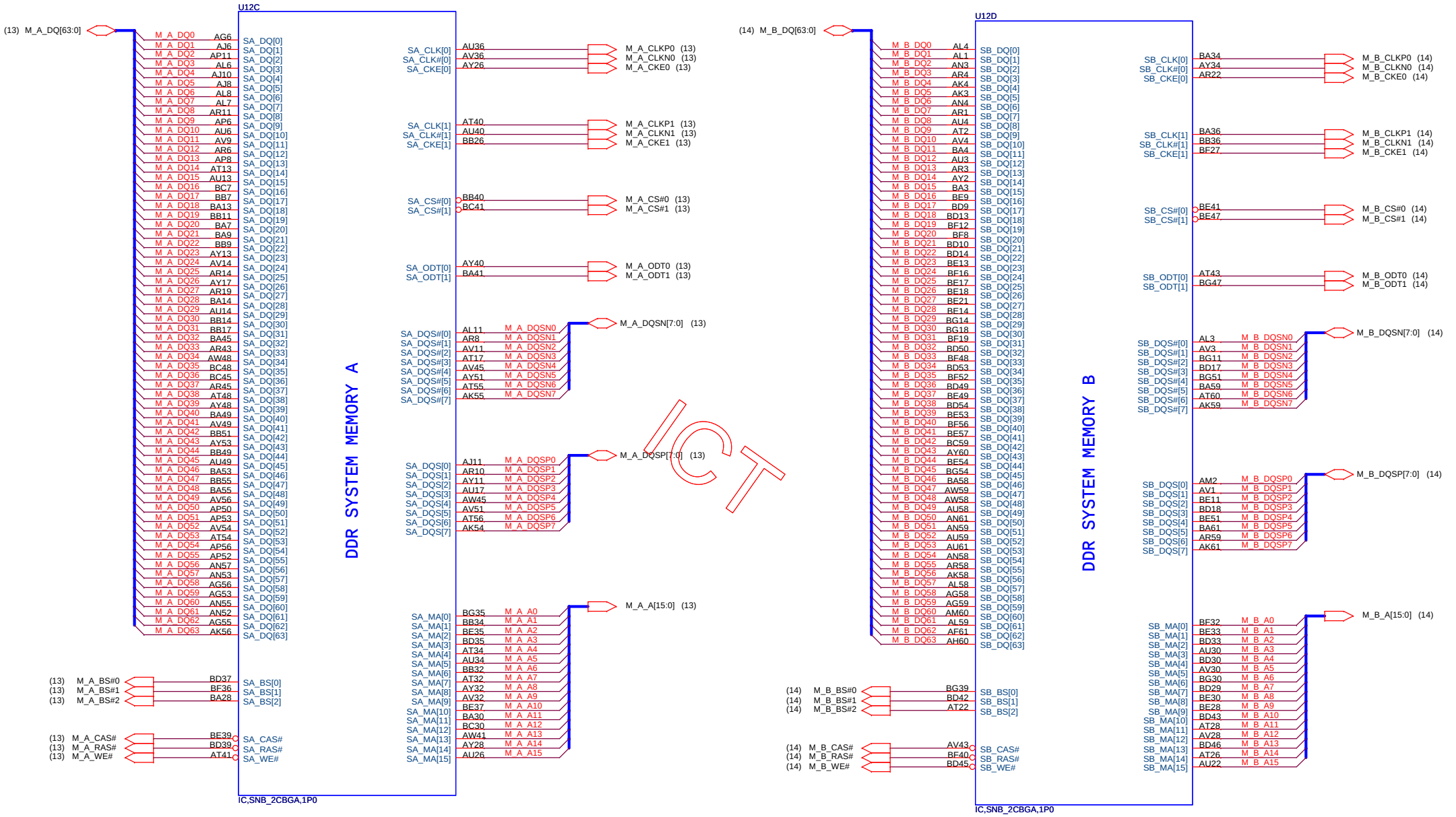
Ivy/Sandy Bridge Processor (DDR3)

04



Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: IVY 2/4 (DDR3 I/F)	Rev: 1A
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Ivy/Sandy Bridge Processor (POWER)

Ivy/Sandy Bridge Processor (GRAPHIC POWER)

05

330uF locate power side

CPU Core Power

IVB:33A

8.5A

33A

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

5A

3.3V_SUS?(PDDG p127)

1.2A

SNB:6A

SNB_IVB# N.A at SNB EDS #27637 0.7v1

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

SVID CLK

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR EC-DV-06

SVID DATA

Place PU resistor close to CPU

EC-DV-03

Place PU resistor close to VR

SVID ALERT

Place PU resistor close to CPU

Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number	Rev
	IVY 3/4 (POWER)	1A
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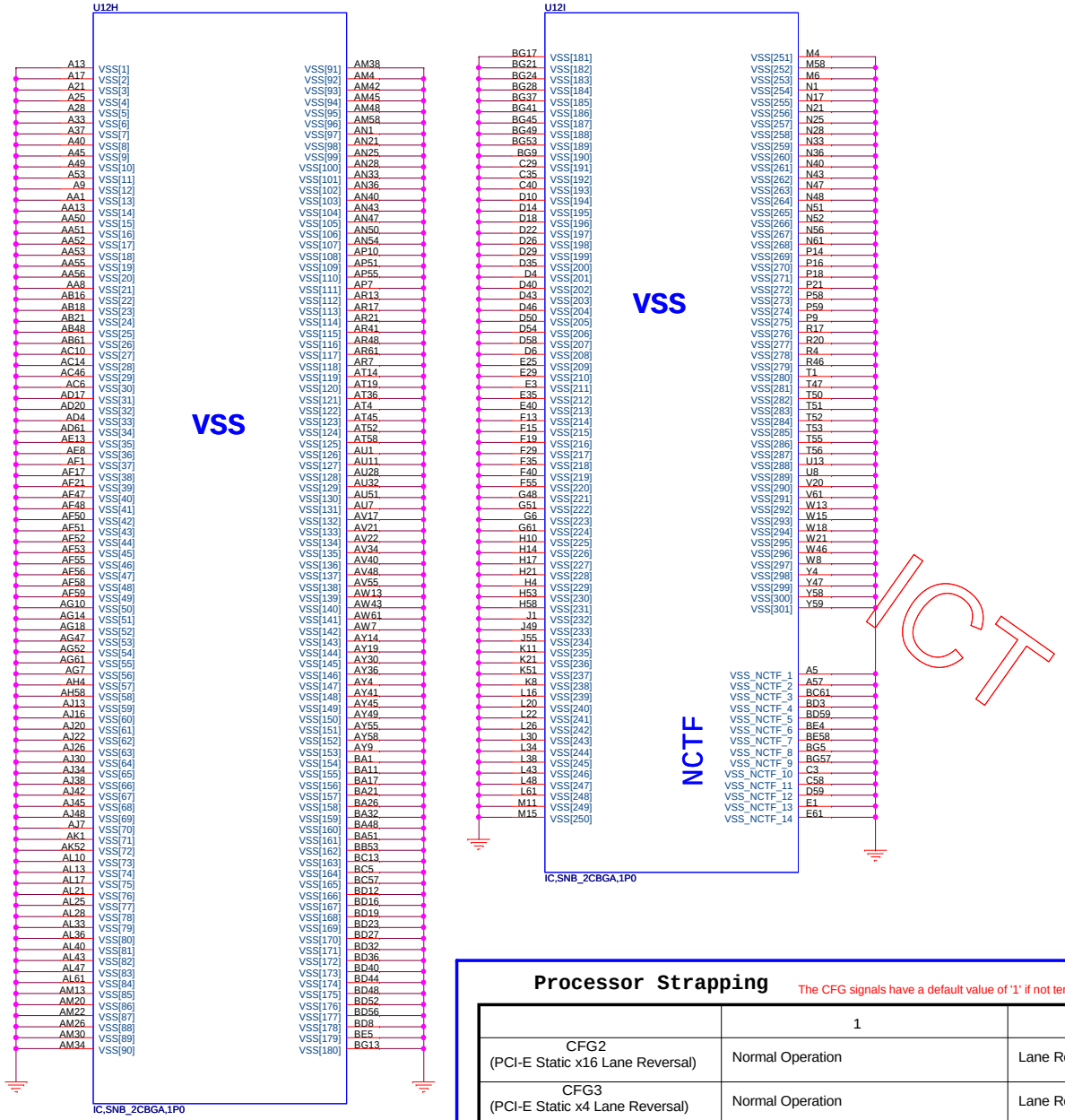
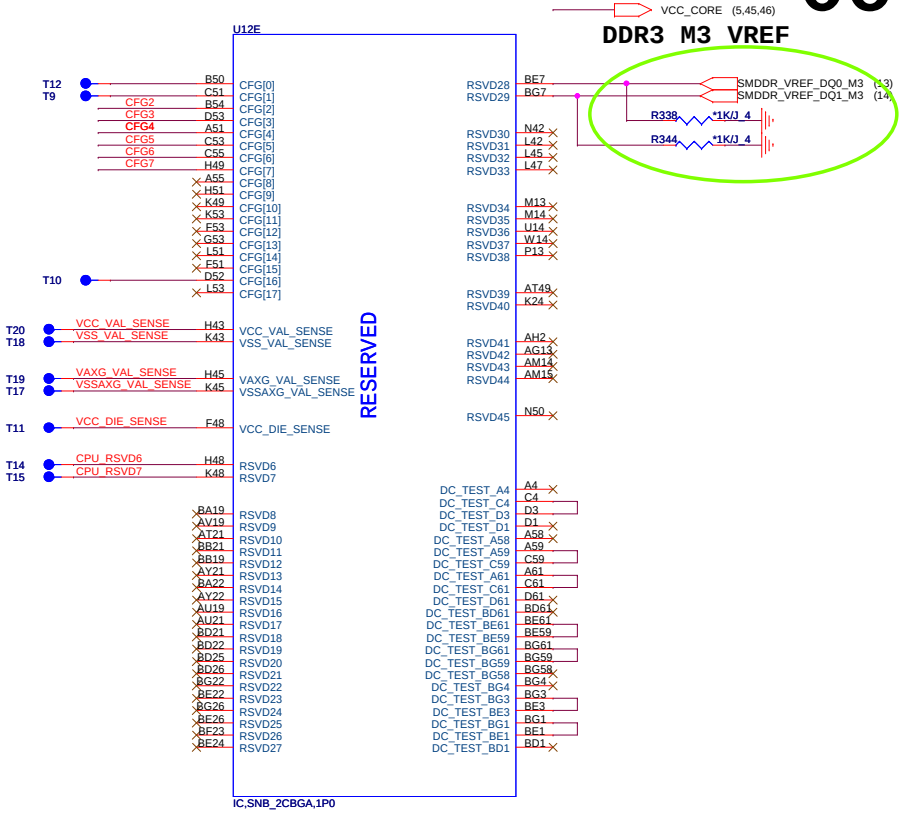
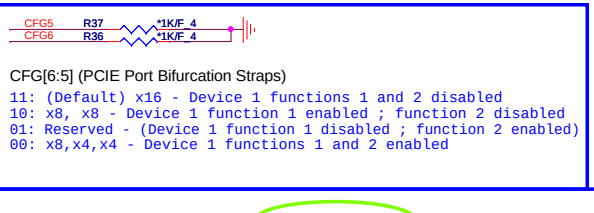
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

06

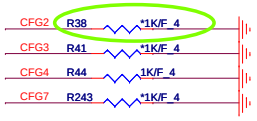




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



Quanta Computer Inc.

PROJECT : LV3D

Size	Document Number	Rev
	IVY 4/4 (GND)	1A

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Panther/Cougar Point (DMI,FDI,PM)

Panther/Cougar Point (LVDS,DDI)

07

U22C

DMI

FDI

System Power Management

BD82PPSM-QPEG-MM#916480

U22D

LVDS

Digital Display Interface

CRT

BD82PPSM-QPEG-MM#916480

wait for B-Stage test

EC-SIT-01

EC-SIT-23

EC-DV-24

Layout note:
AC coupling capacitors of DP are placed on near connector

INT. HDMI

INT. DisPlay Port

Follow PDG eDP disable guide

ESD reserve

mount :Non SBA
un-mount :SBA

PCH Pull-high/low(CLG)

System PWR_OK(CLG)

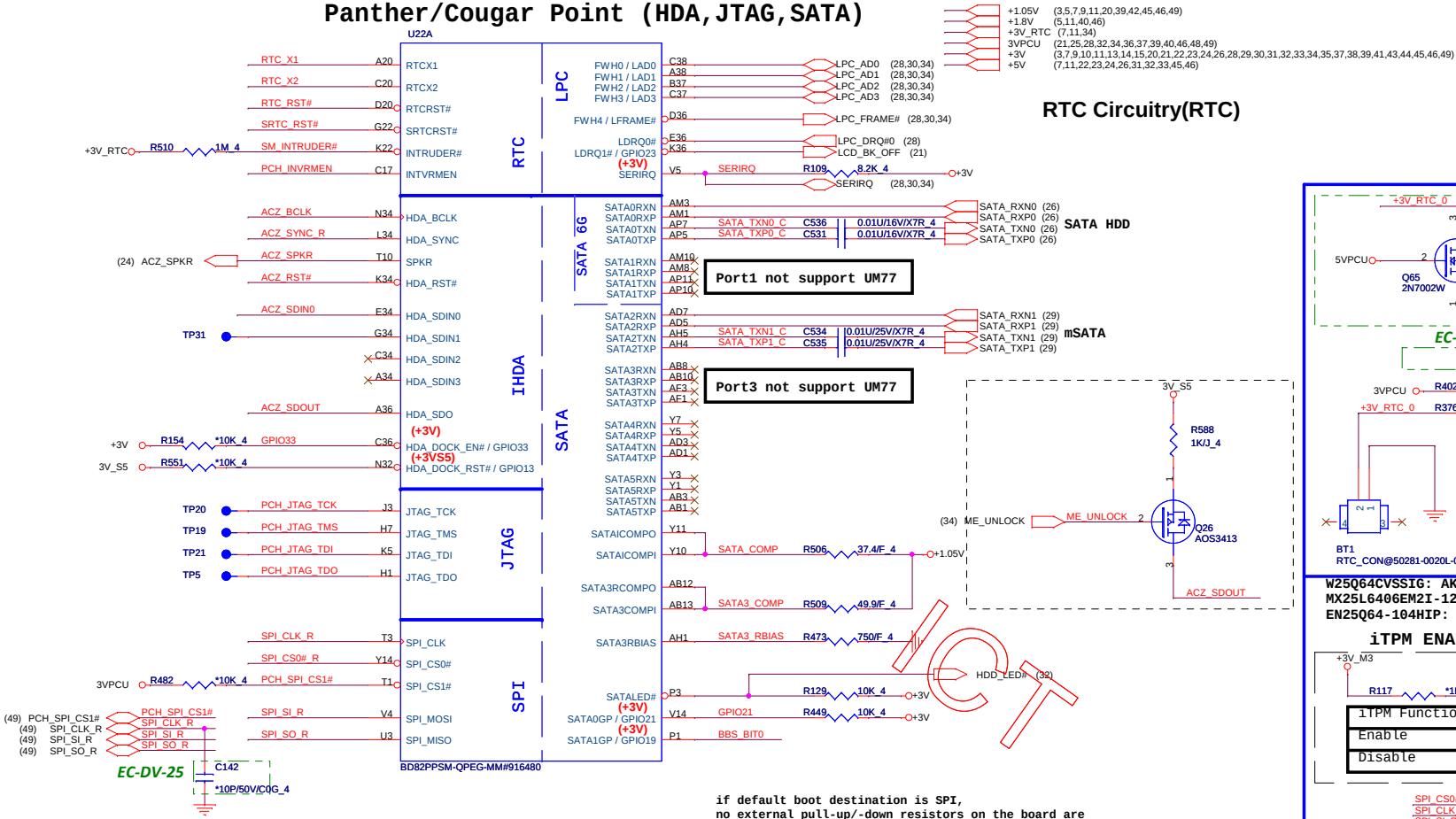
INT HDMI /DisPlay Port DETECT

LVDS from HM77

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

Quanta Computer Inc.
PROJECT : LV3D
Size | Document Number: PCH 1/6 (DMI/FDI/VIDEO) | Rev: 1A
Date: Tuesday, March 13, 2012 | Sheet 7 of 56

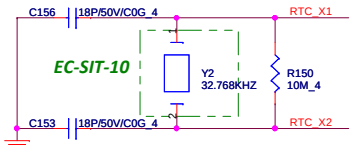
Panther/Cougar Point (HDA,JTAG,SATA)



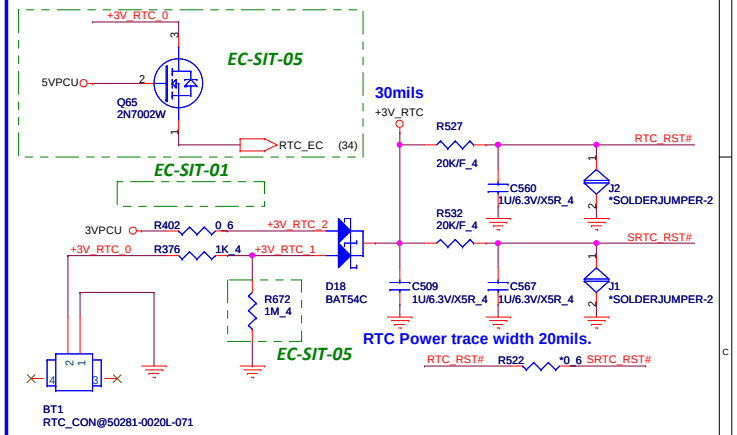
RTC Circuitry(RTC)

+1.05V (3,5,7,9,11,20,39,42,45,46,49)
+1.8V (5,11,40,46)
+3V_RTC (7,11,34)
3VPCU (21,25,28,32,34,36,37,39,40,46,48,49)
+3V (3,7,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
+5V (7,11,22,23,24,26,31,32,33,45,46)

RTC Clock 32.768KHz



08



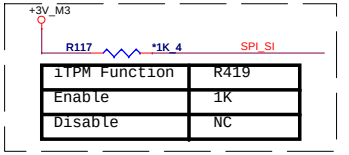
W25Q64CVSSIG: AKE3EFP0N04
MX25L6406EM2I-12G: AKE3NFP0Z00
EN25Q64-104HIP: AKE3EFN0Q00

+3V_M3 (11,25,48,49)

SBA SPI ROM

32Mbit (4M Byte), ME

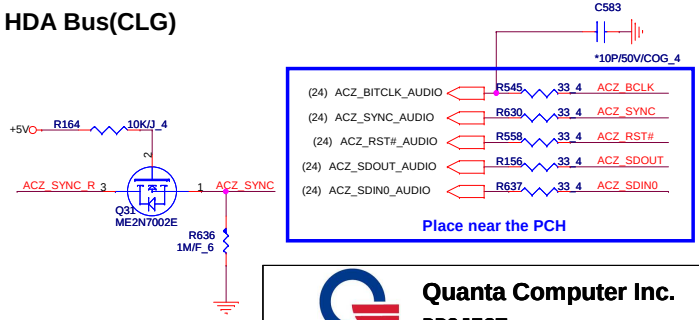
iTPM ENABLE/DISABLE



iTPM Function	R419
Enable	1K
Disable	NC

Support SBA Function will be Mounted

HDA Bus(CLG)



Place near the PCH

Place near the audio codec

if default boot destination is SPI,
no external pull-up/-down resistors on the board are necessary

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R157 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R609 *1K_4, R621 10K_4, +3V, PCI_GNT3# (9)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R524 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R155 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] R127 *1K_4 BBS_BIT0, R618 *1K_4 BBS_BIT1 (9)
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	R471 2.2K_4 +1.8V N.A at CPT EDS 0.7, (3) PROC_SELECT#, R478 1K_4 DF_TVS (10)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R161 1K_4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable	(10) GPIO15 GPIO15 R104 1K_4 3V_S5
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R434 *1K_4 PLL_ODVR_EN (10)
DSWVREN	0: disable 1: enable			

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	PCH 2/6 (SATA/HDA/SPI)	1A

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Panther/Cougar Point-M (PCI,USB,NVRAM)

Panther/Cougar Point-M (PCI-E,SMBUS,CLK)

09

PCI/USBOC# Pull-up(CLG)

+3V
PCI_PIRQA# R625 8.2K_4
PCI_PIRQB# R595 8.2K_4
PCI_PIRQC# R591 8.2K_4
PCI_PIRQD# R575 8.2K_4

+3V
RP13 10K_10P8R_6
10 9 8 7 6 1 2 3 4 5
PIRQH# → MPC_PWR_CTRL#
PWM_SELECT# → PIRQF#
PIRQG# → REQ2#

3V_S5
RP5 10K_10P8R_6
10 9 8 7 6 1 2 3 4 5
USB_OC4# → USB_OC6#
USB_OC1# → USB_OC0#
USB_OC2# → USB_OC7#
USB_OC3# → USB_OC5#

USB3.0

(27) USB30_RX1- / (27) USB30_RX2- → BE28 BC30 TP25 USB30_RX1N TP26 USB30_RX2N
(27) USB30_RX1+ / (27) USB30_RX2+ → BE32 BJ32 TP27 USB30_RX3N TP28 USB30_RX4N BC28 BE30 TP29 USB30_RX1P TP30 USB30_RX2P
(27) USB30_TX1- / (27) USB30_TX2- → BF32 BG32 TP31 USB30_RX3P TP32 USB30_RX4P AV26 BB26 TP33 USB30_TX1N TP34 USB30_TX2N
(27) USB30_TX1+ / (27) USB30_TX2+ → AU28 AY30 TP35 USB30_TX3N TP36 USB30_TX4N AU26 AY26 TP37 USB30_TX1P TP38 USB30_TX2P AV28 AW30 TP39 USB30_TX3P TP40 USB30_TX4P

U22E

RSVD: TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24
RSVD1 AY7, RSVD2 AV7, RSVD3 AU3, RSVD4 BG4, RSVD5 AT10, RSVD6 BC8, RSVD7 AU2, RSVD8 AT4, RSVD9 AT3, RSVD10 AT1, RSVD11 AY3, RSVD12 AT5, RSVD13 AV3, RSVD14 AV1, RSVD15 BB1, RSVD16 BA3, RSVD17 BB5, RSVD18 BB3, RSVD19 BB7, RSVD20 BE8, RSVD21 BD4, RSVD22 BF6, RSVD23 AV5 → TP25, RSVD24 AV10, RSVD25 AT8, RSVD26 AY5, RSVD27 BA2, RSVD28 AT12, RSVD29 BF3

USB: USBP0N C24, USBP0P A24, USBP1N C25, USBP1P B25, USBP2N C26, USBP2P A26, USBP3N K28, USBP3P H28, USBP4N E28, USBP4P D28, USBP5N C28, USBP5P A28, USBP6N C29, USBP6P B29, USBP7N N28, USBP7P M28, USBP8N L30, USBP8P K30, USBP9N G30, USBP9P E30, USBP10N C30, USBP10P A30, USBP11N L32, USBP11P K32, USBP12N G32, USBP12P E32, USBP13N C32, USBP13P A32
USBP0- (27) / USBP0+ (27) → USB 3.0
USBP1- (27) / USBP1+ (27) → USB 3.0 (BIOS debug)
USBP3- (32) / USBP3+ (32) → Camera
USBP4- (28) / USBP4+ (28) → WLAN/BT
USBP5- (29) / USBP5+ (29) → WWAN
USB ports 6 and 7 are disabled on 12 port SKUs(UM77).
USBP10- (31) / USBP10+ (31) → Finger Print
USB ports 12 and 13 are disabled on 10 port SKUs(UM77).
USBRBIAS# C33 → USB_BIAS → R153 22.6/F_4
USBRBIAS B33

PCI: PIRQA# K40, PIRQB# K38, PIRQC# H38, PIRQD# G38
PCI_PIRQA# / PCI_PIRQB# / PCI_PIRQC# / PCI_PIRQD#
(15) DGPU_HOLD_RST# → DGPU_HOLD_RST# → REQ1# / GPIO50 C46 (+3V)
REQ2# / GPIO52 C44 (+3V)
DGPU_PWR_EN → REQ3# / GPIO54 E40 (+3V)
(8) BBS_BIT1 / TP37 → PWM_SELECT# → GNT1# / GPIO51 D47 (+3V)
(8) PCI_GNT3# → GNT2# / GPIO53 F42 (+3V)
GNT3# / GPIO55 F46 (+3V)
MPC_PWR_CTRL# → PIRQE# / GPIO2 G42 (+3V)
PIRQF# → PIRQF# / GPIO3 G40 (+3V)
PIRQG# → PIRQG# / GPIO4 C42 (+3V)
PIRQH# → PIRQH# / GPIO5 D44 (+3V)
TP18 → PME# K10
PCI_PLTRST# → PLTRST# C6

OC0# / GPIO59 (+3V5S) → USB_OC0# A14 → USB_OC0# (27) OC0# For USB3.0
OC1# / GPIO40 (+3V5S) → USB_OC1# K20
OC2# / GPIO41 (+3V5S) → USB_OC2# B17
OC3# / GPIO42 (+3V5S) → USB_OC3# C16
OC4# / GPIO43 (+3V5S) → USB_OC4# L16
OC5# / GPIO9 (+3V5S) → USB_OC5# A16
OC6# / GPIO10 (+3V5S) → USB_OC6# D14
OC7# / GPIO14 (+3V5S) → USB_OC7# C14

(28) PCLK_DEBUG → R608 22_4 → PCLK_DEBUG_C
(30) CLK_LPC_TPM → R600 22_4 → CLK_LPC_TPM_C
(34) PCLK_591 → R599 22_4 → CLK_PCI_FB_R
R598 22_4 → CLK_PCI_FB_C
CLK_PCI_FB → CLKOUT_PCI0 H49, CLKOUT_PCI1 J48, CLKOUT_PCI2 K42, CLKOUT_PCI3 H40, CLKOUT_PCI4

C634 *15P/50V/NPO_4 PCLK_DEBUG_C
C633 *10P/50V/COG_4 PCLK_591

BD82PPSM-QPEG-MM#916480

ESD reserve
PCI_PLTRST# → SC5 *Clamp-Diode_6

WLAN / Card Reader / LAN

WLAN
(28) PCIE_RXN2_WLAN / (28) PCIE_RXP2_WLAN / (28) PCIE_TXN2_WLAN / (28) PCIE_TXP2_WLAN
C580 0.1U/10V/X7R_4 PCIE_TXN2_WLAN_C
C574 0.1U/10V/X7R_4 PCIE_TXP2_WLAN_C

Card Reader
(32) PCIE_RXN3_CARD / (32) PCIE_RXP3_CARD / (32) PCIE_TXN3_CARD / (32) PCIE_TXP3_CARD
C604 0.1U/10V/X7R_4 PCIE_TXN3_CARD_C
C611 0.1U/10V/X7R_4 PCIE_TXP3_CARD_C

LAN
(25) PCIE_RXN4_LAN / (25) PCIE_RXP4_LAN / (25) PCIE_TXN4_LAN / (25) PCIE_TXP4_LAN
C596 0.1U/10V/X7R_4 PCIE_TXN4_LAN_C
C592 0.1U/10V/X7R_4 PCIE_TXP4_LAN_C

Port5-Port8 not support UM77

EHCI1 / EHCI2

WLAN
(28) CLK_PCIE_WLANN / (28) CLK_PCIE_WLANP → AB49 AB47 → CLKOUT_PCIE1N / CLKOUT_PCIE1P
(28) PCIE_CLKREQ_WLAN# → PCIE_CLKREQ_WLAN# M1 → PCIECLKRQ1# / GPIO18

Card Reader
(32) CLK_PCIE_CARDN / (32) CLK_PCIE_CARDP → AA48 AA47 → CLKOUT_PCIE2N / CLKOUT_PCIE2P
(32) PCIE_CLKREQ_CARD# → PCIE_CLKREQ_CARD# V10 → PCIECLKRQ2# / GPIO20

LAN
(25) CLK_PCIE_LANN / (25) CLK_PCIE_LANP → V45 V46 → CLKOUT_PCIE5N / CLKOUT_PCIE5P
(25) PCIE_CLKREQ_LAN# → PCIE_CLKREQ_LAN# L14 → PCIECLKRQ5# / GPIO44

TP6 → PCIECLKRQ0# → J2 → PCIECLKRQ0# / GPIO73
TP7 → PCIECLKRQ3# → A8 → PCIECLKRQ3# / GPIO25
TP33 → CLK_PCIE_REV4N / TP34 → CLK_PCIE_REV4P → Y43 Y45 → CLKOUT_PCIE4N / CLKOUT_PCIE4P
TP23 → PCIECLKRQ4# → L12 → PCIECLKRQ4# / GPIO26
TP22 → CLK_PEGB_REQ# → E6 → PEG_B_CLKRQ# / GPIO56
TP30 → PCIECLKRQ6# → T13 → PCIECLKRQ6# / GPIO45
TP24 → PCIECLKRQ7# → K12 → PCIECLKRQ7# / GPIO46
TP29 → CLK_PCIE_XDPN / TP26 → CLK_PCIE_XDPP → AK14 AK13 → CLKOUT_ITPXDP_N / CLKOUT_ITPXDP_P

(+3V) PCIE_CLKREQ_WLAN# R96 10K_4
PCIE_CLKREQ_CARD# R447 10K_4

3V_S5
PCIECLKRQ0# R114 10K_4
PCIECLKRQ3# R122 10K_4
PCIECLKRQ4# R477 10K_4
PCIECLKRQ7# R458 10K_4
CLK_PEGB_REQ# R465 10K_4
PCIECLKRQ6# R503 10K_4
CLK_PEGA_REQ# R441 DIS@10K_4
PCIE_CLKREQ_LAN# R478 10K_4

CLK_PEGA_REQ# R460 *UMA@10K_4
CLK_BUF_BCLK_N R539 10K_4
CLK_BUF_BCLK_P R543 10K_4
CLK_BUF_PCIE_3GPLL# R519 10K_4
CLK_BUF_PCIE_3GPLL R523 10K_4
CLK_BUF_DREFCLK R528 10K_4
CLK_BUF_DREFCLK# R533 10K_4
CLK_BUF_DREFSSCLK# R484 10K_4
CLK_BUF_DREFSSCLK R485 10K_4
CLK_PCH_14M R597 10K_4
CLOCK TERMINATION for FCIM

PCI-E* / SMBUS / Controller Link

U22B

PERN1 BG34, PERP1 BJ34, PETN1 AV32, PETP1 AU32
PERN2 BE34, PERP2 BF34, PETN2 BB32, PETP2 AY32
PERN3 BG36, PERP3 BJ36, PETN3 AV34, PETP3 AU34
PERN4 BF36, PERP4 BE36, PETN4 AY34, PETP4 BB34
PERN5 BG37, PERP5 BH37, PETN5 AY36, PETP5 BB36
PERN6 BJ38, PERP6 BG38, PETN6 AU36, PETP6 AV36
PERN7 BG40, PERP7 BJ40, PETN7 AY40, PETP7 BB40
PERN8 BE38, PERP8 BC38, PETN8 AW38, PETP8 AY38

SMBUS
(+3VS5) SMBALERT# / GPIO11 → E12 SMBALERT#
SMBCLK → H14 SMB_PCH_CLK
SMBDATA → C9 SMB_PCH_DAT
(+3VS5) SML0ALERT# / GPIO60 → A12 DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH (3)
SML0CLK → C8 SMB_ME0_CLK
SML0DATA → G12 SMB_ME0_DAT
(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 → C13 SML1ALERT#_R
(+3VS5) SML1CLK / GPIO58 → E14 SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 → M16 SMB_ME1_DAT

Controller Link
CL_CLK1 → M7 CL_CLK_R
CL_DATA1 → T11 CL_DAT_R
CL_RST1# → P10 CL_RST#_R

CLOCKS

(+3VS5) PEG_A_CLKRQ# / GPIO47 → M10 CLK_PEGA_REQ# → CLK_PEGA_REQ# (15)
CLKOUT_PEG_A_N → AB37 CLK_PCIE_VGAN_R
CLKOUT_PEG_A_P → AB38 CLK_PCIE_VGAP_R
RP14 4 3 2 1 DX2
CLK_PCIE_VGAN (15)
CLK_PCIE_VGAP (15)

CLKOUT_DMI_N → AV22 CLK_CPU_BCLKN (3)
CLKOUT_DMI_P → AU22 CLK_CPU_BCLKP (3)
CLKOUT_DP_N → AM12 CLK_DPLL_SSCLKN (3)
CLKOUT_DP_P → AM13 CLK_DPLL_SSCLKP (3)
CLKIN_DMI_N → BF18 CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P → BE18 CLK_BUF_PCIE_3GPLL
CLKIN_GND1_N → BJ30 CLK_BUF_BCLK_N
CLKIN_GND1_P → BG30 CLK_BUF_BCLK_P
CLKIN_DOT_96N → G24 CLK_BUF_DREFCLK#
CLKIN_DOT_96P → E24 CLK_BUF_DREFCLK
CLKIN_SATA_N → AK7 CLK_BUF_DREFSSCLK#
CLKIN_SATA_P → AK5 CLK_BUF_DREFSSCLK
REFCLK14IN → K45 CLK_PCH_14M
CLKIN_PCILOOPBACK → H45 CLK_PCI_FB
XTAL25_IN → V47 XTAL25_IN
XTAL25_OUT → V49 XTAL25_OUT
C162 10P/50V/C0G_4
R159 1M_4
Y3 25MHz
C161 10P/50V/C0G_4
XCLK_RCOMP → Y47 XCLK_RCOMP R607 90.9/F_4 +1.05V

FLEX CLOCKS
(+3V) CLKOUTFLEX0 / GPIO64 → K43 CLK_FLEX0 → TP35
(+3V) CLKOUTFLEX1 / GPIO65 → F47 CLK_FLEX1 → TP36
(+3V) CLKOUTFLEX2 / GPIO66 → H47 CLK_FLEX2 → TP8
(+3V) CLKOUTFLEX3 / GPIO67 → K49 DGPU_PRSNT# (10)

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PLTRST#(CLG)

3V_S5
C117 *0.1U/10V/X7R_4
U18 *TC7SH08FU
PCI_PLTRST# → PLTRST#
R95 100K_4
R107 0_4
PLTRST# → PLTRST# (3,15,25,28,29,30,32)

DGPU Power ON

R640 DIS@0_4 → 3V_GPU_EN_EC (34)
(42,43,44,46) GFXON → R627 *DIS@0_4 → DGPU_PWR_EN
R632 *DIS@10K_4 → +3V

SMBus/Pull-up(CLG) EC-DV-28 EC-SIT-11

(18,20,33,34) MBCLK_THRM → Q66A 2N7002KDW → SMB_ME1_CLK
R308 2.2K_4 → +3V
R328 2.2K_4 → 3V_S5
(18,20,33,34) MBDATA_THRM → SMB_ME1_DAT
Q66B 2N7002KDW

EC-DV-28 EC-SIT-11
SMB_PCH_DAT → Q67A 2N7002KDW
R337 4.7K_4 → +3V
R331 4.7K_4 → 3V_S5
SMB_PCH_CLK → Q67B 2N7002KDW → PCLK_SMB (13,14,29,30,31)

PCIE Clock

Layout note:
PCIE_CLKREQ_LAN# layout adjacent to CLK_PEGA_REQ#

DGPU_HOLD_RST# R581 DIS@100K_4
GFXON R616 DIS@100K_4

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R569 *1K_4

SMBus/Pull-up(CLG)

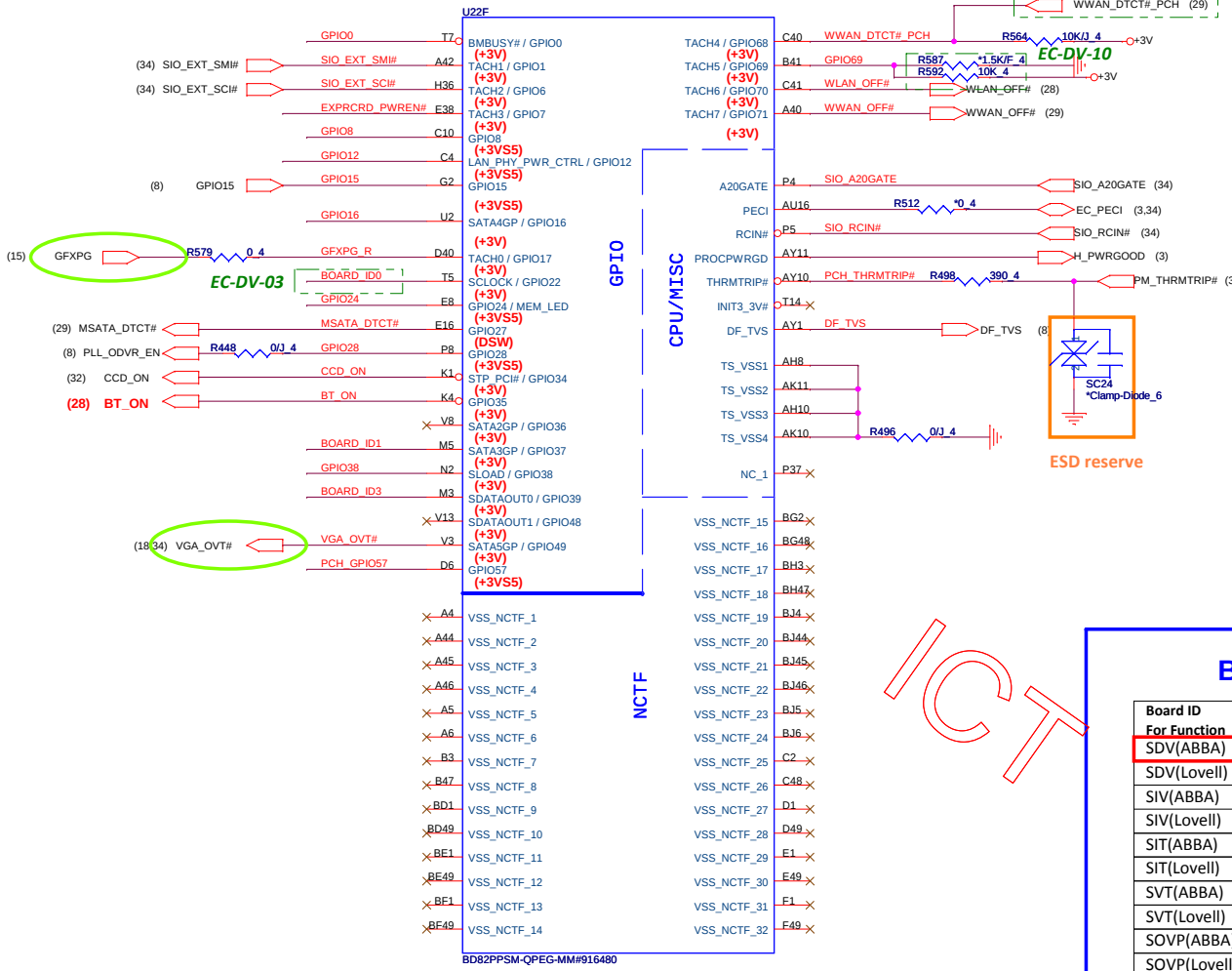
3V_S5
R505 1K_4 DRAMRST_CNTRL_PCH
R491 10K_4 SMBALERT#
R327 2.2K_4 SMB_PCH_CLK
R479 2.2K_4 SMB_PCH_DAT
R121 2.2K_4 SMB_ME0_CLK
R480 2.2K_4 SMB_ME0_DAT
R497 10K_4 SML1ALERT#_R

3V_S5
R430 *10K_4 CL_CLK_R
R406 *10K_4 CL_DAT_R
R453 *10K_4 CL_RST#_R

3V_S5 (3,7,8,10,11,28,34,46)
+3V (3,7,8,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)

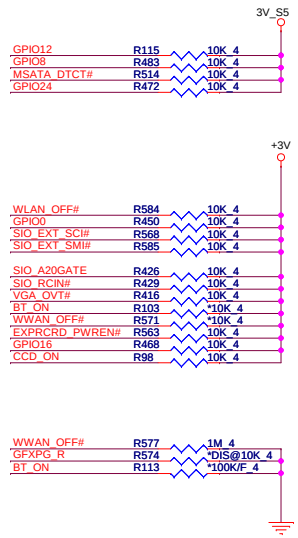
Quanta Computer Inc.
PROJECT : LV3D
Size | Document Number: PCH 3/6 (PCIE/USB/CLK) | Rev 1A
Date: Monday, March 12, 2012 Sheet 9 of 56

Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)



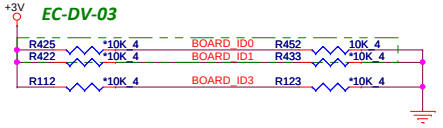
3V_S5 (3,7,8,9,11,28,34,46)
+3V (3,7,8,9,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)

GPIO Pull-up/Pull-down(CLG)



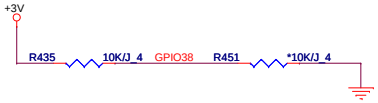
BOARD ID SETTING

Board ID For Function	ID0 GPIO22	ID1 GPIO37	ID2 GPIO38	ID3 GPIO39
SDV(ABBA)	0	0	0	0
SDV(Lovell)				
SIV(ABBA)				
SIV(Lovell)				
SIT(ABBA)				
SIT(Lovell)				
SVT(ABBA)				
SVT(Lovell)				
SOVP(ABBA)				
SOVP(Lovell)				



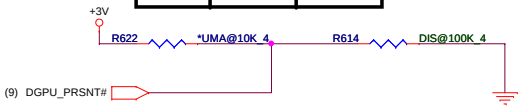
SBA setting

GPI036	Low	N.A
	Hight	SBA

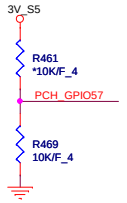


UMA & Optimus seeting

	Optimus	UMA
R546	un-stuff	stuff
R547	stuff	un-stuff



TPM physical presence	
PCH_GPIO57	Low: Default



Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A

Date: Monday, March 12, 2012 Sheet 10 of 56

Panther/Cougar Point-M (POWER)

Panther/COUGAR POINT (POWER)

11

U22J — POWER

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

U22G — POWER

VCC CORE | LVDS | CRT | HVCMOS | DMI | VCCIO | DFT / SPI | FDI

BD82PPSM-QPEG-MM#916480

EC-SIT-01

EC-DV-09

ESD reserve

SC6 *Clamp-Diode_6

(Mobile 1.5V)

+3V_M3 (8,25,48,49)
+1.05V_M3 (48,49)
+3V_RTC (7,8,34)
3V_S5 (3,7,8,9,10,28,34,46)
+3V (3,7,8,9,10,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
5V_S5 (27,46)
+5V (7,8,22,23,24,26,31,32,33,45,46)
+1.05V (3,5,7,8,9,20,39,42,45,46,49)
1.5V_SUS (3,13,14,35,38,42,46)
+1.8V (5,8,40,46)

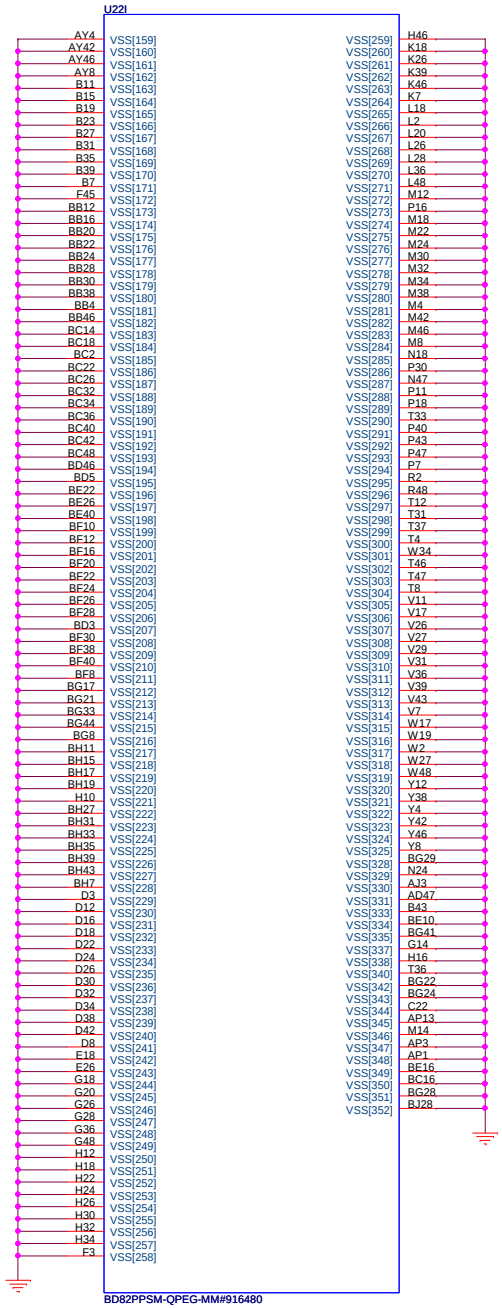
Quanta Computer Inc.

PROJECT : LV3D

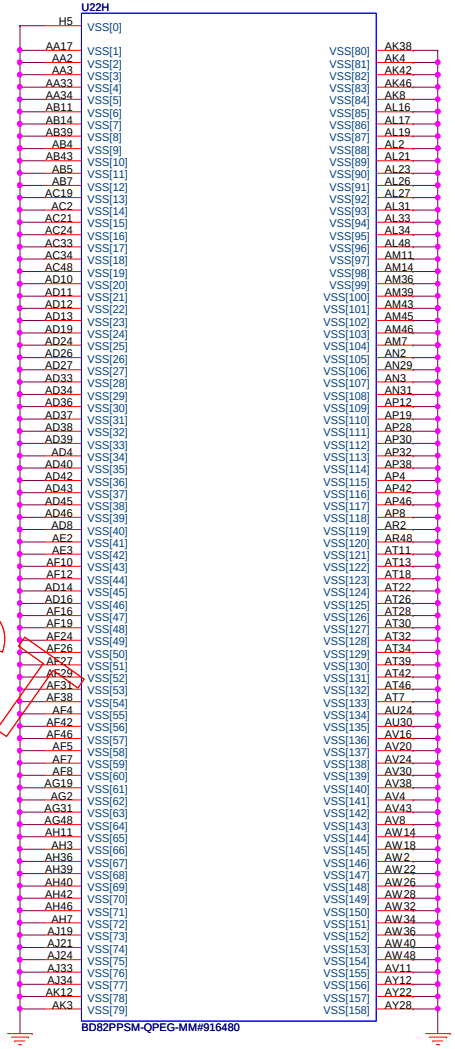
Size | Document Number: PCH 5/6 (POWER) | Rev: 1A

Date: Tuesday, March 13, 2012 | Sheet 11 of 56

Panther/Cougar Point-M (GND)



Panther/Cougar Point-M (GND)



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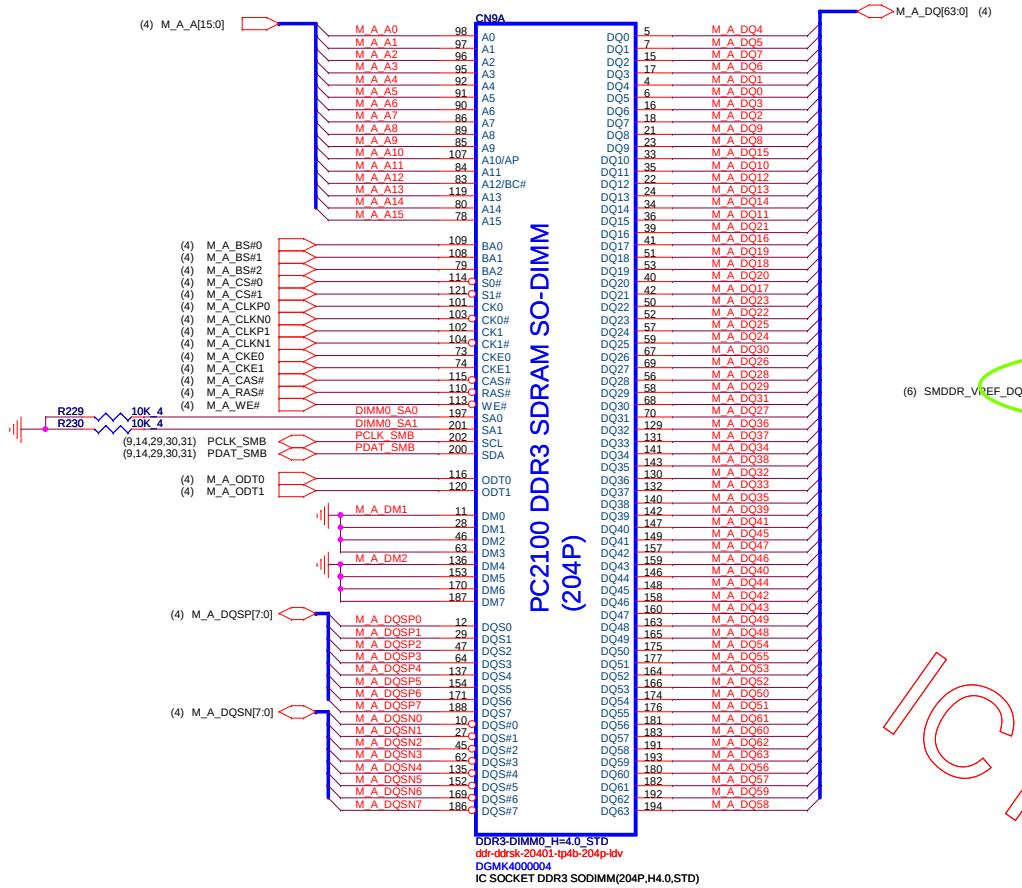
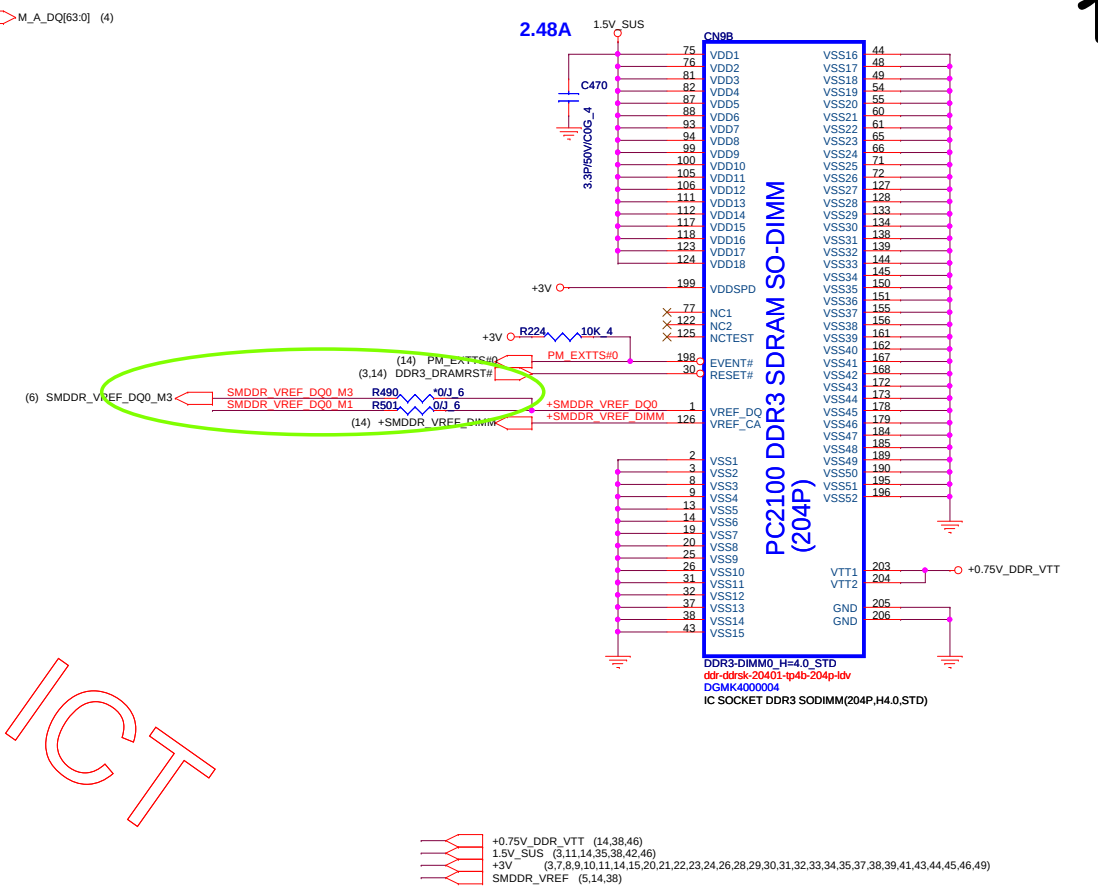
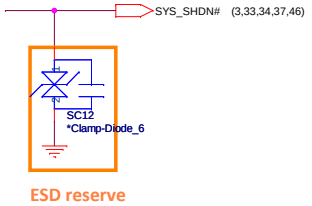
PROJECT : LV3D

Size	Document Number	Rev
	PCH 6/6 (GND)	1A
Date: Monday, March 12, 2012	Sheet 12 of 56	

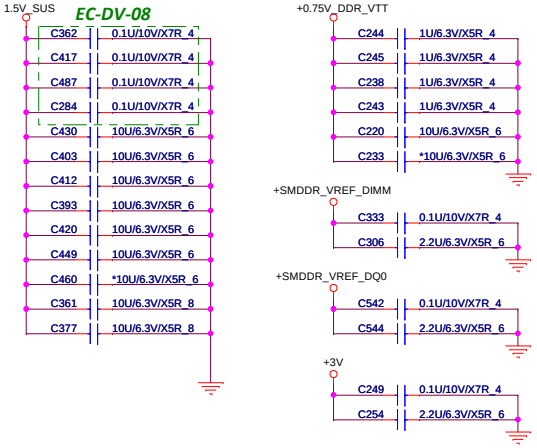




ICT



Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution

Quanta Computer Inc.

PROJECT : LV3D

Size	Document Number	Rev
	DDR3 DIMM0-STD (5.2H)	1A

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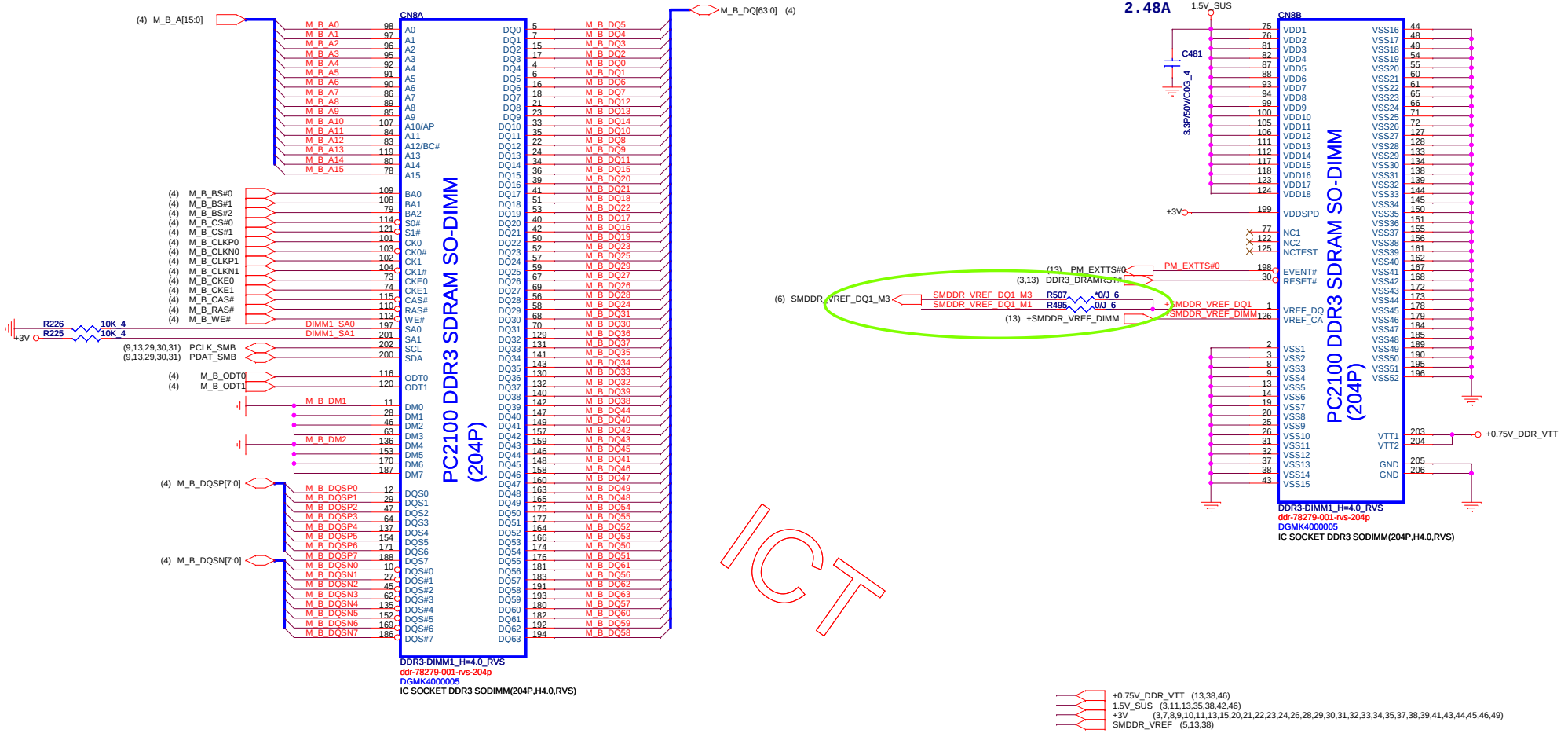
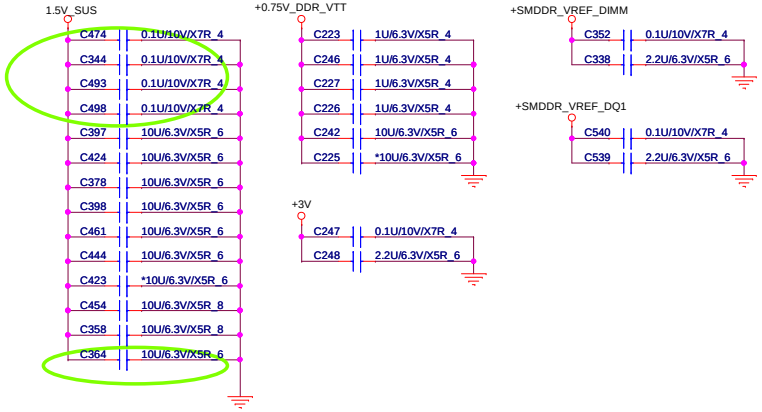


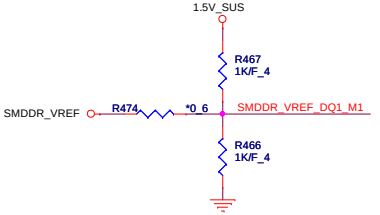
ICT

+0.75V_DDR_VTT (13,38,46)
1.5V_SUS (3,11,13,35,38,42,46)
+3V (3,7,8,9,10,11,13,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
SMDDR_VREF (5,13,38)

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	DDR3 DIMM1-RVS (5.2H)	1A
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<VGA>

U13A
bga595-nvidia-n13m-gs-s-a2
1/14 PCI_EXPRESS

3300mA
210mA
150mA
12~16 mils

PEG CLK detect
GPU RST#(CLG)
U13E
bga595-nvidia-n13m-gs-s-a2
40A
U13C
bga595-nvidia-n13m-gs-s-a2
COMMON

REV-00 IVB@0.22u/10V_4X

EC-SIT-17

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	N13M-GS (PCIE I/F) 1/5	1A
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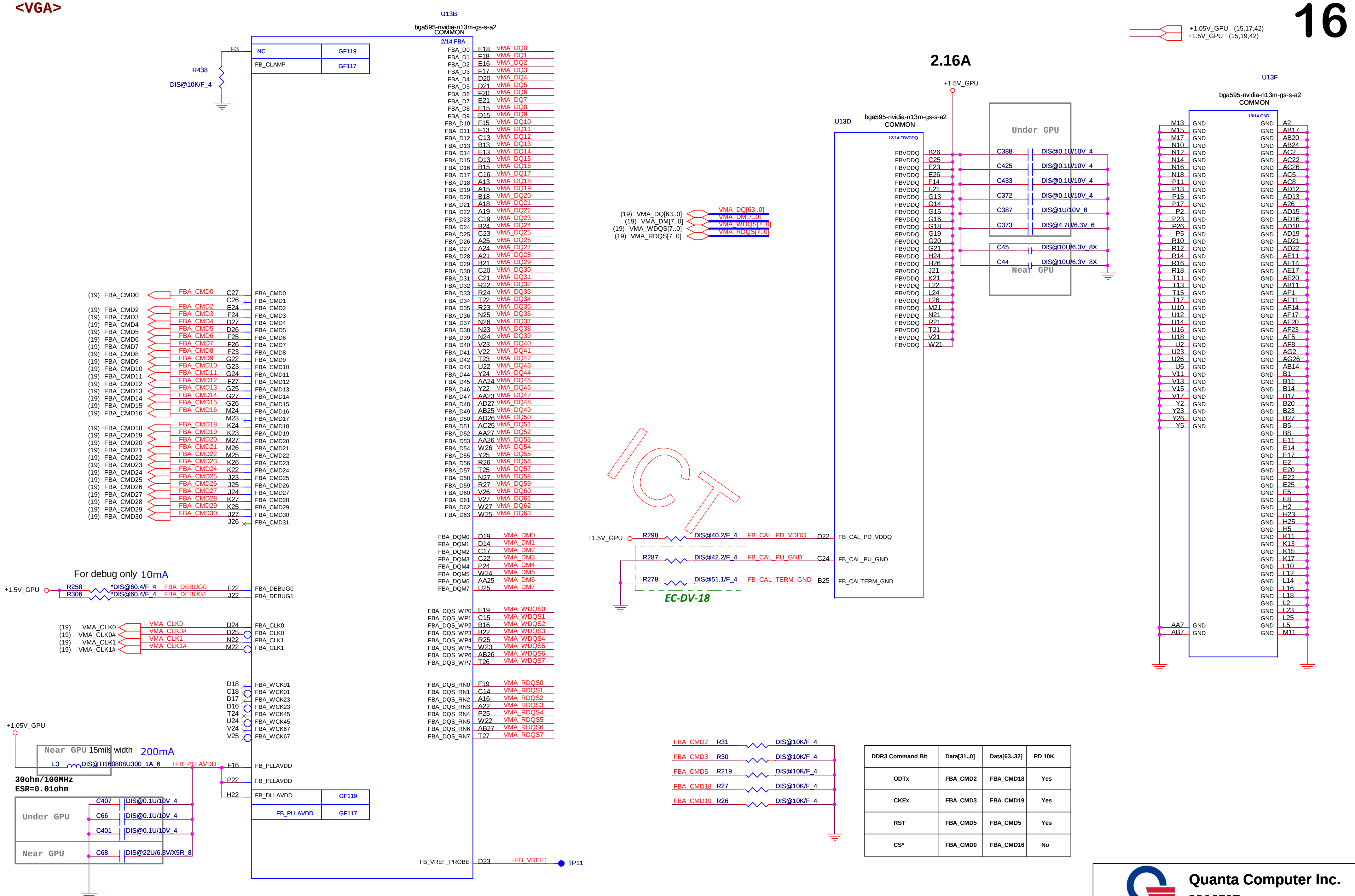
<VGA>


U13B
bga595-nvidia-n13m-gs-s-a2
COMMON
2/14 FBA
NC GF119
FB_CLAMP GF117
F3
R438
DIS@10K/F_4
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
(19) FBA_CMD0 FBA_CMD0 C27 FBA_CMD0
C26 FBA_CMD1
(19) FBA_CMD2 FBA_CMD2 E24 FBA_CMD2
(19) FBA_CMD3 FBA_CMD3 F24 FBA_CMD3
(19) FBA_CMD4 FBA_CMD4 D27 FBA_CMD4
(19) FBA_CMD5 FBA_CMD5 D26 FBA_CMD5
(19) FBA_CMD6 FBA_CMD6 F25 FBA_CMD6
(19) FBA_CMD7 FBA_CMD7 F26 FBA_CMD7
(19) FBA_CMD8 FBA_CMD8 F23 FBA_CMD8
(19) FBA_CMD9 FBA_CMD9 G22 FBA_CMD9
(19) FBA_CMD10 FBA_CMD10 G23 FBA_CMD10
(19) FBA_CMD11 FBA_CMD11 G24 FBA_CMD11
(19) FBA_CMD12 FBA_CMD12 F27 FBA_CMD12
(19) FBA_CMD13 FBA_CMD13 G25 FBA_CMD13
(19) FBA_CMD14 FBA_CMD14 G27 FBA_CMD14
(19) FBA_CMD15 FBA_CMD15 G26 FBA_CMD15
(19) FBA_CMD16 FBA_CMD16 M24 FBA_CMD16
M23 FBA_CMD17
(19) FBA_CMD18 FBA_CMD18 K24 FBA_CMD18
(19) FBA_CMD19 FBA_CMD19 K23 FBA_CMD19
(19) FBA_CMD20 FBA_CMD20 M27 FBA_CMD20
(19) FBA_CMD21 FBA_CMD21 M26 FBA_CMD21
(19) FBA_CMD22 FBA_CMD22 M25 FBA_CMD22
(19) FBA_CMD23 FBA_CMD23 K26 FBA_CMD23
(19) FBA_CMD24 FBA_CMD24 K22 FBA_CMD24
(19) FBA_CMD25 FBA_CMD25 J23 FBA_CMD25
(19) FBA_CMD26 FBA_CMD26 J25 FBA_CMD26
(19) FBA_CMD27 FBA_CMD27 J24 FBA_CMD27
(19) FBA_CMD28 FBA_CMD28 K27 FBA_CMD28
(19) FBA_CMD29 FBA_CMD29 K25 FBA_CMD29
(19) FBA_CMD30 FBA_CMD30 J27 FBA_CMD30
J26 FBA_CMD31
FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7
For debug only 10mA
+1.5V_GPU
R258 *DIS@60.4/F_4 FBA_DEBUG0 F22 FBA_DEBUG0
R306 *DIS@60.4/F_4 FBA_DEBUG1 J22 FBA_DEBUG1
(19) VMA_CLK0 VMA_CLK0 D24 FBA_CLK0
(19) VMA_CLK0# VMA_CLK0# D25 FBA_CLK0
(19) VMA_CLK1 VMA_CLK1 N22 FBA_CLK1
(19) VMA_CLK1# VMA_CLK1# M22 FBA_CLK1
FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7
D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67
FBA_DQS_RN0 E19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7
+1.05V_GPU
Near GPU 15mils width 200mA
L3 DIS@TI160808U300_1A_6 +FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22 FB_DLLAVDD GF119
FB_PLLAVDD GF117
30ohm/100MHz
ESR=0.01ohm
Under GPU
C407 DIS@0.1U/10V_4
C66 DIS@0.1U/10V_4
C401 DIS@0.1U/10V_4
Near GPU
C68 DIS@22U/6.3V/X5R_8
FB_VREF_PROBE D23 +FB_VREF1 TP11
(19) VMA_DQ[63..0] VMA_DQ[63..0]
(19) VMA_DM[7..0] VMA_DM[7..0]
(19) VMA_WDQS[7..0] VMA_WDQS[7..0]
(19) VMA_RDQS[7..0] VMA_RDQS[7..0]
ICT
+1.5V_GPU R298 DIS@40.2/F_4 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
R287 DIS@42.2/F_4 FB_CAL_PU_GND C24 FB_CAL_PU_GND
R278 DIS@51.1/F_4 FB_CAL_TERM_GND B25 FB_CALTERM_GND
EC-DV-18
FBA_CMD2 R31 DIS@10K/F_4
FBA_CMD3 R30 DIS@10K/F_4
FBA_CMD5 R219 DIS@10K/F_4
FBA_CMD18 R27 DIS@10K/F_4
FBA_CMD19 R26 DIS@10K/F_4
2.16A
+1.5V_GPU
U13D
bga595-nvidia-n13m-gs-s-a2
COMMON
12/14 FBVDDQ
FBVDDQ B26, C25, E23, E26, F14, F21, G13, G14, G15, G16, G18, G19, G20, G21, H24, H26, J21, K21, L22, L24, L26, M21, N21, R21, T21, V21, W21
Under GPU
C388 DIS@0.1U/10V_4
C425 DIS@0.1U/10V_4
C433 DIS@0.1U/10V_4
C372 DIS@0.1U/10V_4
C387 DIS@1U/10V_6
C373 DIS@4.7U/6.3V_6
C45 DIS@10U/6.3V_8X
C44 DIS@10U/6.3V_8X
Near GPU
+1.05V_GPU (15,17,42)
+1.5V_GPU (15,19,42)
U13F
bga595-nvidia-n13m-gs-s-a2
COMMON
13/14 GND
GND M13, M15, M17, N10, N12, N14, N16, N18, P11, P13, P15, P17, P2, P23, P26, P5, R10, R12, R14, R16, R18, T11, T13, T15, T17, U10, U12, U14, U16, U18, U2, U23, U26, U5, V11, V13, V15, V17, Y2, Y23, Y26, Y5, AA7, AB7
GND A2, AB17, AB20, AB24, AC2, AC22, AC26, AC5, AC8, AD12, AD13, A26, AD15, AD16, AD18, AD19, AD21, AD22, AE11, AE14, AE17, AE20, AB11, AF1, AF11, AF14, AF17, AF20, AF23, AF5, AF8, AG2, AG26, AB14, B1, B11, B14, B17, B20, B23, B27, B5, B8, E11, E14, E17, E2, E20, E22, E25, E5, E8, H2, H23, H25, H5, K11, K13, K15, K17, L10, L12, L14, L16, L18, L2, L23, L25, L5, M11

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

Quanta Computer Inc.

PROJECT : LV3D

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	N13M-GS (MEMORY/GND) 2/5	1A

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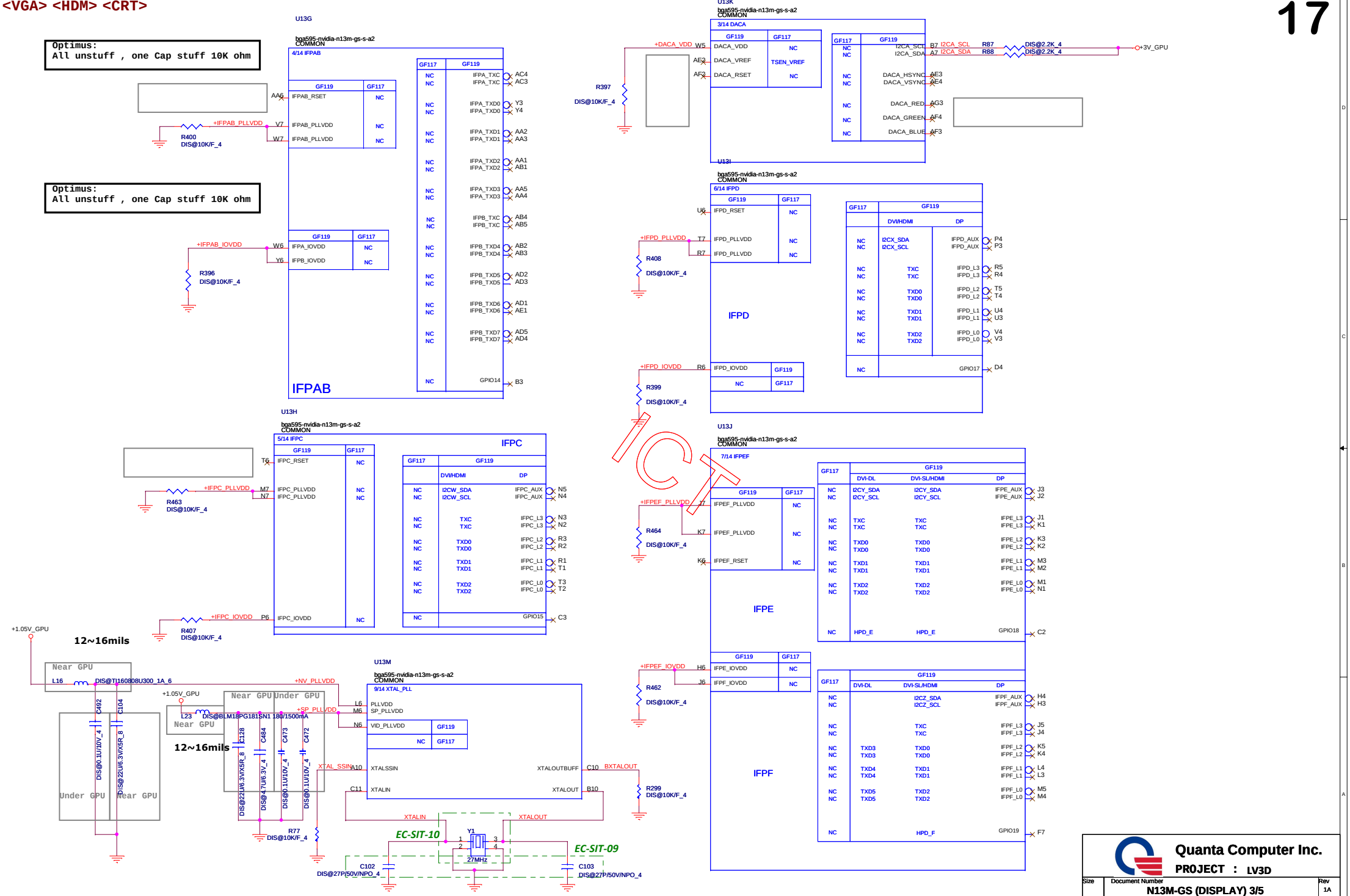
<VGA> <HDM> <CRT>

Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm



Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	N13M-GS (DISPLAY) 3/5	1A
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<VGA>

U13L
bga595-nvidia-n13m-gs-s-a2
COMMON
10/14 MISC2

T3 E10 VMON_IN0
T2 E10 VMON_IN1

STRAP0 D1 STRAP0
STRAP1 D2 STRAP1
STRAP2 E4 STRAP2
STRAP3 E3 STRAP3
STRAP4 D3 STRAP4

GF119	GF117
STRAP5 C1	NC

R432 *DIS@40.2K/F_4 F6 MULTISTRAP_REF0_GND
R431 *DIS@40.2K/F_4 F4 MULTISTRAP_REF1_GND
R419 *DIS@40.2K/F_4 F5 MULTISTRAP_REF2_GND

GF119	GF117
	NC
	NC

U13N
bga595-nvidia-n13m-gs-s-a2
COMMON
8/14 MISC1

T1 E12 THERMDN
T23 F12 THERMDP

GF117	GF119
NC	I2CB_SCL
NC	I2CB_SDA

JTAG_TCK AE5 JTAG_TCK
JTAG_TMS AD6 JTAG_TMS
JTAG_TDI AE6 JTAG_TDI
T4 JTAG_TDO AF6 JTAG_TDO
JTAG_TRST# AG4 JTAG_TRST

GF117	GF119
NC	GPIO16 D5
NC	GPIO20 E6
NC	GPIO21 C4

ROM_CS D12 ROM_CS
ROM_SI B12 ROM_SI
ROM_SO A12 ROM_SO
ROM_SCLK C12 ROM_SCLK
BUFRST D11
PGOOD D10
CEC E9

EC-DV-19
R83 DIS@10K/F_4
R346 DIS@10K/F_4
+3V_GPU

I2CS_SCL D9 DGPU_I2CS_SCL
I2CS_SDA D8 DGPU_I2CS_SDA
I2CC_SCL A9 I2CC_SCL_G R82 DIS@2.2K_4 +3V_GPU
I2CC_SDA B9 I2CC_SDA_G R84 DIS@2.2K_4 +3V_GPU
I2CB_SCL C9 I2CB_SCL_G R343 DIS@2.2K_4 +3V_GPU
I2CB_SDA C8 I2CB_SDA_G R86 DIS@2.2K_4 +3V_GPU

GPIO0 C6 GPU_H_VID4 → GPU_H_VID4 (44)
GPIO1 B2 GPU_H_VID3 → GPU_H_VID3 (44)
GPIO2 D6
GPIO3 C7 R349 *DIS@0_4 → DPRSLP (44)
GPIO4 E9
GPIO5 A3 GPU_H_VID1 → GPU_H_VID1 (44)
GPIO6 A4 GPU_H_VID2 → GPU_H_VID2 (44)
GPIO7 B6 T24 DGPU_GPIO8
GPIO8 A6 ALERT → GPU_H_VID0 (44)
GPIO9 E8
GPIO10 C5
GPIO11 E7 GPU_H_VID0
GPIO12 D7 AC_BATT_DEC_R → D15 2 1 DIS@RB500V-40 → AC_PRESENT (7,34)
GPIO13 B4 GPU_H_VID5 → GPU_H_VID5 (44)

+3V_GPU
R369 DIS@10K/F_4

VRAM Configuration Table STRAP[0..3]

"1" : 10K pull high ; "0" : 10K pull down

DESCRIPTION	Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	0	1	1	0
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	1	0	1	0
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Hynix	H5TQ2G63DFR-11C	0	0	1	1
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Samsung	K4W2G1646F-BC11				

+3V_GPU
R267 R281 R270
ROM_SI ROM_SO ROM_SCLK
*DIS@4.99K/F_4 *DIS@10K/F_4 *DIS@15K/F_4
R272 R286 R285
DIS@10K/F_4 DIS@10K/F_4 DIS@10K/F_4

+3V_GPU
R392 R390 R384 R395 R378
STRAP0 STRAP1 STRAP2 STRAP3 STRAP4
*DIS@10K/F_4 DIS@10K/F_4 DIS@10K/F_4 *DIS@10K/F_4 *DIS@20K/F_4
R394 R383 R379 R391 R371
DIS@10K/F_4 *DIS@10K/F_4 *DIS@10K/F_4 DIS@10K/F_4 DIS@10K/F_4

NVVDD Table

N13M-GS	NVVDD (0.875V)
GPU_H_VID0	0 (R420)
GPU_H_VID1	1 (R389)
GPU_H_VID2	0 (R373)
GPU_H_VID3	0 (R385)
GPU_H_VID4	1 (R418)
GPU_H_VID5	1 (R381)

+3V_GPU
R421 R389 R370 R393 R418 R381
GPU_H_VID0 GPU_H_VID1 GPU_H_VID2 GPU_H_VID3 GPU_H_VID4 GPU_H_VID5
*DIS@10K/F_4 DIS@10K/F_4 *DIS@10K/F_4 *DIS@10K/F_4 DIS@10K/F_4 DIS@10K/F_4
R420 R382 R373 R385 R403 R377
DIS@10K/F_4 *DIS@10K/F_4 DIS@10K/F_4 DIS@10K/F_4 *DIS@10K/F_4 *DIS@10K/F_4

+3V_GPU
DGPU_GPIO8 1 Q25 3 VGA_OVT# (10,34)
DIS@ME2N7002E

+3V_GPU
ROM_CS R292 DIS@10K/F_4
JTAG_TMS R387 *DIS@10K/F_4
JTAG_TDI R388 *DIS@10K/F_4
DGPU_GPIO8 R360 DIS@10K/F_4
ALERT R348 DIS@10K/F_4
JTAG_TRST# R90 DIS@1K/F_4
JTAG_TCK R89 DIS@10K/F_4

2N7002KDW
Q68A
DGPU_I2CS_SCL 4 3 MBCLK_THRM (9,20,33,34)
R443 DIS@2.2K_4
+3V_GPU
R442 DIS@2.2K_4
DGPU_I2CS_SDA 1 6 MBDATA_THRM (9,20,33,34)
Q68B
2N7002KDW
EC-SIT-11

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High= AC, Low= Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

Quanta Computer Inc.
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	N13M-GS (GPIO/STRAPS) 4/5	1A
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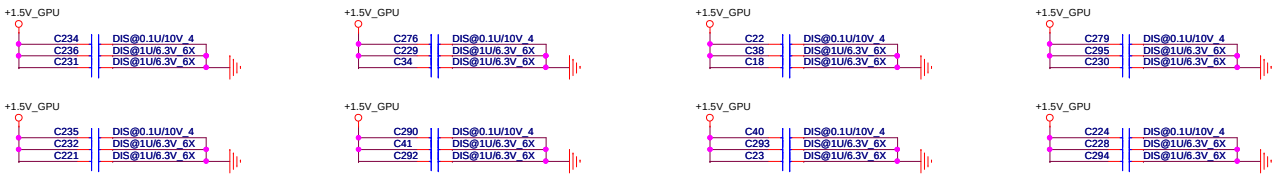
CHANNEL A: 256MB/512MB DDR3
Double T Topology for DDR3 Memory

Hynix 64Mx16 P/N: H5TQ1G63DFR-11C
Hynix 128Mx16 P/N: H5TQ2G63BFR-11C
Samsung 64Mx16 P/N: K4W1G1646C-BC11
Samsung 128Mx16 P/N: K4W2G1646C-HC11

REV-00 change R3086 and R3091 from 240/F_4 to160 Ohms



Close to DRAM

Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: DDR3 VRAM (BGA96) 5/5	Rev: 1A
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Switching Regulator Layout Guideline

1. Place the switching regulator inductor (L3) close to SW_OUT Pin (Pin13).
2. The SW_OUT output traces should be as wide as possible.
3. The GNDX pin (Pin14) should be connected to the main PCB ground plane, with the device GND pins of the PS8622 connected to separate GND island (GNDA) for the device. The GND island (GNDA) should be connected to the main GND plane (GND) with a single-point connection by use of a wide PCB trace.
4. Place the 4.7uF decoupling Capacitor (C4) for VDDIOX close to VDDIOX pin.
5. The GND of the 4.7uF capacitor (C4) for VDDIOX should be placed close to the GND of 4.7uF capacitor (C5) behind Inductor.
6. Place the bead (L2) for VDDIOX close to PS8622.

+3V — L12 BLM18KG221SN1D — VDDIO; C219 0.47UF/10V_X5R_4; C201 1U/10V/X5R_4; GNDA

+3V — L1 BLM18KG221SN1D — VDDIOX; C3 0.47UF/10V_X5R_4; C4 4.7U/10V/X5R_6; EC-SIV-03

SW_OUT — L10 2.2uH/1.2A — VDD12 — L11 BLM18KG221SN1D — VDDRX; C15 4.7U/10V/X5R_6; EC-SIV-03; C187 1U/10V/X5R_4; GNDA

VDDIO — 10K_4 R187 — PD# — 1U/10V/X5R_4

VDDIO — 10K_4 R9 — RST# — C188 2.2U/10V/X5R_6; C2

GND — R197 0/J_4 — GNDA

+1.05V — R188 1K/F_4 — Q6 2N7002K — eDP_HPD# (3); R193 *0_4; eDP_HPD — R189 100K_4

VDDIO — C205 0.1U/10V/X5R_4 — GNDA

EDP_TXLOUTN0 (21)
EDP_TXLOUTP0 (21)
EDP_TXLOUTN1 (21)
EDP_TXLOUTP1 (21)
EDP_TXLOUTN2 (21)
EDP_TXLOUTP2 (21)
EDP_TXLCLKN (21)
EDP_TXLCLKP (21)

Single link LVDS

INT_DPST_PWM (7,21) — R17 *0_4 — +3V

EC-SIV-02 — GNDA

Note:
The decoupling caps C9, C15, C16, C17, C18, C21,C22, C23 shall be close to the power pins as possible

U6 — PS8622 w/o HDCP

(3) eDP_AUXN
(3) eDP_AUXP
(3) eDP_TX0P
(3) eDP_TX0N

VDDRX — C194 0.1U/10V/X5R_4; C189 0.01U/16V/X7R_4 — GNDA

VDDIOX

RST#
PD#
eDP_HPD
I2C_CFG

INT_DISP_ON (7,21)
INT_DPST_PWM_OUT (21)
INT_LVDS_BLON (7,21)
LVDS_DDC_SDA (7,21)
LVDS_DDC_SCL (7,21)

VDDIO — C218 0.1U/10V/X5R_4 — GNDA

VDD12 — C217 0.01U/16V/X7R_4; C203 0.1U/10V/X5R_4 — GNDA

EC-SIV-02 — GNDA

SW_OUT
GND
GPIO0
RLV_CFG
RLV_SSC
CSDA/MSDA
CSCL/MSCL
REXT
RLV_AMP
GNDA

VDD12 — C196 0.01U/16V/X7R_4; C216 0.1U/10V/X5R_4 — GNDA

R16 4.99K/F_4; R18 4.99K/F_4

Note:
R14: LVDS output swing control
4.99K for default swing, change the value for swing adjust

Power On Configuration

VDDIO — R192 *4.7K_4 — I2C_CFG — R186 4.7K_4

I2C_CFG: Initial code loading selection, internal pull-down ~80K
L: Reserved
M: No initial code loading, external I2C control is expected
H: Load initial code from external EEPROM through MSCL/MSDA

VDDIO — R13 4.7K_4 — RLV_SSC — R12 *4.7K_4

RLV_SSC: LVDS SSC selection, internal pull-down ~80K
L: SSC off
M: +/- 0.5% central spreading
H: +/- 1% central spreading

VDDIO — R11 *4.7K_4 — RLV_CFG — R10 4.7K_4

RLV_CFG: LVDS color depth and data mapping selection, internal pull-down ~80K
L: 8-bit LVDS, VESA mapping
M: 8-bit LVDS, JEIDA mapping
H: 6-bit LVDS, both VESA and JEIDA mapping

EC-SIT-06

+3V — R212 4.7K_4; R218 4.7K_4

(9,18,33,34) MBCLK_THRM — Q70A 2N7002KDW — CSCL/MSCL
+3V
(9,18,33,34) MBDATA_THRM — Q70B 2N7002KDW — CSDA/MSDA

+3V (3,7,8,9,10,11,13,14,15,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
+3V (3,7,8,9,10,11,13,14,15,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)

Quanta Computer Inc.
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	PS8622 LVDS Converter	1A
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+3V (3,7,8,9,10,11,13,14,15,20,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
3VPCU (8,25,28,32,34,36,37,39,40,46,48,49)
+15V (30,32,37,38,42,43,46,48)
+5V (7,8,11,22,23,24,26,31,32,33,45,46)
VIN (35,36,37,38,39,41,44,45,46)
5VPCU (8,36,37,38,39,40,41,42,43,44,46,48)

LCDVCC

+15V, +3V, +LCDVCC
R203 330K_4
Q10 AO3404
EC-SIT-14
F5 FUSE_3A_6V
C9 10U/6.3V/X5R_8
R206 22_8
LCDVCC_ON
C190 0.022U/25V/X7R_6
5VPCU
Q35 2N7002W
Q32 2N7002W
R202 100K_4
Q34 PDTC144EU
(7,20) INT_DISP_ON
R190 100K/J_4

Back Light

3VPCU, +3V
R204 10K_4
R191 *4.7K_4
(32,34) LID#
RB500V-40 D11, D12 RB500V-40
DISPON
C198 0.1U/10V/X7R_4
R198 100K_4
C202 *47P/50V/NPO_4
(7,20) INT_LVDS_BLON
R201 2.2K_4
R207 100K/J_4
C192 *1U/10V/X5R_6
Q33 PDTC144EU
LCD_BK_OFF (8)

LOGO_LED_A#
For EMI C160 2200P/50V/X7R_4
LOGO_LED_A#
*Clamp-Diode_4 C158

eDP converter HM76

(20) INT_DPST_PWM_OUT R20 0/J_4
(7,20) INT_DPST_PWM R19 *0/J_4
VADJ_PWM
C6 *47P/50V/NPO_4

GFX_PWR_SRC
C13 0.1U/25V/X7R_6
C12 0.1U/25V/X7R_6
C14 *10U/25V/X6S_12
R15 0_8 VIN

LVDS@GS12303-11141-9H
C193 2.2U/6.3V/X5R_6
+LCDVCC, +3V
(7,20) LVDS_DDC_SCL
(7,20) LVDS_DDC_SDA
LVDS_DDC_SCL
LVDS_DDC_SDA
INT_TXLOUTN0
INT_TXLOUTP0
INT_TXLOUTN1
INT_TXLOUTP1
INT_TXLOUTN2
INT_TXLOUTP2
INT_TXLCLKN
INT_TXLCLKP
VADJ_PWM
DISPON
GFX_PWR_SRC
CN4

+3V
C210 *47P/50V/NPO_4
C207 *47P/50V/NPO_4
close to CN2
+3V
R22 2.2K_4
R21 2.2K_4
LVDS_DDC_SCL
LVDS_DDC_SDA

LVDS (11.6") (1024x600, 1366x768)

(7) INT_TXLCLKP_HM76
(7) INT_TXLCLKN_HM76
RP4 *0_4P2R_04 INT_TXLCLKP INT_TXLCLKN

(7) INT_TXLOUTP0_HM76
(7) INT_TXLOUTN0_HM76
RP3 *0_4P2R_04 INT_TXLOUTP0 INT_TXLOUTN0

(7) INT_TXLOUTP1_HM76
(7) INT_TXLOUTN1_HM76
RP2 *0_4P2R_04 INT_TXLOUTP1 INT_TXLOUTN1

(7) INT_TXLOUTP2_HM76
(7) INT_TXLOUTN2_HM76
RP1 *0_4P2R_04 INT_TXLOUTP2 INT_TXLOUTN2

(20) EDP_TXLCLKN
(20) EDP_TXLCLKP
RP9 0_4P2R_04 INT_TXLCLKN INT_TXLCLKP

(20) EDP_TXLOUTN0
(20) EDP_TXLOUTP0
RP8 0_4P2R_04 INT_TXLOUTN0 INT_TXLOUTP0

(20) EDP_TXLOUTN1
(20) EDP_TXLOUTP1
RP7 0_4P2R_04 INT_TXLOUTN1 INT_TXLOUTP1

(20) EDP_TXLOUTN2
(20) EDP_TXLOUTP2
RP6 0_4P2R_04 INT_TXLOUTN2 INT_TXLOUTP2

For EMI
LVDS_DDC_SCL
LVDS_DDC_SDA
C10 *2200P/50V/X7R_4
C11 *2200P/50V/X7R_4
INT_TXLCLKN
INT_TXLCLKP
C7 *6.8P/50V/NPO_4
C8 *6.8P/50V/NPO_4

ESD reserve
+LCDVCC
LVDS_DDC_SCL
LVDS_DDC_SDA
SC14 *Clamp-Diode_6
SC1 *Clamp-Diode_6
SC2 *Clamp-Diode_6

Quanta Computer Inc.
PROJECT : LV3D
Size | Document Number: LCD/CAMERA | Rev 1A
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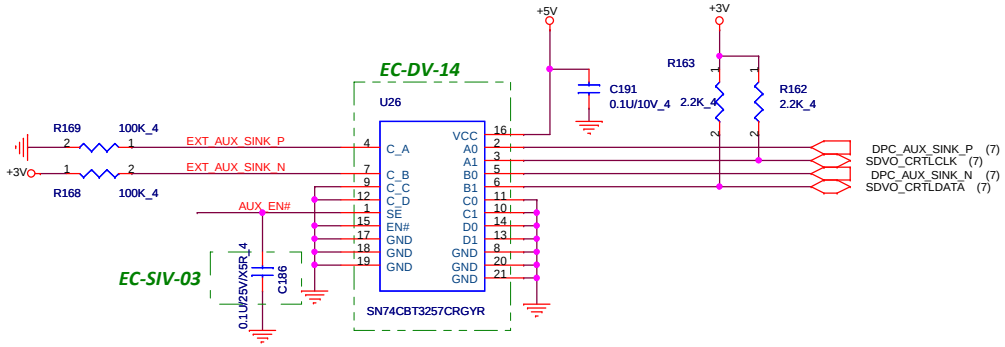
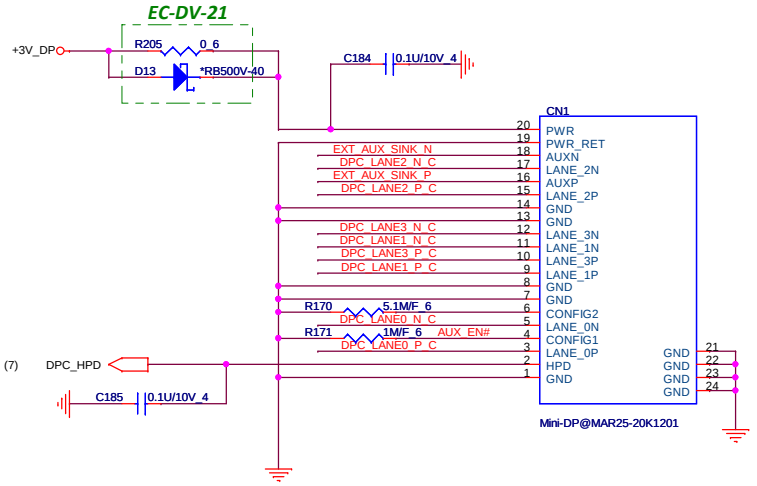
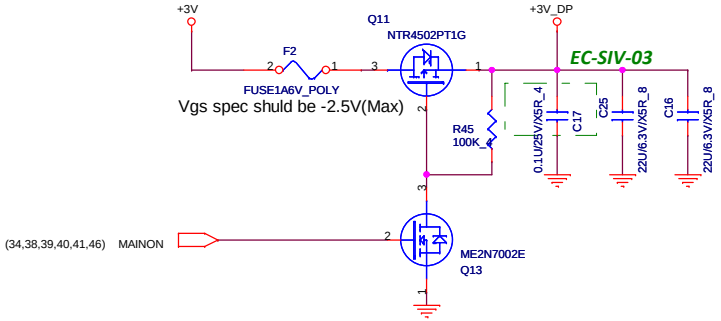
+3V (3,7,8,9,10,11,13,14,15,20,21,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
+5V (7,8,11,23,24,26,31,32,33,45,46)

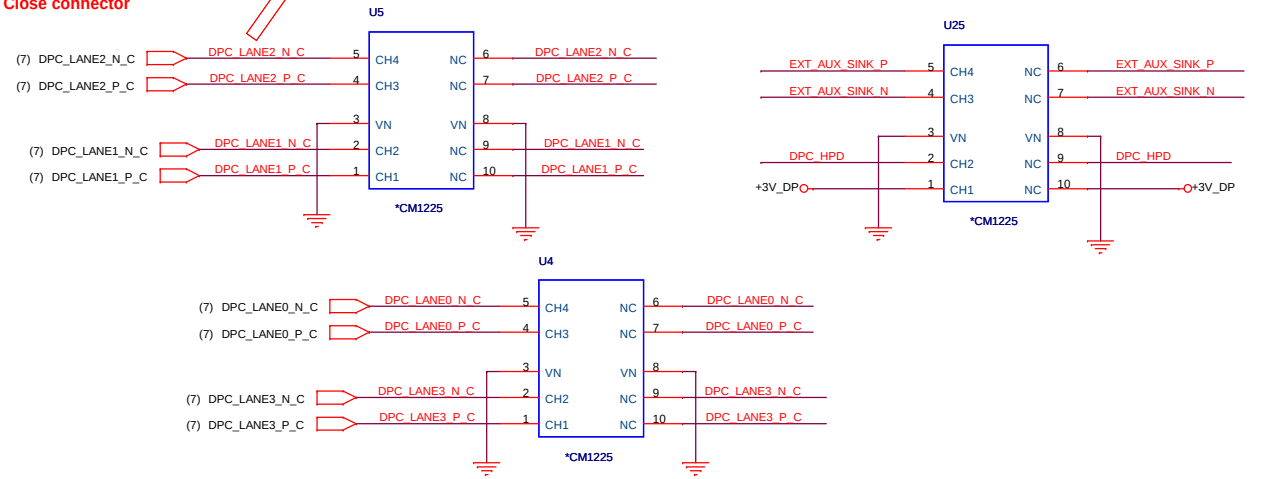


Low : Display port (Default)
High : Dongle attache(covert to DVI)





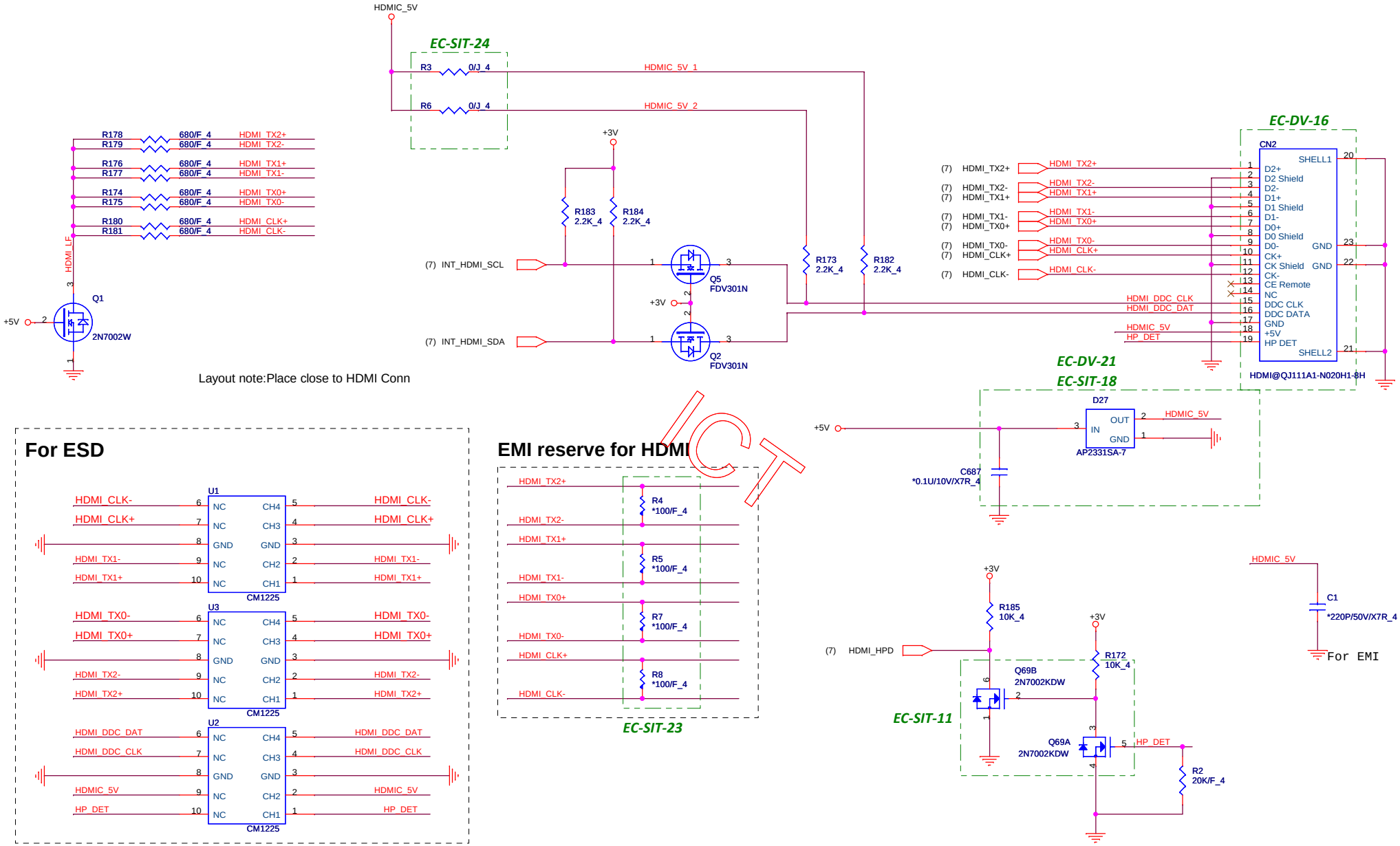
Reserve For ESD
Close connector



Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	Mini Display Port	1A
Date: Monday, March 12, 2012	Sheet 22 of 56	

(3,7,8,9,10,11,13,14,15,20,21,22,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49) +3V
(7,8,11,22,24,26,31,32,33,45,46) +5V



Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: HDMI CONN	Rev: 1A
Date: Monday, March 12, 2012	Sheet 23 of 56	

CODEC(ADO)

<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

ESD reserve
HPOUT_R
HPOUT_L
SC30 Clamp-Diode_6
SC29 Clamp-Diode_6

EMI Reserved
R530 0/J_4
C151 *10P/50V/C0G_4
EC-DV-25
AGND

Please see Design Guide for audio grounding.
DIGITAL GND
ANALOG GND

Close to CODEC

ALC3202-VC3-GR
(MQFN-48)

U48
AVSS2 AVDD2 PVDD1 SPK-L+ SPK-L- PVSS1 PVSS2 SPK-R- SPK-R+ PVDD2 EAPD SPDIFO T_PAD
CBP CBN CPVEE HP-OUT-R HP-OUT-L MIC1-VREFO-L MIC1-VREFO-R MIC2-VREFO LDO-CAP VREF AVSS1 AVDD1
LINE1-R LINE1-L MIC1-R MIC1-L MONO-OUT JDREF Sense-B MIC2-R MIC2-L LINE2-R LINE2-L Sense A
DVDD1 GPIO0/DMIC-DATA GPIO1/DMIC-CLK PD# SDATA-OUT BIT-CLK DVSS2 SDATA-IN DVDD-IO SYNC RESET# PCBEEP

L32 FBMH1608HM151_6
C175 10U/6.3V/X5R_6
C177 10U/6.3V/X5R_6
C178 0.1U/10V/X7R_4
C180 0.1U/10V/X7R_4
C650 2.2U/10V/X5R_6
C656 2.2U/10V/X5R_6 CODEC_CBP
C644 10U/6.3V/X5R_6
C639 1U/10V/X5R_4
C638 0.1U/10V/X7R_4
C640 CODEC_CBN
C641 CODEC_CPVEE
C642 CODEC_LDO
C643 CODEC_VREF

ESD reserve
EXT_MIC_R
EXT_MIC_L
SC27 Clamp-Diode_6
SC26 Clamp-Diode_6

R603 20K/F_4
R604 39.2K/F_4
R158 *20K/F_4
CODEC_SENSE
JACK_SENSE
EXT_MIC

ESD reserve
ACZ_RST#_AUDIO
SC28 *Clamp-Diode_6

DIGITAL
ANALOG
Moat 40 mil

(32) DMIC_DATA
(32) DMIC_CLK
PC_BEEP
ACZ_RST#_AUDIO ACZ_RST#_AUDIO (8)
ACZ_SYNC_AUDIO ACZ_SYNC_AUDIO (8)
ACZ_SDIN0_AUDIO ACZ_SDIN0_AUDIO (8)
ACZ_BITCLK_AUDIO ACZ_BITCLK_AUDIO (8)
ACZ_SDOUT_AUDIO ACZ_SDOUT_AUDIO (8)
C659 *22P/50V/NPO_4
(34) VOLMUTE#
R648 *0/J_4
RB500V-40 D7
COMBOJACK_EAPD
*RB500V-40 D8
R643 *4.7K/J_4

Codec Power(ADO)

+5V (7,8,11,22,23,26,31,32,33,45,46)
+3V (3,7,8,9,10,11,13,14,15,20,21,22,23,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)

+5V_CODEC
R655 0/J_8
C168 0.1U/10V/X7R_4
C174 0.1U/10V/X7R_4
C172 4.7U/10V/X5R_6
C165 4.7U/10V/X5R_6
Close to CODEC
AGND

HDA Power(ADO)

*Intel HDA Either +1.5V_S5 or +3V_S5

+3V_CODEC
R654 0/J_8
C169 1U/10V/X5R_4
C170 0.1U/10V/X7R_4
Close to CODEC

PC BEEP

+5V_CODEC
C164 0.1U/10V/X7R_4
Close to codec
From EC (34) PCBEEP_AD
From PCH (8) ACZ_SPKR
BEEP1 R586 33K/F_4 BEEP2
C642 0.1U/10V/X7R_4 PC_BEEP
R601 10K/J_4
U24 TC7SET32FU

External MIC/Headphone Combo

HPOUT_L R538 75/J_4 HPOUT_LR
HPOUT_R R160 75/J_4 HPOUT_RR
L26 BLM18BD601SN1D 0.2A
L27 BLM18BD601SN1D 0.2A
C621 100P/50VNPO_4
C598 100P/50VNPO_4
HPOUT_LB
HPOUT_RB
JACK_SENSE
EXT_MIC
CN18
COMBO_JACK@JA6424230SB-7H

MIC1-VREFO-L R537 2.2K/J_4 MIC1-VREFO-LL
EXT_MIC_R C582 2.2U/10V/X5R_6 EXT_MIC_RL R541 1K/J_4
EXT_MIC_L C573 2.2U/10V/X5R_6
L7 BLM18BD601SN1D 0.2A
R152 470K/F_4
C154 *100P/50V/NPO_4
COMBOJACK_EAPD
R151 22K/J_4
C155 10U/6.3V/X5R_6

Audio Combo Jack

Important for Jack detect behavior:
The Pin 4 & Pin 5 of COMBO-JACK must use Normal-Open type.

Internal Speaker

<<Attention>>
Place there EMI components next to codec; For EMI issue,
please also refer our ALC269 Layout guide document

SPK_R+ R628 FCM1608KF-601T02(600,0.2A)_6
SPK_R- R633 FCM1608KF-601T02(600,0.2A)_6
SPK_L- R638 FCM1608KF-601T02(600,0.2A)_6
SPK_L+ R646 FCM1608KF-601T02(600,0.2A)_6
SPK_R+_OUT SPK_R-_OUT SPK_L-_OUT SPK_L+_OUT
CN20 Speaker@88266-04001-06
C661 C657 C651 C647 *100P/50V/NPO_4

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

ESD reserve
SPK_R+ SPK_R- SPK_L- SPK_L+
SC31 SC32 SC33 SC34 *Clamp-Diode_6

EMI Reserve

C167 0/J_4 C660 0/J_4 C159 0/J_4 C152 0/J_4 AGND

ESD Reserve

HPOUT_LB HPOUT_RB JACK_SENSE EXT_MIC DMIC_DATA DMIC_CLK
C608 *TVS_4
C617 *TVS_4
C163 Clamp-Diode_6
C157 *TVS_4
C199 Clamp-Diode_6
C195 Clamp-Diode_6

FOR EMI Reserve

ACZ_RST#_AUDIO ACZ_SDOUT_AUDIO ACZ_BITCLK_AUDIO DMIC_DATA DMIC_CLK
C649 *22P/50V/NPO_4
C653 *22P/50V/NPO_4
C652 *22P/50V/NPO_4
C666 *33P/50V/NPO_4
C662 *33P/50V/NPO_4

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	AUDIO (ALC3203-GR)	1A
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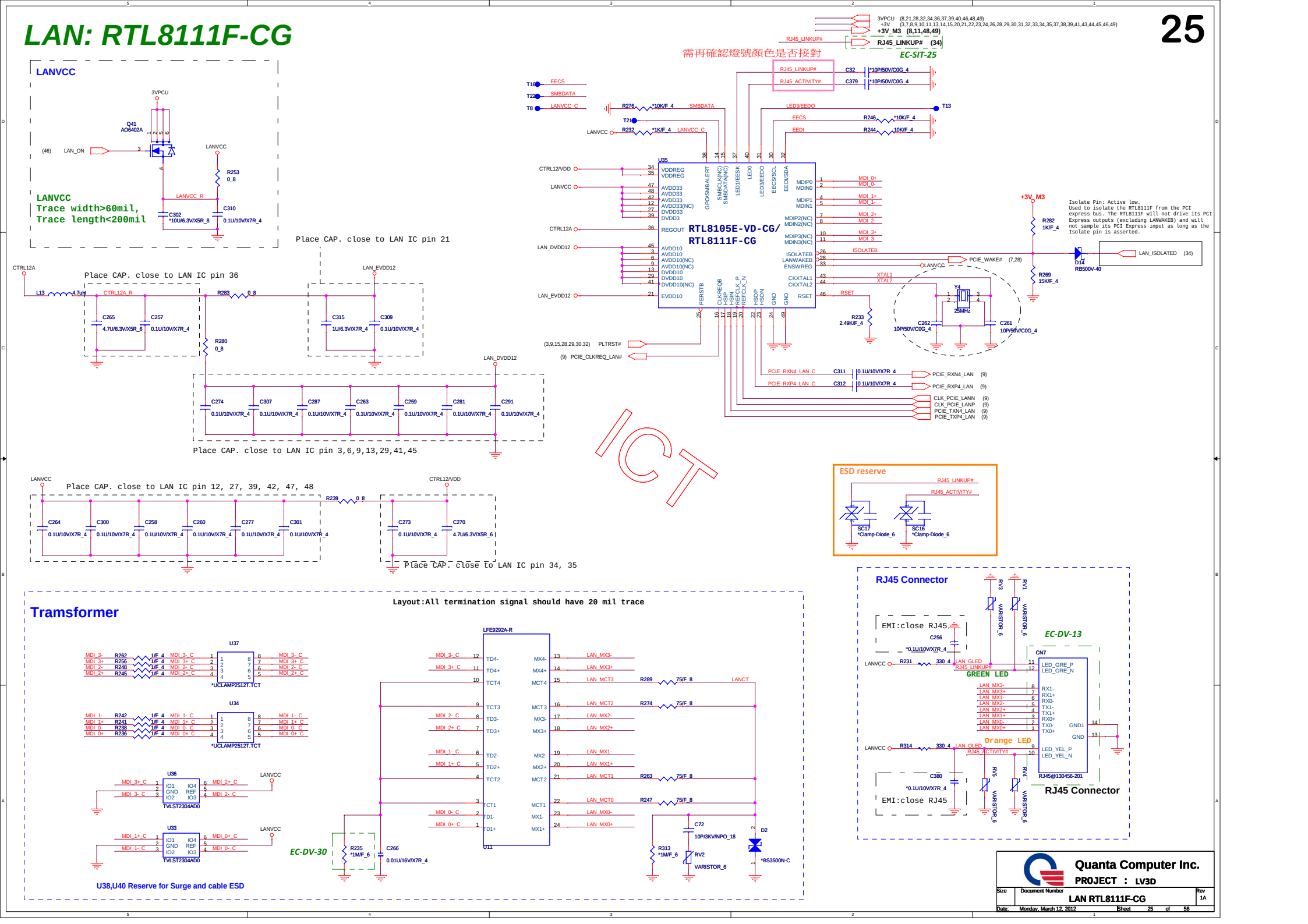
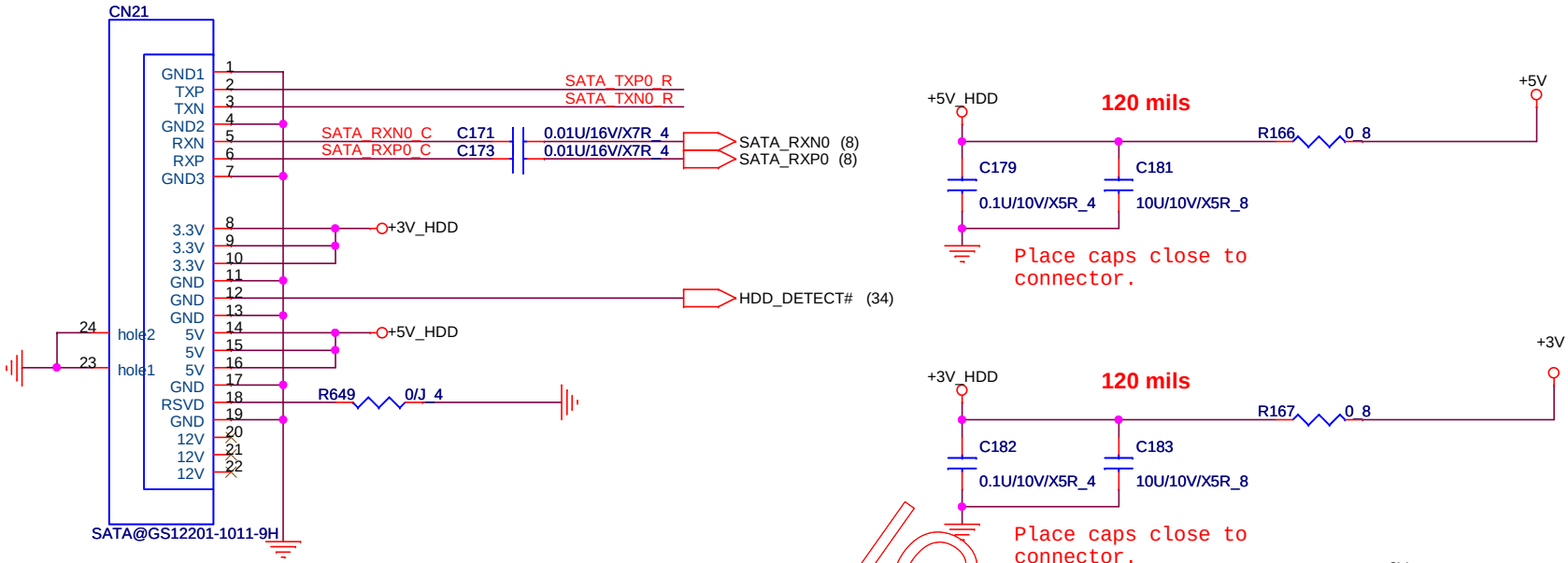
LAN: RTL8111F-CG



Quanta Computer Inc.			
PROJECT : LV3D			
Size	Document Number		Rev
	LAN RTL8111F-CG		1A
Date: Monday, March 12, 2012		Sheet 25 of 56	

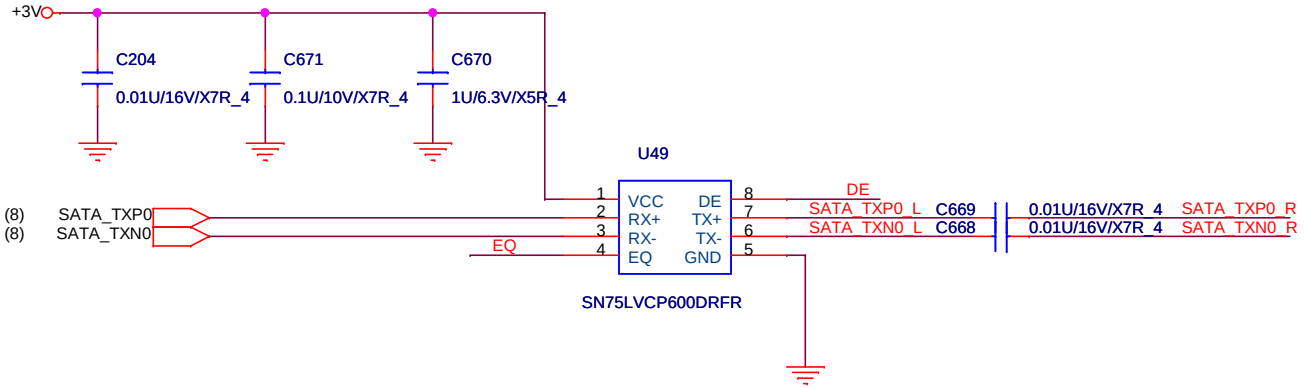
SATA Connector

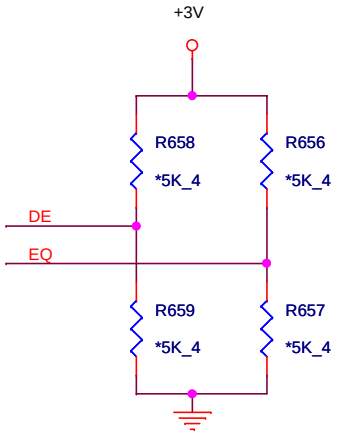
+5V (7,8,11,22,23,24,31,32,33,45,46)
+3V (3,7,8,9,10,11,13,14,15,20,21,22,23,24,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)



ICT

SATA Re-driver





Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	SATA HDD	1A
Date: Monday, March 12, 2012	Sheet 26 of 56	

5V_S5 (11,46)

EC-SIT-20

5V_S5
C682
1U/10V/X5R_6
U54
APL3510DXI-TRG
VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC
40 mils (Iout=1A)
USB3PWR_0
C683 *470P/50V/NPO_4
C684 0.1U/10V/X7R_4
+C685 150U/6.3V/ESR15_7343
EC-SIT-30
(28) USB_ON#
USB_OC0# (9)

USB3PWR_0
U53
AZ1065-06F
C681 0.1U/10V_4
USB30_RX1- USB30_RX1+
USBP0+_C USBP0-_C
USB30_TX1-_C USB30_TX1+_C

5V_S5
C680
1U/10V/X5R_6
U52
APL3510DXI-TRG
40 mils (Iout=1A)
USB3PWR_1
C677 *470P/50V/NPO_4
C678 0.1U/10V/X7R_4
+C679 150U/6.3V/ESR15_7343
EC-SIT-30
(28) USB_ON#
USB_OC0# (9)

USB3PWR_1
U55
AZ1065-06F
C686 0.1U/10V_4
USB30_RX2- USB30_RX2+
USBP1+_C USBP1-_C
USB30_TX2-_C USB30_TX2+_C
EC-SIT-28

EC-SIT-22
CML2
MCM2012B900GBE
USB3PWR_0
USB3.0 PORT1
(9) USBP0-
(9) USBP0+
USBP0-_C
USBP0+_C
(9) USB30_RX1-
(9) USB30_RX1+
(9) USB30_TX1-
(9) USB30_TX1+
C533 0.1U/10V/X5R_4
C532 0.1U/10V/X5R_4
CN12
1 VBUS
2 D-
3 D+
4 GND
5 SSRX-
6 SSRX+
7 GND
8 SSTX-
9 SSTX+
13 12 11 10
EC-SIT-27
USB3.0@ABA-USB-053-P14

EC-SIT-22
CML1
MCM2012B900GBE
USB3PWR_1
USB3.0 PORT2
(9) USBP1-
(9) USBP1+
USBP1-_C
USBP1+_C
(9) USB30_RX2-
(9) USB30_RX2+
(9) USB30_TX2-
(9) USB30_TX2+
C477 0.1U/10V/X5R_4
C478 0.1U/10V/X5R_4
CN10
1 VBUS
2 D-
3 D+
4 GND
5 SSRX-
6 SSRX+
7 GND
8 SSTX-
9 SSTX+
13 12 11 10
EC-SIT-27
USB3.0@ABA-USB-053-P14

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	USB3.0 X 2	1A
Date: Tuesday, March 13, 2012	Sheet 27 of 56	

MiniCard WLAN connector

3VPCU (8,21,25,32,34,36,37,39,40,46,48,49)
+3V (3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
+1.5V (11,29,38)
3V_S5 (3,7,8,9,10,11,34,46)

CN19 EC-SIT-37

(29) MINICARD_PME#	MINICARD_PME#	1	WAKE#	3.3V_1	2
		3	RESERVED_1	GND0	4
		5	RESERVED_2	1.5V_1	6
(9) PCIE_CLKREQ_WLAN#		7	CLKREQ#	UIM_PWR	8
		9	GND1	UIM_DATA	10
(9) CLK_PCIE_WLANN		11	REFCLK-	UIM_CLK	12
(9) CLK_PCIE_WLANP		13	REFCLK+	UIM_RESET	14
		15	GND2	UIM_VPP	16
(8,30,34) SERIRQ	R589 0/J_4	17	UIM_C8	GND3	18
T25		19	UIM_C4	W_DISABLE#	20
		21	GND4	PERST#	22
(9) PCIE_RXN2_WLAN		23	PERn0	3.3VAUX1	24
(9) PCIE_RXP2_WLAN		25	PERp0	GND5	26
		27	GND6	1.5V_2	28
		29	GND7	SMB_CLK	30
(9) PCIE_TXN2_WLAN		31	PETn0	SMB_DATA	32
(9) PCIE_TXP2_WLAN		33	PETp0	GND8	34
		35	GND9	USB_D-	36
		37	RESERVED_3	USB_D+	38
		39	RESERVED_4	GND10	40
		41	RESERVED_5	LED_WWAN#	42
		43	RESERVED_6	LED_WLAN#	44
		45	RESERVED_7	LED_WPAN#	46
		47	RESERVED_8	1.5V_3	48
		49	RESERVED_9	GND11	50
		51	RESERVED_10	3.3V_2	52

WLAN@B32P101-0100N-H

+3.3V_WLAN, +1.5V

LPC_FRAME# (8,30,34)
LPC_AD0 (8,30,34)
LPC_AD1 (8,30,34)
LPC_AD2 (8,30,34)
LPC_AD3 (8,30,34)

WLAN_OFF_R#
R596 0/J_4 PLTRST# (3,9,15,25,29,30,32)
R605 0/J_4
R619 0/J_4 PCLK_DEBUG (9) LPC_DRQ#0 (8)
USBP4- R
USBP4+ R
R641 0_4
R642 0_4 USBP4- (9) USBP4+ (9)

U47 *PJSR05
USBP4- R
USBP4+ R
IO1 VIN IO2 GND
+3.3V_WLAN

PCI-Express TX and RX direct to connector

R650 0_4
(10) BT_ON
D25 RB500V-40
R653 0_4
R652 10K/J_4

ESD reserve
PLTRST#
SC25 *Clamp-Diode_6

3V_S5
R567 10K_4
(7,25) PCIE_WAKE#
Q60 PDTC144EU
MINICARD_PME#

ICT

AOAC

EC-SIT-34
3VPCU
Q59 AOS3413
+3.3V_WLAN
+3V
R560 *0/J_8
R573 4.7K_4
R549 100K/F_4

EC-DV-29
EC
PCH
(34) WLAN_AOAC_EN R342 *0_4
(7) WLAN_AOAC_ON R362 0_4
Q61 PDTC144EV

WLAN_OFF_R#
D24 RB500V-40
WLAN_OFF# (10)
R613 *0_4

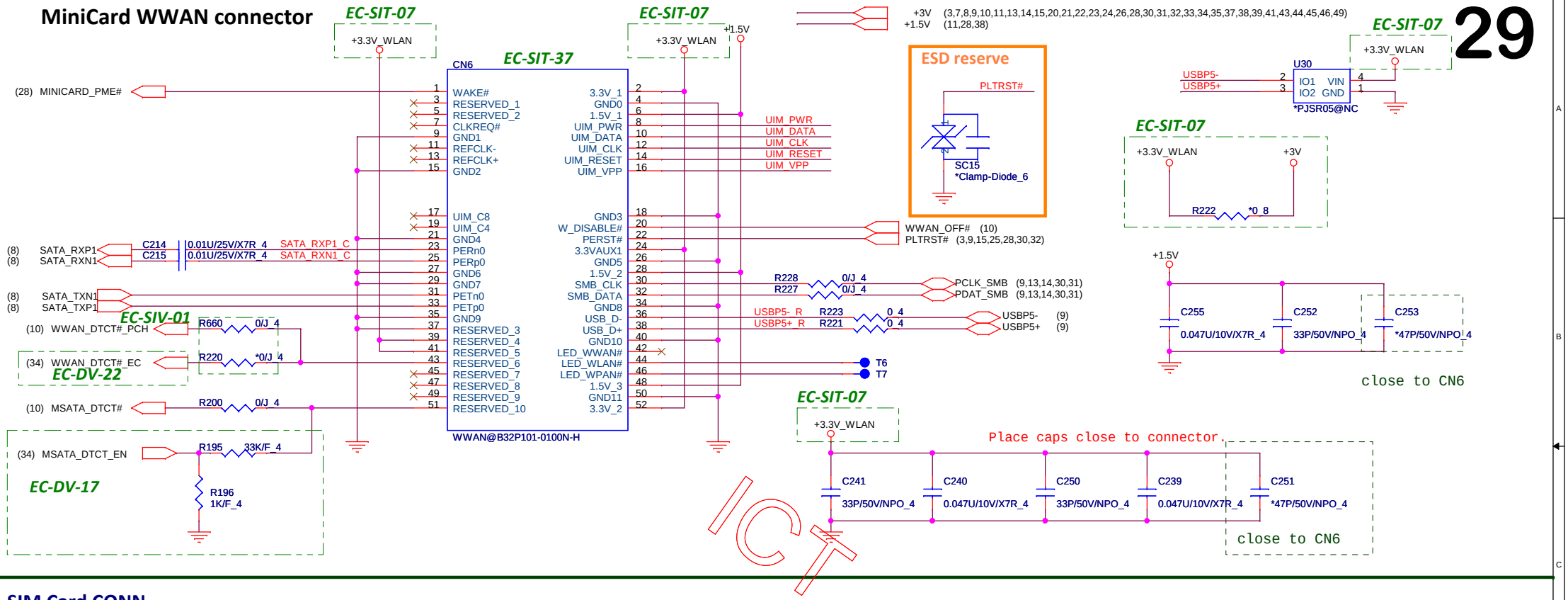
+3.3V_WLAN
Place caps close to connector.
close to CN22
C658 0.1U/10V/X7R_4
C667 0.047U/10V/X7R_4
C593 0.1U/10V/X7R_4
C636 0.047U/10V/X7R_4
C663 4.7U/6.3V/X5R_6
C654 *47P/50V/NPO_4

+1.5V
C664 0.01U/16V/X7R_4
C607 0.1U/10V/X7R_4
C655 10U/6.3V/X5R_8
C645 *47P/50V/NPO_4
close to CN22

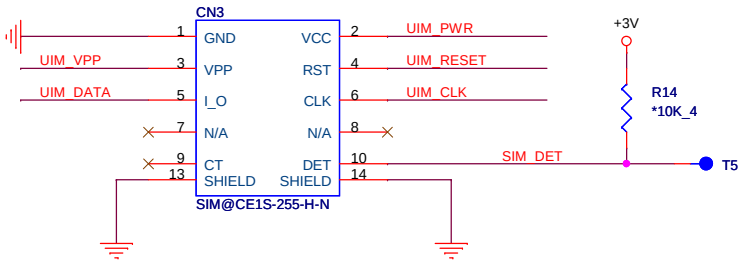
Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	WLAN/BT	1A
Date: Wednesday, March 14, 2012	Sheet 28 of 56	

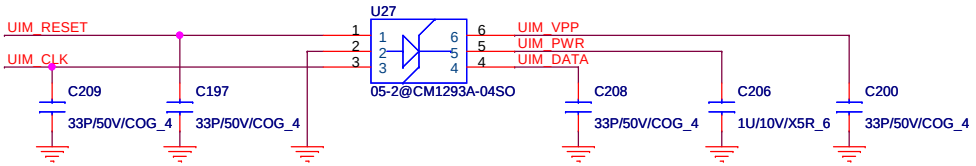
MiniCard WWAN connector



SIM Card CONN



Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible



Quanta Computer Inc.		
PROJECT : LV3D		
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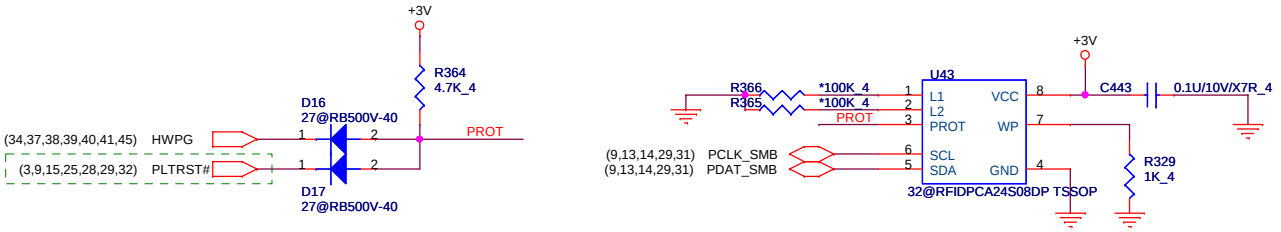
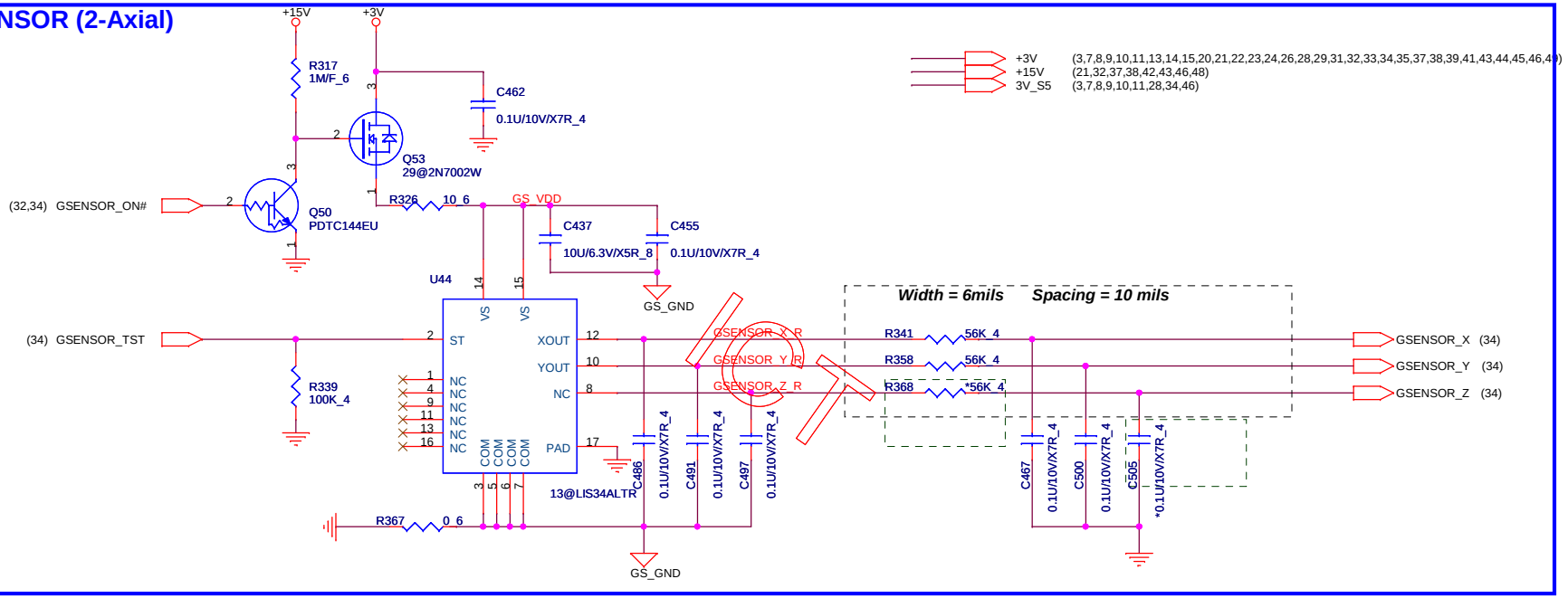
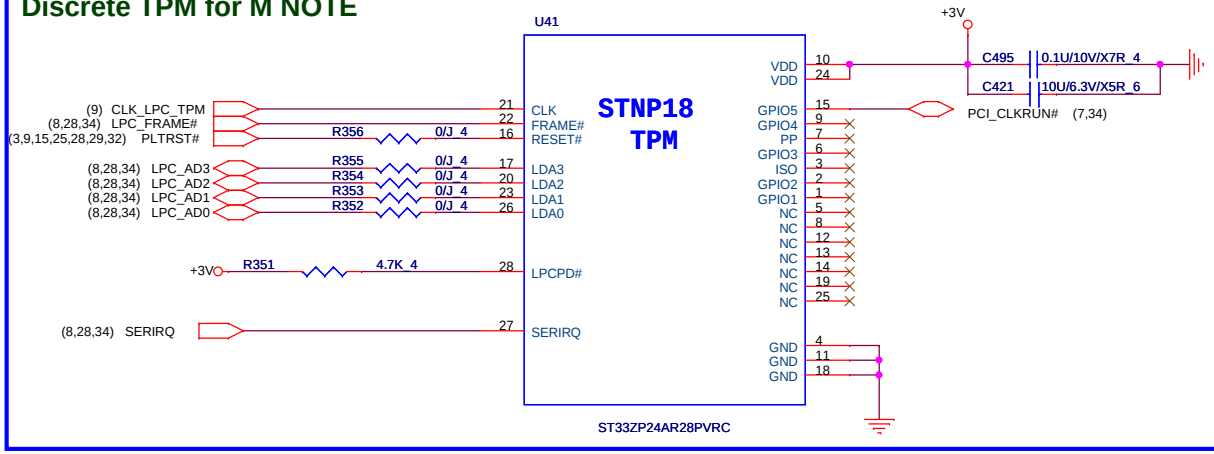
RFID



G-SENSOR (2-Axial)



Discrete TPM for M NOTE



Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: G-SENSOR/TPM/RFID	Rev: 1A
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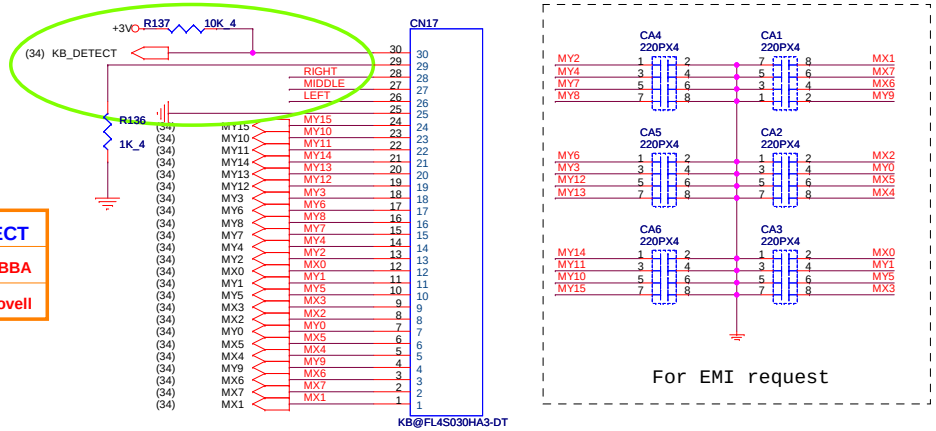
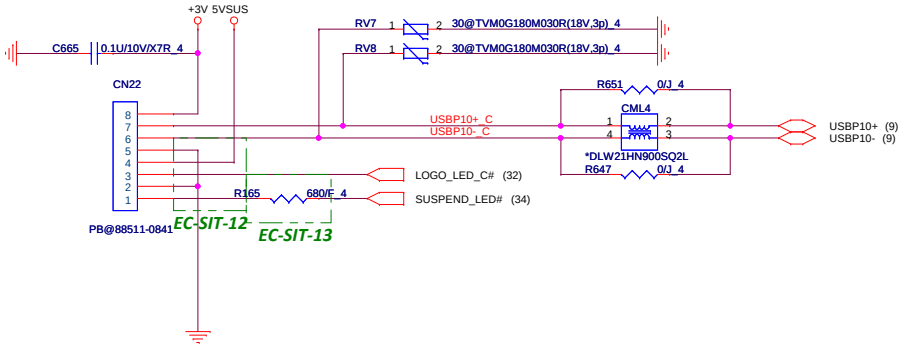
KEYBOARD

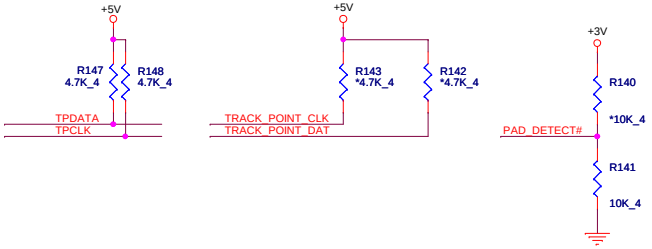


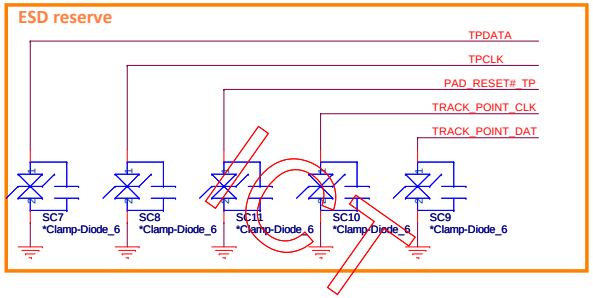
KB_DETECT	
High	ABBA
Low	Lovell

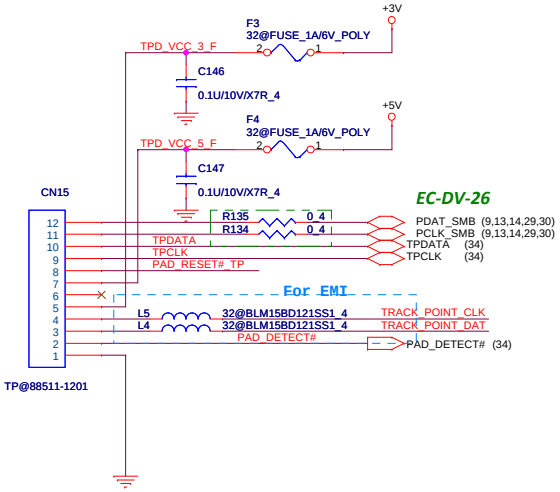
FINGER PRINT with C cover & Front LED

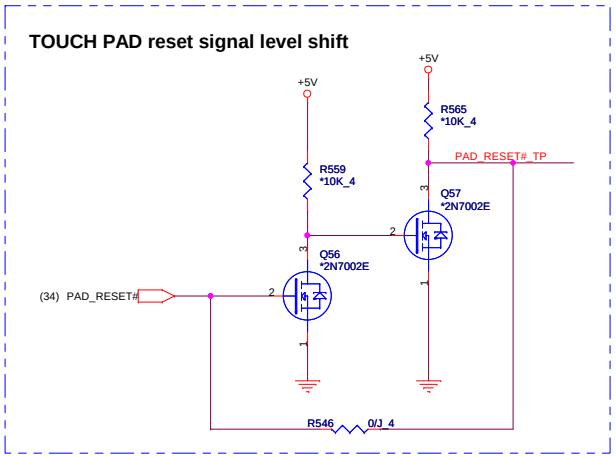


CLICK PAD

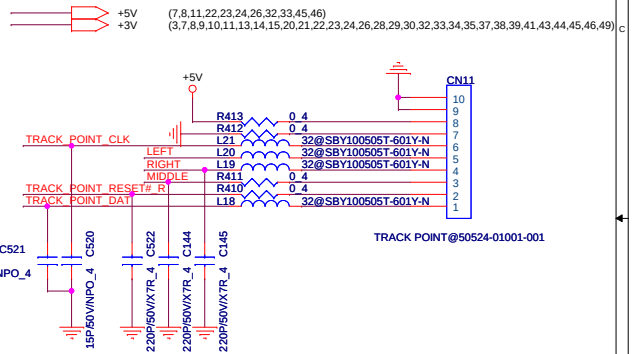


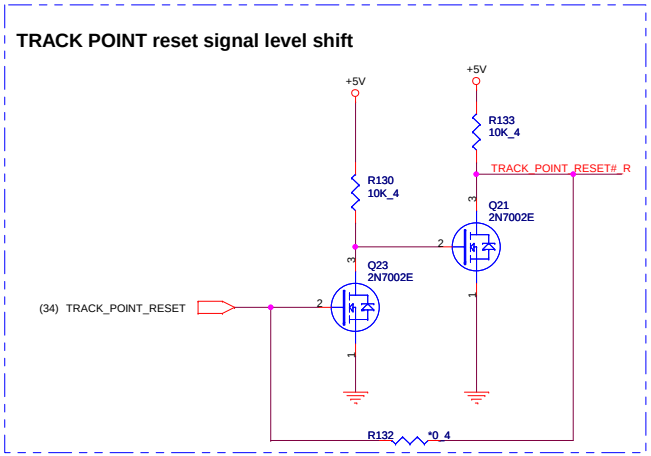






TRACK POINT





Quanta Computer Inc.

PROJECT : LV3D

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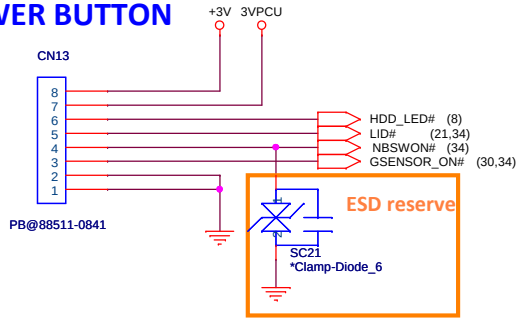
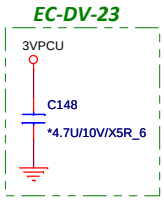
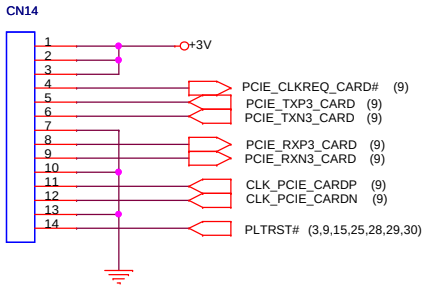
POWER BUTTON

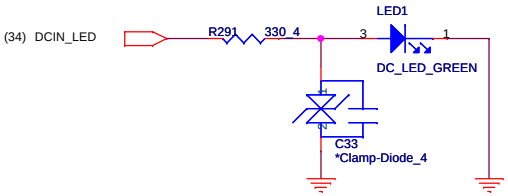




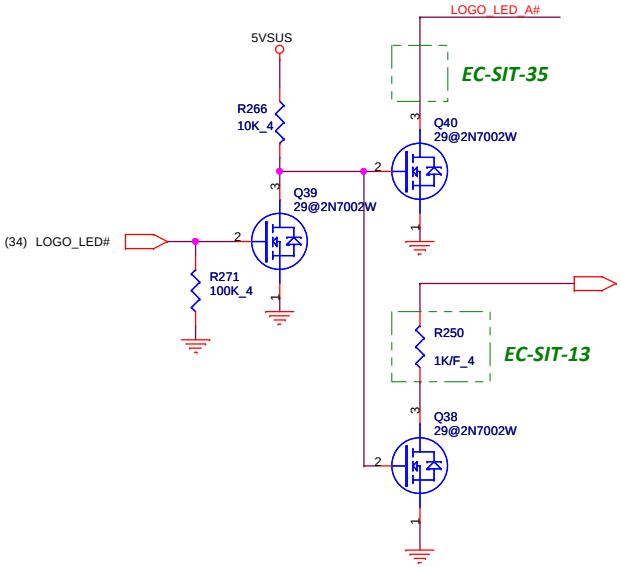
Card Reader Board



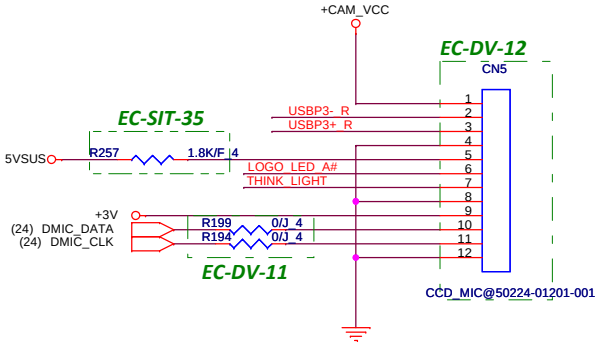
DC-IN LED



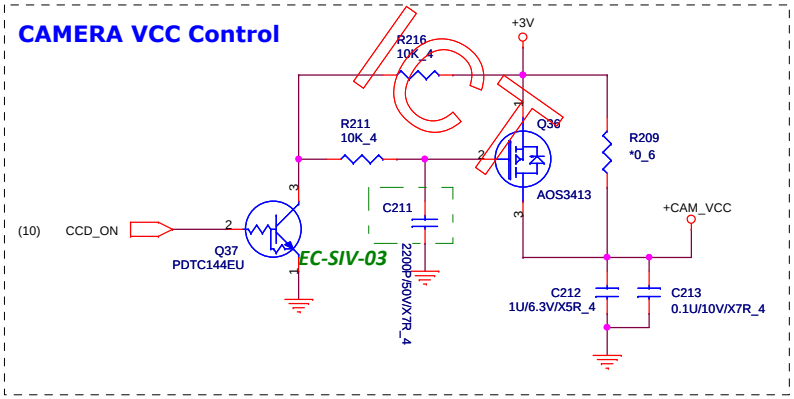
A cover LED



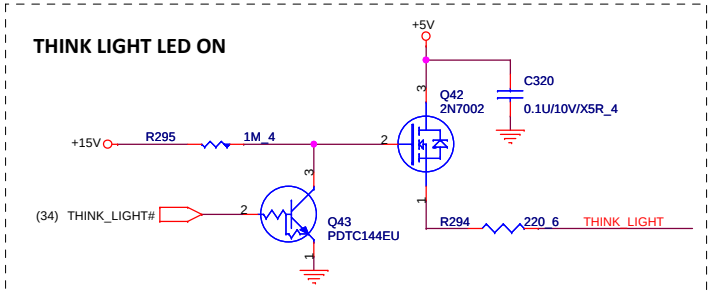
A cover LED/Camera BUTTON



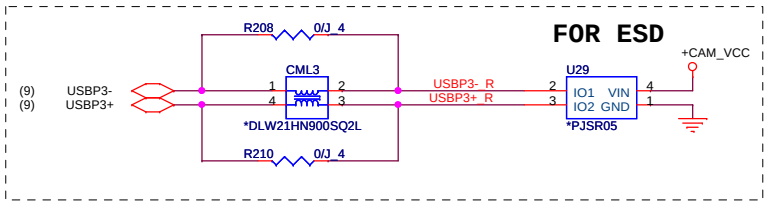
CAMERA VCC Control



THINK LIGHT LED ON



FOR ESD



+3V (3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,33,34,35,37,38,39,41,43,44,45,46,49)
3VPCU (8,21,25,28,34,36,37,39,40,46,48,49)
3V_S5 (3,7,8,9,10,11,28,34,46)
5VSUS (31,46)

Quanta Computer Inc.
PROJECT : LV3D

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	Daughter board CON/LED/CCD	1A
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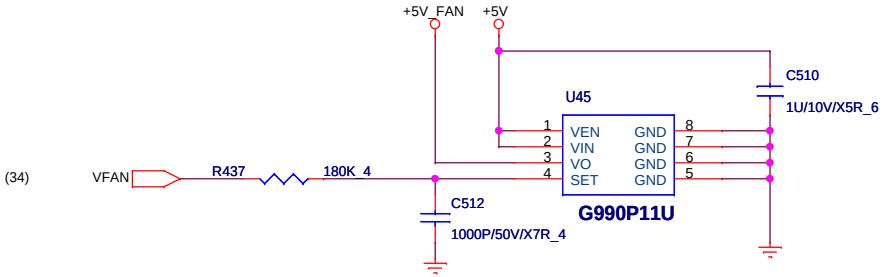
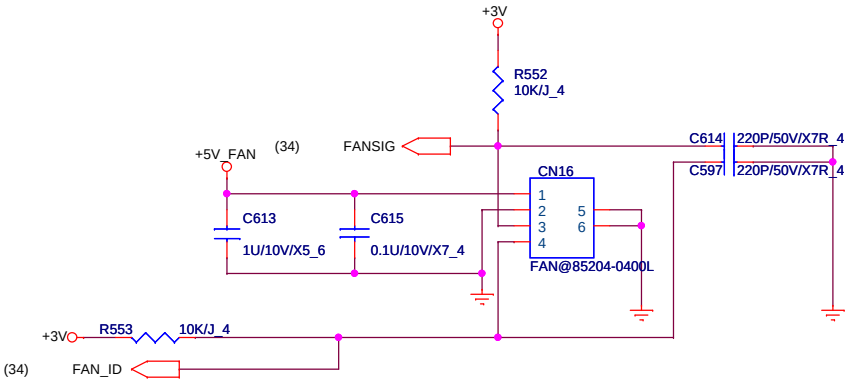
FAN CONTROL

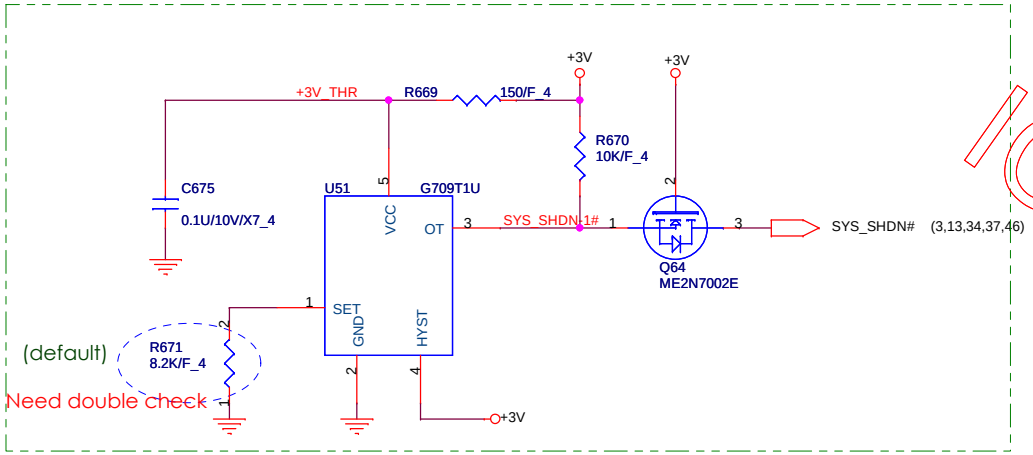
(3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,34,35,37,38,39,41,43,44,45,46,49) +3V
(7,8,11,22,23,24,26,31,32,45,46) +5V



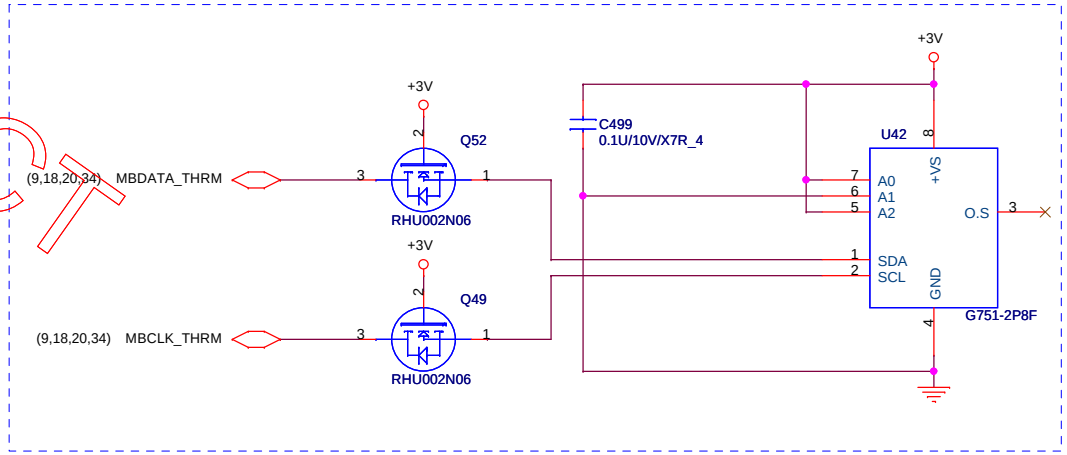


CPU Thermal Sensor

EC-SIT-03



Charger Thermal Sensor



ADDRESS: 9AH

ADDRESS

1	0	0	1	A2	A1	A0	0

MSB LSB

Quanta Computer Inc.		
PROJECT : LV3D		
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	FAN & THERMAL	1A
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IT8518

EC Reset

Borad ID

DIS =>R296
UMA=>R297

R101	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

POWER SWITCH/ CARE BUTTON

4Mbit (512k Byte), SPI

Winbond AKE37FN0N01
MAX AKE37FP0Z02

Delay time(ms)=88000 x CMR(uF)

Quanta Computer Inc.
PROJECT : LV3D
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Boundary Hole

HOLE22 *h-c315d228p2
EC-SIT-29
HOLE4 *h-c315d228p2
HOLE5 *h-c315d228p2
HOLE18 *h-c315d228p2
HOLE3 *h-c315d228p2
HOLE2 *h-c315d228p2
HOLE21 *h-c315d228p2
EC-SIT-39
HOLE16 *hg-c315d98p2

MiniCard WWAN

HOLE15 H-TC217BIC142D102P2
HOLE14 H-C98D98N

MiniCard WLAN

HOLE20 H-TC217BIC142D102P2

1.5V_SUS (3,11,13,14,38,42,46)
+3V (3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,37,38,39,41,43,44,45,46,49)
VIN (21,36,37,38,39,41,44,45,46)

Hole for GPU support

HOLE8 *h-c217d157p2
HOLE13 *h-c217d157p2
HOLE11 *h-c157d157n

KB NUT hole

HOLE10 *h-c339d339n

Hole for CPU support

HOLE12 *h-c217d157p2
HOLE17 *h-c217d157p2
HOLE9 *h-c157d157n

1.5V_SUS
EC18 EC17 EC19 EC15 0.1U/10V/X7R_4

+3V
EC16 EC23 0.1U/10V/X7R_4

Non PTH hole

EC-SIT-31
HOLE6 *h-c87d87n
HOLE19 *H-O146X87D146X87N
HOLE1 *H-C157D157N

PAD

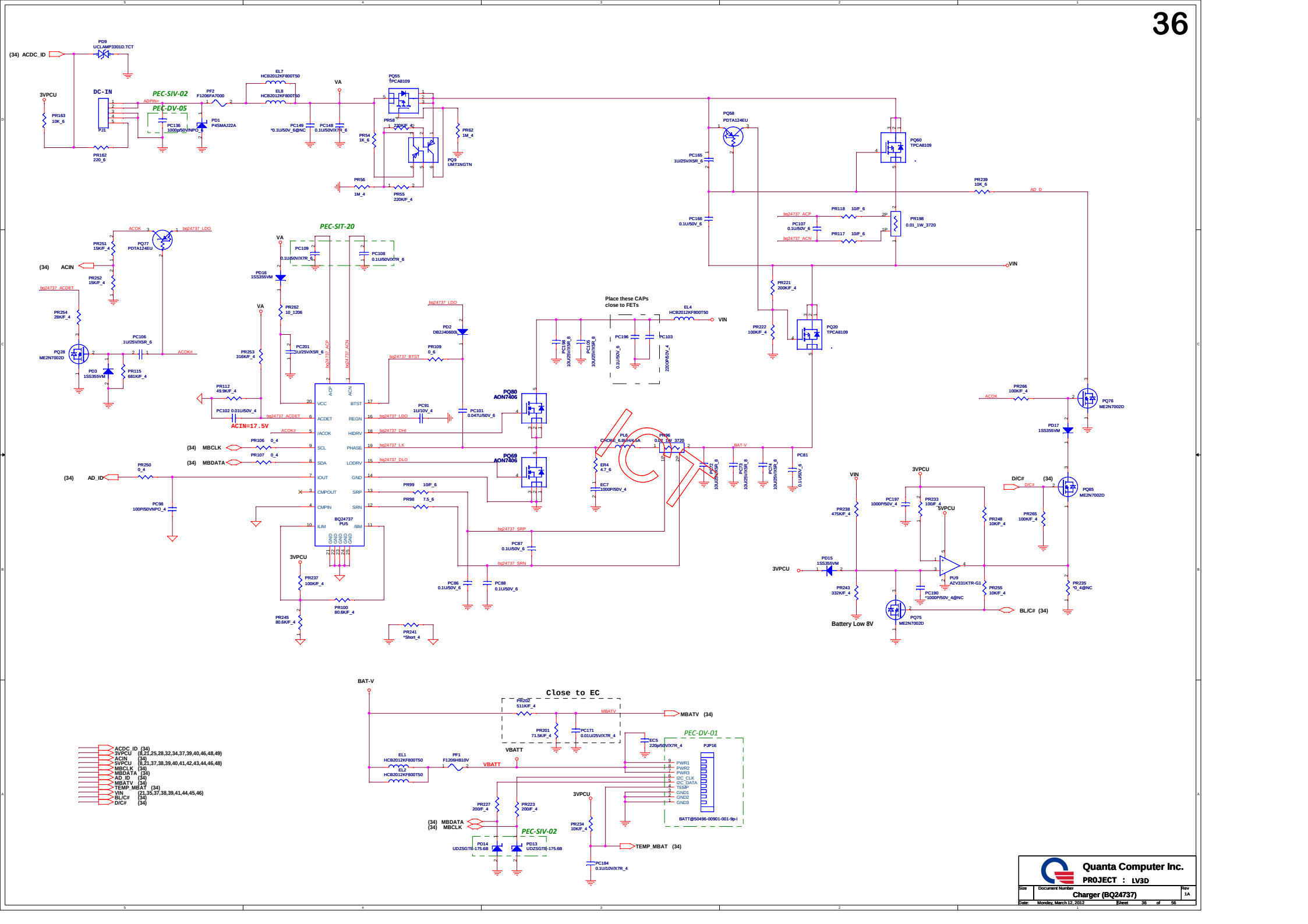
EC-SIT-32
GP1 *O-LV3D-1
GP2 *O-LV3D-1
GP3 *PAD-S50
EC-SIT-32
GP4 *spad-re1870x245np

VIN
EC22 EC4 EC20 EC3 EC11 EC9 EC14 EC10 0.1U/25V/X5R_4

EC-SIT-33
+1.05V
C689 C690 0.1U/10V/X7R_4

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	Screw Hole/EMI/ESD	1A
Date: Thursday, March 15, 2012	Sheet 35 of 56	



Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	Charger (BQ24737)	1A
Date: Monday, March 12, 2012	Sheet 36 of 56	

(8,21,25,28,32,34,36,39,40,46,48,49) 3VPCU
(8,21,36,38,39,40,41,42,43,44,46,48) 5VPCU
(21,30,32,38,42,43,46,48) +15V
(21,35,36,38,39,41,44,45,46) VIN

5V_AL
PR273 39K/F_4
PEC-SIT-23
PR123
(3,13,33,34,46) SYS_SHDN#
3V5V_EN
*0_4S

ESD reserve
PGOOD
SC13 *Clamp-Diode_6

5VPCU
Freq. 365KHz
Peak= 7.41A
O.C.P.= 9.64A

3VPCU
Freq. 460KHz
Peak=7.44A
O.C.P.=9.67A

PEC-SIV-01
PEC-SIT-21
Place these CAPs close to FETs
VIN
PC214 10U/25V/X5R_8
PC118 10U/25V/X5R_8
PC119 2200P/50V/X7R_4
PC218 0.1U/50V/X7R_6

PEC-DV-09
PR126 *390K_4
PR125 *150K/F_4
PEC-SIT-23
PR275 *0_6S
PC123 10U/6.3V/X5R_6
PC219 10U/10V/X5R_6
+2VREF
3V_AL
PC116 0.1U/50V/X7R_6
PEC-SIV-02
PC128 0.22U/10V/X5R_4
PR136 *0_4@NC
PR137 *0_4S

PQ30 AON7406
PQ88 AON7406
PQ31 AON7702
PQ87 AON7702

PU6 TPS51123RGER
TPS51123EN
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
PGOOD
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
EN0 VIN VREG3 VREG5 REF TONSEL
UGATE1 BOOT1 PHASE1 LGATE1 VOUT1 FB1 PGOOD
UGATE2 BOOT2 PHASE2 LGATE2 OUT2 FB2
ENTRIP1 ENTRIP2 ENC SKIPSEL GND GND

PC120 0.1U/25V/X5R_4
PR127 2.2/F_6
PR128 2.2/F_6
PC121 0.1U/25V/X5R_4
PR130 *10K_4
+3V
PR285 *0_4S
(30,34,38,39,40,41,45) HWPG
PR133 115K/F_4
PR132 127K/F_4
PR124 0_4
PR278 *0_4
PEC-DV-06
PEC-SIT-02

PEC-SIV-01
PEC-SIT-21
Place these CAPs close to FETs
VIN
PC114 0.1U/50V/X7R_6
PC115 2200P/50V/X7R_4
PC215 10U/25V/X5R_8
PC113 10U/25V/X5R_8

5VPCU
External Adjustable
PL9 PCMC063T-2R2MN
PEC-SIT-29
PEC-SIT-23
PC205 0.1U/10V/X7R_4
PC208 4.7U/10V/X5R_6
PC111 100U/6.3V/ESR45_3528
PC104 220U/6.3V/ESR25_7343
PR139 *0_4S
PR134 15.4K/F_4
PR135 10K/F_4
ER9 *4.7/F_6
EC24 *1000P/50V/X7R_4

3VPCU
External Adjustable
PL8 PCMC063T-2R2MN
PR141 *0_4S
PEC-SIT-23
PR140 6.8K/F_4
PR138 10K/F_4
ER5 *4.7/F_6
EC8 *1000P/50V/X7R_4
PC97 220U/6.3V/ESR25_7343
PC206 4.7U/10V/X5R_6
PC209 0.1U/10V/X7R_4

PC112 0.1U/25V/X5R_4
PR270 *0_6S
2V_LGATE2
PEC-SIT-23
PD4 BAT54S
PC212 0.1U/25V/X5R_4
PC213 0.1U/25V/X5R_4
PD5 BAT54S
PR268 22_8
+15V
+15V_ALWP
PC211 *0.1U/25V/X5R_4@NC
PC210 0.1U/25V/X5R_4

3V5V_EN
PC117 *0.1U/10V_4
PEC-SIV-03

Quanta Computer Inc.
PROJECT : LV3D

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	SYSTEM 5V/3V (TPS51123RGER)	1A
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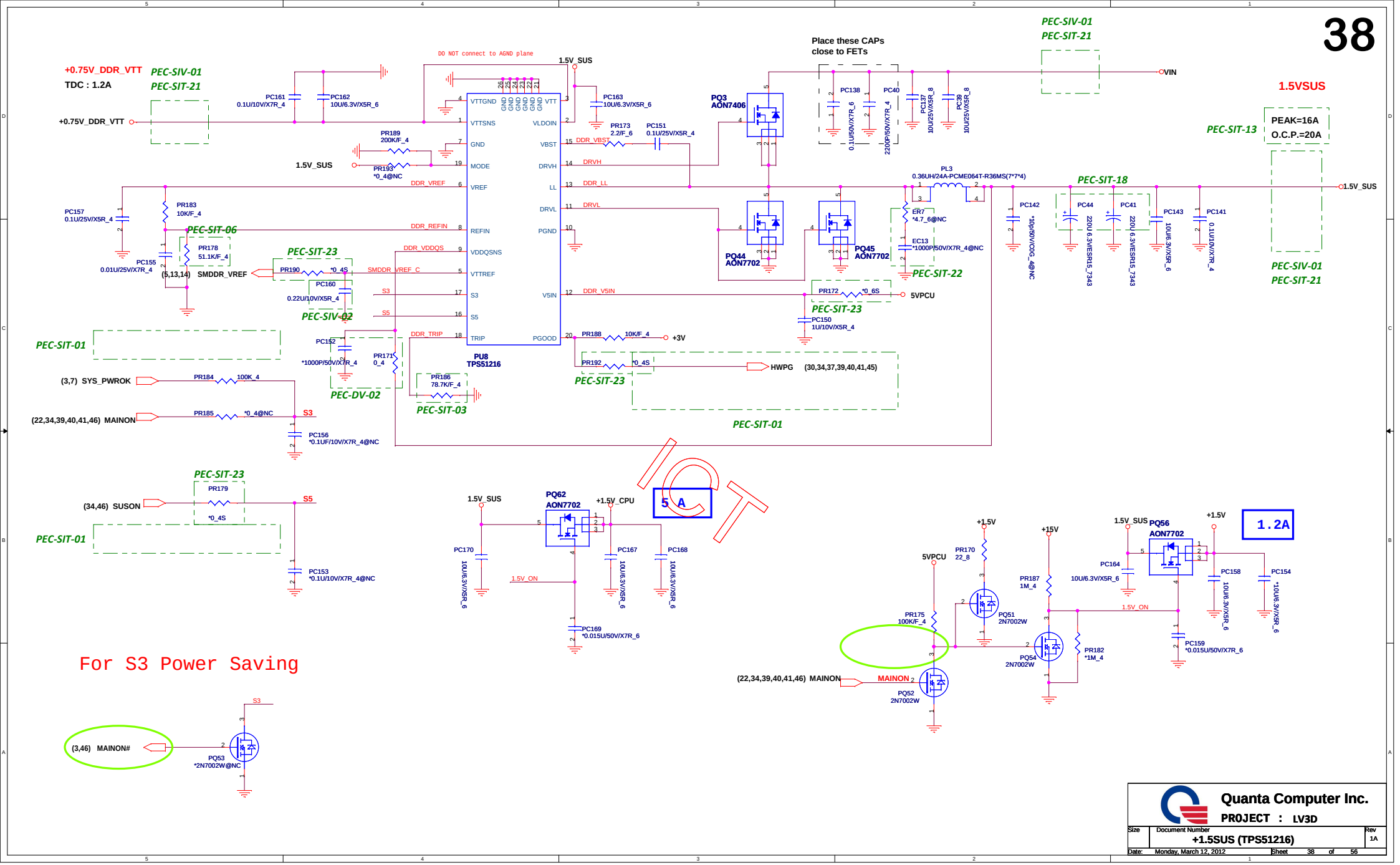
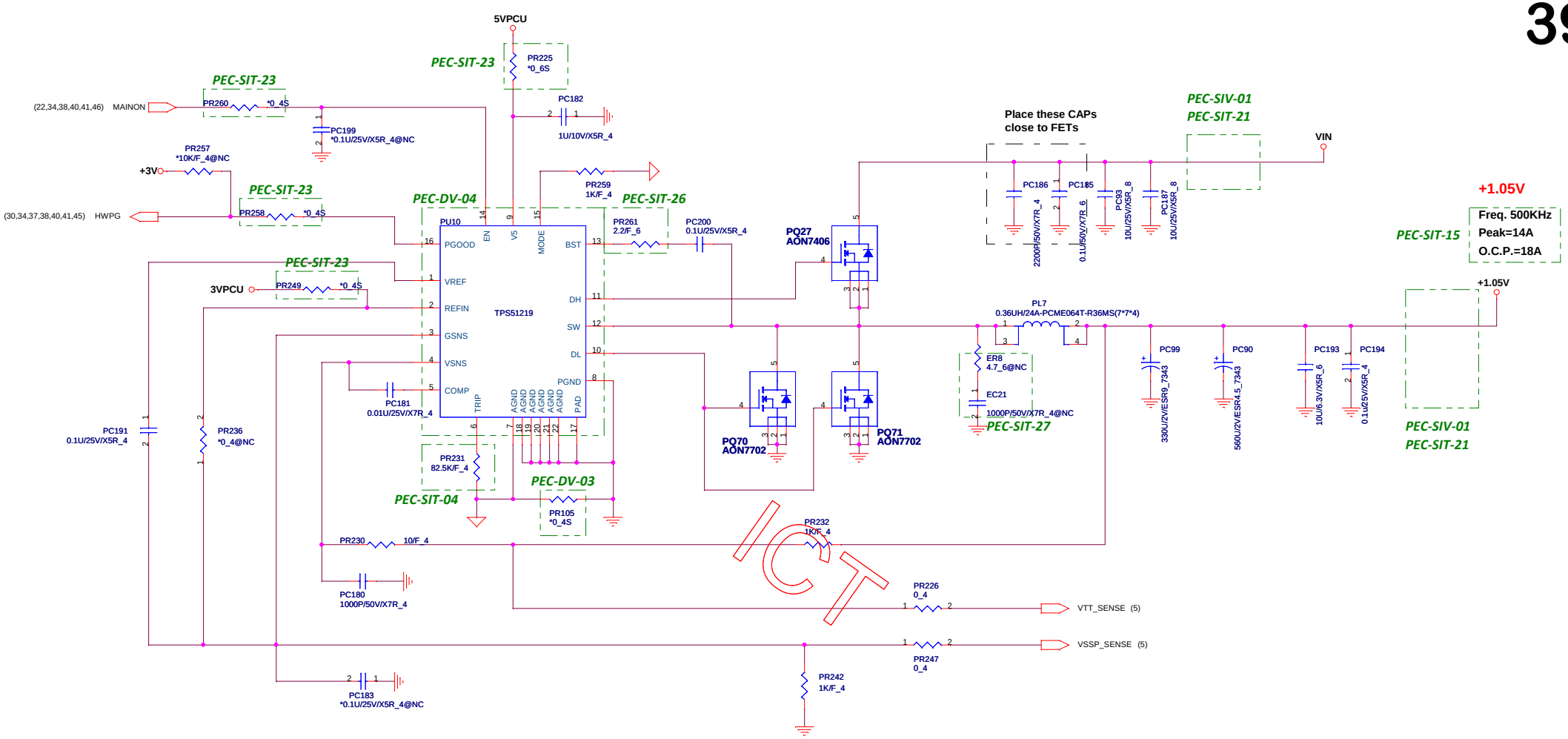


Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: +1.5SUS (TPS51216)	Rev: 1A
Date: Monday, March 12, 2012	Sheet 38 of 56	



Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: +1.05V (TPS51219)	Rev: 1A
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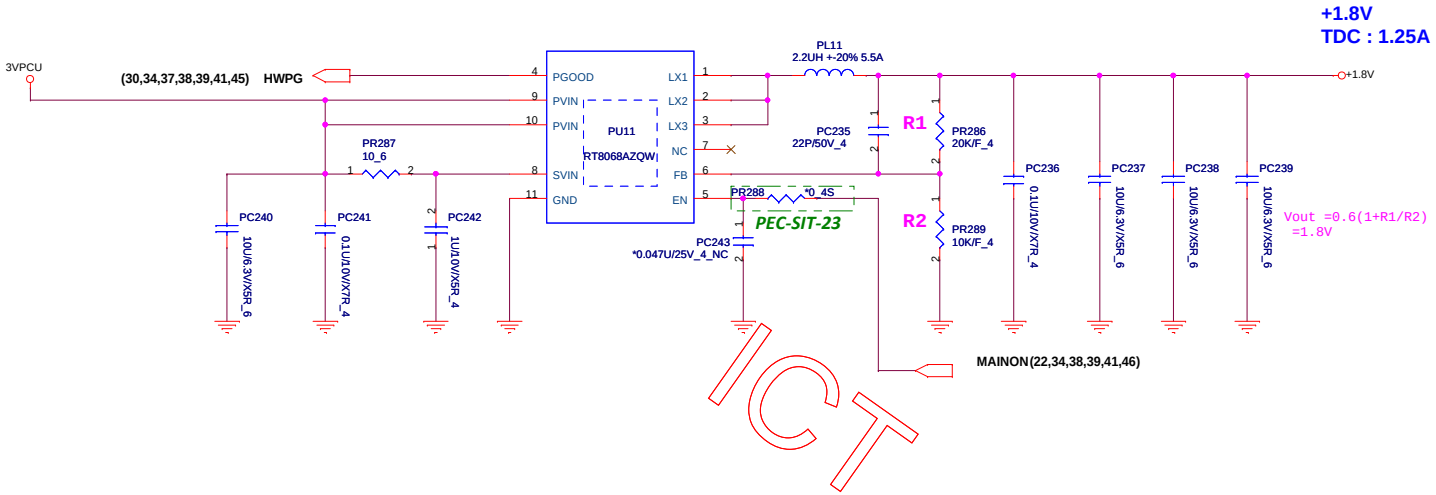
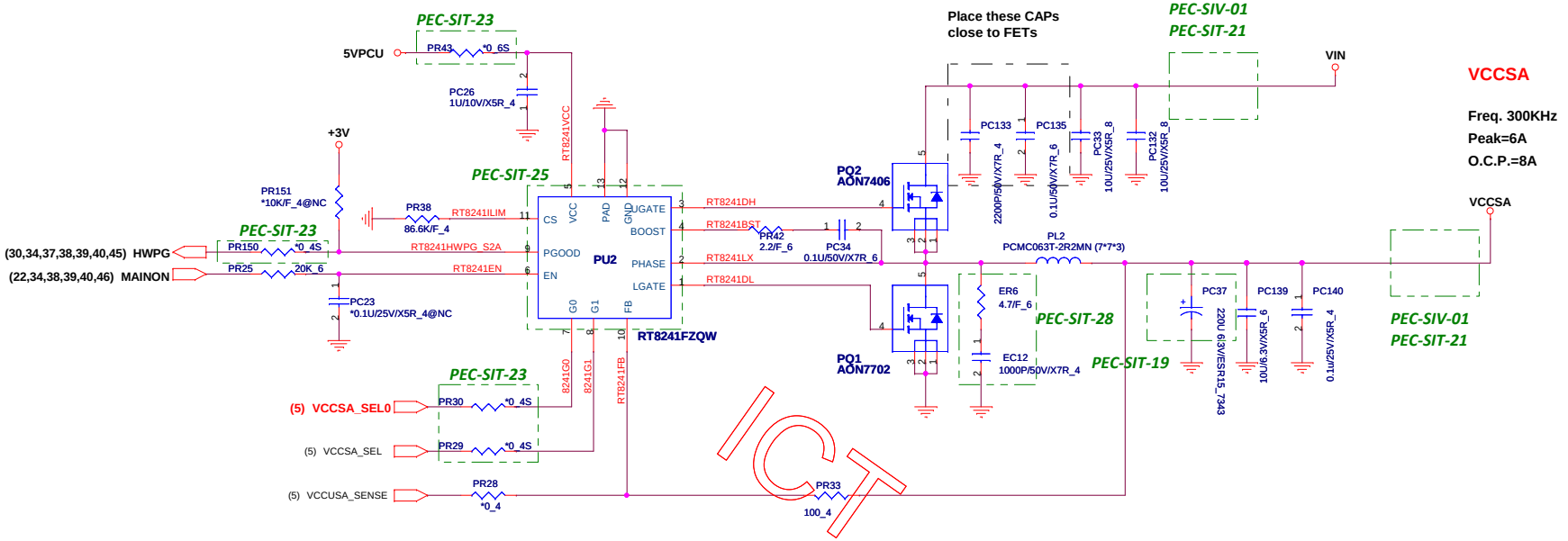
MAINON (22,34,38,39,41,46)
3VPCU (8,21,25,28,32,34,36,37,39,46,48,49)
+1.8V (5,8,11,46)



Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: +1.8V (RT8068AZQW)	Rev: 1A
Date: Monday, March 12, 2012	Sheet 40 of 56	

MAINON (22,34,38,39,40,46)
VCCSA_SEL (5)
5VPCU (8,21,36,37,38,39,40,42,43,44,46,48)
VIN (21,35,36,37,38,39,44,45,46)
VCCSA (5,46)
+3V (3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,43,44,45,46,49)
HWPG (30,34,37,38,39,40,45)
VCCUSA_SENSE (5)



Processor	VCCSA_SEL0 G0	VCCSA_SEL G1	VCCSA Ultra segments
Sandy Bridge	0	0	0.9V
	0	1	0.85V
Ivy Bridge (ES sample)	1	0	0.725V
	1	1	0.675V

PEC-SIT-25

Processor	VCCSA_SEL0 G0	VCCSA_SEL G1	VCCSA Ultra segments
Sandy Bridge	0	0	0.9V
	0	1	0.85V
Ivy Bridge (QS sample)	1	0	0.775V
	1	1	0.75V

VCCSA

Freq. 300KHz
Peak=6A
O.C.P.=8A

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	+VCCSA (RT8241D)	1A

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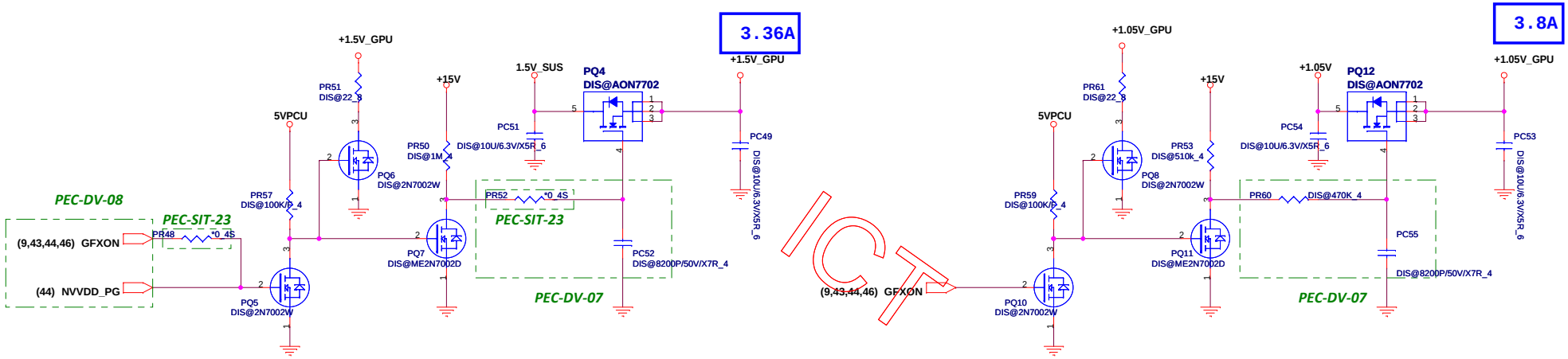

Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: 1.5VGPU/1.05V_GPU	Rev: 1A
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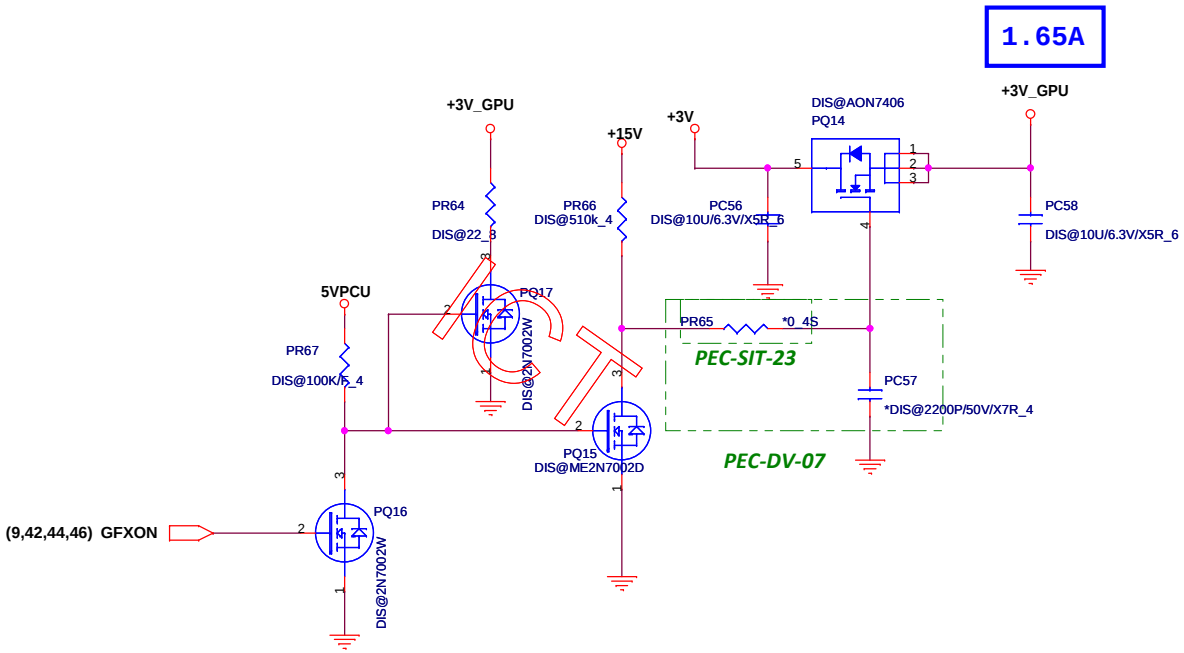


Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: +3V_GPU	Rev: 1A
Date: Monday, March 12, 2012	Sheet 43 of 56	

(3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,45,46,49) +3V
(8,21,36,37,38,39,40,41,42,43,46,48) 5VPCU
(21,35,36,37,38,39,41,45,46) VIN

Place these CAPs close to FETs

PEC-SIV-01
PEC-SIT-21

PEC-SIV-05
PEC-SIT-23
PEC-SIT-10
PEC-SIT-09
PEC-SIT-14

GFX_CORE
Fs=300K
GPS MAX : 25.36
No-GPS MAX : 21.78
OCP : 38A

Parallel

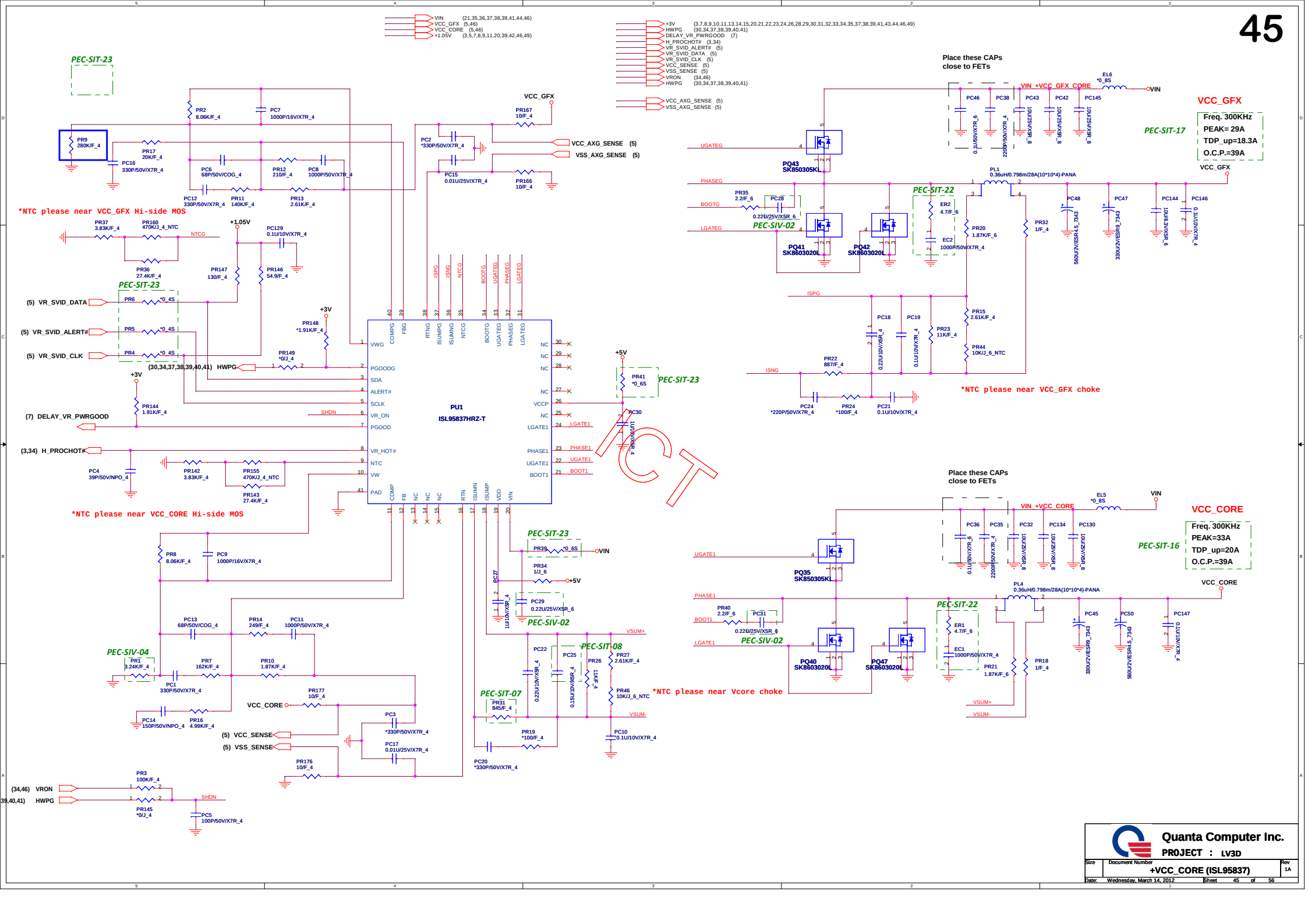
If IMON PULL HIGH, THEN DISABLE LOAD LINE

Place PR331,PC313 close to PIN14 & PIN15

Close to Phase 1 Inductor

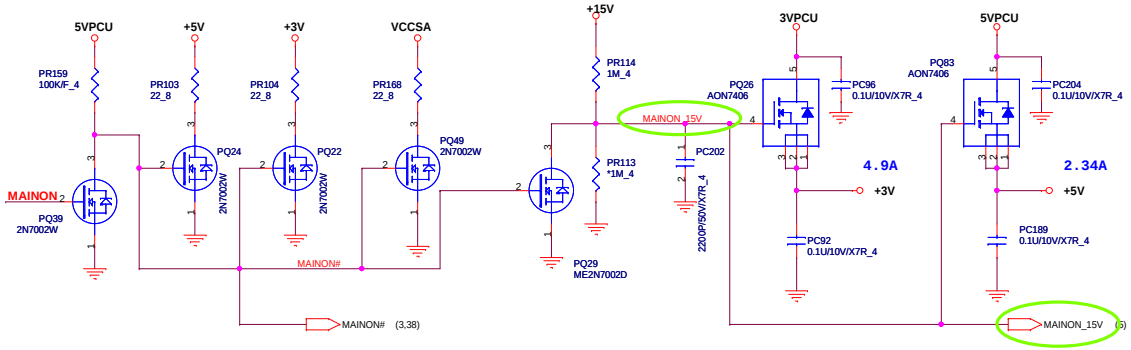
Panasonic ERT-J1VR103J

Quanta Computer Inc.	
PROJECT : LV3D	
Size	Document Number: VGA(ISL62882C) 1 PHASE
Rev	1A
Date: Monday, March 12, 2012	Sheet 44 of 56

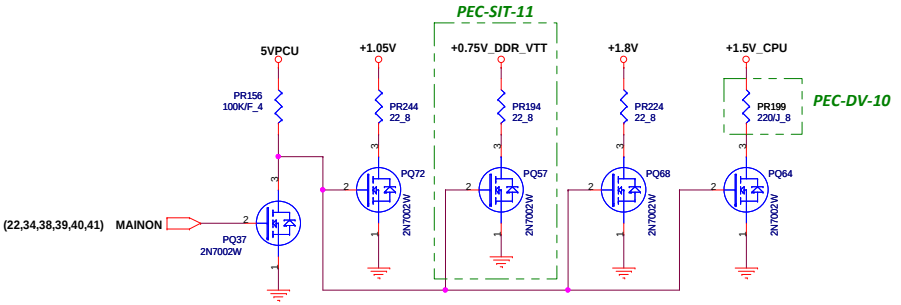


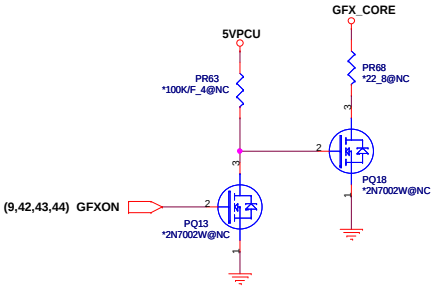
Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: +VCC_CORE (ISL95837)	Rev: 1A
Date: Wednesday, March 14, 2012	Sheet 45 of 56	

+3.3V, +5V

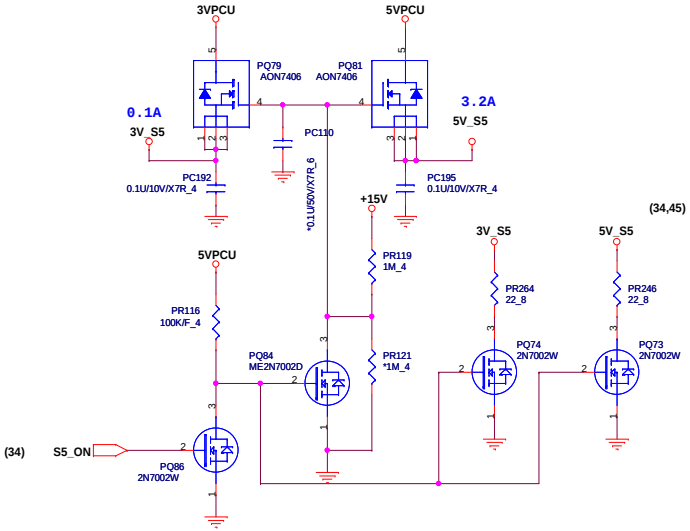


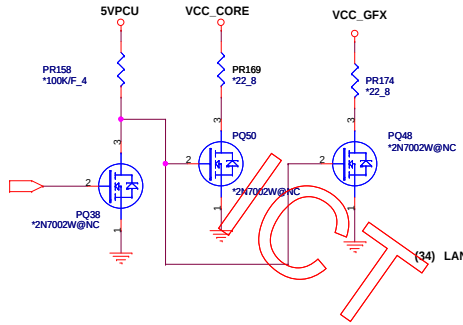
PEC-SIT-11



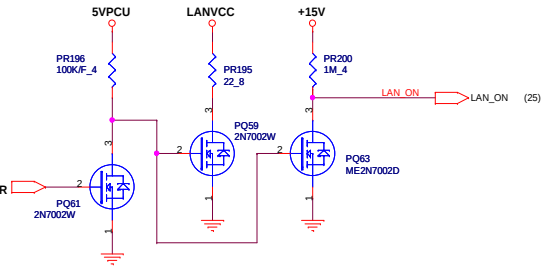


3V_S5, 5V_S5

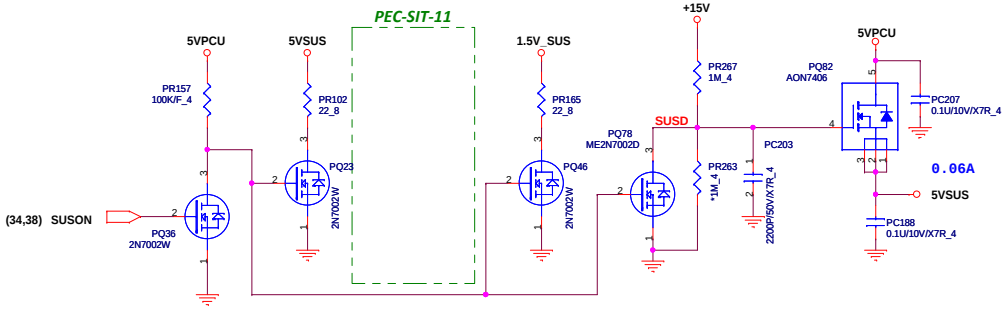


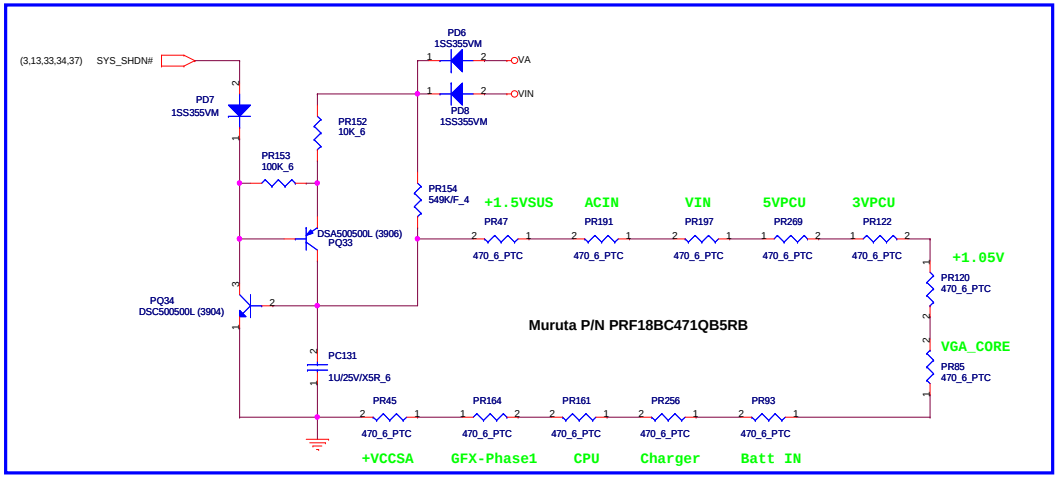


LANVCC

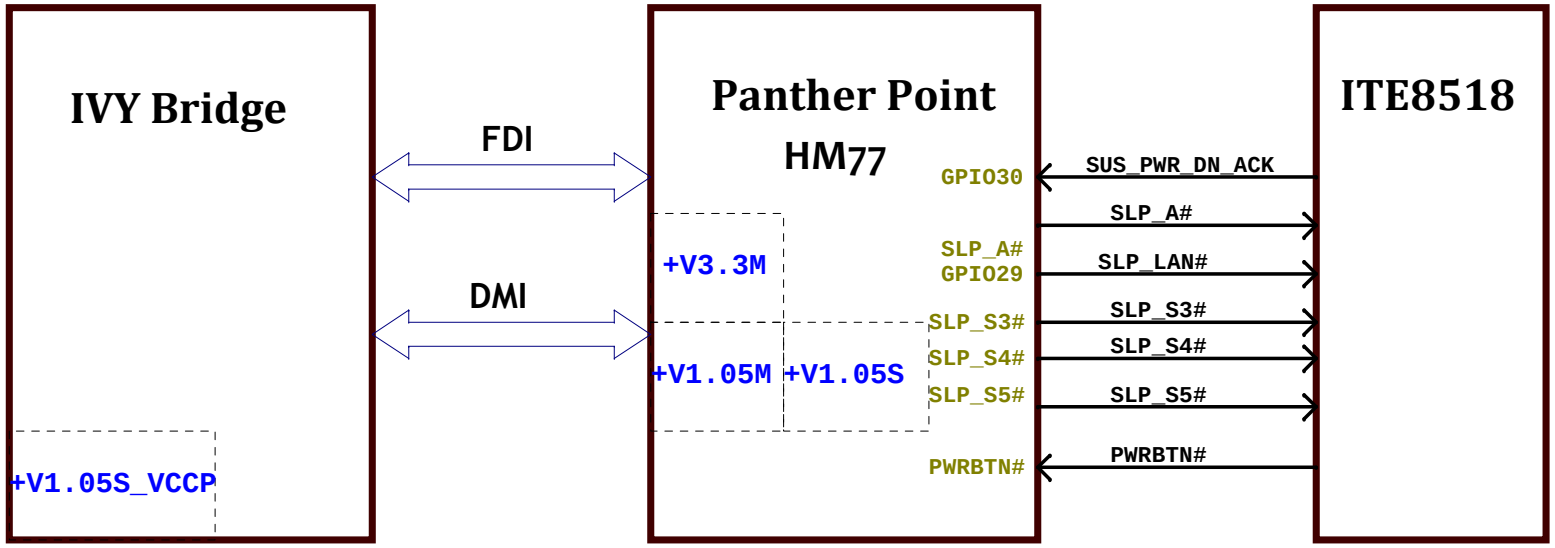


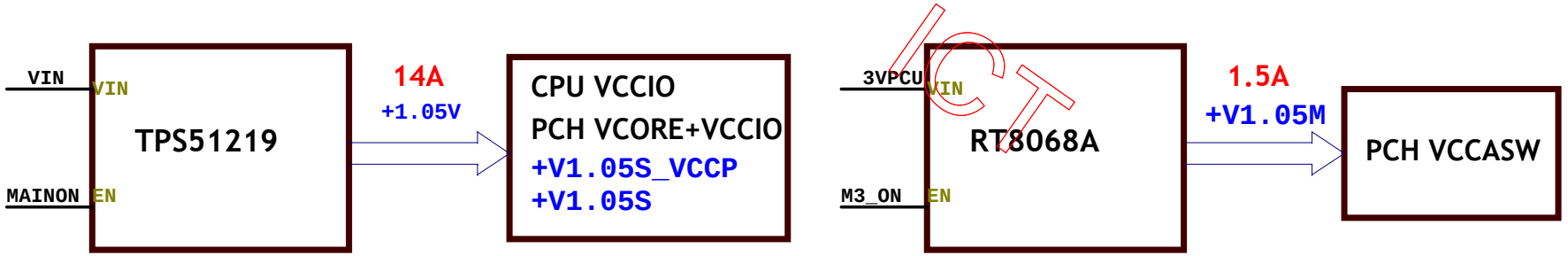
5VSUS

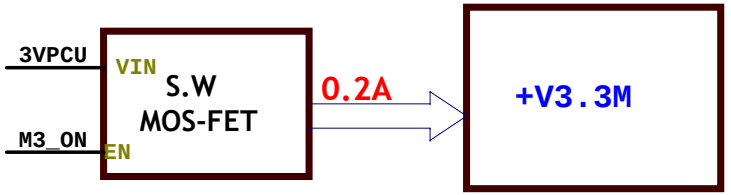




Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number	Rev
	POWER_Discharge	1A
Date: Monday, March 12, 2012	Sheet 46 of 56	

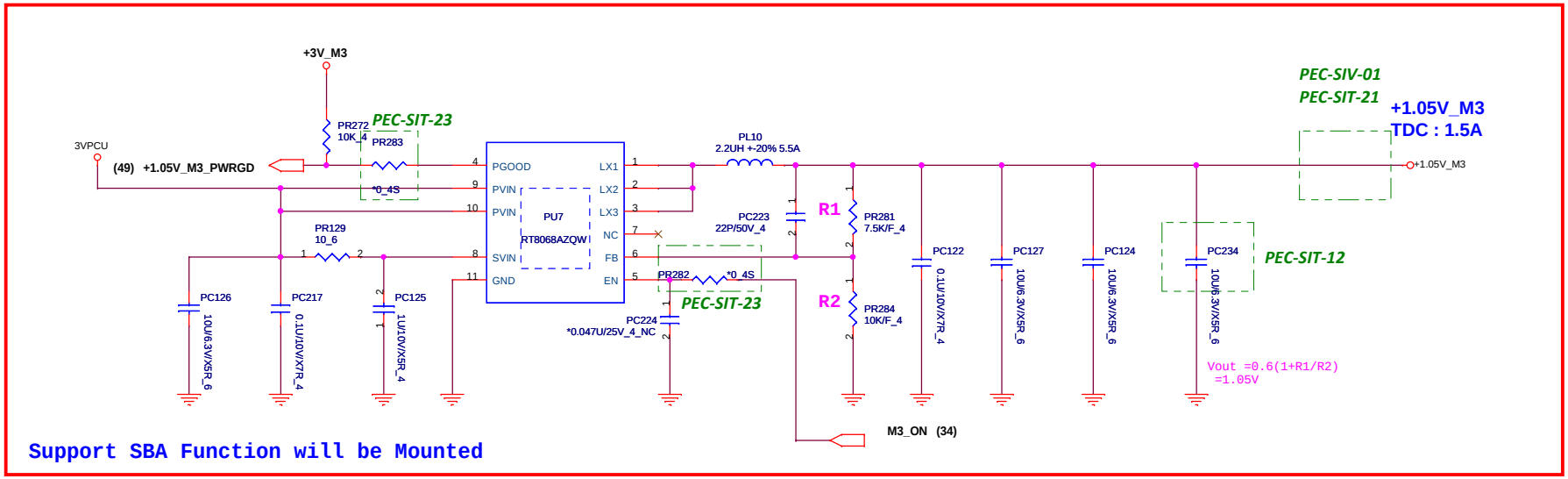


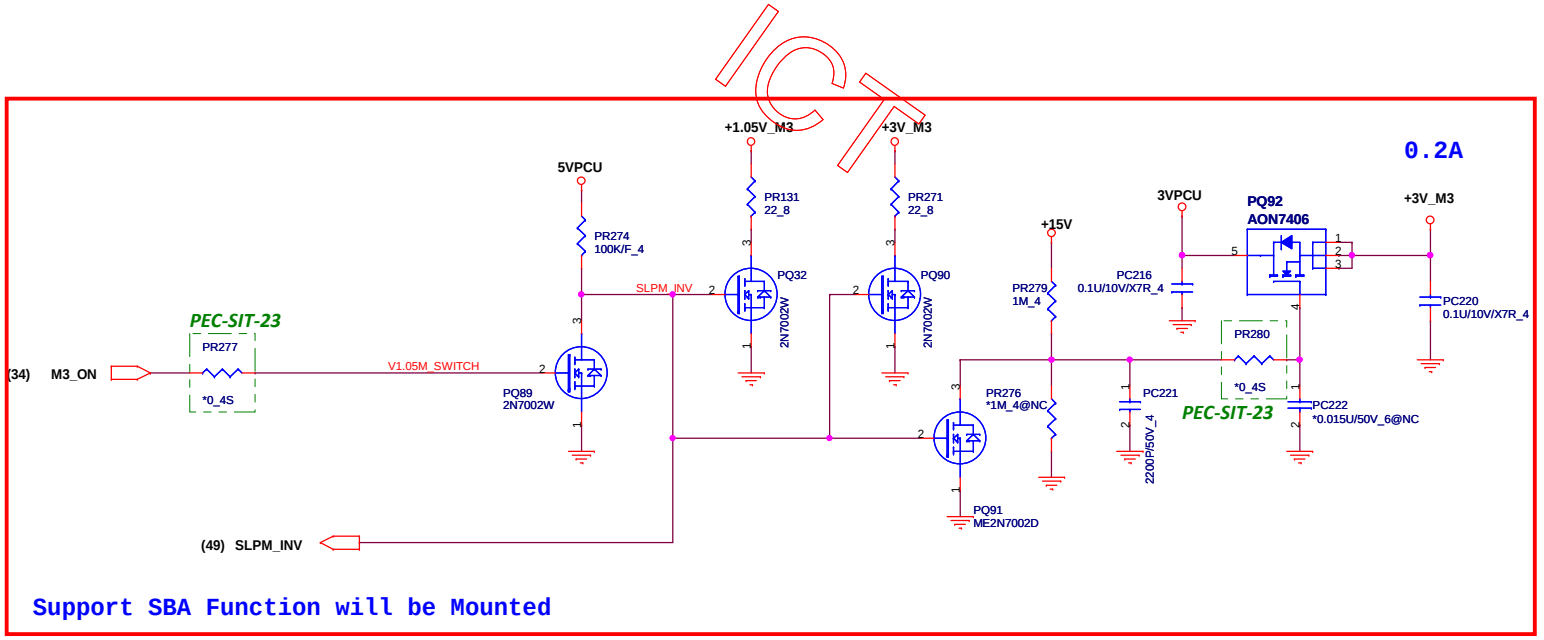




Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number: SBA Block	Rev: 1A
Date: Monday, March 12, 2012	Sheet 47 of 56	

+3V_M3 (8,11,25,49)
+1.05V_M3 (11,49)





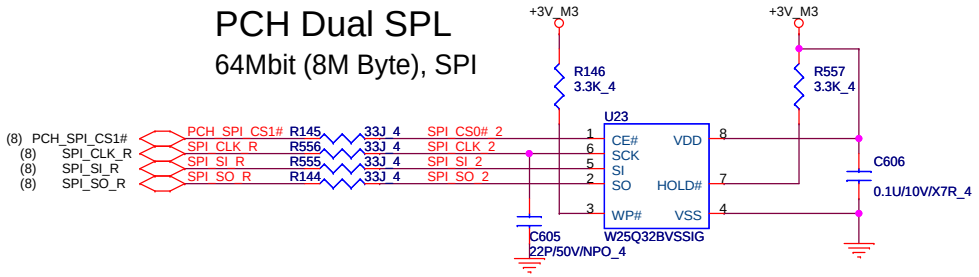
Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	SBA M3 Power(RT8068A)	1A
Date: Monday, March 12, 2012	Sheet 48 of 56	

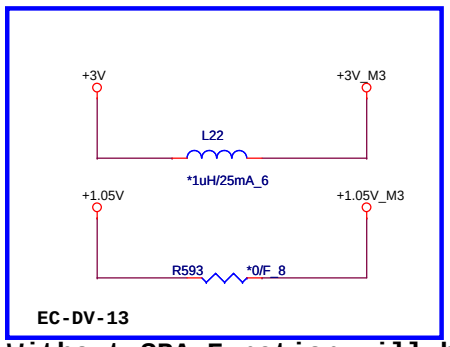
+1.05V (3,5,7,8,9,11,20,39,42,45,46)
3VPCU (8,21,25,28,32,34,36,37,39,40,46,48)
+3V_M3 (8,11,25,48)
+1.05V_M3 (11,48)

PCH Dual SPL

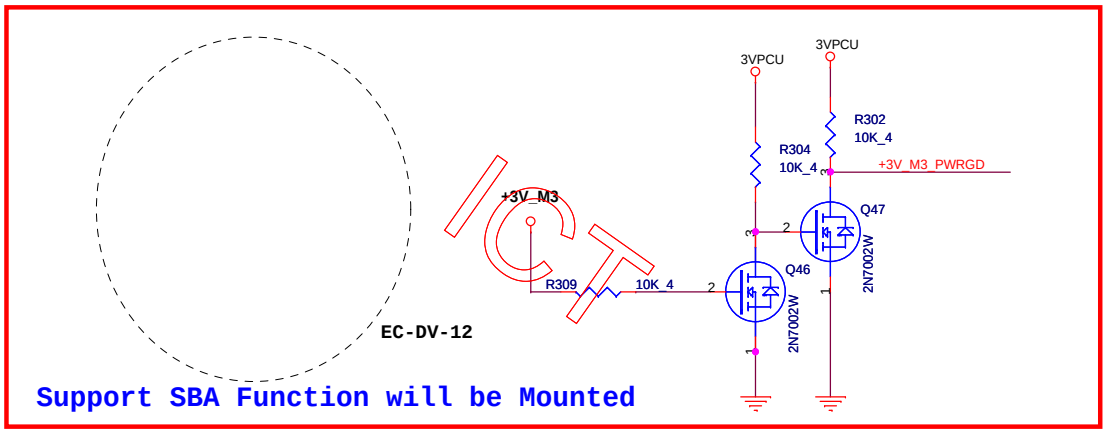
64Mbit (8M Byte), SPI



SBA POWERGD/SBA Power select

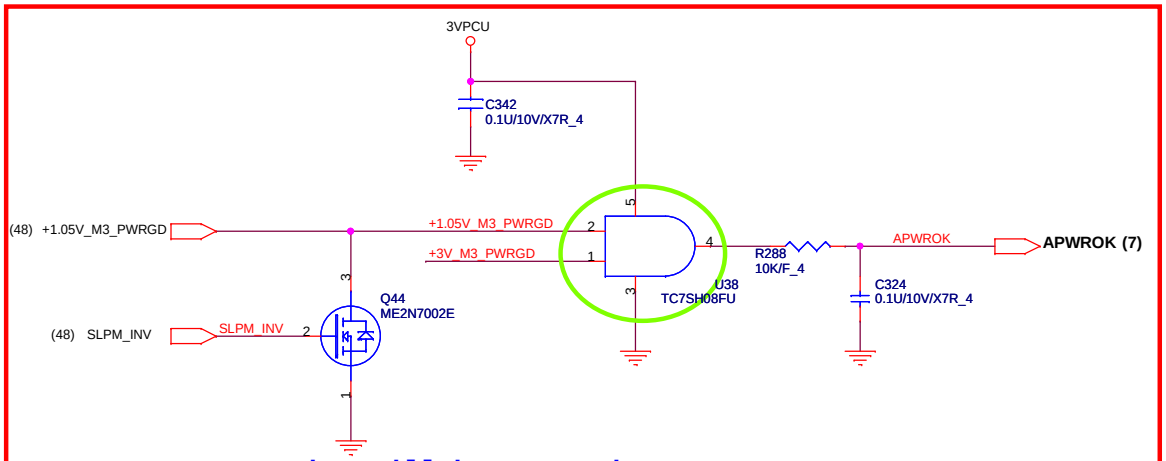


Without SBA Function will be Mounted



Support SBA Function will be Mounted

SBA LOGIC



Support SBA Function will be Mounted

Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	Circuit for Intel SBA	1A
Date: Monday, March 12, 2012	Sheet 49 of 56	

LV3D Schematic EC Tracking Record DV (for DV)Dec. 14, 2011

EC #	Page	Description	Part Affected
EC-DV-01	5	Follow Intel schematic review suggestion	C487,C92,C93,C512,C478
EC-DV-02	3	Follow Intel schematic review suggestion to add resistor	R458
EC-DV-03	10	Reserve one board ID to identify ABBA & Lovell PCBA	R602,R605
EC-DV-04	5	Change component to "stuff" based on Intel suggestion	R433
EC-DV-05			
EC-DV-06	5	Change component to "stuff" based on Intel suggestion	R429
EC-DV-07	5	Add 0.002 ohm series resistor on +1.8V based on Intel suggestion	R166
EC-DV-08	13	Change 1.5V rail decoupling Caps from 1uF to 0.1uF based on Intel suggestion	C8561,C584,C574,C296
EC-DV-09	11	Change component to "stuff" based on Intel suggestion	C585,C586
EC-DV-10	10	External pull high for GPIO69 based on Intel suggestion	R595
EC-DV-11	32	Reserve 0 ohm for EMI	R459,R465
EC-DV-12	32	Modify CCD CONN to 12 pin	CN14
EC-DV-13	25	Modify RJ45 footprint	CN24
EC-DV-14	7,22	Reserve DP switch to support DP to DVI dongle by customer request	U2000
EC-DV-15	26	Stuff SATA Tx & Rx repeater IC for customer request	U10
EC-DV-16	23	Modify HDNI CONN footprint	CN10
EC-DV-17	29	Connect "MSATA_DTCT_EN" to EC to fix leakage issue if both have mSATA & WWAN design	R638,R8023
EC-DV-18	16	Follow up nVIDIA suggestion to modify Res value	R3014,R3015
EC-DV-19	18	Follow up nVIDIA suggestion to stuff PD Res	R3041
EC-DV-20	19	Follow up nVIDIA suggestion to modify Res value	R3086,R3091
EC-DV-21	22,23	Reserve diode to prevent leakage current from DP & HDMI device	R615,D26,R616,D29
EC-DV-22	29,34	Reserve WWAN_DTCT# pin from mini-PCIE slot to EC	
EC-DV-23	21	DXF team suggest keep 4.7uF to avoid using poor quaity Hall Sensor ic	C435
EC-DV-24	7	DXF team suggest stuff the Res based on Intel Spec	R126
EC-DV-25	8,24	Reserve CAP for RF request	C656,C657,C659
EC-DV-26	31	Reserve 0 ohm Res for SMBus click pad inter touch function	R276,R279
EC-DV-27	3	If eDP is used, then the HPD should be pulled-high	R17
EC-DV-28	9	Change PN the same with LI2	
EC-DV-29	28,34	Reserve AOAC control GPIO from EC by customer request	
EC-DV-30	25	Reserve 1M Res to GND for Hi-pot test	

LV3D Schematic POWER EC Tracking Record DV (for DV)Dec. 14, 2011

EC #	Page	Description	Part Affected
PEC-DV-01	36	Modify battery connector fottprint	PJP1
PEC-DV-02	38	Reserve RC	PC268,PR323
PEC-DV-03	39	Short signal GND & digital GND	PR95
PEC-DV-04	39	Modify +1.05V power control IC footprint	PU7
PEC-DV-05	36	Follow FAE suggestion change PC2 to 100p CH11006JB18	PC2
PEC-DV-06	37	Follow FAE suggestion to reserve PR79 connect PU3.14 to 5VAL	PR79
PEC-DV-07	42,43	Reserve RC circuit to adjust VGA power up sequence	
PEC-DV-08	42	Follow LZ8 design to change +1.5V_GPU enable signal	
PEC-DV-09	37	Follow LI2 design to un-stuff component	
PEC-DV-10	46	Follow LI2 design to change Res value	
PEC-DV-11			
PEC-DV-12			
PEC-DV-13			
PEC-DV-14			
PEC-DV-15			
PEC-DV-16			
PEC-DV-17			
PEC-DV-18			

LV3D Schematic EC Tracking Record SIV (for SDV-->SIV)Jan. 02, 2012

EC #	Page	Description	Part Affected
EC-SIV-01	10,29	Follow up LI2 design to connect WWAN_DTCT# to PCH GPIO68	R660,R220
EC-SIV-02	20	Follow up LI2 vendor suffestion to connect pin57 to GNDA	U6
EC-SIV-03	20,22,32	Modify components footprint and PN for EOD parts	C211,C4,C15,C17,C186

LV3D Schematic POWER EC Tracking Record SIV (for SDV-->SIV)Jan. 02, 2012

EC #	Page	Description	Part Affected
PEC-SIV-01	37~41 44,45	Modify power jump to short pad	PJP11,PJP12,PJP14,PJP2,PJP4,PJP5,PJP17,PJP9,PJP8,PJP1,PJP3, PJP15,PJP6,PJP7,PJP13
PEC-SIV-02	45	Modify CAP value from 20% to 10%	PC28,PC29,PC31
PEC-SIV-03	37	Stuff the CAP to stable enable signal	PC117
PEC-SIV-04	45	Modify RES value to make OTP stable	PR1

ICT

Quanta Computer Inc.
PROJECT : LV3D
Size | Document Number: EC RECORD DV | Rev: 1A
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LV3D Schematic EC Tracking Record SIT (for SIV-->SIT)March. 05, 2012

EC #	Page	Description	Part Affected
EC-SIT-01	3,7,8 11,34	Remove Deep S3 circuit	Delete R79,R492,R499,R363,R372,D4,D5,Q29,R617,R626,Q30,C624,R297 R544,Q27,Q55,Q54,Q28,R536,R404,R415,R375,R361, Un-stuff R499,R361 Add R668
EC-SIT-02	34	Add EC Reset IC circuit	Add U50,D26,C672,C673,C674,C676,R664,R674,R675,R665,R662
EC-SIT-03	33	Add CPU temperature switch circuit	Add U51,Q64,R669,R670,R671,C675
EC-SIT-04	3	Add THERMTRIP# assert to SYS_SHDN# circuit	Add Q62,Q63,R667
EC-SIT-05	8	Add RTC detect circuit	Add Q65,R672
EC-SIT-06	20	Swap EC between MBDATA_THRM and MBCLK_THRM for eDP converter & remove EEPROM	Delete U28,Q7,Q8 ; Add Q70
EC-SIT-07	29	Add AOAC circuit need to support with WWAN	Un-stuff R222
EC-SIT-08	34	Change WWAN_DTCT#_EC GPIO pin	
EC-SIT-09	17	BOM NG,correct CAP value to 27p	C102,C103
EC-SIT-10	8,17	Modify XTAL PN & footprint for single source issue	Y1,Y2
EC-SIT-11	9,18,23	Change MOS to dual-MOS	Delete Q45,Q51,Q18,Q19,Q22,Q24,Q3,Q4 Add Q66,Q67,Q68,Q69
EC-SIT-12	31	Decrease 5VSUS to 1pin to add 1pin to GND	
EC-SIT-13	31,32	Change LOGO LED limited-current RES value due to FP/B no layout spacing	R165,R250
EC-SIT-14	21	Follow LI2 design to add LCD_VCC fuse	Add F5
EC-SIT-15	34	Change SUSPEND_LED# to PWM GPIO	
EC-SIT-16	34	Reserve G SENSOR_Z GPIO	
EC-SIT-17	5	Delete CAP due to DV test is Pass and found no issue if un-stuff it	Delete C87,C99,C5,C129
EC-SIT-18	23	Add diode to fix +5V under S5 leakage current issue	Delete R1,D1,F1 ; Add D27,C687
EC-SIT-19			
EC-SIT-20	27	Change USB power switch and add ESD component to fix USB port CDE fail issue	Delete C93,U15,C73,C143,C96 Add C680,U52,C677,C678,C679,C681,U53,C682,U54,C683,C684,C685 C686,U55
EC-SIT-21	34	Modify EC USB ON GPIO to low active for new USB power switch	
EC-SIT-22	27	Stuff USB common choke to fix EMI issue	Delete R138,R139,R80,R85 Stuff CML1,CML2
EC-SIT-23	7,23	Change CAP & RES footprint from 0402 to 0201 to fix ESD issue	C626,C627,C628,C629,C630,C631,C640,C641,R4,R5,R7,R8
EC-SIT-24	23	Delete diode due to we change design	Delete D9,D10
EC-SIT-25	25,34	Reserve EC GPIO RJ45_LINKUP# to support IBM wake up solution	

LV3D Schematic EC Tracking Record SIT (for SIV-->SIT)March. 05, 2012

EC #	Page	Description	Part Affected
EC-SIT-26	03	Reserve CAP for S3 resume hang up issue	C688
EC-SIT-27	27	Change ESD solution	Delete U46,U21,U40,U14
EC-SIT-28	27	Swap net name for layout more smooth	U55
EC-SIT-29	35	ME no need for this screw hole	Delete HOLE7
EC-SIT-30	27	Change CAP size from 3528 to 7343 for shortage issue	C679,C685
EC-SIT-31	35	Modify Non-PTH hole footprint for layout request	HOLE19
EC-SIT-32	35	Add GND PAD for ESD request	GP3,GP4
EC-SIT-33	35	Add CAP to fix ESD issue	C689,C690
EC-SIT-34	28	Change MOSFET Spec to 3A to support WLAN/WWAN AOAC function	Q59
EC-SIT-35	32	Move the A cover LED limit-current RES near power side prevent from cable short risk	R257
EC-SIT-36	32	Change Thinklight LED limit-current RES footprint from 0402 to 0603	R294
EC-SIT-37	28,29	Modify footprint for SMT request	CN6,CN19
EC-SIT-38	34	Change debug switch footprint prevent from interference with ME base	SW1
EC-SIT-39	35	Change hole footprint for ESD request	HOLE16

LV3D Schematic POWER EC Tracking Record SIT (for SIV-->SIT)Mar. 05, 2012

EC #	Page	Description	Part Affected
PEC-SIT-01	38	Remove Deep S3 circuit	Delete PR180,PR181,PD10,PD11
PEC-SIT-02	37	Modify Res value to 127k for 3VPCU OCP fine tune	PR132
PEC-SIT-03	38	Modify Res value to 78.7k for 1.5V_SUS OCP fine tune	PR186
PEC-SIT-04	39	Modify Res value to 82.5k for 1.05V OCP fine tune	PR231
PEC-SIT-05	44	Stuff Res for VGA power good pull high	PR75
PEC-SIT-06	38	Modify Res value to 51.1k for 1.5V_SUS regulation fine tune	PR178
PEC-SIT-07	45	Modify Res value to 845 for Vcc_Core load line	PR31
PEC-SIT-08	45	Modify CAP value to 0.15u for Vcc_Core load line	PC25
PEC-SIT-09	44	Modify Res value to 681 for VGA OCP fine tune	PR78
PEC-SIT-10	44	Modify Res value to 9.09k for VGA OCP fine tune	PR205
PEC-SIT-11	46	Discharge gate change to mainon for 0.75V discharge stable	PQ57,PR194
PEC-SIT-12	48	Output add 10uF/6.3V CAP for 1.05V_M3 output stable	PC234
PEC-SIT-13	38	Updated 1.5V_SUS power budget to 16A,OCP change to 20A	
PEC-SIT-14	44	Updated VGA power budget to fix actual loading	
PEC-SIT-15	39	Updated 1.05V power budget to 14A,OCP change to 18A	
PEC-SIT-16	45	Updated VCC_CORE power budget to fix actual loading,add TDP-up 20A	
PEC-SIT-17	45	Updated VCC_GFX power budget to fix actual loading,add TDP-up 18.3A	
PEC-SIT-18	38	Change CAP footprint from 3528 to 7343 due to vendor can't support	PC41,PC44
PEC-SIT-19	41	Change CAP PN due to vendor can't support	PC37
PEC-SIT-20	36	Change CAP PN for component stress request	PC108,PC109
PEC-SIT-21		Delete power jump	PJP1 PJP2 PJP3 PJP4 PJP5 PJP8 PJP11 PJP12 PJP13 PJP14 PJP6 PJP7 PJP9 PJP10 PJP15 PJP17
PEC-SIT-22	38,45	Stuff components to fix EMI issue	Stuff ER1,ER2,ER7,EC1,EC2,EC13
PEC-SIT-23	37,38,39 41,42,43 44,45,48	Change 0 ohm RES footprint to short pad	PR137,PR139,PR141,PR285,PR123,PR270,PR275,PR179,PR190,PR192 PR172,PR249,PR258,PR260,PR225,PR150,PR29,PR30,PR43,PR52,PR48 PR65,PR214,PR217,PR80,PR84,PR92,PR77,PR79,PR83,PR87,PR88,PR89 PR91,PR4,PR5,PR6,PR39,PR41,PR277,PR280,PR282,PR283,PR288
PEC-SIT-24	40	Change +1.8V from LDO to PWM to enhance battery life	Delete PR240,PQ25,PQ67,PR111,PR229,PR97,PC89,PQ21,PR110,PC94 EL3,PC100,PC95,PR101,PC85,PR108,PU4,PR94,PR95,PC79,PC84,PC80 PR228 Add PC235,PC236,PC237,PC238,PC239,PC240,PC241,PC242,PC243,PU11 PR286,PR287,PR288,PR289,PL11
PEC-SIT-25	41	Change VCCSA VR chip for QS sample CPU	PU2

LV3D Schematic POWER EC Tracking Record SIT (for SIV-->SIT)Mar. 05, 2012

EC #	Page	Description	Part Affected
PEC-SIT-26	39	PR261 change to 2.2ohm for power stable	PR261
PEC-SIT-27	39	Add RC snubble for power stable	Stuff ER8,EC21
PEC-SIT-28	41	Add RC snubble for power stable	Stuff ER6,EC21
PEC-SIT-29	37	Un-stuff CAP for vendor not support 3525 size	PC111
PEC-SIT-30			
PEC-SIT-31			