R63 INTEL SYSTEM DIAGRAM

01

+3V/+5V S5 PG.36

+1.05V PG.37

CPU Core PG.40~41

DDR3L PG.38

Charge PG.35

Dis-Charge PG.39

+VGACORE PG.42

+1.5 VGA PG.43

+1.0V/+1.8/ +3 VGA PG.44

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A

SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

INTEL Haswell
Processor : Daul / Quad Core
Power : 37 / 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)
PG.2~5

PCI-E x8 — **AMD Mars / SUN XT** 29mm X 29mm TDP 35W / 25W PG.14~20

eDP (5.4Gb/s)

DDI (5.4Gb/s)

DDR3 900MHz — **VRAM** 128Mx16x8,128bit PG.21~22

FDI DMI

HDD PG.33 — SATA0

ODD PG.33 — SATA1

INTEL PCH
Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)
PG.6~11

eDP — RTD 2136 S/R DP to LVDS Converter PAGE 23 — LVDS Interface — LVDS PG.25

DP Port B — HDMI PG.26

CRT — CRT PG.25

PCI-E x 1 — LANE2 — LAN RTL8166EH 10/100 PG.30

PCI-E x 1 — LANE1 — WLAN BT COMBO PG.34 — USB 2.0 PORT10

USB 3.0 — USB3.0 Ports X2 PG.29 — Webcam PG.25

USB 2.0 PORT1,2 — PORT4 — PORT0,1 — USB2.0 Ports PG.29

PCI-E x 1 LANE3 — Accelerometer PG.34 — SMBUS — Card Reader RTS5237 PG.27

LPC — KBC EnE KB3940QF A1 PG.31 — KB PG.32 — TP PG.32 — ROM PG.31 — FAN PG.32

AUDIO CODEC ALC 3227 PG.28 — Speaker PG.28 — HP/MIC PG.29 — Analog MIC PG.29

Stackup

TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02

U24A

DMI_TXN0 D21 DMI_RX#[0]
DMI_TXN1 C21 DMI_RX#[1]
DMI_TXN2 B21 DMI_RX#[2]
DMI_TXN3 A21 DMI_RX#[3]
DMI_TXP0 D20 DMI_RX[0]
DMI_TXP1 C20 DMI_RX[1]
DMI_TXP2 B20 DMI_RX[2]
DMI_TXP3 A20 DMI_RX[3]
DMI_RXN0 D18 DMI_TX#[0]
DMI_RXN1 C17 DMI_TX#[1]
DMI_RXN2 B17 DMI_TX#[2]
DMI_RXN3 A17 DMI_TX#[3]
DMI_RXP0 D17 DMI_TX[0]
DMI_RXP1 C18 DMI_TX[1]
DMI_RXP2 B18 DMI_TX[2]
DMI_RXP3 A18 DMI_TX[3]

DMI

FDI_TXN0 P33 FDI_TX#[0]
FDI_TXN1 N32 FDI_TX#[1]
FDI_TXP0 R33 FDI_TX[0]
FDI_TXP1 P32 FDI_TX[1]
FDI_INT J29 FDI_INT
FDI_CSYNC R71 *0_4/S FDI_CSYNC_R H29 FDI_CSYNC

FDI

DPB_LANE0_N T28 DDIB_TX#[0]
DPB_LANE1_N T30 DDIB_TX#[1]
DPB_LANE2_N U29 DDIB_TX#[2]
DPB_LANE3_N U31 DDIB_TX#[3]
DPB_LANE0_P U28 DDIB_TX[0]
DPB_LANE1_P U30 DDIB_TX[1]
DPB_LANE2_P V29 DDIB_TX[2]
DPB_LANE3_P V31 DDIB_TX[3]

T34 DDIC_TX#[0]
U35 DDIC_TX#[1]
U32 DDIC_TX#[2]
U33 DDIC_TX#[3]
U34 DDIC_TX[0]
V35 DDIC_TX[1]
T32 DDIC_TX[2]
V33 DDIC_TX[3]

P29 DDID_TX#[0]
N28 DDID_TX#[1]
P31 DDID_TX#[2]
N30 DDID_TX#[3]
R29 DDID_TX[0]
P28 DDID_TX[1]
R31 DDID_TX[2]
P30 DDID_TX[3]

Intel(R) DDI

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

eDP_RCOMP E24 eDP_RCOMP
EDP_DISP_UTIL R59 *0_4 INT_eDP_HPD_Q P27 EDP_DISP_UTIL
eDP_HPD
EDP_AUXP N27 eDP_AUX
EDP_AUXN M27 eDP_AUX#
EDP_TXP0 R35 eDP_TX[0]
EDP_TXP1 P34 eDP_TX[1]
EDP_TXN0 P35 eDP_TX#[0]
EDP_TXN1 N34 eDP_TX#[1]

eDP

HSW_RPGA_EDS_PGA

PCI EXPRESS* - GRAPHICS

PEG_COMP
PEG_RCOMPO E23

PEG_RX#[0..7] 14
PEG_RX#0 M29
PEG_RX#1 K28
PEG_RX#2 M31
PEG_RX#3 L30
PEG_RX#4 M33
PEG_RX#5 L32
PEG_RX#6 M35
PEG_RX#7 L34
PEG_RX#8 E29
PEG_RX#9 D28
PEG_RX#10 E31
PEG_RX#11 D30
PEG_RX#12 E35
PEG_RX#13 D34
PEG_RX#14 E33
PEG_RX#15 E32

PEG_RX[0..7] 14
PEG_RX0 L29
PEG_RX1 L28
PEG_RX2 L31
PEG_RX3 K30
PEG_RX4 L33
PEG_RX5 K32
PEG_RX6 L35
PEG_RX7 K34

PEG_TX#0 H35 C_PEG_TX#0
PEG_TX#1 H34 C_PEG_TX#1
PEG_TX#2 J33 C_PEG_TX#2
PEG_TX#3 H32 C_PEG_TX#3
PEG_TX#4 J31 C_PEG_TX#4
PEG_TX#5 G30 C_PEG_TX#5
PEG_TX#6 C33 C_PEG_TX#6
PEG_TX#7 B32 C_PEG_TX#7
PEG_TX#8 B31
PEG_TX#9 A30
PEG_TX#10 B29
PEG_TX#11 A28
PEG_TX#12 B27
PEG_TX#13 A26
PEG_TX#14 B25
PEG_TX#15 A24

PEG_TX[0] J35 C_PEG_TX0
PEG_TX[1] G34 C_PEG_TX1
PEG_TX[2] H33 C_PEG_TX2
PEG_TX[3] G32 C_PEG_TX3
PEG_TX[4] H31 C_PEG_TX4
PEG_TX[5] H30 C_PEG_TX5
PEG_TX[6] B33 C_PEG_TX6
PEG_TX[7] A32 C_PEG_TX7
PEG_TX[8] C31
PEG_TX[9] B30
PEG_TX[10] C29
PEG_TX[11] B28
PEG_TX[12] C27
PEG_TX[13] B26
PEG_TX[14] C25
PEG_TX[15] B24

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

TP50 SKTOCC# AP32
TP46 TP_CATERR# AN32
9,31 EC_PECI R537 43_4 H_PECI AR27
C770 *47P/50V_4
4/30 CRB 1.0 Add
+VCCST AK31
HPECI Ra,Ca need placement close to EC.
Ra
Ca

PROCHOT# (50ohm)
Trace Length <11 inches
31,40 H_PROCHOT# R263 56.2/F_4 H_PROCHOT#_R AM30
C38 47P/50V_4
Cb need placment near VR
Cb

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
9,31 PM_THRMTRIP#R PM_THRMTRIP#_R AM35
Rb need placment near PCH
4/30 CRB 1.0 Add
+1.05V R354 *100/F_4 Rb

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
6 PM_SYNC R533 *0_4/S PM_SYNC_R AT28
C729 *0.1U/10V_4

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
9 H_PWRGOOD R502 *0_4/S H_PWRGOOD_R AL34
R503 10K_4

PM_DRAM_PWRGD_R AC10

CPU RESET#
8,14,27,30,31,34 PLTRST# R531 *1.5K/F_4 AT26
9,31 CPU_PLTRST#R
R532 *750/F_4
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
7/26: DB phase modify

U24B

SKTOCC# AP32
CATERR# AN32
PECI AR27
FC_AK31
PROCHOT# AM30
THERMTRIP# AM35
PM_SYNC AT28
UNCOREPWRGOOD AL34
SM_DRAMPWROK AC10
RESET# AT26

MISC
THERMAL
PWR MANAGEMENT

HSW_RPGA_EDS_PGA

BCLK E26 CLK_CPU_BCLKP
BCLK# D26 CLK_CPU_BCLKN
SSC_DPLL_REF_CLK E27 CLK_DPLL_SSCLKP
SSC_DPLL_REF_CLK# F27 CLK_DPLL_SSCLKN
DPLL_REF_CLK H28 CLK_DPLL_NSCCLKP
DPLL_REF_CLK# G28 CLK_DPLL_NSCCLKN

CLOCKS

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

SM_DRAMRST# AN3 CPU_DRAMRST#

DDR3 MISC

SM_RCOMP[0] AP3 SM_RCOMP_0 R250 100/F_4
SM_RCOMP[1] AR3 SM_RCOMP_1 R526 75/F_4
SM_RCOMP[2] AP2 SM_RCOMP_2 R525 100/F_4
SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,

JTAG & BPM

PRDY# AR29 XDP_PRDY#
PREQ# AT29 XDP_PREQ#
TCK AM34 XDP_TCLK
TMS AN33 XDP_TMS
TRST# AM33 XDP_TRST#
TDI AM31 XDP_TDI_R
TDO AL33 XDP_TDO
DBR# AP33 XDP_DBRST#
R524 *1K_4 +3V
XDP_DBRST# 6
BPM#[0] AR30 XDP_BPM0
BPM#[1] AN31 XDP_BPM1
BPM#[2] AN29 XDP_BPM2
BPM#[3] AP31 XDP_BPM3
BPM#[4] AP30 XDP_BPM4
BPM#[5] AN28 XDP_BPM5
BPM#[6] AP29 XDP_BPM6
BPM#[7] AP28 XDP_BPM7

CPU XDP
TP100 TP57 TP42 TP41 TP94 TP36 TP39 TP101 TP53 TP59 TP99 TP95 TP56 TP97 TP58

SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3VS5
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
10/22: SI modify
R75 100K_4 R66 100K_4 C44 0.1U/10V_4
+1.35V_CPU R80 1.8K/F_4
DG 498556 -> 1.8K
38 51216PG R65 *0_4/S
U2 74AHC1G09GW
4PM_DRAM_PWRGD_C
R78 0_4 PM_DRAM_PWRGD_R
10/12: SI modify
C929 0.047U/10V_4
D15 *MEK500V-40
10/15: SI Del
R79 3.3K_4 C930 *0.047U/10V_4
DG 498556 -> 3.3K
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches

DDR3 DRAM RESET

DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches
+1.35VSUS R471 *1K_4 R785 *0_4/S
12,13 DDR3_DRAMRST# R472 *0_4/S CPU_DRAMRST#
10/18: SI modify
CPU_DRAMRST#_R Q29 *ME2N7002E
8 DRAMRST_CNTRL_PCH *0_4 R468 R464 *4.99K/F_4
31 DRAMRST_CNTRL_EC *0_4 R467 C628 *0.047U/10V_4
8,12,13 DRAMRST_CNTRL_DDR
FOR DS3
0529 remove R825 pull hi due to EC is output pin

+VCCIO_OUT 4,40
+VCCIOA_OUT 4
+1.05V 4,9,10,11,31,34,37
+1.35V_CPU 3,4,12,13,38
+1.35VSUS 3,4,12,13,38
+3VS5 6,7,9,10,34,36,38,39,42,44
+3V 6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44

4/30 CRB V1.0 -> 10K

+VCCIO_OUT
R218 10K_4
INT_eDP_HPD_Q
Q12 ME2N7002E
EDP_HPD 24,25
R219 100K_4

PEG x8 disable (UMA only remove)

14 PEG_TX[0..7]

C_PEG_TX0	C688	0.22U/10V_4	PEG_TX0
C_PEG_TX1	C705	0.22U/10V_4	PEG_TX1
C_PEG_TX2	C698	0.22U/10V_4	PEG_TX2
C_PEG_TX3	C708	0.22U/10V_4	PEG_TX3
C_PEG_TX4	C699	0.22U/10V_4	PEG_TX4
C_PEG_TX5	C690	0.22U/10V_4	PEG_TX5
C_PEG_TX6	C715	0.22U/10V_4	PEG_TX6
C_PEG_TX7	C730	0.22U/10V_4	PEG_TX7

0.22uF AC coupling Caps for PCIE GEN1/2/3

14 PEG_TX#[0..7]

C_PEG_TX#0	C697	0.22U/10V_4	PEG_TX#0
C_PEG_TX#1	C707	0.22U/10V_4	PEG_TX#1
C_PEG_TX#2	C703	0.22U/10V_4	PEG_TX#2
C_PEG_TX#3	C714	0.22U/10V_4	PEG_TX#3
C_PEG_TX#4	C704	0.22U/10V_4	PEG_TX#4
C_PEG_TX#5	C700	0.22U/10V_4	PEG_TX#5
C_PEG_TX#6	C716	0.22U/10V_4	PEG_TX#6
C_PEG_TX#7	C733	0.22U/10V_4	PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+VCCIOA_OUT R138 24.9/F_4 eDP_RCOMP
eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

+VCCIOA_OUT R132 24.9/F_4 PEG_COMP
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU)

H_PROCHOT# R257 62_4 +VCCIO_OUT
CLK_DPLL_SSCLKP R128 *10K_4
CLK_DPLL_SSCLKN R129 *10K_4
XDP_TDO R234 51_4
XDP_TMS R239 *51_4 +1.05V
XDP_TDI_R R226 *51_4
XDP_PREQ# R269 *51_4
XDP_TCLK R246 51_4
XDP_TRST# R519 51_4
check

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

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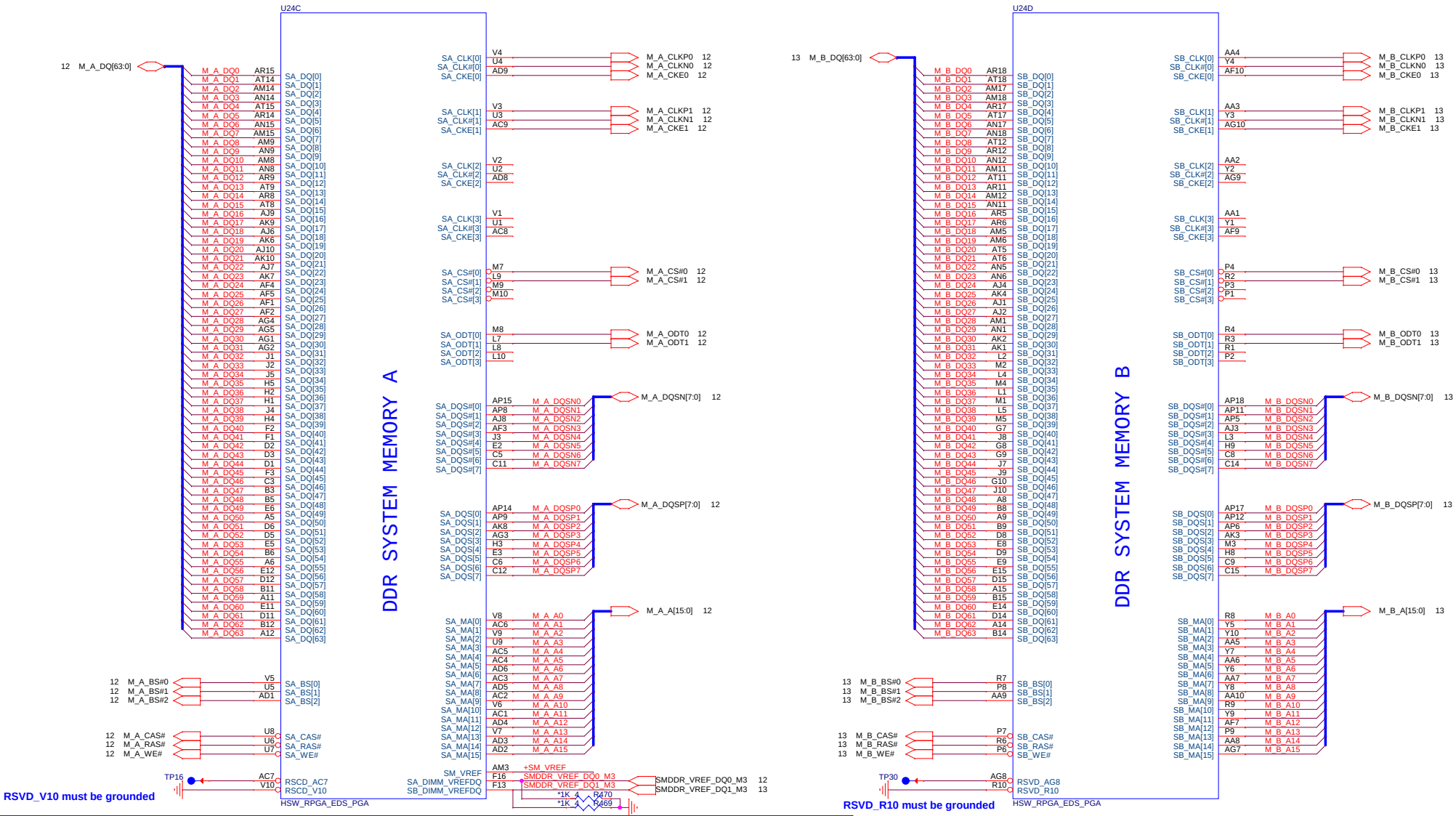
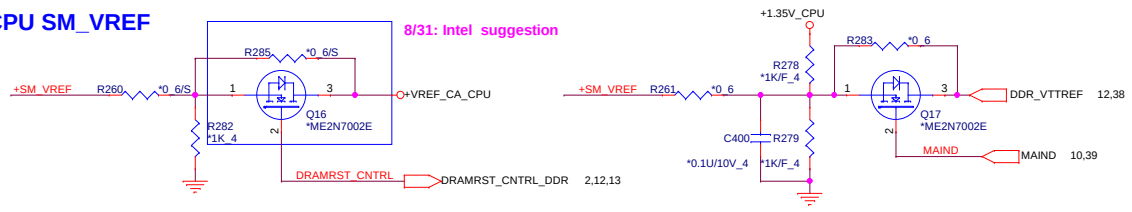
Haswell Processor (DDR3)

03



CPU SM_VREF

8/31: Intel suggestion



+1.35V_CPU 2,4,12,13,38
+VREF_CA_CPU 12

PROJECT : R63
Quanta Computer Inc.

NB5

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Haswell Processor (POWER)

04

POWER

+VCCIN 95A

+VCC_CORE

U24F

HSW_RPGA_EDS_PGA

CORE SUPPLY

C650 22U/6.3VS_8, C709 22U/6.3VS_8, C668 22U/6.3VS_8
C286 22U/6.3VS_8, C711 22U/6.3VS_8, C284 22U/6.3VS_8
C651 22U/6.3VS_8, C194 22U/6.3VS_8, C270 22U/6.3VS_8
C644 22U/6.3VS_8, C285 22U/6.3VS_8, C646 22U/6.3VS_8
C695 22U/6.3VS_8, C710 22U/6.3VS_8, C713 22U/6.3VS_8
C667 22U/6.3VS_8, C158 22U/6.3VS_8, C269 22U/6.3VS_8
C271 22U/6.3VS_8, C196 22U/6.3VS_8, C683 22U/6.3VS_8
C666 *22U/6.3VS_8, C195 *22U/6.3VS_8, C645 22U/6.3VS_8
C682 22U/6.3VS_8, C159 22U/6.3VS_8, C681 10U/6.3V_8
C649 10U/6.3V_8, C694 10U/6.3V_8, C712 10U/6.3V_8

AA26 VCC1, AA28 VCC2, AA34 VCC3, AA30 VCC4, AA32 VCC5, AB26 VCC6, AB29 VCC7, AB25 VCC8, AB27 VCC9, AB28 VCC10, AB30 VCC11, AB31 VCC12, AB33 VCC13, AB34 VCC14, AB32 VCC15, AC26 VCC16, AB35 VCC17, AC28 VCC18, AD25 VCC19, AC30 VCC20, AD28 VCC21, AC32 VCC22, AD31 VCC23, AC34 VCC24, AD34 VCC25, AD26 VCC26, AD27 VCC27, AD29 VCC28, AD30 VCC29, AD32 VCC30, AD33 VCC31, AD35 VCC32, AE26 VCC33, AE32 VCC34, AE28 VCC35, AE30 VCC36, AG28 VCC37, AG34 VCC38, AE34 VCC39, AF25 VCC40, AF26 VCC41, AF27 VCC42, AF28 VCC43, AF29 VCC44, AF30 VCC45, AF31 VCC46, AF32 VCC47, AF33 VCC48, AF34 VCC49, AF35 VCC50, AG26 VCC51, AH26 VCC52, AH29 VCC53, AG30 VCC54, AG32 VCC55, AH32 VCC56, AH35 VCC57, AH25 VCC58, AH27 VCC59, AH28 VCC60, AH30 VCC61, AH31 VCC62, AH33 VCC63, AH34 VCC64, AJ25 VCC65, AJ26 VCC66, AJ27 VCC67, AJ28 VCC68, AJ29 VCC69, AJ30 VCC70, AJ31 VCC71, AJ32 VCC72, AJ33 VCC73, AJ34 VCC74, AJ35 VCC75, G25 VCC76, H25 VCC77, J25 VCC78, K25 VCC79, L25 VCC80, M25 VCC81, N25 VCC82, P25 VCC83, R25 VCC84, T25 VCC85, U25 VCC86, U26 VCC87, V25 VCC88, V26 VCC89, W26 VCC90, W27 VCC91, Y25 VCC92, Y26 VCC93, Y27 VCC94, Y28 VCC95, Y29 VCC96, Y30 VCC97, Y31 VCC98, Y32 VCC99, Y33 VCC100, Y34 VCC101, Y35 VCC102, K26 VCC103, F25 VCC104

PEG AND DDR

+1.35V_CPU 4.2A

+1.35V_CPU

VDDQ1 AB11, VDDQ2 AB2, VDDQ3 AB5, VDDQ4 AB8, VDDQ5 AE11, VDDQ6 AE2, VDDQ7 AE5, VDDQ8 AE8, VDDQ9 AH11, VDDQ10 K11, VDDQ11 N11, VDDQ12 N8, VDDQ13 T11, VDDQ14 T2, VDDQ15 T5, VDDQ16 T8, VDDQ17 W11, VDDQ18 W2, VDDQ19 W5, VDDQ20 W8

C648 22U/6.3VS_8, C161 22U/6.3VS_8, C647 22U/6.3VS_8
C273 22U/6.3VS_8, C198 22U/6.3VS_8, C643 22U/6.3VS_8
C642 22U/6.3VS_8, C160 22U/6.3VS_8, C692 22U/6.3VS_8
C693 22U/6.3VS_8, C221 22U/6.3VS_8, C274 10U/6.3V_8
C665 10U/6.3V_8, C691 10U/6.3V_8, C272 10U/6.3V_8
C197 10U/6.3V_8, C680 10U/6.3V_8, C243 10U/6.3V_8
C679 10U/6.3V_8, C664 10U/6.3V_8, C162 10U/6.3V_8, +C231 *330U/2V_7343

RSVD K27, RSVD L27, RSVD T27, RSVD V27, RSVD N26, RSVD AL27, RSVD AK27, RSVD E17, RSVD W32, RSVD AL16, RSVD AL13, RSVD J27

VCCIO_OUT AN35 +VCCIO_OUT_R *0_1206/S R513 +VCCIO_OUT 300mA
VCCIO2PCH A23 +VCCIO_PCH_R *0/F_1206 R466 +VCCIO_PCH 300mA
VCOMP_OUT F22 +VCCIOA_OUT_R *0_1206/S R87 +VCCIOA_OUT
VSS_AP35 AP35

SVID

VIDALERT# AM28 H_CPU_SVIDALRT#
VIDSCLK AM29 H_CPU_SVIDCLK
VIDSOUT AL28 H_CPU_SVIDDAT
PWR_DEBUG H27 PWR_DEBUG_R 0_4 R61 TP1
AP34 0_4 R518

VSS AT34, VSS AL22, VSS AT33, VSS AM21, VSS AM25, VSS AM22, VSS AM20, VSS AM24, VSS AL19, VSS AM23, VSS AT32, VSS

RSVD_TP AT35, RSVD_TP AR35, RSVD_TP AR32, RSVD_TP AL26

SENSE LINES

R223 100_4 +VCC_CORE
VCC_SENSE AL35 VCC_SENSE 40
VSS_SENSE AK35 VSS_SENSE 40
R222 100_4

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

+VCCIOA_OUT 2
+VCCIO_OUT 2,40
+VCCIO_PCH 10
+1.5V 6,7,8,10,28,34,38,44
+1.35V_CPU 2,3,12,13,38
+1.05V 2,9,10,11,31,34,37
+VCC_CORE 40,41
+VCCST 2
+1.35VSUS 2,3,12,13,38

IO Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R774 16.5K/F_4 — THRM_MOINTOR 31
C62 0.1U/10V_4
R775 3.3K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 31
R776 100K_4 NTC
C54 0.1U/10V_4

4/30: CRB 1.0 add

+1.05V — R256 *0_8 — +VCCST
C392 *22U/6.3VS_8
C381 *22U/6.3VS_8

Power Test Propose

+1.05V — R60 150/F_4 — PWR_DEBUG_R
R62 *10K_4

+1.05V — R510 *0_8 — +VCCIO_OUT
C753 10U/6.3V_6

+1.05V — R462 0_6 — +VCCIO_PCH
CRB 1.0 stuff
C631 *4.7U/6.3V_6

4/30: DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP

SVID CLK

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

H_CPU_SVIDCLK — VR_SVID_CLK 40

SVID DATA

+VCCIO_OUT
Place PU resistor close to CPU
R253 130/F_4
7/26: DB sch modify, Del R23
Place PU resistor close to VR
DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm
H_CPU_SVIDDAT — VR_SVID_DATA 40

SVID ALERT

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

C337 0.1U/10V_4
+VCCIO_OUT — R247 75/F_4
H_CPU_SVIDALRT# — R248 43_4 — VR_SVID_ALERT# 40

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

CPU VDDQ

+1.35V_CPU — +1.35VSUS

Placement close to CPU.

C235 0.1U/10V_4
C225 *0.1U/10V_4

Note: please keep plane is enough for VDDQ 4.2A

P

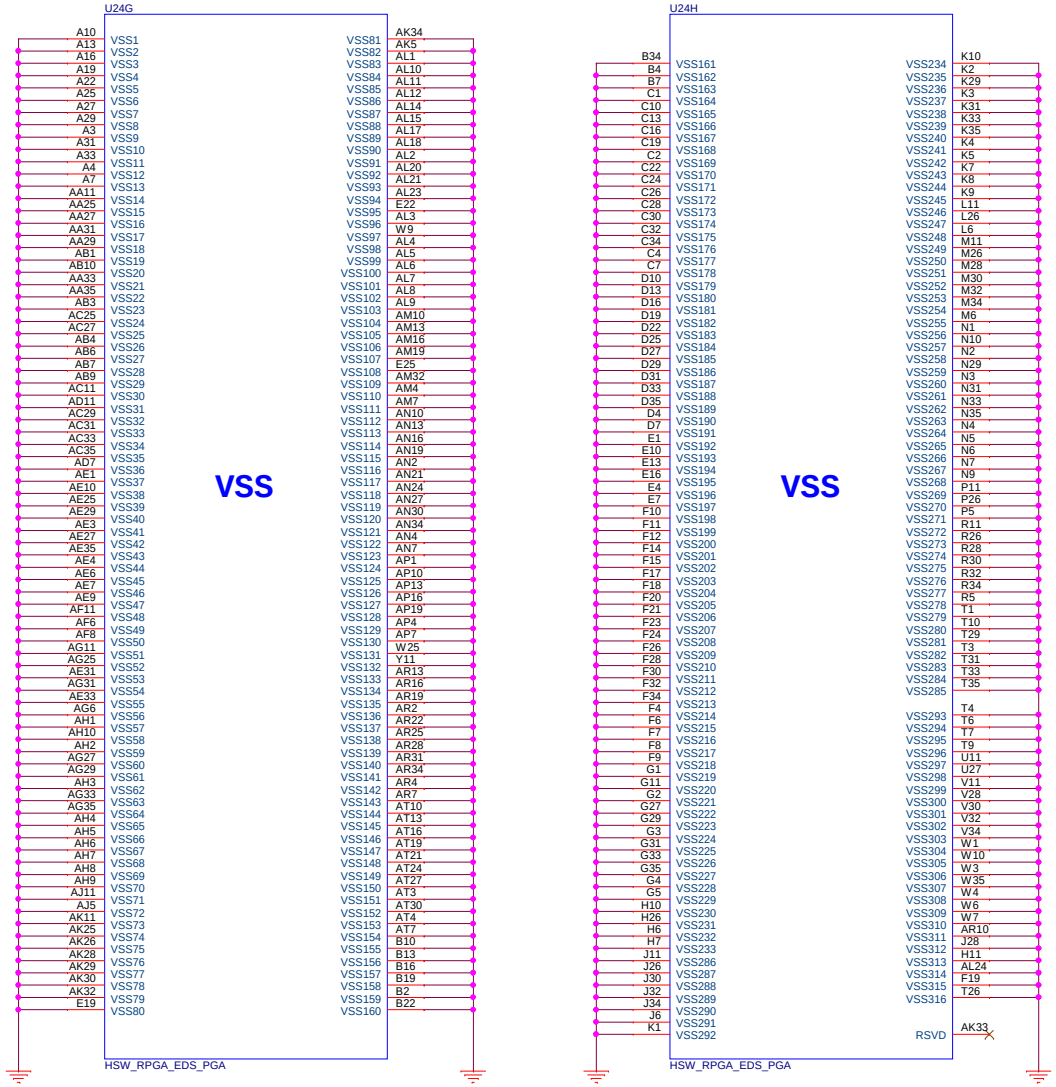
NB5

PROJECT : R63
Quanta Computer Inc.

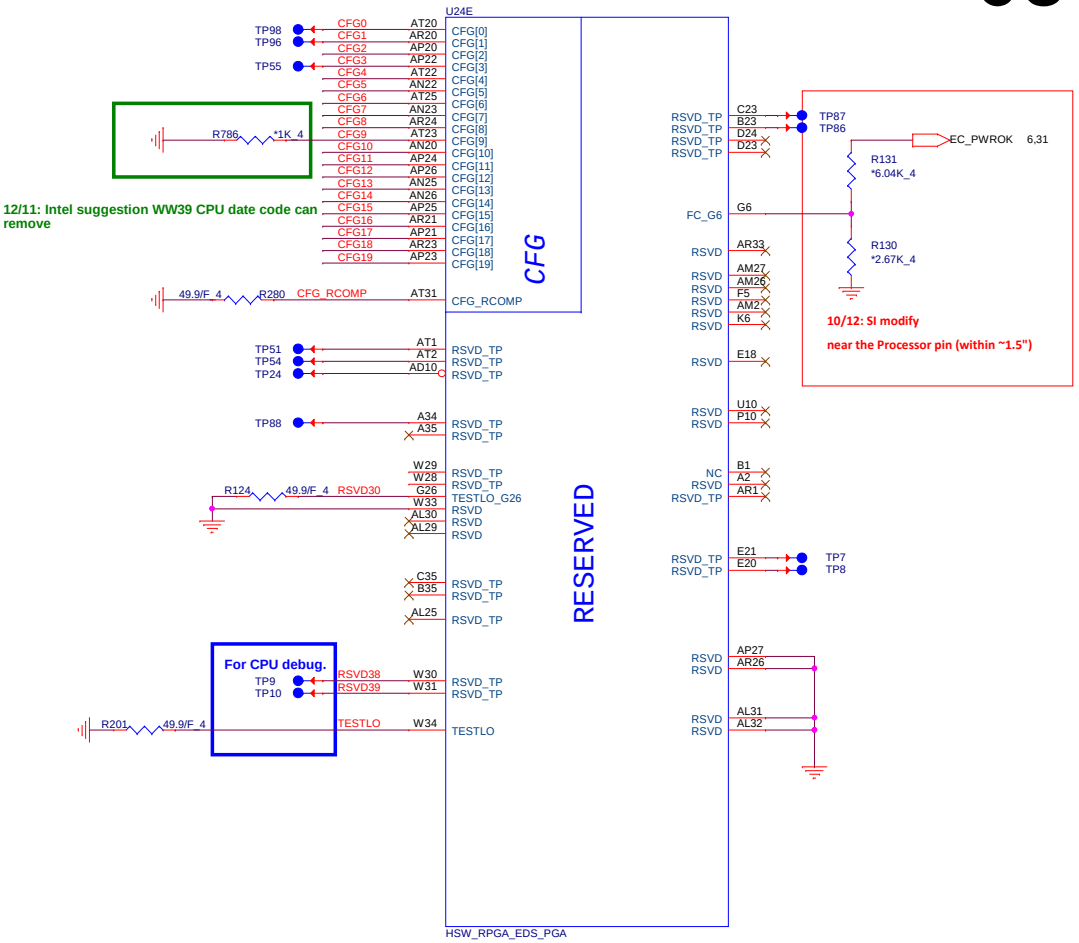
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

Date: Friday, December 21, 2012 Sheet 4 of 44

Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



05

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : R63 Quanta Computer Inc.		
NB5	Size: Custom; Document Number: SNB 4/4 (GND)	Rev: 1A
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Lynx Point (DMI,FDI,PM)

Lynx Point (DDI)

06

U33C

U33D

DMI

FDI

System Power Management

LVDS

CRT

Digital Display Interface

INT. HDMI

5/16 for DS3

12/17 PV modify

Reserve for power on sequence

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm

DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS

Reserve from EMI request

LPT_PCH_M_EDS/BGA

+3V_DEEP_SUS 7,8,9,10,39
+3V_RTC 7,10,11
+1.05V 2,4,9,10,11,31,34,37
+3VPCU 4,7,9,11,25,31,32,34,35,36
+3VS5 2,7,9,10,34,36,38,39,42,44
+3V 2,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+5V 7,23,26,28,29,32,33,34,39

PCH Pull-high/low(CLG)

for DS3

10/14: SI phase modify

10/12: SI phase modify

INT HDMI Detect Function

System PWR_OK(CLG)

7/26 DB Modify

10/17: SI Modify change to 10 Kohm

7/26 DB Modify

On Die DSW VR Enable
High = Enable (Default) Low = Disable

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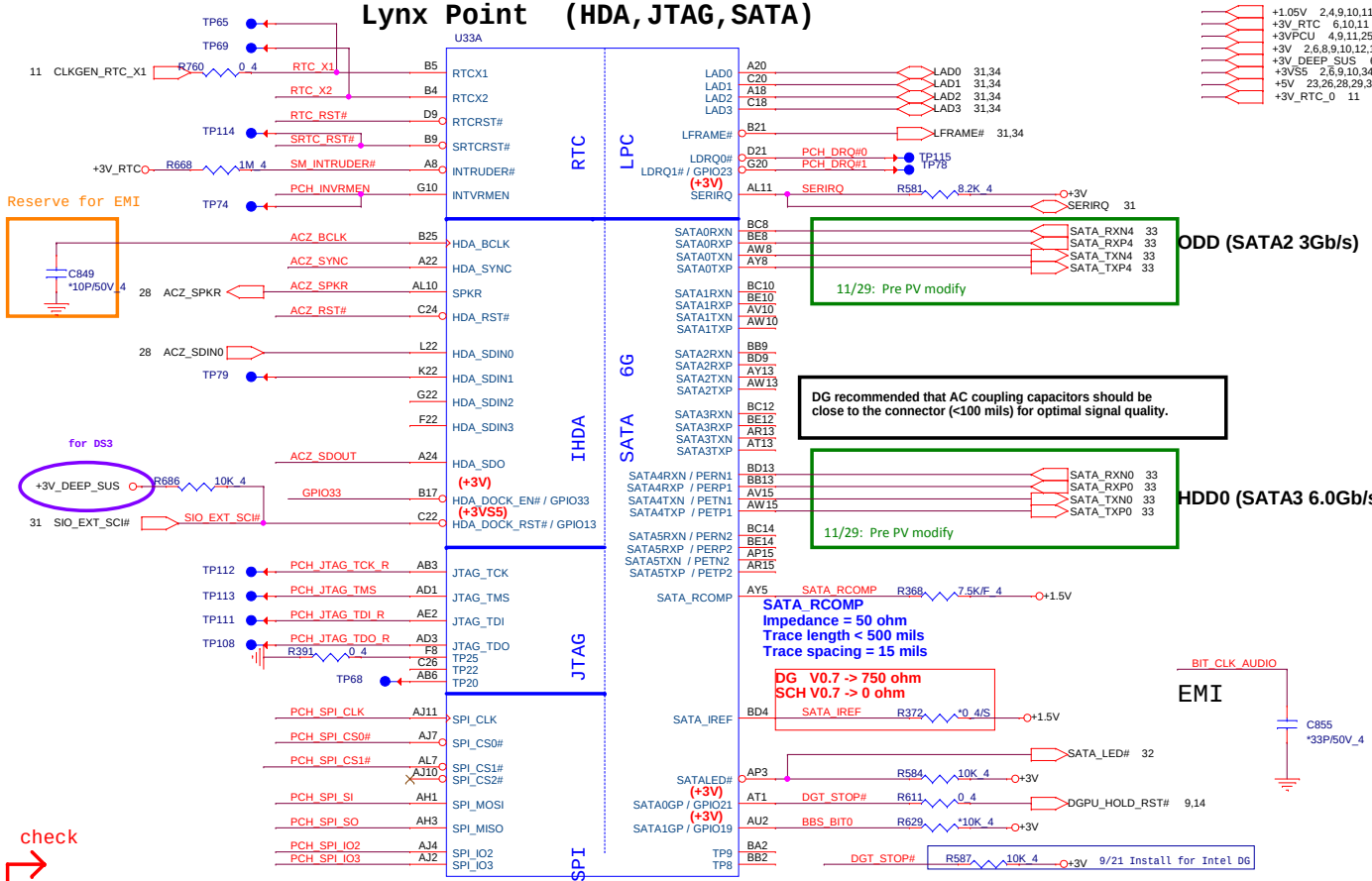
Quanta Computer Inc.

NB5

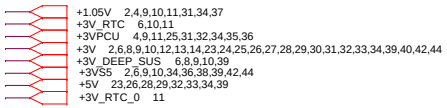
Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Monday, December 24, 2012	Sheet 6 of 44	

Lynx Point (HDA,JTAG,SATA)



PCH Strap Table

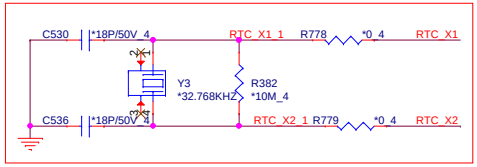
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R569 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R563 *1K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R389 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R680 *0_4 +3V 10/18: SI Modify [Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0; GNT0# 1 0; Boot Location SPI LPC	R613 *1K_4 BBS_BIT0 R390 *1K_4 BBS_BIT1 8
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R684 *1K_4 ACZ_SYNC 12/13: PV modify
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	31 GPIO33_E ACZ_SDOUT R693 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R621 *1K_4 BT_OFF# 9,34
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R571 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R374 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	R564 *1K_4 PCH_SUSCLK 6,31



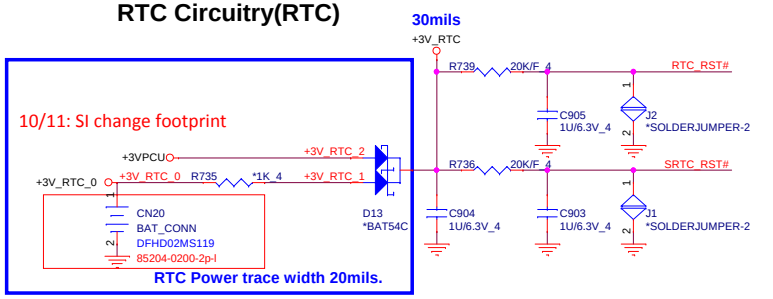
10/18: SI Modify

RTC Clock 32.768KHz

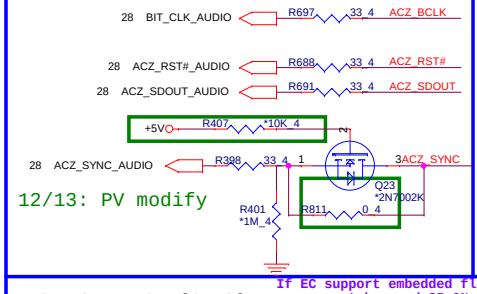
07



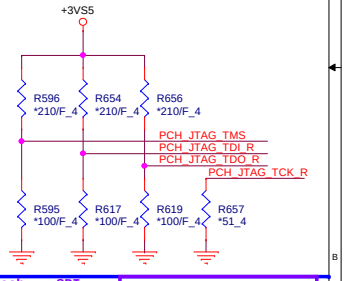
RTC Circuitry(RTC)



HDA Bus(CLG)

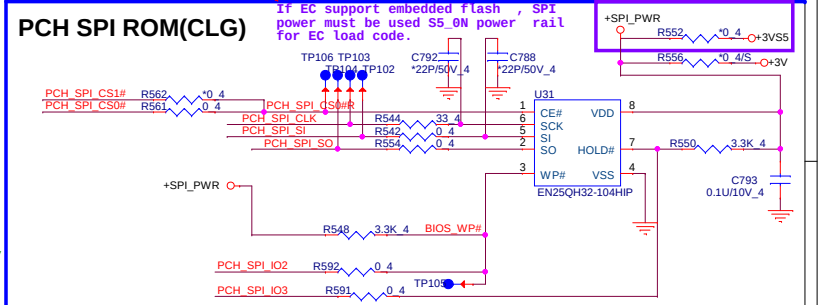


PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.



10/18: Del R350 , R344

Vender	Size	P/N
EON	4MB	AKE39ZN0Q03 EON EN25QH32-104HIP
AMIC	4MB	AKE39ZN0800 AMIC A25QE32M-F (QE)
Socket		DFHS08FS023

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

USB3.0

USB2.0

USB2.0/USB3.0 COMBO 1st

USB2.0

USB2.0/USB3.0 COMBO 2nd

WLAN

LAN

Cardreader

Webcam

Touch screen

12/11: PV modify

Right_USB

WLAN

PCI

USB

Thermal

C- Link

SMBUS

PCI-E*

CLOCKS

FLEX CLOCKS

RF

10/12: SI modify

10/18: SI modify

change 25M to small size

check

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

PLTRST#(CLG)

7/26 DB modify

PEG Clock detect (SG only)

7/26 DB modify

SMBus/Pull-up(CLG)

12/18 PV modify

CLK_REQ/Strap Pin(CLG)

for DS3

7/26 DB modify

SG : Rb ; UMA : Ra

CLOCK TERMINATION for FCIM

PCIE Clock

WLAN

LAN

GPU

Remove for UMA only.

SMBus/Pull-up(CLG)

for DS3

+1.05V	2,4,9,10,11,31,34,37
+1.5V	6,7,10,28,34,38,44
+3VS5	2,6,7,9,10,34,36,38,39,42,44
+3V	2,6,7,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+3V_DEEP_SUS	6,7,9,10,39

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

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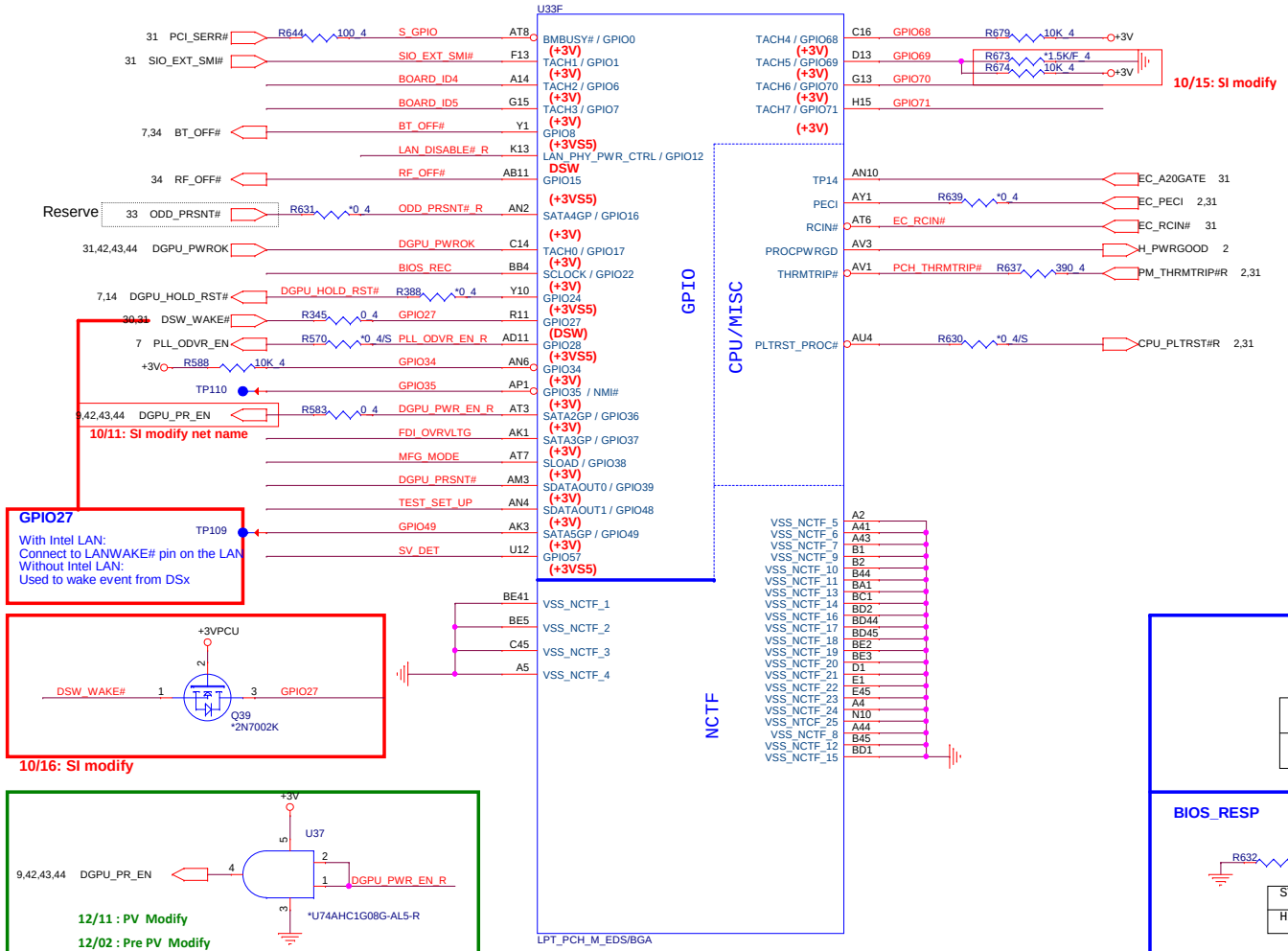
Lynx Point (GPIO,VSS_NCTF,RSVD)



Clock Gen Power OK (CLG)

+3V_DEEP_SUS 6,7,8,10,39
+3VS5 2,6,7,10,34,36,38,39,42,44
+3V 2,6,7,8,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+5VS5 23,29,30,34,36,37,38,39,40,41,42,43,44

09

PCH MISC PU /PD

EC_A20GATE R638 10K_4 +3V
EC_RCIN# R609 10K_4
PCH_THRMTRIP# R636 *1K_4 +1.05V

MFG-TEST

MFG_MODE R567 10K_4 +3V
R568 *0_4

GPIO Pull-up/Pull-down(CLG)

for DS3

DGPU_HOLD_RST# R610 *10K_4 +3V_DEEP_SUS
BT_OFF# R622 10K_4
10/14: SI modify
GPIO35 R649 10K_4 +3V
SIO_EXT_SMI# R694 10K_4
GPIO70 R364 10K_4
GPIO71 R371 10K_4
ODD_PRSNT#_R R589 10K_4
DGPU_PWROK R677 *10K_4
Power already stuffed. R616 10K_4
GPIO49 R653 *10K_4
DGPU_PWROK R678 *10K_4
10/12: SI modify
LAN_DISABLE#_R R362 *10K_4 +3VS5
GPIO27 R578 10K_4
10/17: SI modify Del R577

Swap GPIO

0 = SGPIO
1 = Default

S_GPIO R646 1K_4 +3V
R645 *0_4

for DS3

RF_OFF# R572 1K_4 +3V_DEEP_SUS

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

R666 *0_4 BIOS_REC R667 10K_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

BIOS_RESP

R632 *0_4 TEST_SET_UP R650 10K_4 +3V

SV_SET_UP
High = Strong (Default)

SV Detect

0 = SV Detect
1 = Default

10/17: SI modify

R574 *100K_4
SV_DET R575 10K_4 +3V_DEEP_SUS
for DS3

GPIO36

Internal PD

DGPU_PWR_EN_R R582 *1K_4 +3V

SATA3GP/GPIO37

TLS Confidentiality

0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

FDI_OVRVLTG R594 *1K_4 +3V

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4		BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R63 UMA				0	0	0
DB R63 DIS				0	0	1
SI R63 UMA				0	0	0
SI R63 DIS				0	0	1
PV R63 UMA				1	0	0
PV R63 DIS				1	0	1

8 BOARD_ID0 BOARD_ID0
8 BOARD_ID1 BOARD_ID1
8 BOARD_ID2 BOARD_ID2
BOARD_ID3 BOARD_ID3

for DS3

R359 RD0 *10K_4 BOARD_ID0 R365 RU0 10K_4 +3V_DEEP_SUS
R618 RD1 10K_4 BOARD_ID1 R655 RU1 *10K_4
R600 RD2 *10K_4 BOARD_ID2 R647 RU2 10K_4
11/29 : Pre PV Modify
+3V
R676 RD4 10K_4 BOARD_ID4 R675 RU4 *10K_4
R379 RD5 10K_4 BOARD_ID5 R375 RU5 *10K_4

GFX Present

Rb R652 *100K_4 DGPU_PRSNT# R615 10K_4 Ra +3V

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
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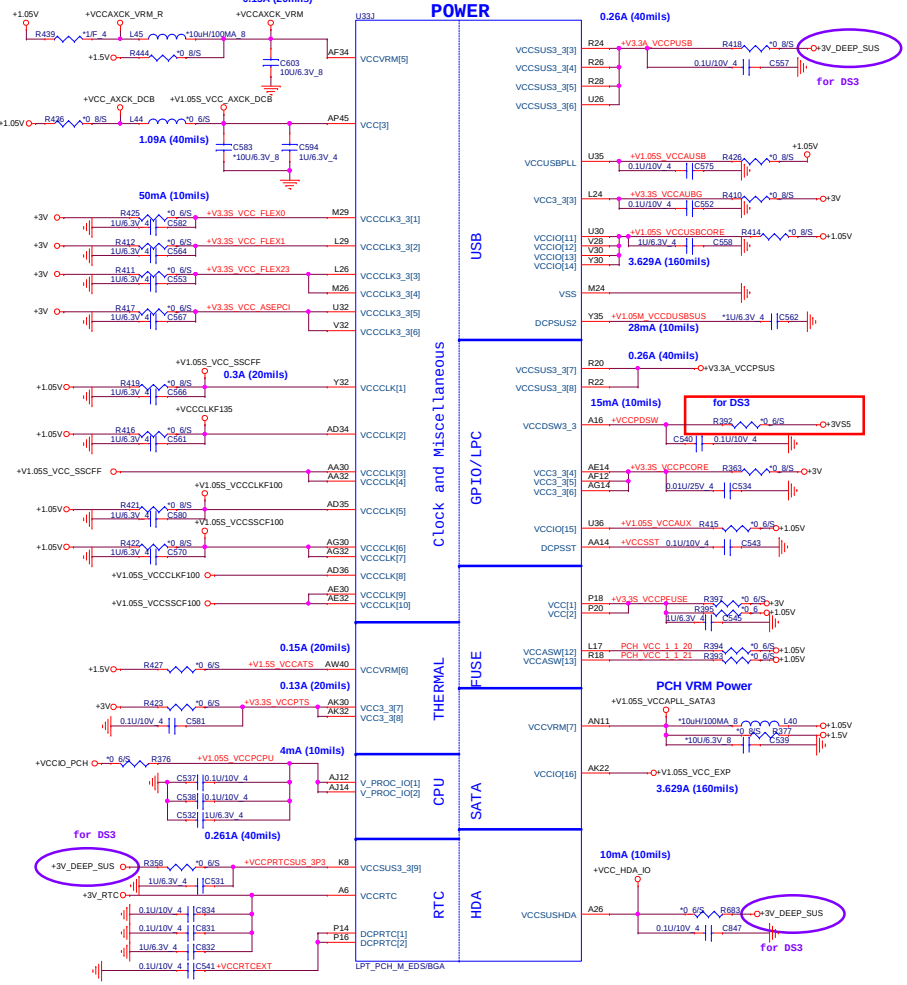
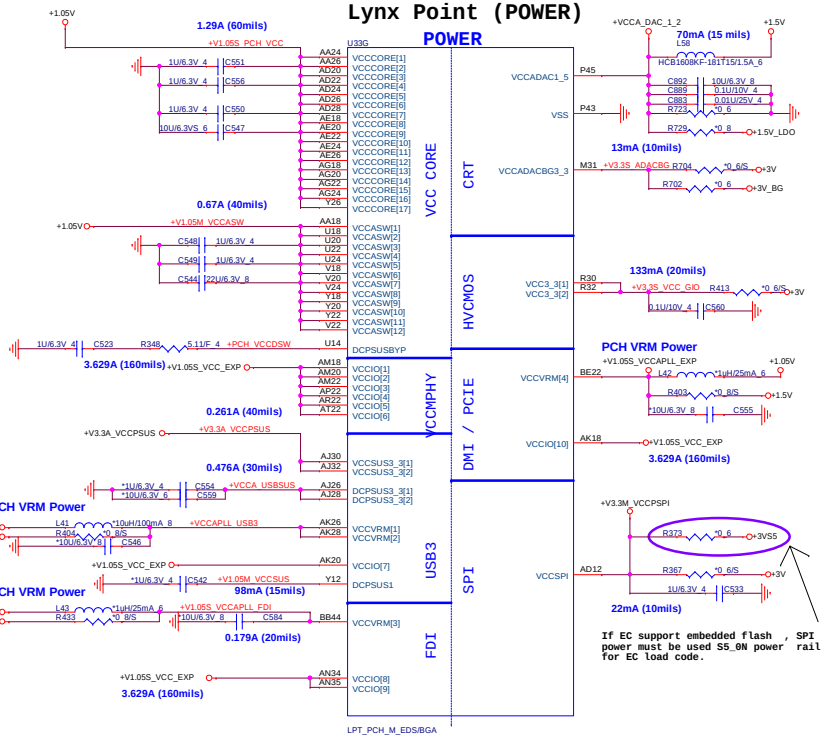
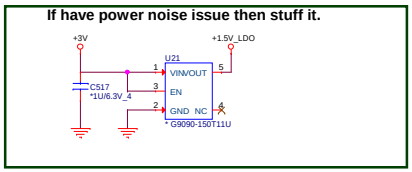
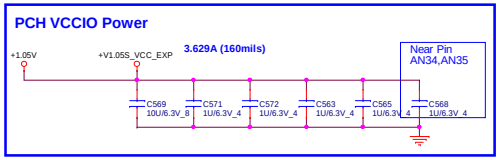
Lynx Point (POWER)

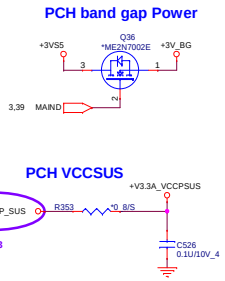


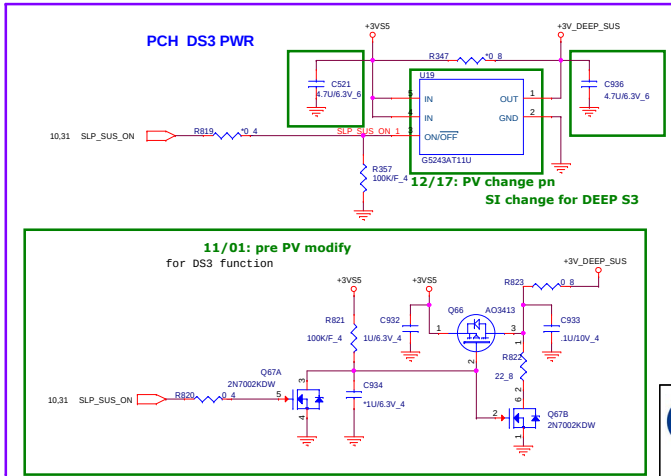
Lynx Point (POWER)

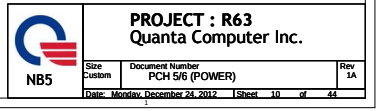




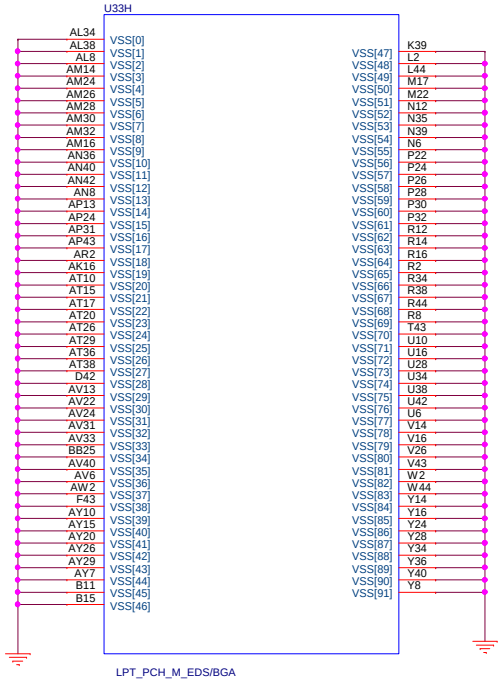




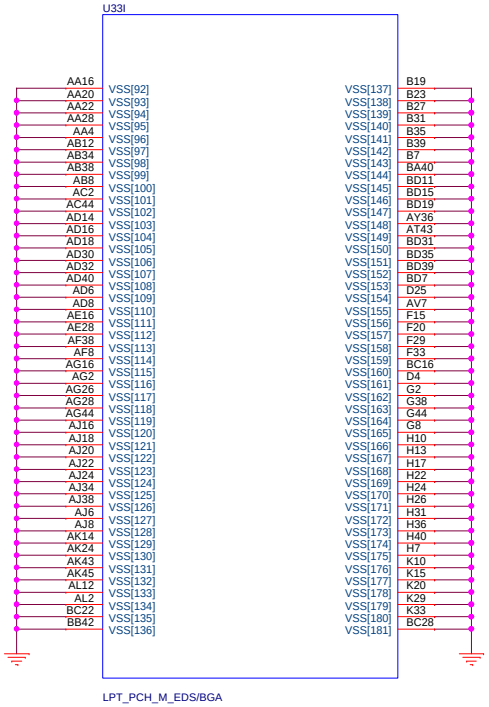




Lynx Point (GND)

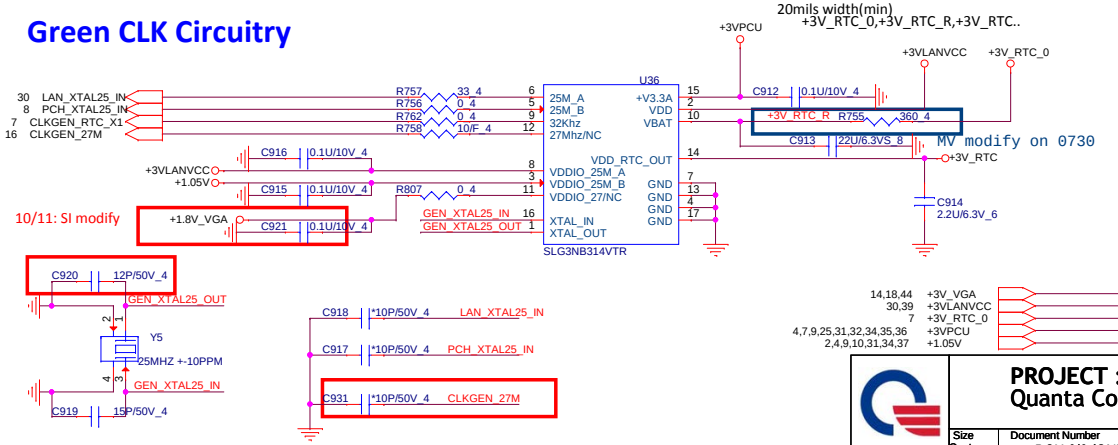


Lynx Point (GND)



	U36 P/N
UMA	AL3NB244000
DIS	AL000314000

Green CLK Circuitry



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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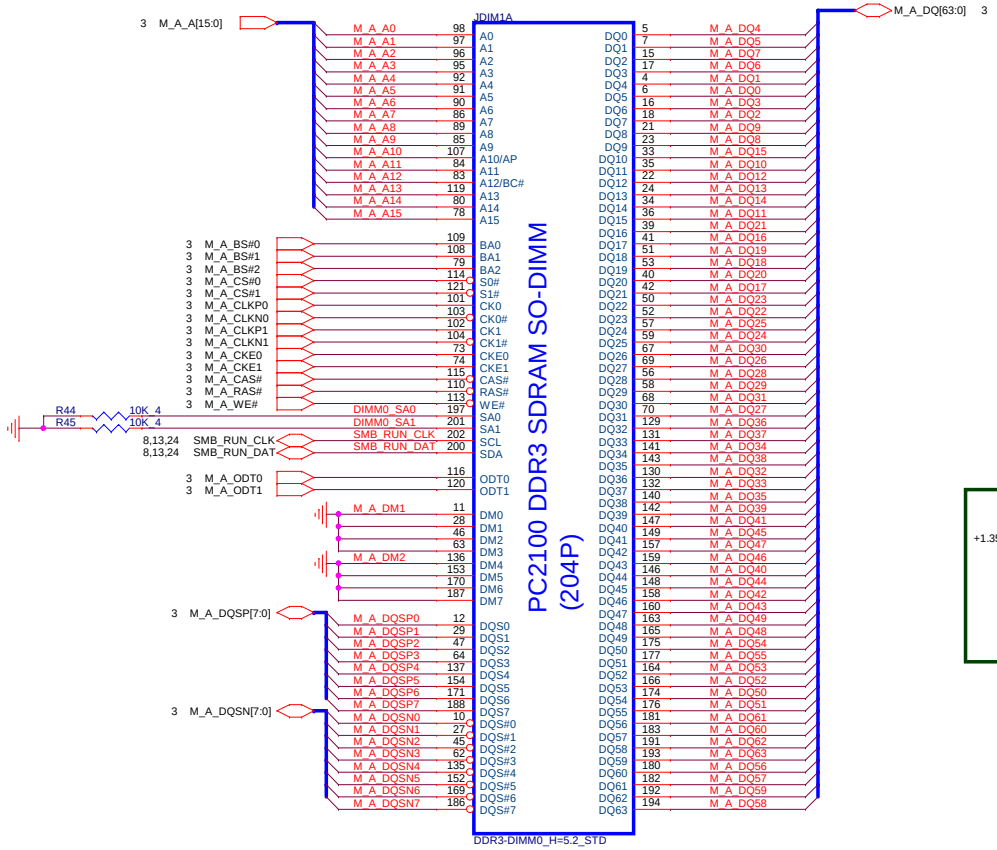
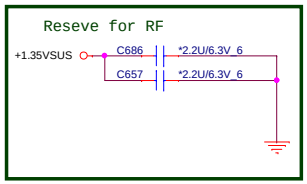
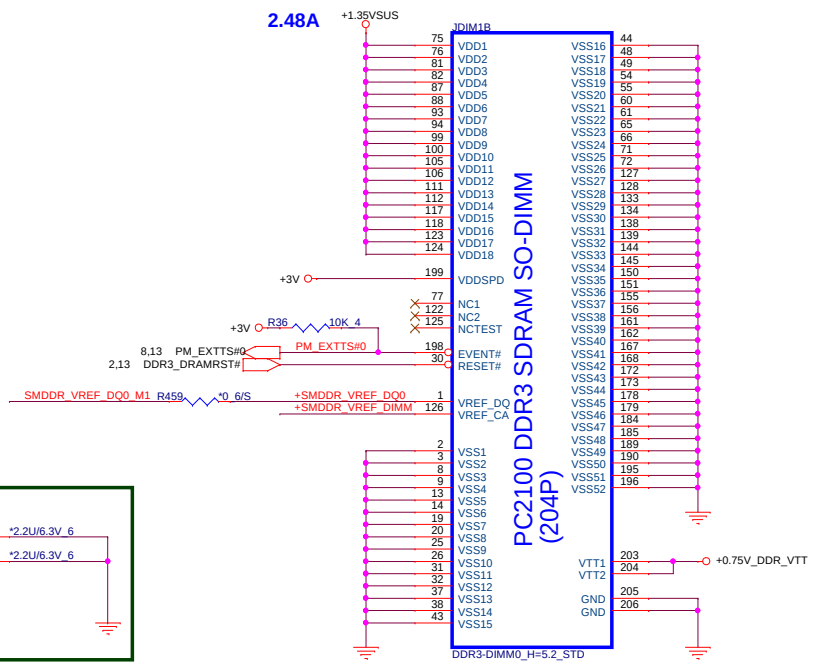
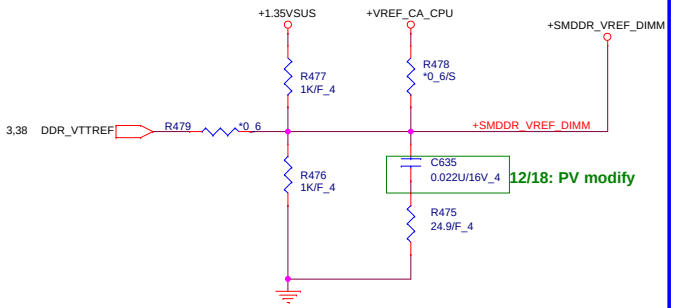


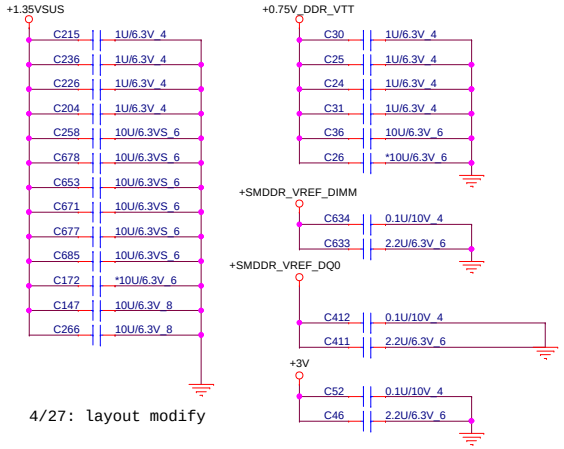




+SMDDR_VREF_DIMM 13
+VREF_CA_CPU 3
+0.75V_DDR_VTT 13,38,39
+1.35VSUS 2,3,4,13,38
+3V 2,6,7,8,9,10,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44



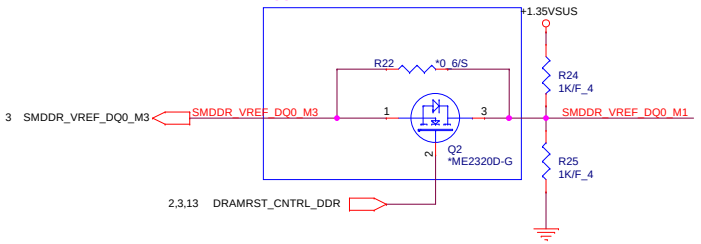
Place these Caps near So-Dimm0.



4/27: layout modify

VREF DQ0 M1 Solution

8/31: Intel suggestion



10/17: SI modify

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A
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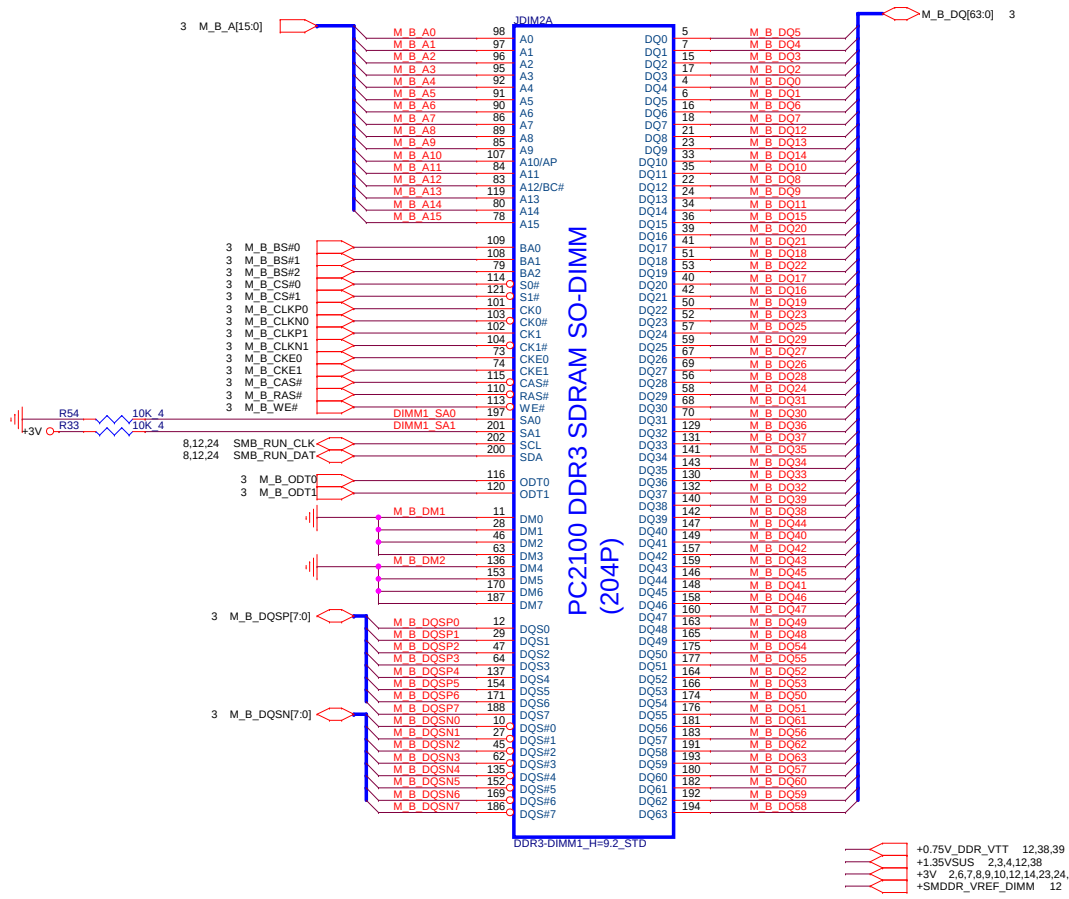
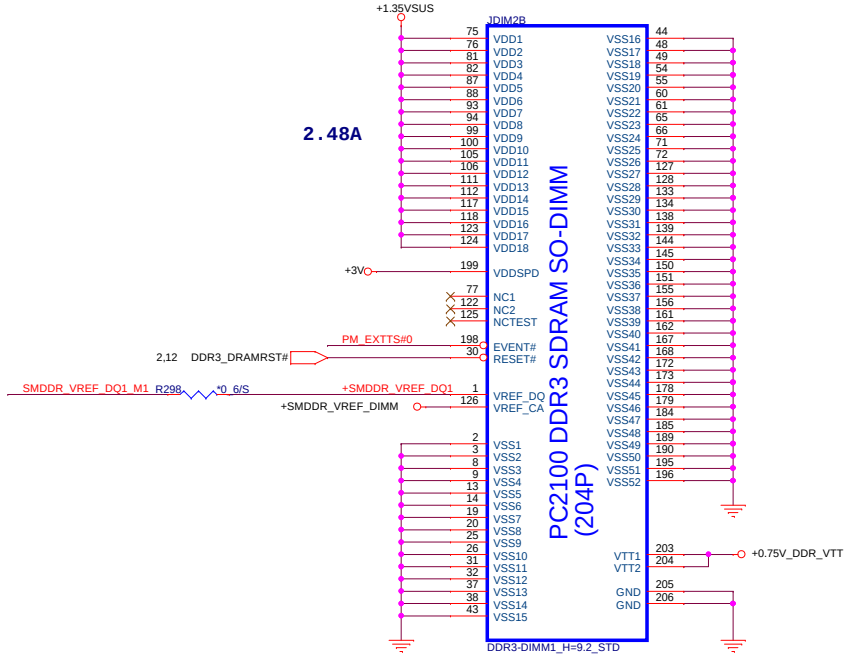
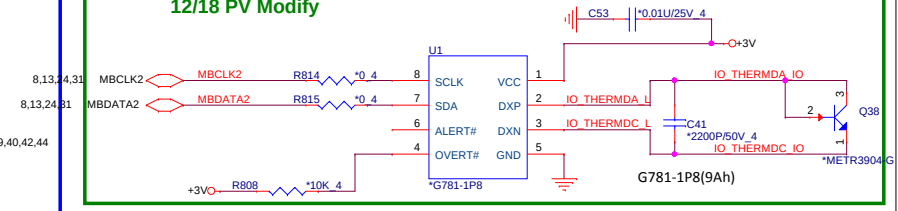


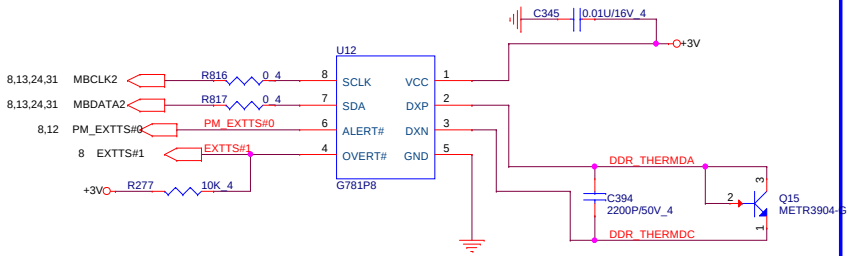


Local Thermal Sensor

12/18 PV Modify

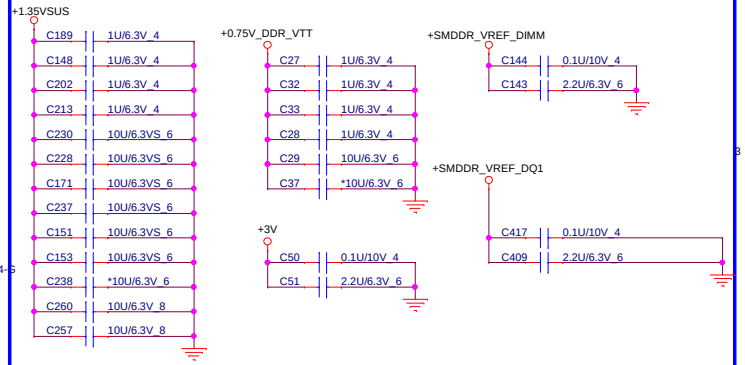


DDR Thermal Sensor



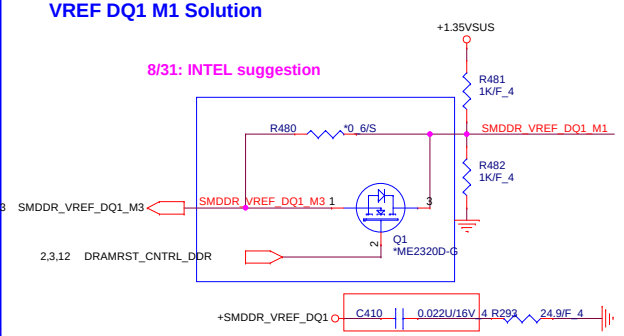
Address: G781P8(98h)

Place these Caps near So-Dimm1.

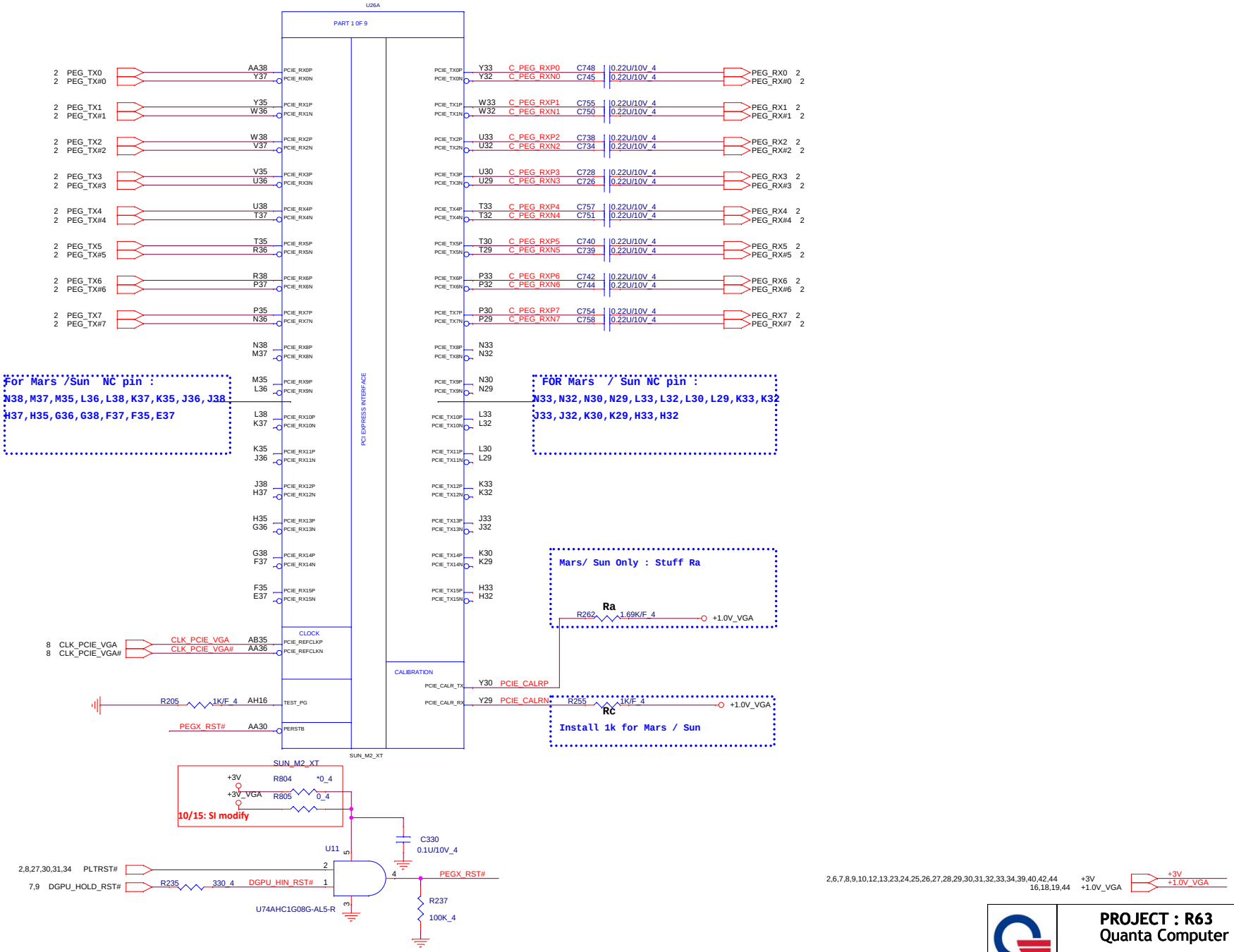


VREF DQ1 M1 Solution

8/31: INTEL suggestion



NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM1-RVS (9.2H)	Rev: 1A
Date: Friday, December 21, 2012	Sheet 13 of 44	



NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: THAMES_PCIE_Interface	Rev: 1A
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For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD29 /AC29 /AJ21 /AK21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

10/17: SI modify

12/13: PV modify

8/24: DB Modify

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20
AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff
For Sun Nc: R167, R141, C155
10/14: SI modify

FOR MARS: AD37/ AE38 / AD35 AVSSN to GND
FOR SUN : AD37/ AE38 / AD35 NC pin

8/15 DB Modify

10/14 SI Modify
DEL R747 R748 R749

10/14: SI modify , DEL R751, R753

FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36
AF37/ AC36 / AC38 / AB34 /

8/15 Modify

PV, change to 0ohm

PV, change to 0ohm

PV, change to DNI

For Mars: Stuff Ra, Rc=> VDDC 1.1V

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AM27, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

Thermal Solution(Close to GPU)

12/13: PV modify

Address: G781-1P8(9Ah)

Reserve for Power Play

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

PS3 BIT3=>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pces	AKD5PGWTW08 IC SDRAM(96P)H5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M16HA-093G:E	256Mx16 *4 pces	AKD5PZSTL01 IC SDRAM(96P)MT41J256M16HA-093G:E	2G
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pces	AKD5PZDT501 IC SDRAM(96P)K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FRR-11C	128Mx16 *4 pces	AKD5MZDTW03 IC SDRAM(96P)H5TC2G63FRR-11C	1G
100	4	Micron	MT41J128M16JT-093G:E	128Mx16 *4 pces		1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pces	AKD5MGGT535 IC SDRAM(96P)K4W2G1646E-BC1A	1G

14,16,18,19,44 +1.0V_VGA → +1.0V_VGA
11,16,18,19,44 +1.8V_VGA → +1.8V_VGA
17,18 +3V_DELAY → +3V_DELAY

NB5

PROJECT : R63
Quanta Computer Inc.

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Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

La
+1.8V_VGA — L23 *0_6/S — +1.8V_DPLL_PVDD
C259 10U/6.3V_8, C264 1U/6.3V_4, C265 0.1U/10V_4
Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

Lb
+1.0V_VGA — L21 *0_6/S — +1.0V_DPLL_VDDC
C253 10U/6.3V_8, C268 1U/6.3V_4, C267 0.1U/10V_4
1.0V(125mA DPLL_VDDC)
DPLL_VDDC : 0.935V @ 140mA
DPLL_PVSS

+1.8V_MPLL_PVDD
HCB1608KF-471T10 L35
C441 10U/6.3V_8, C437 1U/6.3V_4, C438 0.1U/10V_4
MPLL_PVDD : 1.8V @ 150mA

+1.8V_SPLL_PVDD
+1.8V_VGA — L16 FCM1005KF-121T03
C167 10U/6.3V_8, C176 1U/6.3V_4, C191 0.1U/10V_4
SPLL_PVDD : 1.8V @ 75mA

+1.0V_SPLL_VDDC
+1.0V_VGA — L19 HCB1608KF-471T10
C181 10U/6.3V_8, C222 1U/6.3V_4, C216 0.1U/10V_4
1.0V(125mA DPLL_VDDC)
SPLL_VDDC : 0.935V @ 150mA
SPLL_PVSS

DPEF_VDD18
R212 Ra *0_4
R249 Rb *0_4
reserve Ra, Rb for future ASIC

10/14: SI modify

U26I
PART 9 OF 9
AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS
PLL5XTAL
SUN_M2_XT

XTALIN AV33 — 0_4 R759 — CLKGEN_27M 11
XTALOUT AU34 — *0_4 R792 — EVGA-XTALI — *22P/50V_4 C244
R207 *10M_6 — Y2 *7A27000010 — C2
EVGA-XTALO — *0_4 R793 — *22P/50V_4 C245
11/29: Pre PV modify
XO_IN AW34 — TP129
12/13: PV modify del
XO_IN2 AW35 — R487 *0_4

CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB
C193 *0.1U/10V_4, C227 *0.1U/10V_4
R171 *51.1/F_4, R181 *51.1/F_4
Debug only,
for clock observation,
if not needed, DNI
route 50ohms
single-ended/
100ohms diff and keep short

U26F
PART 6 OF 9
PCIE_VSS: AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39
GND: F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N6 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27
GND: A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13
VSS_MECH: A39 AW1 AW39
SUN_M2_XT

AG22 is nc pin

14,18,19,44 +1.0V_VGA → +1.0V_VGA
11,15,18,19,44 +1.8V_VGA → +1.8V_VGA

PROJECT : R63
Quanta Computer Inc.
NB5
Size: Custom | Document Number: THAMES_XTAL | Rev: 1A
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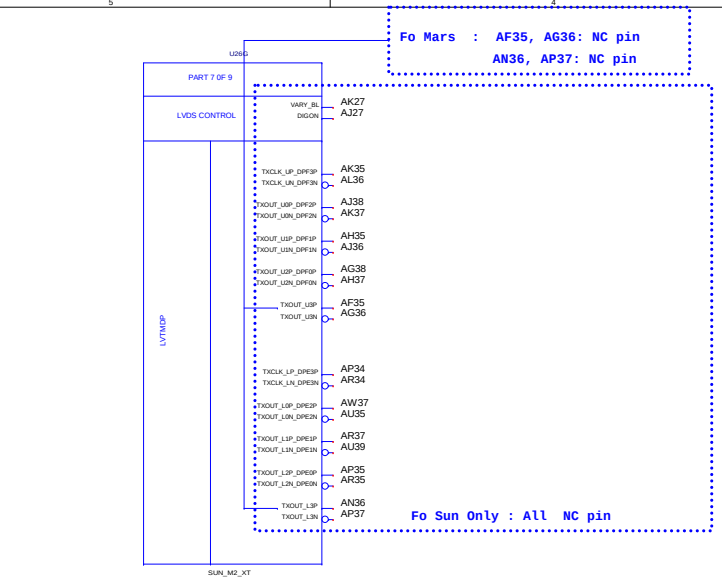
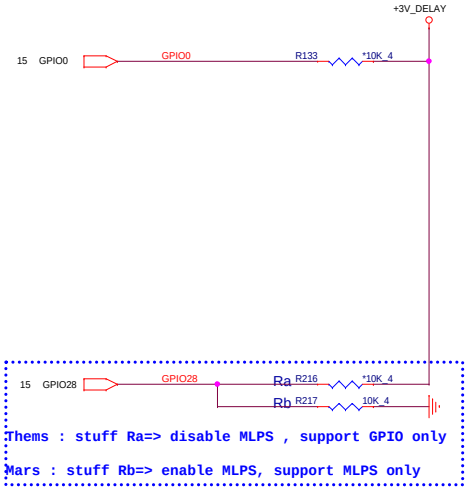




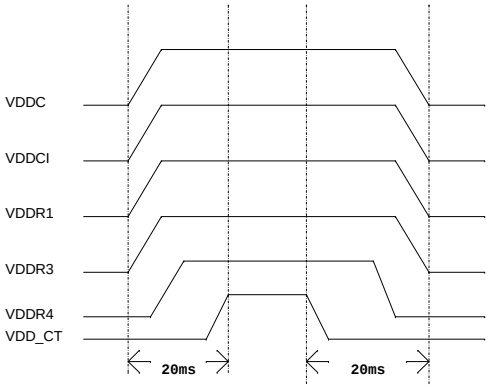
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50%_Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+3.3V_Delay
0	512M	1	0	0	+1.8V_VGA
0	1G	1	0	1	+1.8V_VGA
0	2G	1	1	0	
0	4G	1	1	1	

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_LVDS / STRAP	1A
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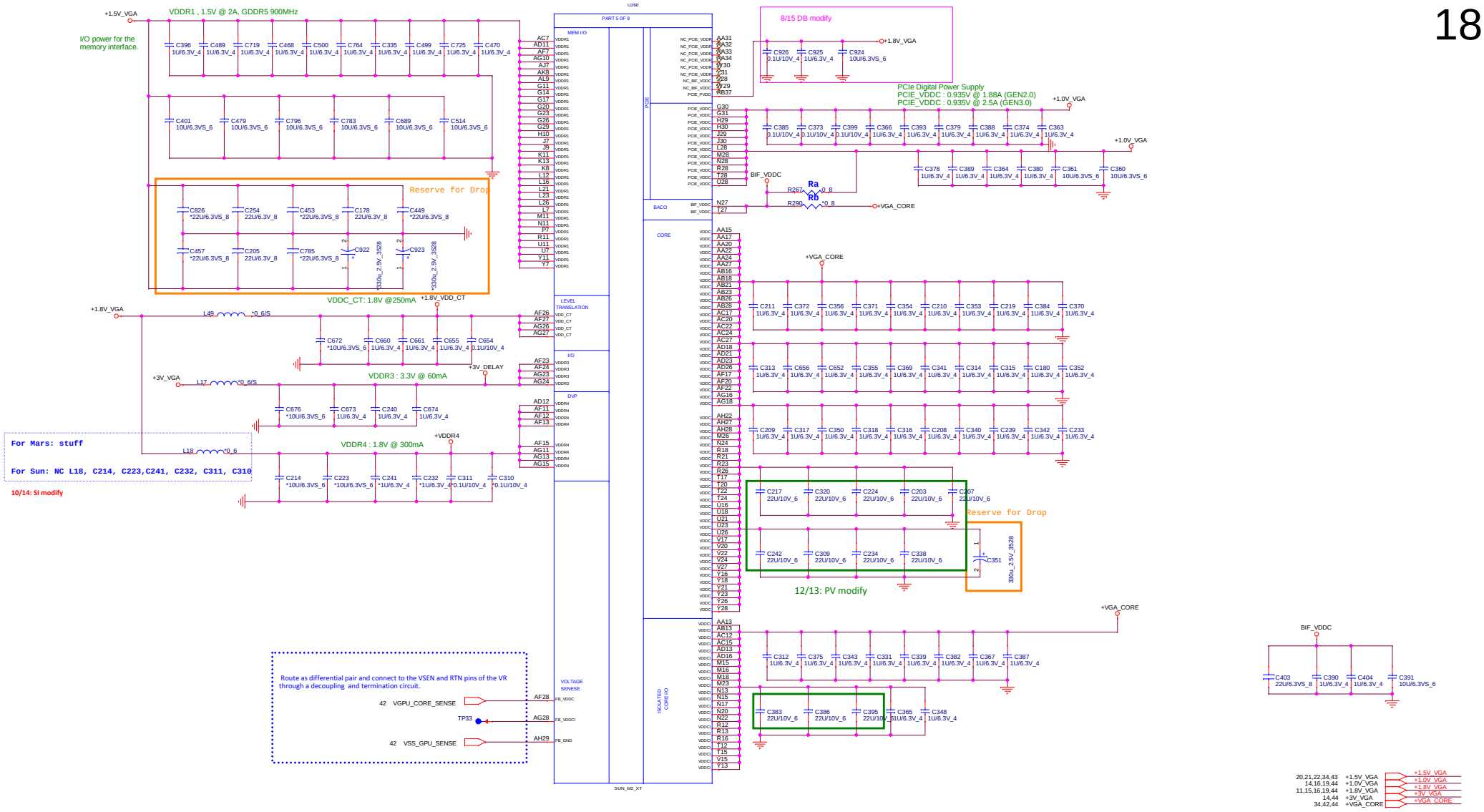

Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

PROJECT : R63	Quanta Computer Inc.
NB5	Size: Custom; Document Number: THAMES_Power & BACO; Rev: 1A
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For Mars : L20 sutff
For Sun: L20 , C247 , C246 , C252 NC

+1.0V_VGA
DPAB_VDD10
L20 *0_6
C247 *0.1U/10V_4
C246 *1U/6.3V_4
C252 *10U/6.3VS_6

10/14: SI modify

U26H
PART 8 0F 9
DP_VDDR
DP_VDDC
DP GND
CALIBRATION

DP_VDDC: AP31, AP32, AN33, AP33
DP_VDDC: AP13, AT13, AP14, AP15
DP_VDDC: AL33, AM33, AK33, AK34

DP_VDDR: AN24, AP24, AP25, AP26, AU28, AV29
DP_VDDR: AP20, AP21, AP22, AP23, AU18, AV19
DP_VDDR: AH34, AJ34, AF34, AG34, AM37, AL38

10/14: SI modify

For Mars : L26 sutff
For Sun: L26 , C279 , C281 , C282 NC

+1.8V_VGA
L26 *0_6
DPEF_VDD18
C279 *10U/6.3VS_6
C281 *1U/6.3V_4
C282 *0.1U/10V_4

10/14: SI modify

DPEF_VDD10
L25 *0_6
+1.0V_VGA
C291 *0.1U/10V_4
C290 *1U/6.3V_4
C293 *10U/6.3VS_6

For Mars : L25 sutff
For Sun : L25/ C293/C290/C291 NC

DP_VSSR: AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, AM35

AW28 DPAB_CALR
AW18 DPCD_CALR
AM39 DPEF_CALR

10/14: SI modify

R495 *150/F_4

For Mars : R495 sutff
For Sun : R495 NC

10/14: SI modify DEL R754

For Mars : R754 sutff
For Sun : R754 NC

SUN_M2_XT

14,16,18,44 +1.0V_VGA
11,15,16,18,44 +1.8V_VGA

+1.0V_VGA
+1.8V_VGA

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_DP Powers	1A

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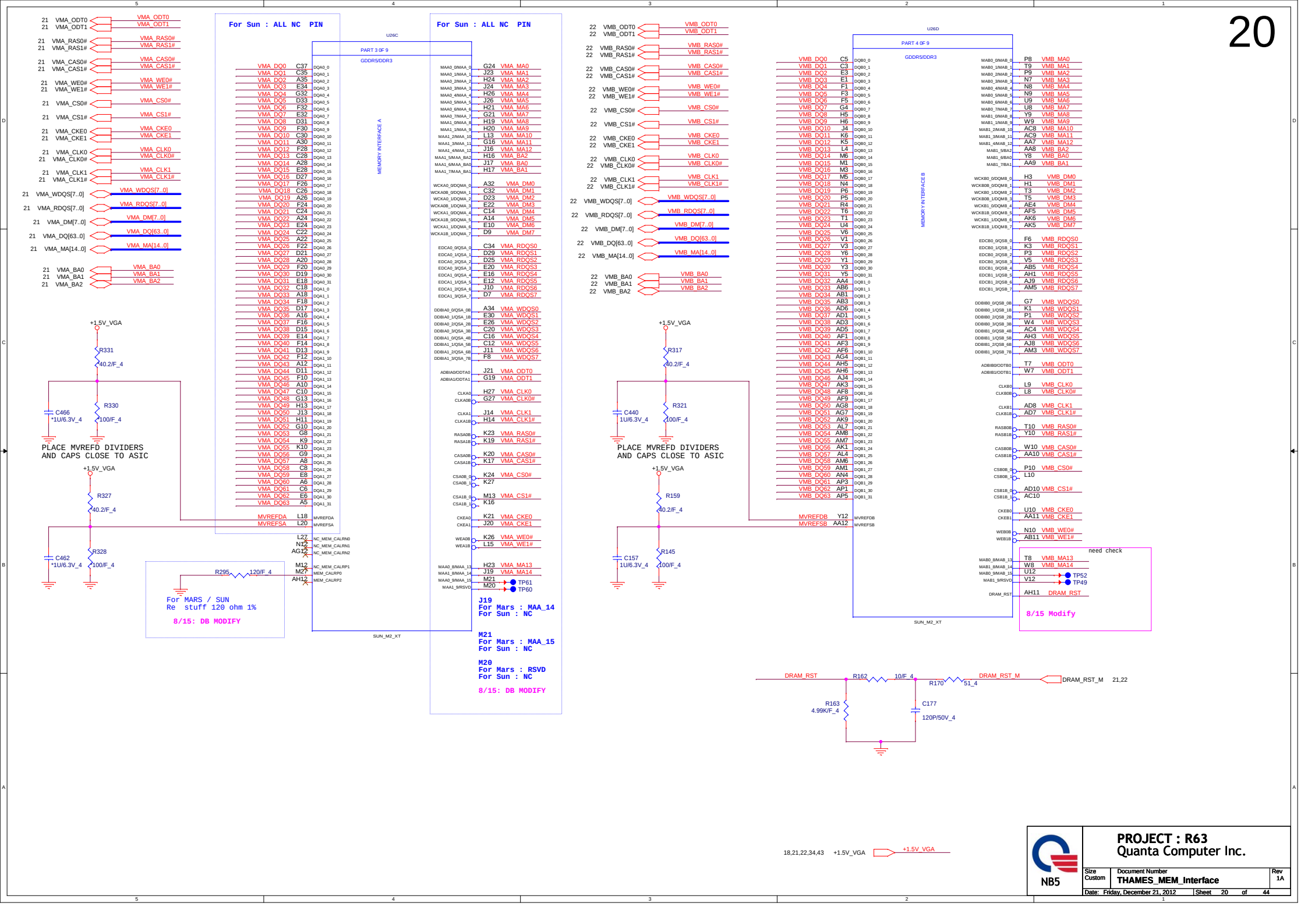

PROJECT : R63	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: THAMES_MEM_Interface
Rev: 1A	
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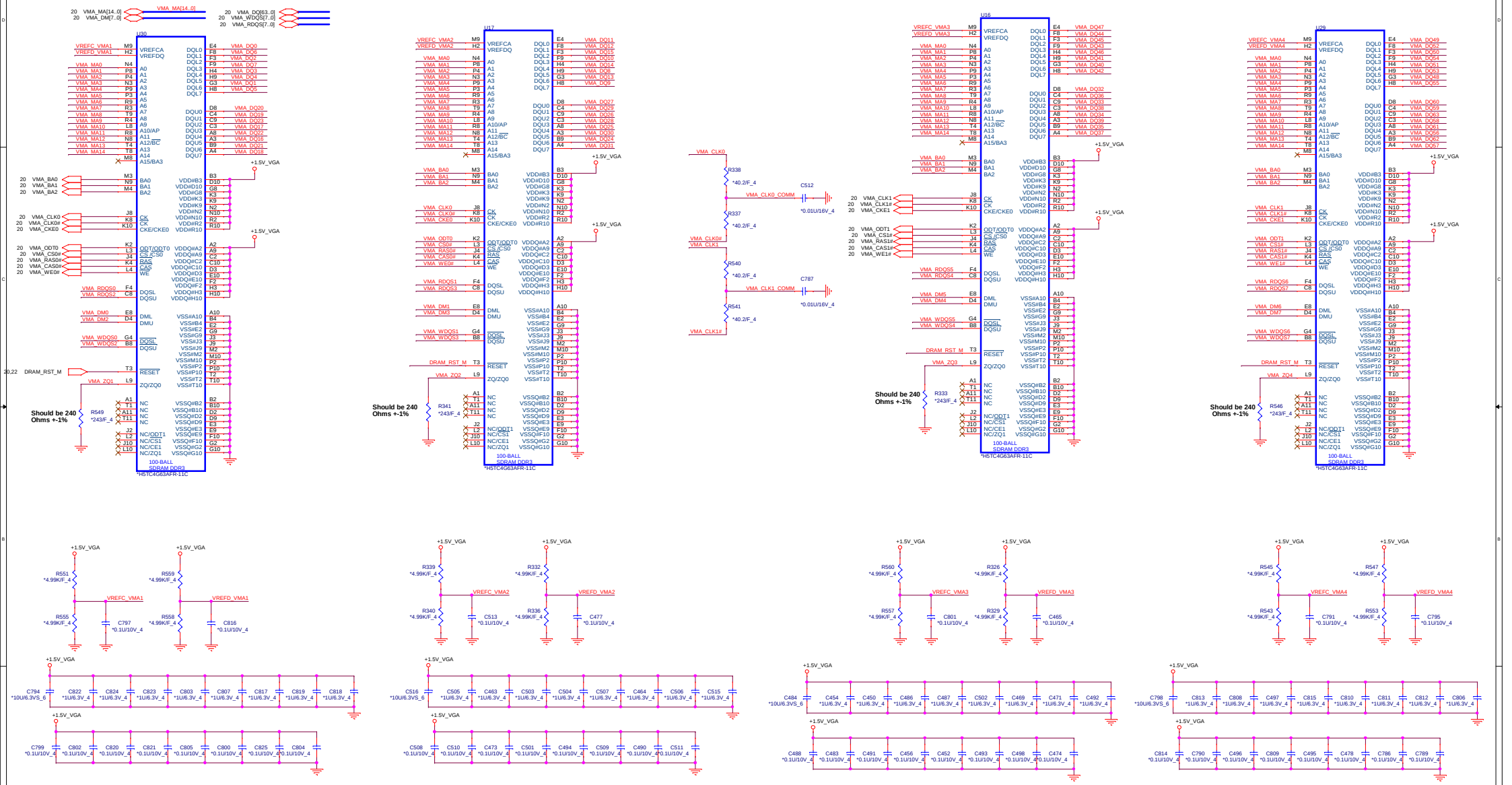
CHANNEL A: 256MB/512MB DDR3



18,20,22,34,43 +1.5V_VGA +1.5V_VGA

NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: VRAM-A (DDR3 BGA96)	Rev: 3A
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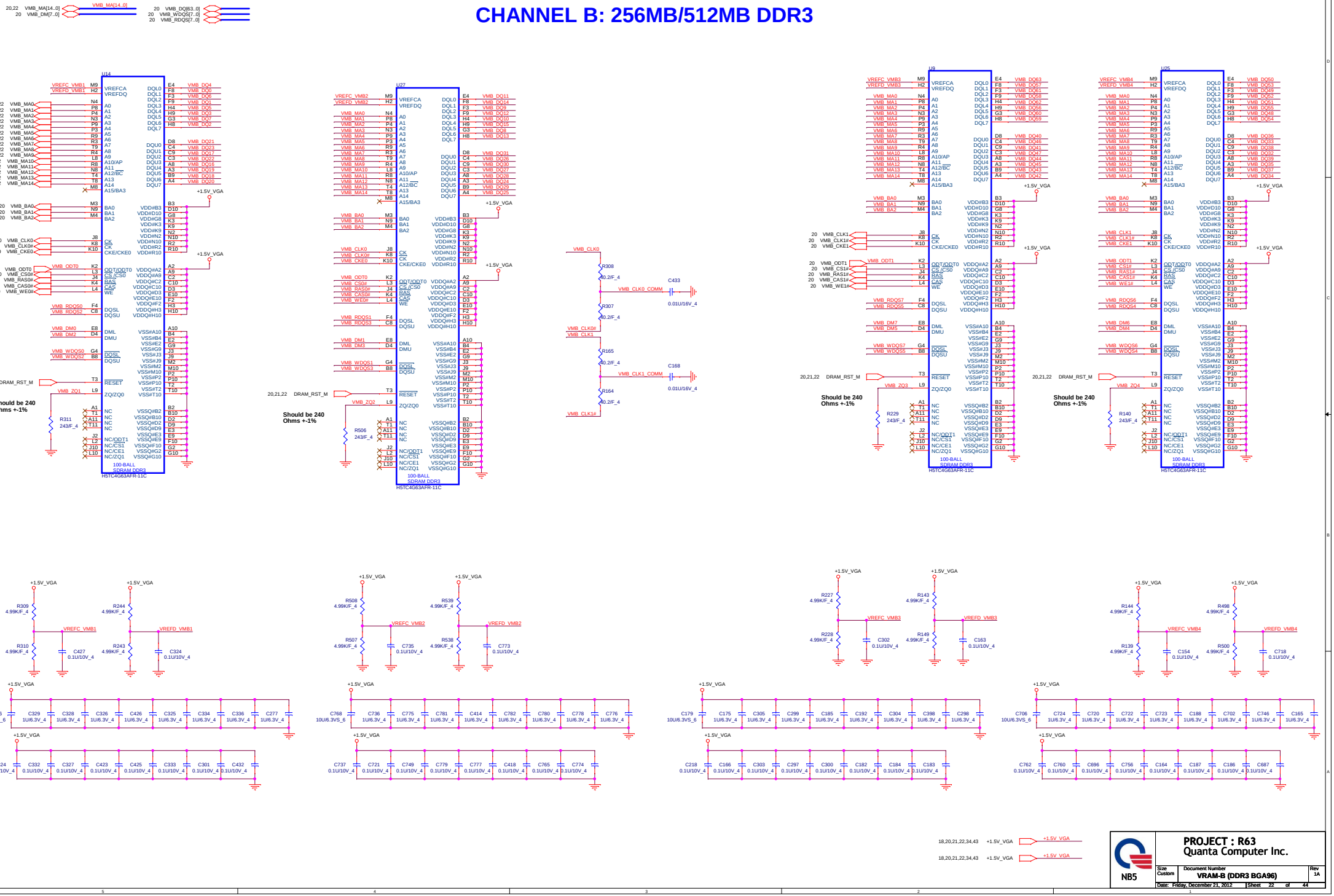
CHANNEL B: 256MB/512MB DDR3



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Quanta Computer Inc.	
NB5	Size: Custom
Document Number: VRAM-B (DDR3 BGA96)	Rev: 1A
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7,26,28,29,32,33,34,39 +5V
2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
29,30,34,36,37,38,39,40,41,42,43,44 +5VS5
26 +5V_HDMIC

CRT PORT

10/24: SI modify

12/13: PV modify

6 CRT_R
6 CRT_G
6 CRT_B

CRT_R → L15 BLM18BB470 → CRT_R1
CRT_G → L14 BLM18BB470 → CRT_G1
CRT_B → L13 BLM18BB470 → CRT_B1

R112 150/F_4
R104 150/F_4
R100 150/F_4
C131 22P/50V_4
C115 22P/50V_4
C125 22P/50V_4
C101 22P/50V_4
C102 22P/50V_4
C138 22P/50V_4
EMI

+5V_HDMIC
CRTDDCDAT2 C170 *470P/50V_4
CRTHSYNC C199 10P/50V_4
CRTVSYNC C200 10P/50V_4
CRTDDCCLK2 C174 *470P/50V_4
CRT CONN
CN9

DFDS15FR362
dsub-dsd-15atxb-15p

6 HSYNC_COM
6 VSYNC_COM
6 DDCCLK
6 DDCDATA

HSYNC_COM
VSYNC_COM
DDCCLK
DDCDATA

+5V
+3V
C134 0.22U/25V_6
CRT_BYP

U7
TPD7S019
+5V_CRT2
VCC_SYNC
VCC_DDC
BYP
VCC_VIDEO
VIDEO_1
VIDEO_2
VIDEO_3
GND
SYNC_OUT2
SYNC_OUT1
SYNC_IN2
SYNC_IN1
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2

CRT_VSYNC1 R157 22_4 CRTVSYNC
CRT_HSYNC1 R156 22_4 CRTHSYNC
VSYNC_COM
HSYNC_COM
DDCCLK
DDCDATA
VGA_DDC_CLK_RT
VGA_DDC_DAT_RT
CRTDDCCLK2
CRTDDCDAT2

+5V_CRT2
R148 2.2K_4
R160 2.2K_4

DDCCLK R168 2.7K_4
DDCDATA R169 2.7K_4
+3V

+5V_HDMIC
+5V_HDMIC
MEK500V-40 D3
+5V_CRT2
C146 0.1U/10V_4
9/27 EMI request

9/29 EMI request
+5VS5
C609 0.1U/10V_4
C64 0.1U/10V_4
C71 0.1U/10V_4

HOLE

H27 *spad-r63-8np
H16 *h-tc354bc315ic150d110p2
H5 *h-c354ic150d110p2
H6 *h-c354ic150d110p2
H4 *h-c354ic150d110p2

12/20: PV add

H20 *H-C315IC150D110P2
H22 *h-c197d110p2
H21 *h-c315ic150d110p2
H3 *H-C197D110P2
H17 *h-tc276bc315d236p2
H25 *spad-re197x79np

10/17: SI modify add H25

H26 *H-C87D87N

11/30: Pre PV modify add H26

12/13: PV modify H26 Del gnd

FAN hole
H2 *O-LX9-1

PCH BKT
H19 h-tc177bc276ic162d122p2
H18 h-tc177bc276ic162d122p2
Nut PN:MBUL1001010

CPU BKT
H11 *intel-cpu-bkt2

VGA BKT
H15 *H-TC248BC197D150P2
H14 *H-TC248BC197D150P2
H10 *H-TC248BC197D150P2

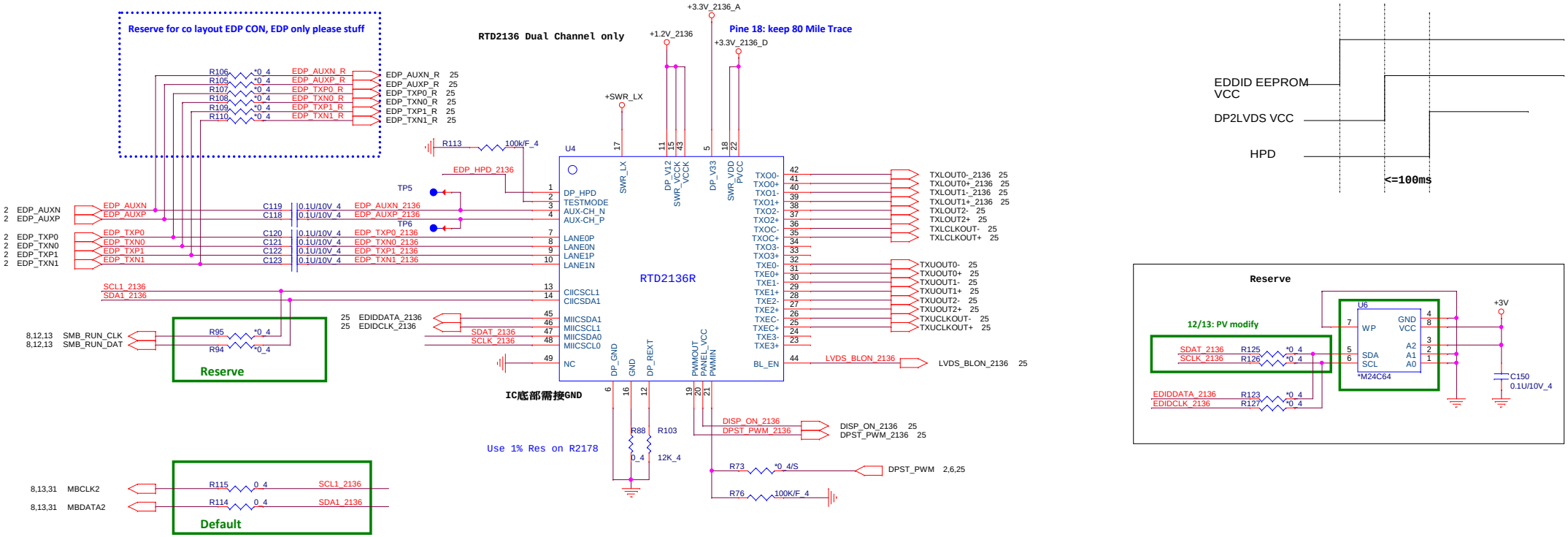
THERMAL BKT
H9 h-tc177bc276ic162d122p2
H1 *h-tc256bc276d168x155p2
H24 *h-e315x278d110p2

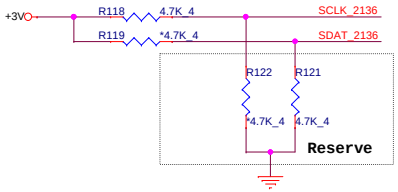
KB lock
H13 *H-TC354BC315IC150D110P2
H8 *H-TC354BC315IC150D110P2

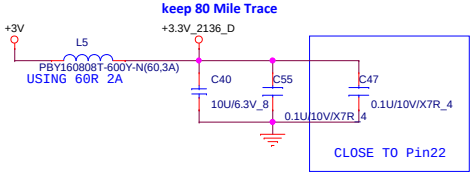
NB5

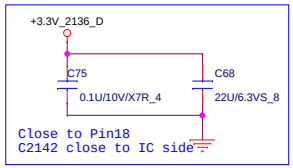
PROJECT : R63
Quanta Computer Inc.

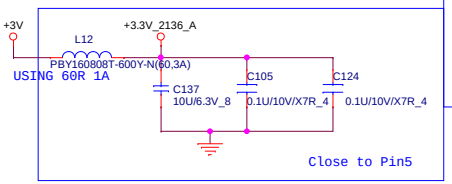
Size	Document Number	Rev
Custom	CRT,Hole	1A
Date: Friday, December 21, 2012	Sheet 23 of 44	



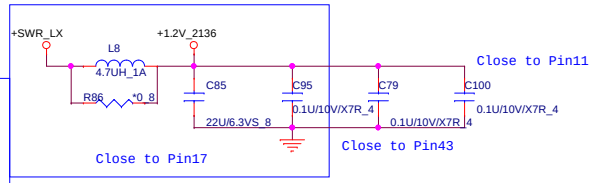








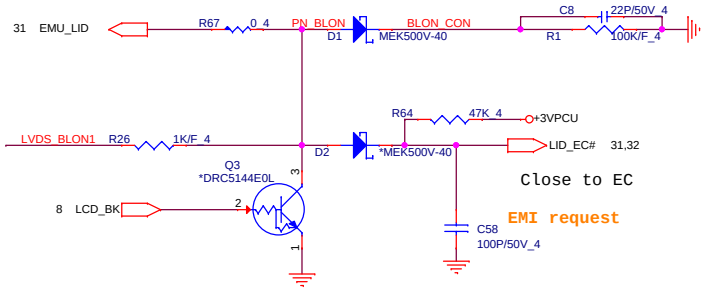
L8: need use CV-4709MN00 for Vendor suggestion

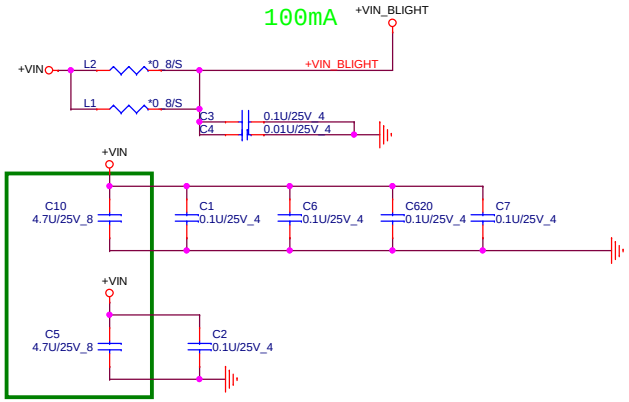


SWR MODE	LDO MODE
Stuff L8	Stuff R86

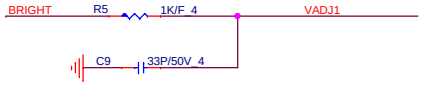
NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: RTD2136	Rev: 1A
Date: Friday, December 21, 2012	Sheet 24 of 44	

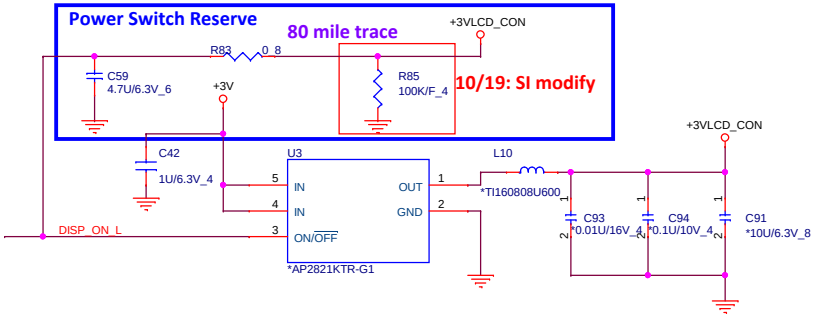
LID Switch

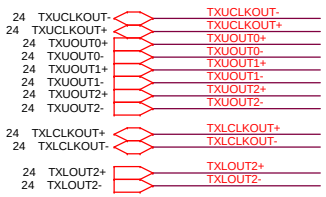


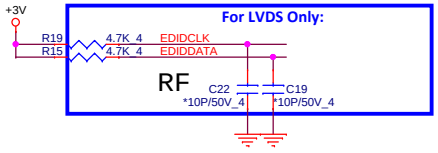


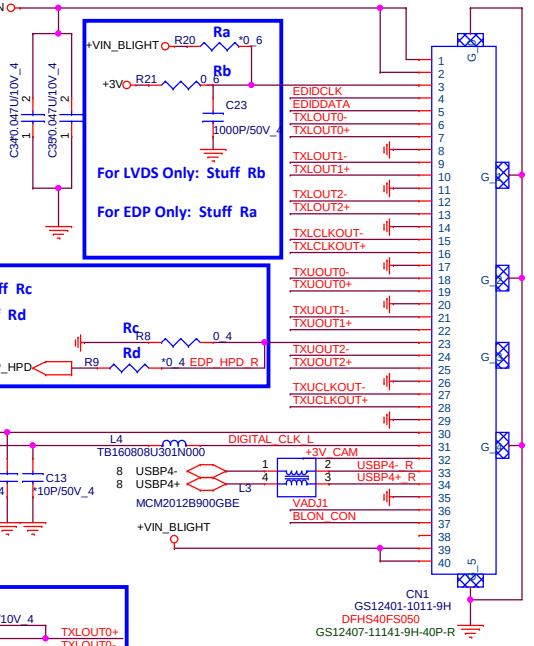
12/17: PV modify pn for 0.85 height

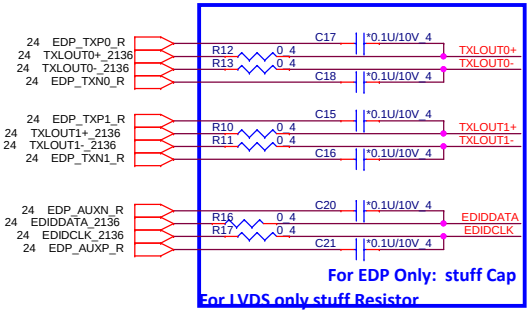


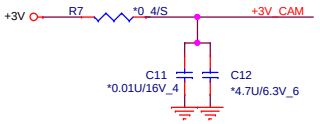


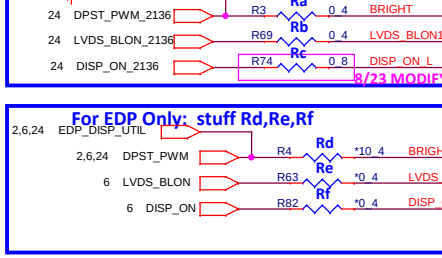


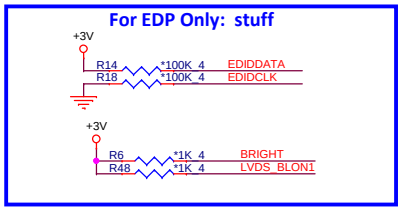


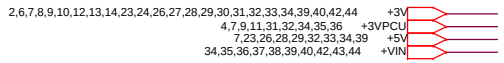












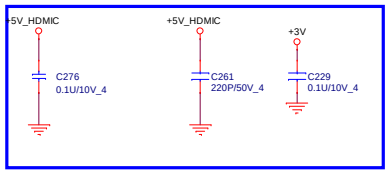
NB5

PROJECT : R63
Quanta Computer Inc.

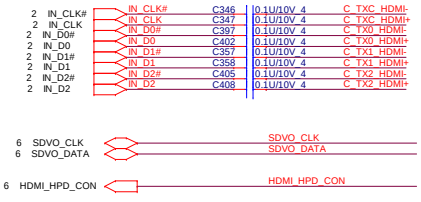
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Friday, December 21, 2012	Sheet 25 of 44	

7,23,28,29,32,33,34,39 +5V
23 +5V_HDMIC
2,6,7,8,9,10,12,13,14,23,24,25,27,28,29,30,31,32,33,34,39,40,42,44 +3V

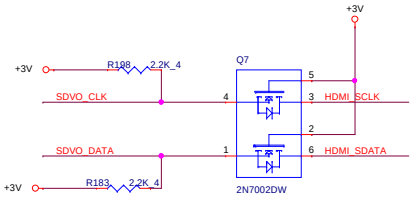
EMI request



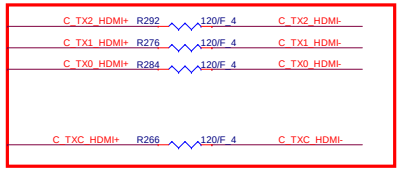
close to HDMI conn

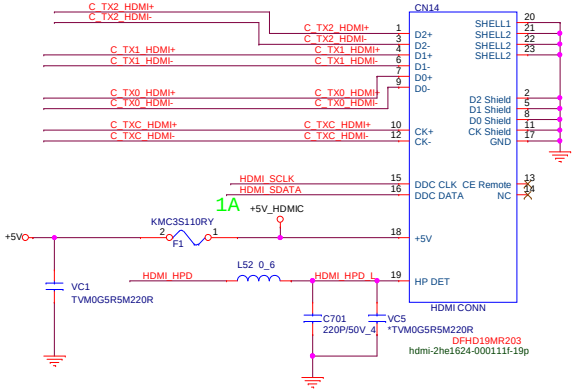


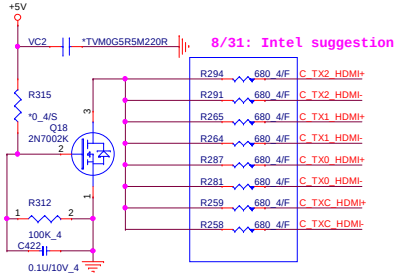
Close to HDMI Connector

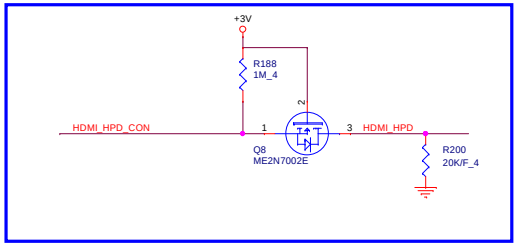


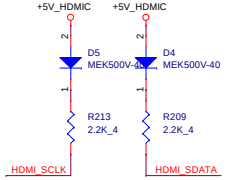
10/14: SI for EMI request







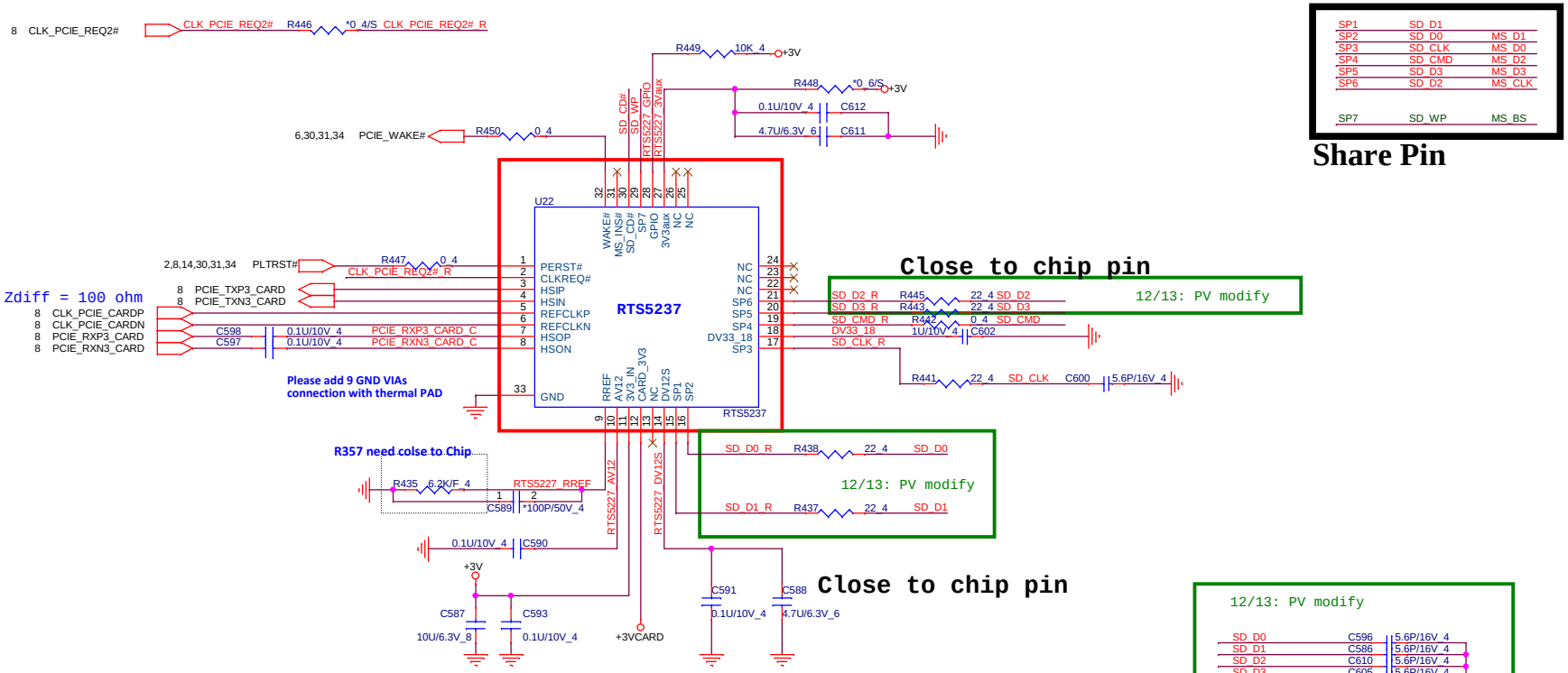




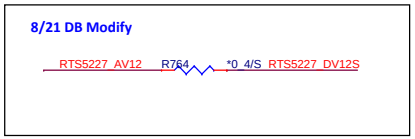
NB5

PROJECT : R63
Quanta Computer Inc.

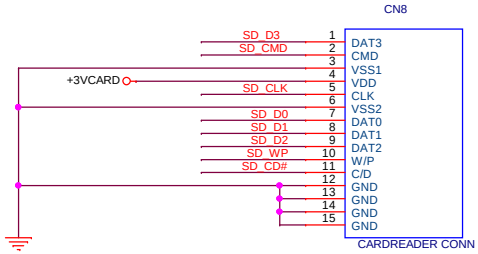
Size	Document Number	Rev
Custom	HDMI CONN	1A
Date: Friday, December 21, 2012	Sheet 26 of 44	



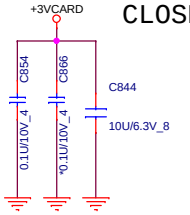
Share Pin



SD / MMC CARD READER



Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p



CLOSE CONN

2,6,7,9,10,34,36,38,39,42,44 +3VS5
2,6,7,8,9,10,12,13,14,23,24,25,26,28,29,30,31,32,33,34,39,40,42,44 +3V
+3VCARD

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	RTS5229 & CR SOCKET	1A

Date: Friday, December 21, 2012 Sheet 27 of 44

Close to PIN1

+3V L57 HCB1608KF-181T15_6 +3V_DVDD
C848 1U/6.3V_4
C860 10U/6.3VS_6
C862 0.1U/10V_4

>40mils trace

+5V_AVDD L59 HCB1608KF-181T15_6 +5V
C886 10U/6.3VS_6
C887 0.1U/10V_4
AZ5125-01H D14
Close to PIN26
AGND

+1.5V_AVDD L56 HCB1608KF-181T15_6 +1.5V
C856 10U/6.3VS_6
AGND
Close to PIN40

7,23,26,29,32,33,34,39 +5V
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,34,39,40,42,44 +3V
6,7,8,10,34,38,44 +1.5V

10/14 : SI modify

10/18 : Change PN for HP request

+5V_AVDD
C908 *2.2U/6.3V_6
U35 * TLV702475DBVR
Vout Vin BYP GND EN
C911 *1U/6.3V_4
C909 *0.1U/10V_4
R746 *10K_4 +5V
Vset=1.242V

TO Digital MIC

25 DIGITAL_D1 C867 10P/50V_4 R701 *0_4/S DMIC0
25 DIGITAL_CLK R703 100_4 DMIC_CLK_R C869 10P/50V_4

U34

1 DVDD
2 GPIO0/ DMIC-DATA
3 GPIO1 / DMIC-CLK
4 DVSS
5 SDATA-OUT
6 BCLK
7 LDO3-CAP
8 SDATA-IN
9 DVDD-IO
10 SYNC
11 RESETB
12 PCBEEP
34 CPVEE
35 CBN
37 CBP
36 CPVDD
42 SPK-L+
43 SPK-L-
44 SPK-R-
45 SPK-R+
49 NC
41 PVDD1
46 PVDD2
47 PDB
48 SPDIF-OUT/GPIO2

Digital

Analog

AVDD1 26
AVDD2 40
AVSS1 25
AVSS2 38
LDO1-CAP 27
LDO2-CAP 39
VREF 28
HPOUT-L (PORT I) 32
HPOUT-R (PORT I) 33
LINE2-L 24
LINE2-R 23
LINE1-L (PORTC) 22
LINE1-R (PORTC) 21
MIC1-R (PORTB) 20
MIC1-L (PORTB) 19
MIC1-VREFO-L 31
MIC1-VREFO-R 30
MIC2-R (PORTF) 18
MIC2-L (PORTF) 17
MIC2-VREFO 29
MONO-OUT 16
13 SenseA
14 SenseB
15 JDREF

C875 10U/6.3VS_6
C863 10U/6.3VS_6
C870 0.1U/10V_4
C874 2.2U/6.3V_6
Close to PIN28

HPOUT_L HPOUT_L 29
HPOUT_R HPOUT_R 29
AGND SHIELD
AGND SHIELD
AGND SHIELD
TO Headphone jack

10/5: SI for library modify

VREFOUT_C R706 2.2K_4 EXT_MIC_R
C877 *1U/6.3V_4

R726 *0_4/S MUTE_LED_CNTL 32

MIC_R1 C928 *2.2U/6.3V_6
MIC_L1 C893 2.2U/6.3V_6
R722 1K/F_4 EXT_MIC_R 29
TO Audio Jack MIC

VREFOUT_C 29
10/11 : SI for reserve

ALC3227 x QFN48

R725 20K/F_4 AGND
SENSE_A_1 R724 39.2K/F_4 SENSE_A 29
Close to Pin 13

COMBO_GPI 29

7 ACZ_SDOUT_AUDIO C873 *10P/50V_4 R705 0_4 HD_SDOUT
7 BIT_CLK_AUDIO HD_BCLK
10U/6.3VS_6 C876
7 ACZ_SDIN0 R707 33_4 HD_SDIN0

Close to Pin 9
+3V_DVDD 0.1U/10V_4 C882

HD_SYNC
7 ACZ_SYNC_AUDIO R720 *0_4/S C888 *10P/50V_4
12/13: PV add
7 ACZ_RST#_AUDIO C939 *0.1U/10V_4
AMP_BEEP

C842 1U/6.3V_4
CAP-
C845 1U/6.3V_4
CAP+
+3V_DVDD
+3V_DVDD
4.7U/6.3V_6 C885
Close to Pin 34,35,36

L_SPK+
L_SPK-
R_SPK-
R_SPK+

+5V_DVDD
+5V L55 HCB1608KF-181T15_6 +5V_DVDD
0.1U/10V_4 C858
10U/6.3VS_6 C853
Close to Pin 41
+5V_DVDD
Close to Pin 46
0.1U/10V_4 C859
10U/6.3VS_6 C852

PD#

TO Internal Speakers

AMP_BEEP
C895 0.1U/10V_4
AMP_BEEP_L
check value
R728 100K/F_4
AMP_BEEP_R2
C897 0.01U/10V_4
C896 0.01U/25V_4
R727 10K_4
+5V_AVDD
R732 10K_4
ME2N7002E Q37
ACZ_SPKR 7
AGND

Check layout mount location

+3V_DVDD
R696 1K/F_4
ACZ_RST#_AUDIO
D12 *MEK500V-40
PD#
31 VOLMUTE#
D11 MEK500V-40
R690 10K_4

Keep L_SPK+/-, and R_SPK+/- trace width 40 mil least

Close to CODEC
Speaker 4 ohm: 40mils

L_SPK+ L11 TI160808U600 L_SPK+_R
L_SPK- L9 TI160808U600 L_SPK-_R
R_SPK- L7 TI160808U600 R_SPK-_R
R_SPK+ L6 TI160808U600 R_SPK+_R
INT SPEAKER CONN
CN3 DFHD04MR236 3800-X04N-00X-4P-L
C98 1000P/50V_4
C88 1000P/50V_4
C70 1000P/50V_4
C56 1000P/50V_4

C830 0.1U/25V_4
C599 0.1U/25V_4
C839 *0.1U/25V_4
C894 0.1U/25V_4
C841 0.1U/25V_4
AGND
Close to CODEC
place to near U37 or under U37.
R420 *0_8/S
AGND

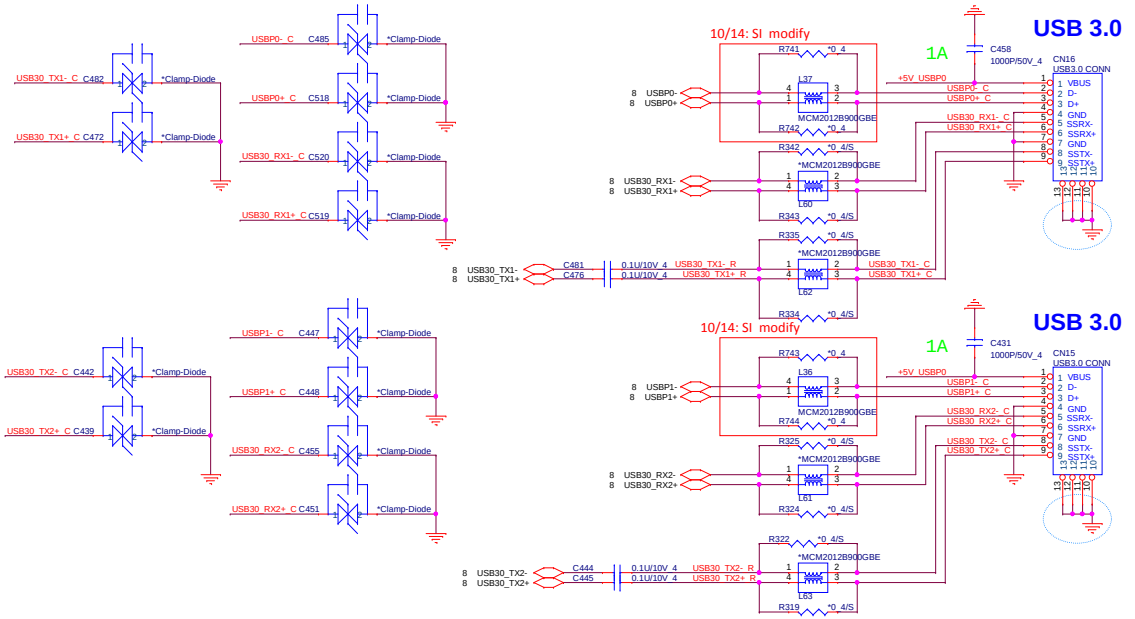
BIT_CLK_AUDIO
ACZ_SDIN0
C872 *33P/50V_4
C881 *33P/50V_4
FOR EMI

NB5

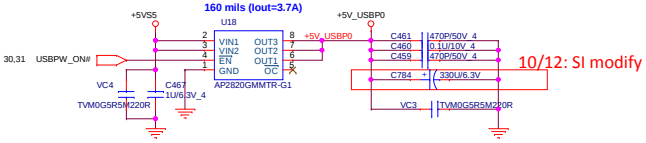
PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC3227	1A

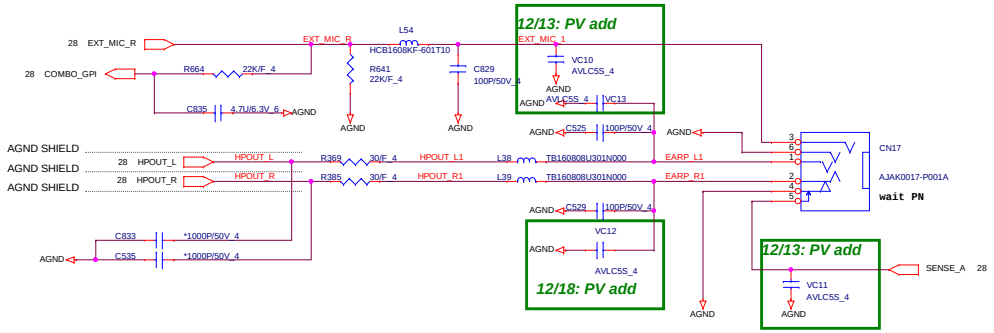
Date: Friday, December 21, 2012 Sheet 28 of 44



USB3.0 X 2/USB2.0 COMBO



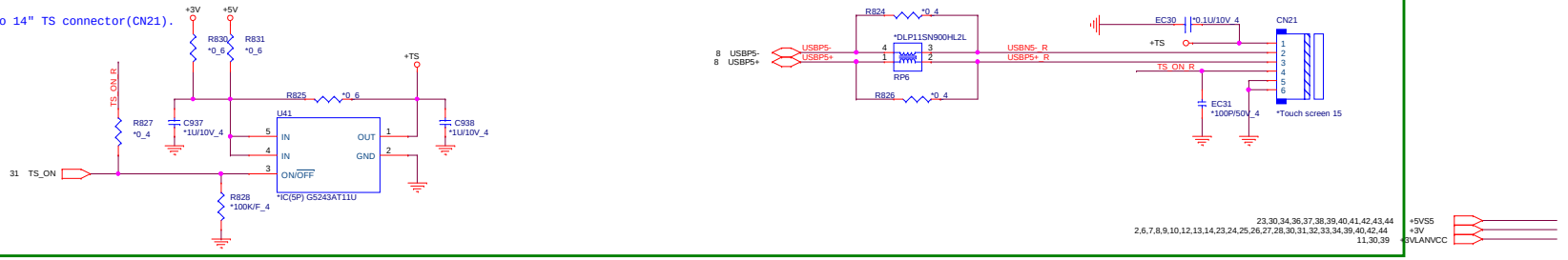
COMBO JACK



12/11: PV add

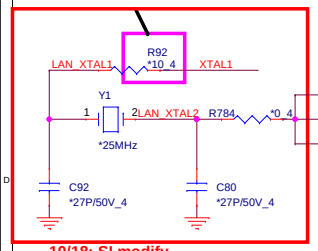
Touch Screen Connector

close to 14" TS connector(CN21).



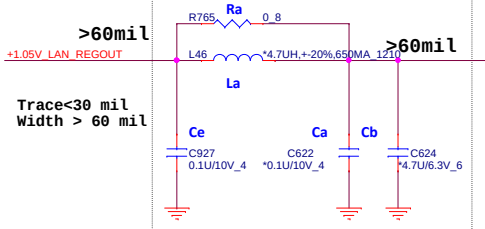
NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: USB/BT/Audio JacK	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 29 of 44	

For EMI 0 ~ 22 ohm



10/18: SI modify

Power trace Layout 寬度> 60mil

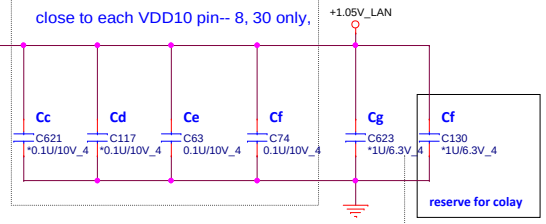


For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb
STUFF : Ra, Ce

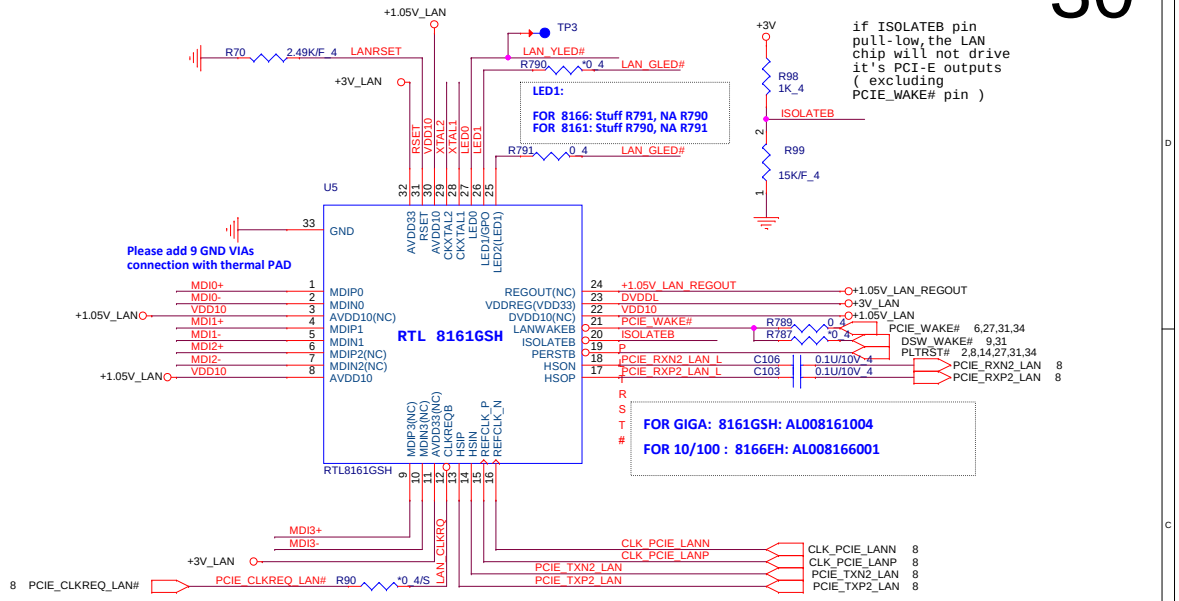
For GbE
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf
* Place Ce , Cf
close to each VDD10 pin-- 8, 30 only,



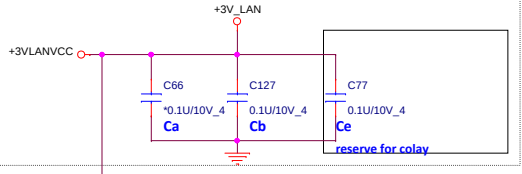
For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

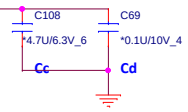


For 10/100
* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23

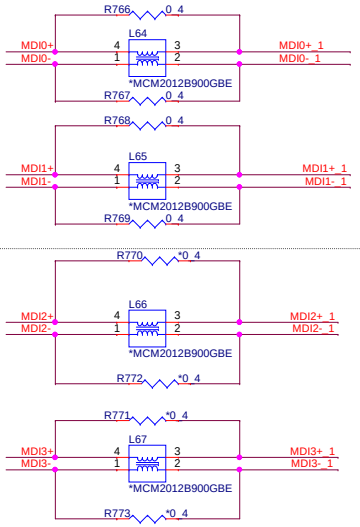


Remove For Not Using SWR mode

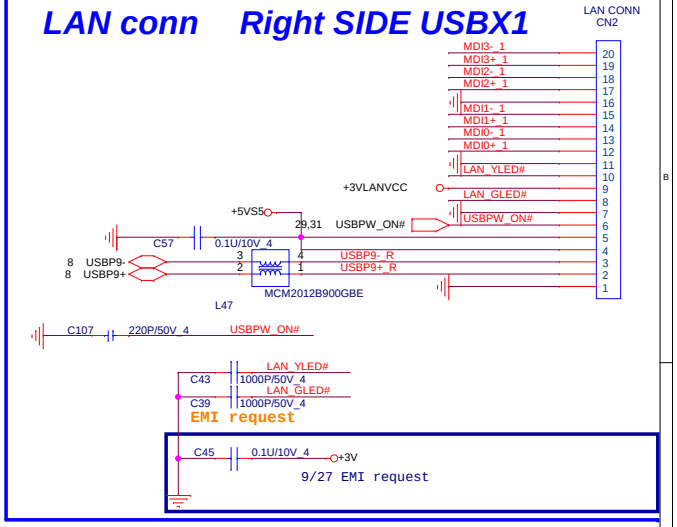
For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

For 10/100 only



LAN conn Right SIDE USBX1



For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100
BOT: TST1284R LF DB0EL5LAN00
FCE :NS892408 ,DB0EF7LAN01

2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,31,32,33,34,39,40,42,44
11,39
+3V
+3VLANVCC

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: RTL 8105E/RJ45	Rev: 1A
Date: Friday, December 21, 2012	Sheet 30 of 44	

U13

KB3940QF A1

500mA

for Battery charge/charge and cap board

for CPU thermal

For GPU thermal

For Gsensor

12/12: PV Modify

10/17: SI Modify

10/17: SI Modify

10/17: SI Modify

Reserve for ENE timing issue

If use PCH SUSCLK should change to 20P.

12/19: PV add

FOR SG/DIS

10/14: SI add BOM ID

adapter Type check

Change to 1SS355 as Current loss

adapter select for EC

Hi ==> DIS/SG

Low ==>UMA

PROCHOT control

For +VIN noise

Socket: DFHS08FS023

2M byte SPI EC ROM

EON AKE38ZN0802 EN25QH16-104HIP

AMIC AKE38ZN0Q00 A25LQ16M-F/Q

AKE38ZN0802

SOIC8-8-1_27

Open Drain need pu high

10/14: SI modify

PROJECT : R63	
Quanta Computer Inc.	
Size: Custom	Document Number: EC (KB3940 A1)/ROM
Rev: 1A	
Date: Friday, December 21, 2012	Sheet 31 of 44

NB5

KEYBOARD Con.

31 MY[0..17] MY[0..17]
31 MX[0..7] MX[0..7]

KB CONN 50698-03201-001-32p-l
DFFC32FR035

MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17

SATA_LED

C902 *AVLC 5S
7 SATA_LED#
8 ACC_LED#
SATA_LED#
SATA_R_LED1
R734 39_6
+3V
LED2
LED 3P WHITE/AMBER
(Amber)
R733 200/F_6
C899 *AVLC 5S

KEYBOARD PULL-UP

RP2
+3VPCU
MY6 MY3 MY12 MY13
MY15 MY10 MY11 MY14
*10P8R-8.2K

RP1
MY9 MY0 MY5 MY1
MY8 MY7 MY4 MY2
*10P8R-8.2K

R173 *8.2K_4 MY16
R176 *8.2K_4 MY17

MY5 C109 *220P/50V_4
MY6 C142 *220P/50V_4
MY3 C145 *220P/50V_4
MY7 C140 *220P/50V_4
MY8 C141 *220P/50V_4
MY9 C76 *220P/50V_4
MY10 C173 *220P/50V_4
MY11 C169 *220P/50V_4
MY1 C128 *220P/50V_4
MY2 C136 *220P/50V_4
MY4 C139 *220P/50V_4
MY0 C96 *220P/50V_4
MX4 C82 *220P/50V_4
MX6 C73 *220P/50V_4
MX3 C104 *220P/50V_4
MX2 C97 *220P/50V_4
MX7 C67 *220P/50V_4
MX0 C133 *220P/50V_4
MX5 C90 *220P/50V_4
MX1 C61 *220P/50V_4
MY12 C149 *220P/50V_4
MY13 C152 *220P/50V_4
MY14 C156 *220P/50V_4
MY15 C190 *220P/50V_4
MY16 C201 *220P/50V_4
MY17 C206 *220P/50V_4

31 CAPSLED#
R185 200/F_6 CAPSLED#_R
R191 200/F_6 MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R
+3V
+3VPCU
CN6

28 MUTE_LED_CNTL
Q6
2N7002K
R147
10K/F_4

SI, add Mute LED feature

EC KB3930 has included K/B pull-up resistor and function

9/15 SI for H/W.

+5V +3V
R196 1K/F_4
R777 *200/F_6
R195 *200/F_6
Q10
DRC5144E0L
31 WIRELESS_ON
WIRELESS_ON_R

+5V
R199 1K/F_4
R208 *200/F_6
Q9
DRC5144E0L
31 WIRELESS_OFF
WIRELESS_OFF_R

R440 39_6
+3VPCU
LED1
3P WHITE LED
C601 *AVLC 5S
DEEP_PWRLED#

12/20 PV modify

PWR_LED

SATA_LED#
C607 1000P/50V_4
DEEP_PWRLED#
C604 1000P/50V_4

POWER BOTTON CONNECT

100mA
C116 *4.7U/6.3V_6
C114 1U/10V_4
C113 0.1U/10V_4
+3VPCU
25,31 LID_EC#
31 NBSWON1#
31,32 PWR_LED#
R116 *0_4
DEEP_PWRLED# R117 *0_4/S
CN4
PWR BTN CONN
DFFC06MR001
88513-0601-6P-L-SMT

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

+3VPCU
R120 10K/F_4
C110 PWR_LED# *0.1U/10V_4
C112 LID_EC# 0.1U/10V_4
C111 NBSWON1# 0.1U/10V_4
31,32 PWR_LED#
Q5
DRC5144E0L
C135 0.1U/10V_4
DEEP_PWRLED#
for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.

+3VSUS
R318 4.7K_4 TP_SMB_CLK
R323 4.7K_4 TP_SMB_DATA

change to +3VSUS
close conn

+3VSUS
R304 4.7K_4 TPCLK
R303 4.7K_4 TPDATA

88513-0601-6P-L-SMT
DFFC06MR001
PWR BTN CONN
C429 10P/50V_4
31 TPCLK
31 TPDATA
L34 TB160808B470N001
L33 TB160808B470N001
C428 10P/50V_4
TPCLK-1
TPDATA-1
TP_SMB_DATA
TP_SMB_CLK
CN7

25 mils

+3VSUS C430 0.1U/10V_4

+3VSUS
Q19
TP_SMB_CLK
TP_SMB_DATA
SMB_PCH_CLK 8
SMB_PCH_DAT 8
*2N7002DW

PV , HP request Image sensor
SMBUS reserve to PCH

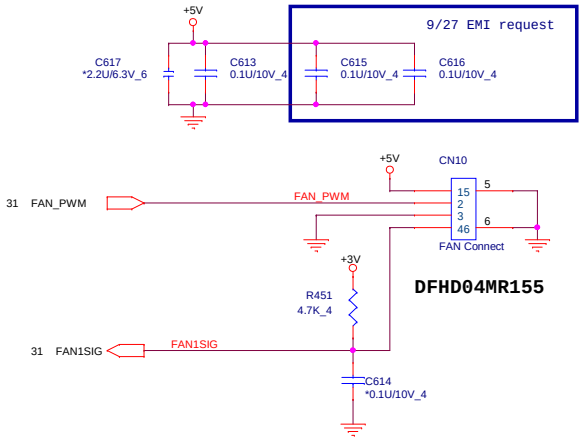
4,7,9,11,25,31,34,35,36 +3VPCU
7,23,26,28,29,33,34,39 +5V
39 +3VSUS
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,33,34,39,40,42,44 +3V

NB5

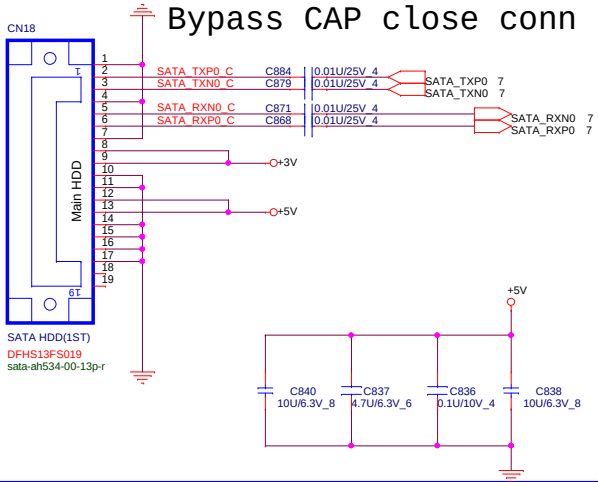
PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A
Date: Friday, December 21, 2012	Sheet 32 of 44	

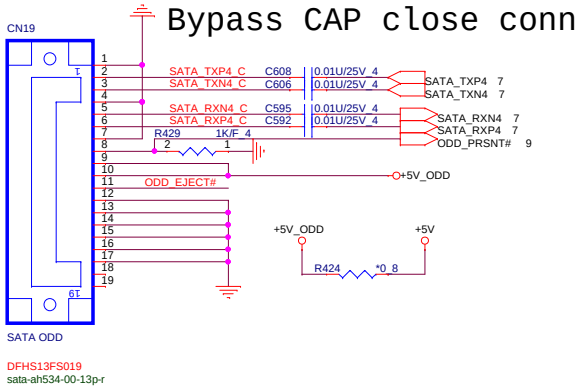
CPU FAN

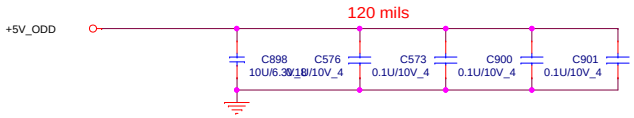


SATA HDD CONNECTOR

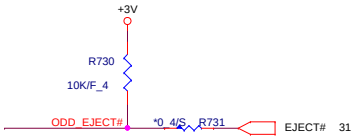


SATA ODD CONNECTOR

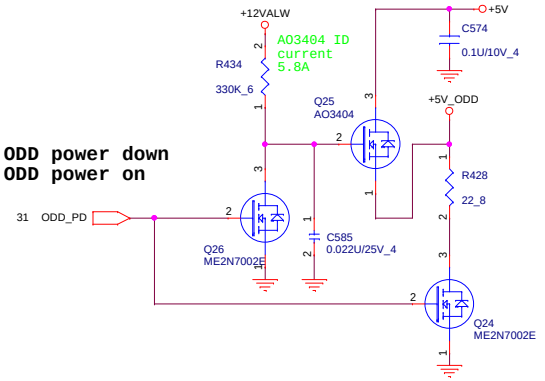




follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,34,39,40,42,44 +3V
4,7,9,11,25,31,32,34,35,36 +3VPCU
7,23,26,28,29,32,34,39 +5V
35,39,44 +12VALW

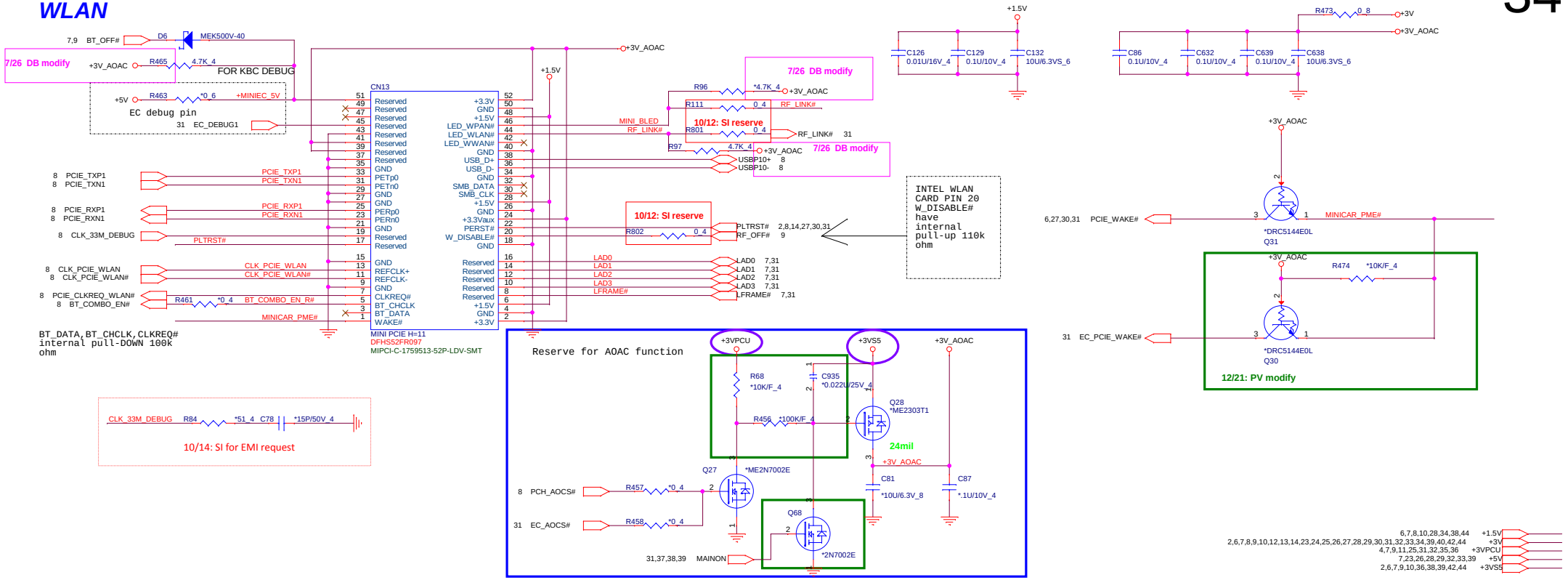
NB5

PROJECT : R63
Quanta Computer Inc.

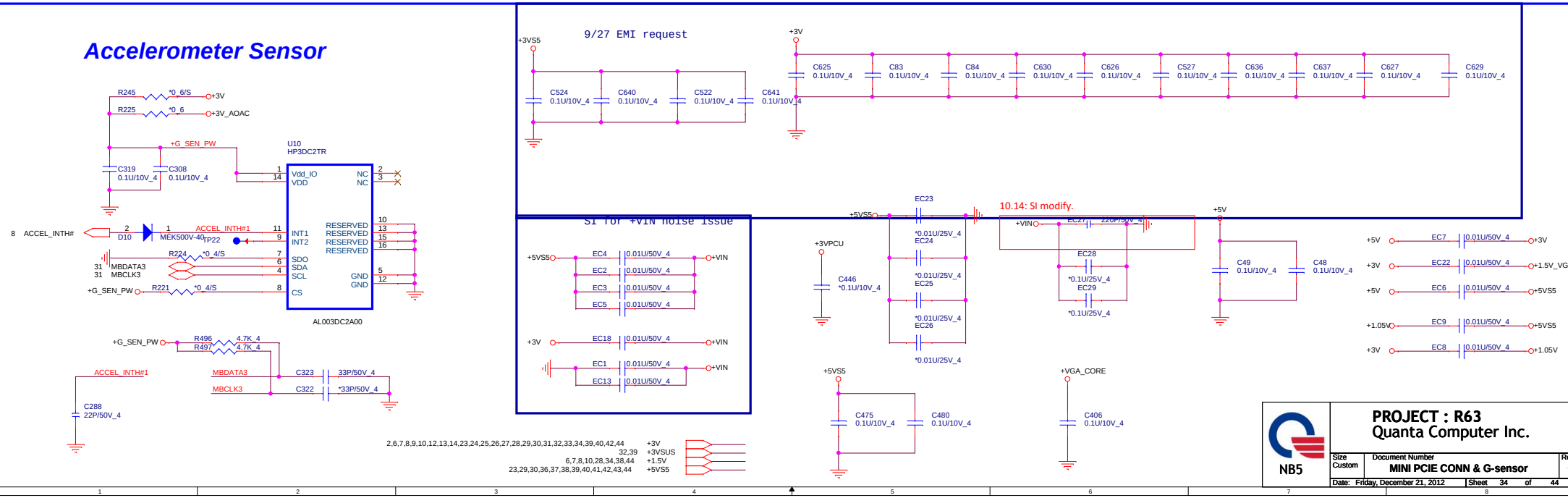
Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

Date: Friday, December 21, 2012 | Sheet 33 of 44

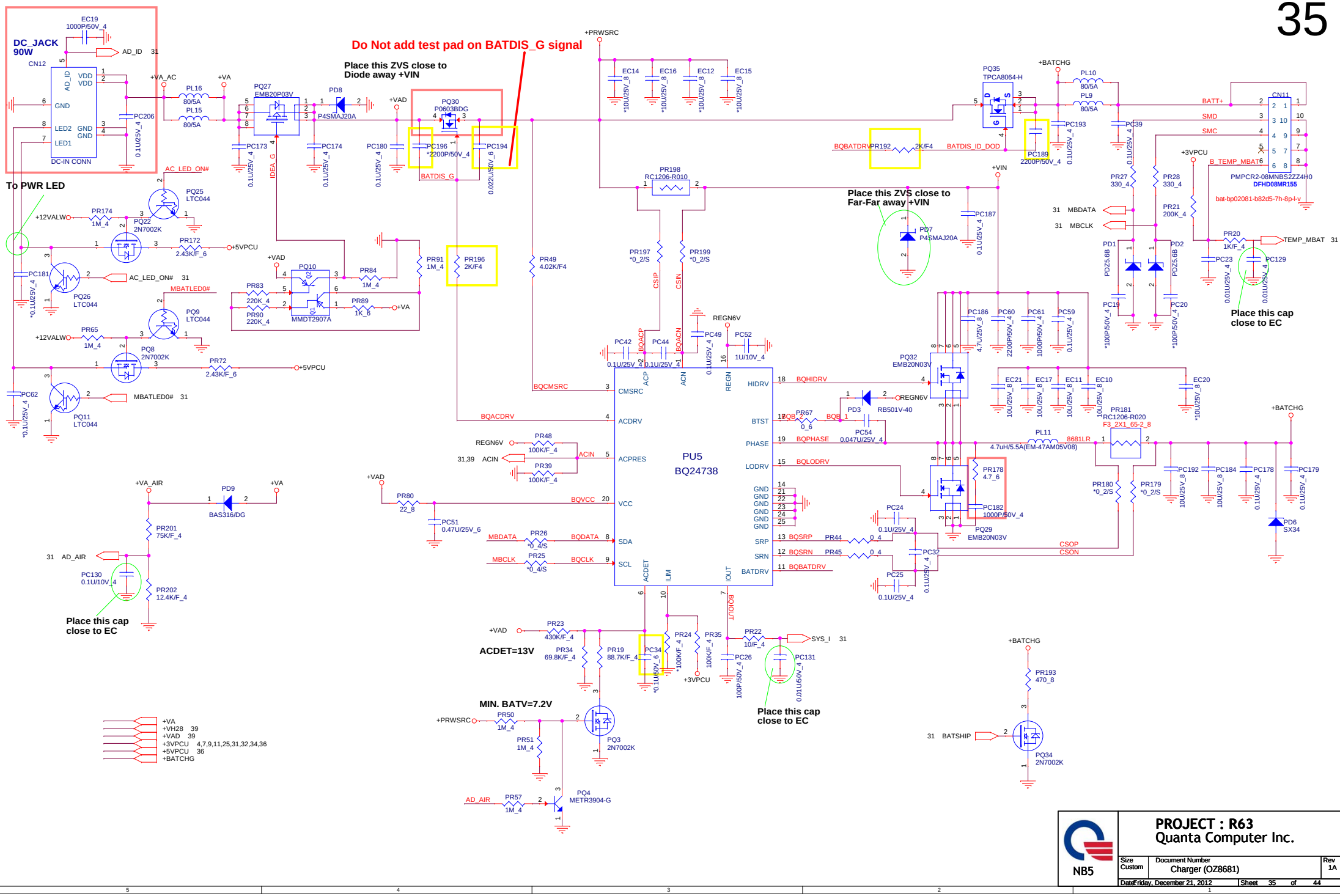
Mini PCI-E Card 1 WLAN



Accelerometer Sensor

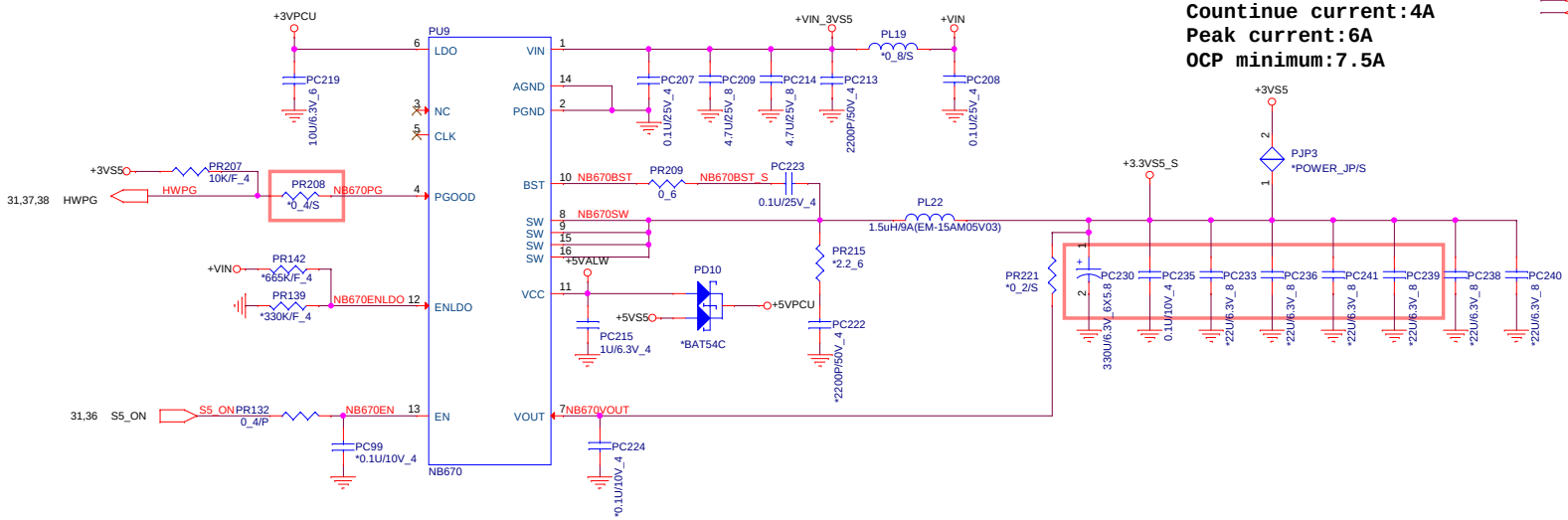


NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCIE CONN & G-sensor	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 34 of 44	


DC_JACK
90W
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
PU5
BQ24738
ACDET=13V
MIN. BATV=7.2V
+PRWSRC
+VIN
+BATCHG
+VA
+VAD
+3VPCU
+5VPCU
+12VALW
REGN6V
SYS_I
BATSHIP
TEMP_MBAT
PROJECT : R63
Quanta Computer Inc.
NB5
Charger (OZ8681)
Friday, December 21, 2012

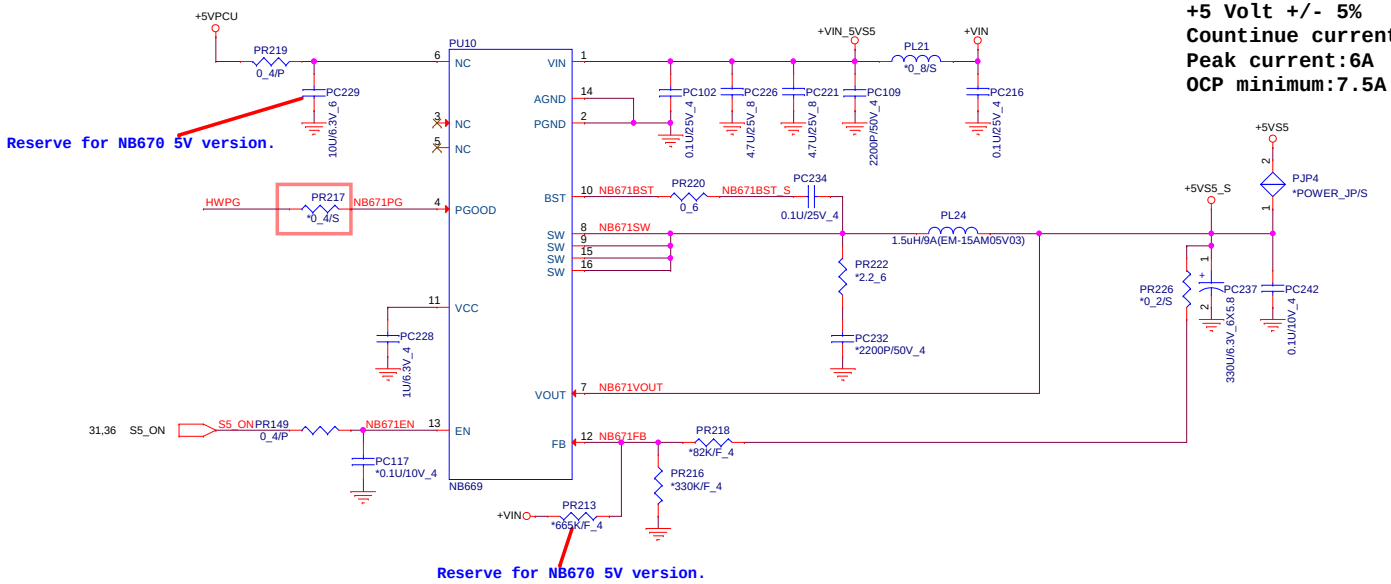
DC/DC +3VS5/+5VS5

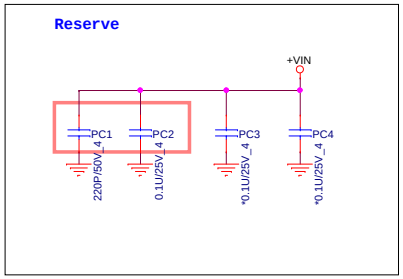
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



+3VS5 2,6,7,9,10,34,38,39,42,44
+5VS5 23,29,30,34,37,38,39,40,41,42,43,44

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

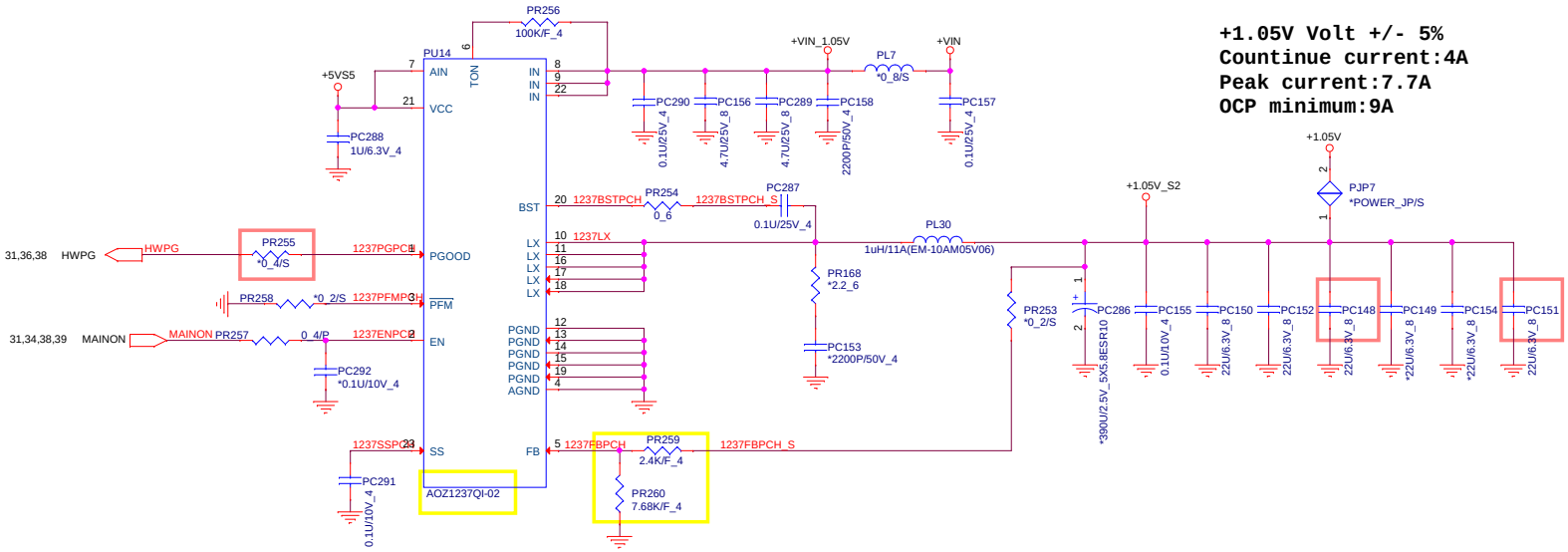




NB5

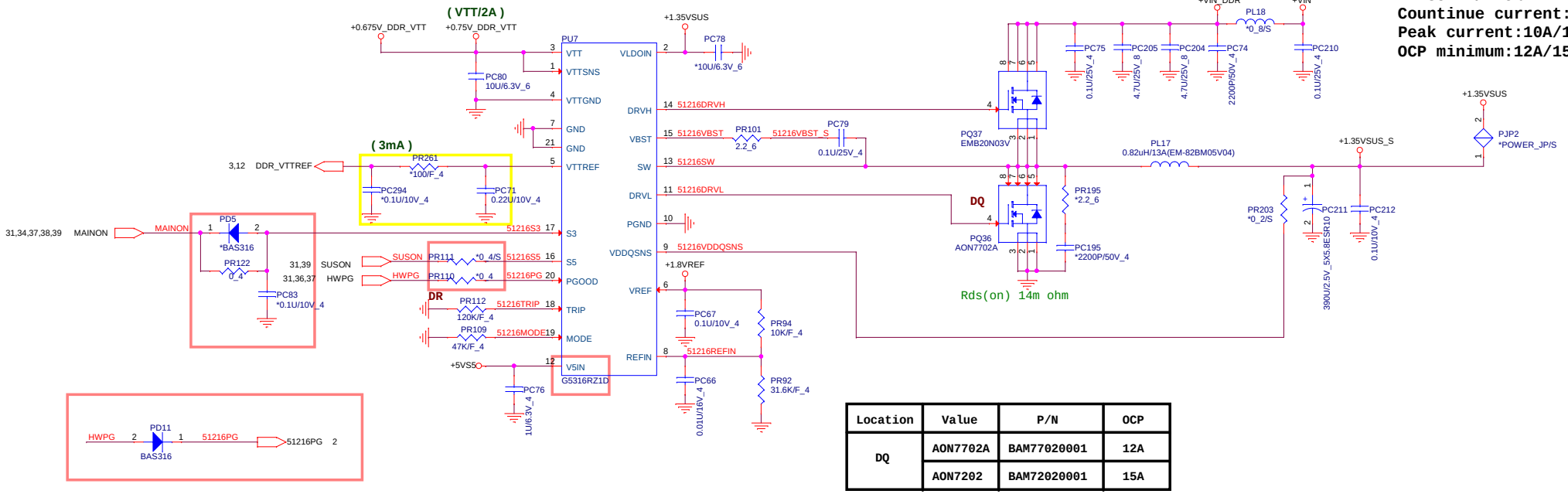
PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A
Date: Friday, December 21, 2012	Sheet 36 of 44	


+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A
PR256
100K/F_4
PU14
AIN
VCC
TON
BST
LX
PGND
AGND
EN
PGOOD
PFM
SS
FB
IN
AOZ1237QI-02
+5VS5
+VIN_1.05V
+VIN
PL7
*0_8/S
PC290
PC156
PC289
PC158
PC157
PC288
1U/6.3V_4
PR254
0_6
1237BSTPCH
1237BSTPCH_S
PC287
0.1U/25V_4
1237LX
PL30
1uH/11A(EM-10AM05V06)
PR168
*2.2_6
PC153
*2200P/50V_4
PR255
*0_4/S
HWPG
31,36,38 HWPG
1237PGPCH
PR258
*0_2/S
1237PFMPCH
31,34,38,39 MAINON
MAINON
PR257
0_4/P
1237ENPCH
PC292
*0.1U/10V_4
1237SSPCH
PC291
0.1U/10V_4
1237FBPCH
PR259
2.4K/F_4
1237FBPCH_S
PR260
7.68K/F_4
+1.05V_S2
PR253
*0_2/S
PC286
*390U/2.5V_5X5.8ESR10
PC155
PC150
PC152
PC148
PC149
PC154
PC151
0.1U/10V_4
22U/6.3V_8
*22U/6.3V_8
+1.05V
PJP7
*POWER_JP/S
+1.05V 2,4,9,10,11,31,34
NB5
PROJECT : R63
Quanta Computer Inc.
Size Custom
Document Number
1.05V(RT8228BZ)
Rev 1A
Date: Friday, December 21, 2012
Sheet 37 of 44

+1.35VSUS 2,3,4,12,13
+1.5V 6,7,8,10,28,34,44

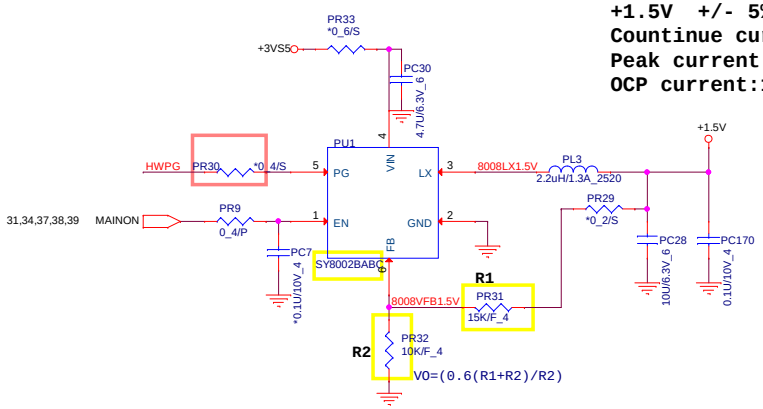
+1.35V +/- 5%
Countinue current:6A/8A
Peak current:10A/12A
OCP minimum:12A/15A



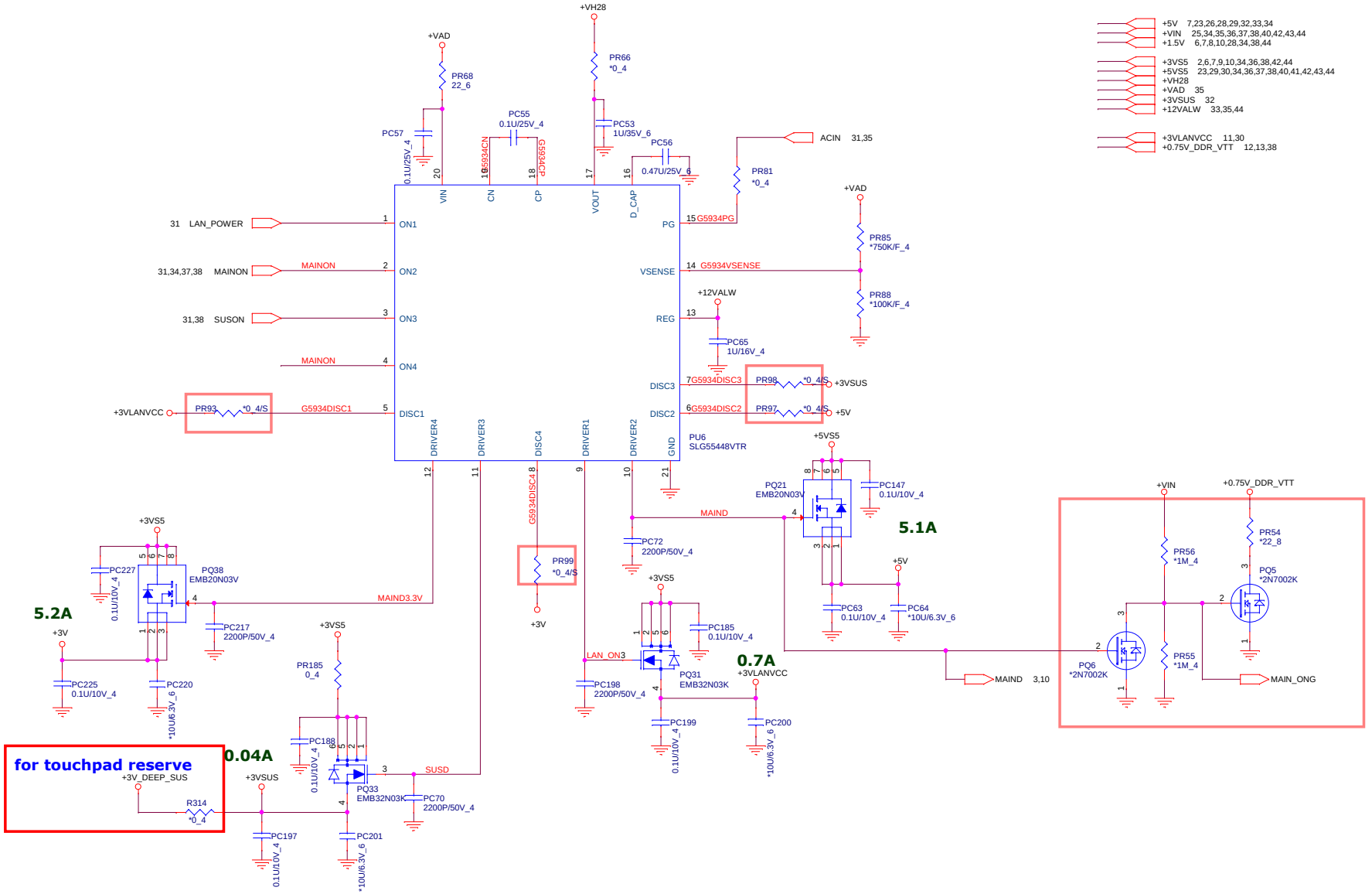
Location	Value	P/N	OCP
DQ	AON7702A	BAM77020001	12A
	AON7202	BAM72020001	15A

Location	Value	P/N	OCP
DR	120K	CS41202FB17	12A
	76.8K	CS37682FB00	15A

+1.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
OCP current:1.2A



NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: DDR3L(APW8819)	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 38 of 44	



+5V 7,23,26,28,29,32,33,34
+VIN 25,34,35,36,37,38,40,42,43,44
+1.5V 6,7,8,10,28,34,38,44

+3VS5 2,6,7,9,10,34,36,38,42,44
+5VS5 23,29,30,34,36,37,38,40,41,42,43,44
+VH28
+VAD 35
+3VSUS 32
+12VALW 33,35,44

+3VLANVCC 11,30
+0.75V_DDR_VTT 12,13,38

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (G5934)	Rev: 1A
Date: Friday, December 21, 2012	Sheet 39 of 44	

CPU	Re	PR18
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

PUT COLSE TO VCORE Phase 1 Inductor

Dummy Rc For 2 phase

Rc

PR8 *147K/F_6 SWN2 → SWN2 40,41

PR3 147K/F_6 SWN3 → SWN3 40

PR12 147K/F_6 SWN1 → SWN1 40

CPU	Rd	PR14
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

Dummy Ra and Ca For 2 phase

Ca: PC6 *0.047U/25V_4 — PR7 *20K/F_4 — PR10 *5.11K/F_4 — Ra → SWN2 40,41

PC5 0.047U/25V_4 — PR2 *20K/F_4 — PR1 5.11K/F_4 → SWN3 40

PC13 0.047U/25V_4 — PR11 *20K/F_4 — PR13 5.11K/F_4 → SWN1 40

+5VS5

Rb: PR4 0_4

POP Rb for 2 phase

+VCC_CORE 4,41

PR191 220K_6 NTC — PR5 75K/F_4 — PR6 165K/F_4 — 81103GND

PC10 1200P/50V_4 — PC17 1000P/50V_4 — CSREF → CSREF 40,41

PC14 *330P/50V_4

CSSUM — CSP3 — CSP2 — CSP1

DRON → DRON 41

81103_PWM → 81103_PWM 41

CSCOMP

Rd: PR14 43.2K/F_4

Re: PR18 9.09K/F_4

+VCCIO_OUT

PR76 130/F_4 — PR77 *75/F_4 — PR78 54.9/F_4 — PC58 0.1U/10V_4

SDIO — ALERT# — SCLK

+VIN_VCC_CORE

PR36 1K/F_4 — PC29 0.01U/50V_4 — 81103GND

PR52 49.9/F_4 — PC40 330P/50V_4 — PC38 10P/50V_4

PR47 1K/F_4 — PR43 5.9K/F_4

PR17 22.1K/F_4 — PC22 470P/50V_4 — 81103GND

81103ILIM 28 — 81103IOUT 29 — 81103VRAMP 30 — 81103COMP 31 — 81103FB 32 — 81103DIFFOUT 33 — 81103VSN 34 — 81103VSP 35 — 81103VCC 36

PR70 0_4 — PR53 1K/F_4 — PR43 2200P/50V_4 — PC48 1000P/50V_4 — PR71 0_4

4 VSS_SENSE — 4 VCC_SENSE

PR74 2.2_6 — PC47 2.2U/6.3V_6 — 81103GND

PR170 *0_4/S

PU4 NCP81103

ILIM IOUT VRMP COMP FB DIFFOUT VSN VSP VCC GND

EN VRHOT# SDIO ALERT# SCLK VR_RDY ROSC TSENSE VBOOT

CSCOMP CSSUM CSREF CSP3 CSP2 CSP1 DRON PWM2/IMAX HG3

BST3 SW3 LG3 PGND HG1 BST1 SW1 LG1 PVCC

PC18 0.22U/25V_6 — 81103SW3

81103LG3

81103HG1

PC41 0.22U/25V_6 — 81103SW1

81103LG1

+5VS5

PC35 2.2U/6.3V_6

PR73 45.3K/F_4 — 81103GND

PC50 0.1U/10V_4 — 81103GND

PR64 25.5K/F_4 — 81103GND

81103HG3 — PR173 1_6 — 81103HG3_G

PQ23 RJK03P3

PQ1 *RJK03S3

81103SW3 — PR177 4.7_6 — PC175 1000P/50V_4

PR82 1_6 — 81103HG1_G

PQ28 RJK03P3

PQ7 *RJK03S3

81103SW1 — PR176 4.7_6 — PC172 1000P/50V_4

+VIN_VCC_CORE

PC165 4.7U/25V_8 — PC15 4.7U/25V_8 — PC166 4.7U/25V_8

PC160 0.1U/25V_4 — PC161 2200P/50V_4

PL1 *0_8/S — PL2 *0_8/S — PC202 470U/25V_EC_10H — PC9 0.1U/25V_4 — +VIN

PL12 0.24uH/24A_7X7X4

PR186 *0_2/S — PR86 10/F_4 — CSREF

PR182 *0_2/S → SWN3 40

PC46 4.7U/25V_8 — PC183 4.7U/25V_8 — PC45 4.7U/25V_8

PC176 0.1U/25V_4 — PC177 2200P/50V_4

PL14 0.24uH/24A_7X7X4

+VCC_CORE

PC203 *390U/2.5V_5X5.8ESR10 — PC190 *330U/2.5V_6X4.5ESR12 — PC191 *330U/2.5V_6X4.5ESR12 — PC68 *330u_2.5V_7343 — PC128 3300u_2V_7343

PR188 *0_2/S — PR87 10/F_4 — CSREF → CSREF 40,41

PR184 *0_2/S → SWN1 40

SV 37W CPU
VID1=1.8V
IccMax=55A
Icc_Dyn=35A
Icc_TDC=26A
R_LL=1.5m ohm
OCP~60A

31 VRON

+VCCIO_OUT — PR75 *75/F_4

2,31 H_PROCHOT# — 4 VR_SVID_DATA — 4 VR_SVID_ALERT# — 4 VR_SVID_CLK — 6 IMVP_PWRGD

PR59 *0_4/S — PR60 *0_4/S — PR61 *0_4/S — PR62 *0_4/S — PR63 *0_4/S — PR58 *0_4/S

+3V — PR79 10K/F_4

TSENSE — PR189 0_4/P — PR194 8.25K/F_4 — PR190 TH05-3L104FR

PUT COLSE TO VCORE HOT SPOT

For 37W CPU ; PC128 Placed 330uF_9 mohm
For 47W CPU ; PC128 Placed 560uF_4.5 mohm

CPU	PC128
37W	CH733RY8802
47W	CH756RM8802

CPU	Ra	Ca	Rb	Rc	Rd	Re		
37W	Dummy	Dummy	POP	Dummy	CS34322FB00	CS29092FB27	CH733RY8802	Dummy Page 41
47W	POP	POP	Dummy	POP	CS36652FB16	CS31472FB14	CH756RM8802	POP Page 41
R63 Location	PR10	PC6	PR4	PR8	PR14	PR18	PC128	

NB5

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Size Custom | Document Number CPUCORE (NCP81103) | Rev 1A

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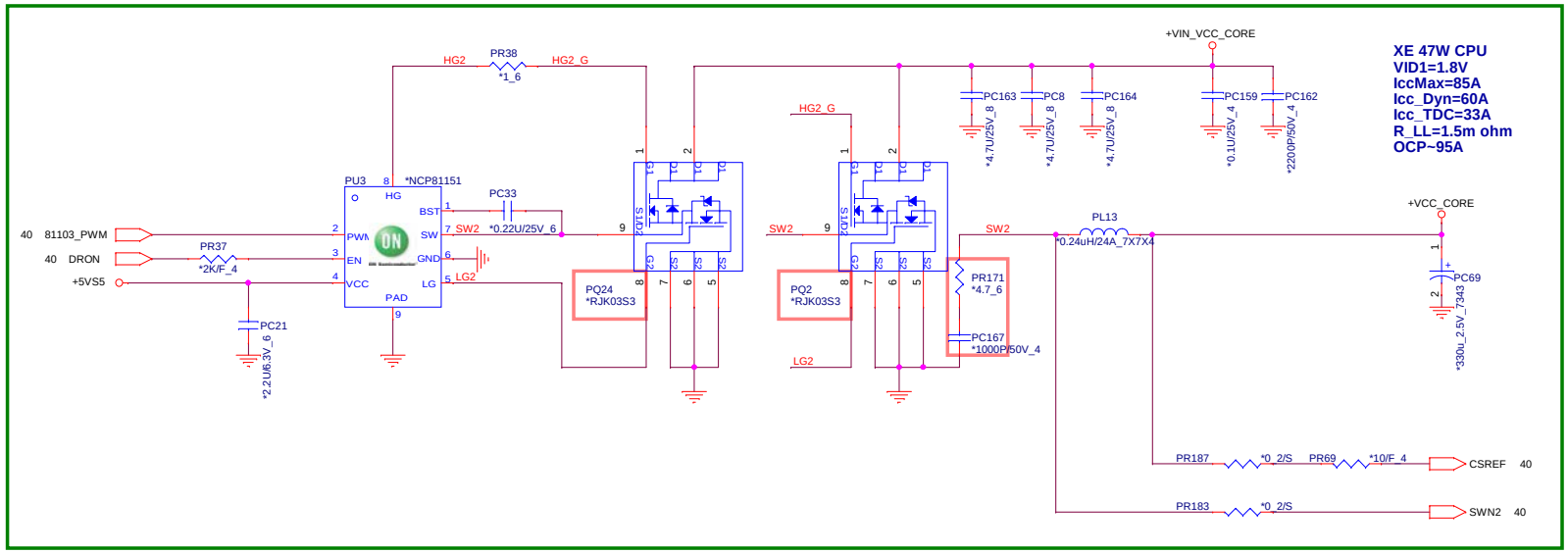

For 37W CPU
Dummy these components

+VCC_CORE 4,40

NB5

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VGA Core

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default

GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

Default

+VGA_CORE 18,34,44

42

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L=0mV/A

DCR_1.4m ohm

DCR_1.4m ohm

PU8
NCP3218G

This NTC Close to Phase 1 MOSFET

Close to Phase 1 Inductor

Shortest the net trace

VSS_GPU_SENSE 18

VGPU_CORE_SENSE 18

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NB5

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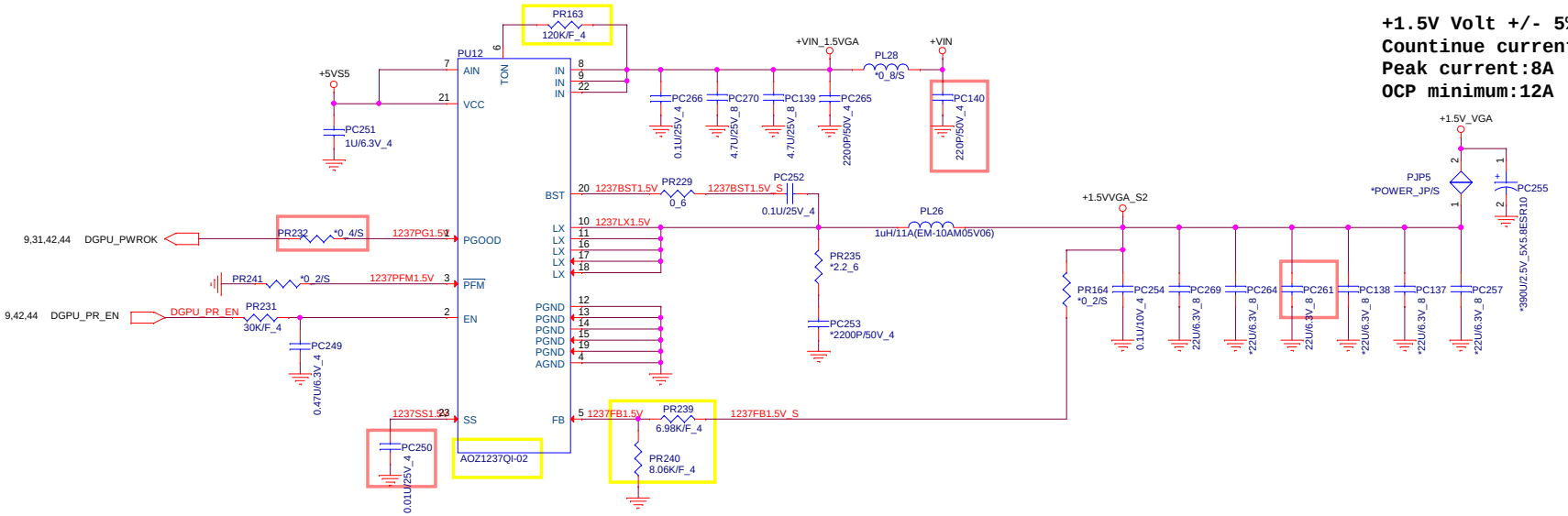

NB5	PROJECT : R63 Quanta Computer Inc.	
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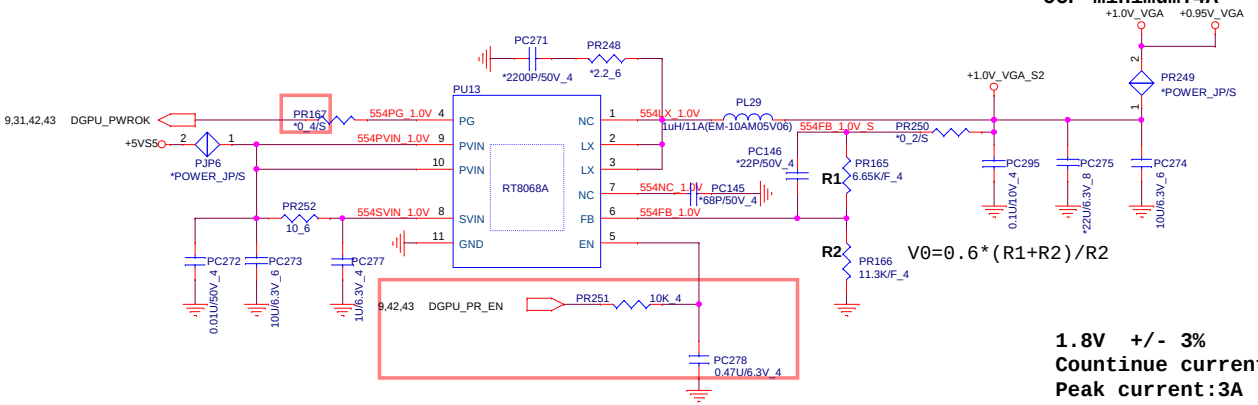
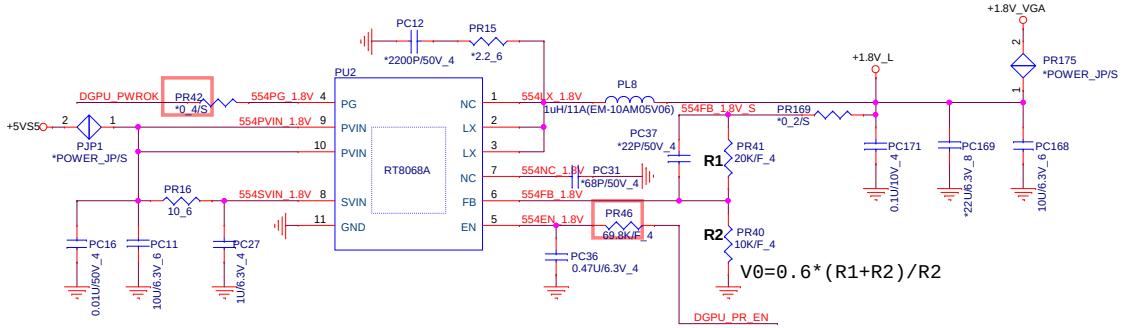
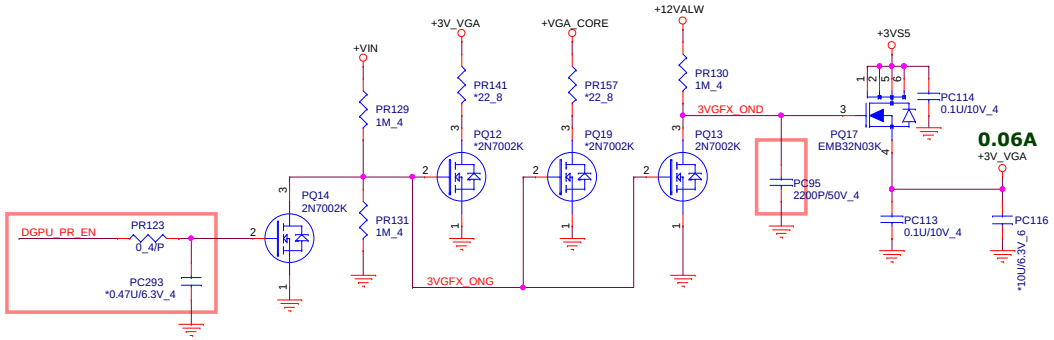
VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

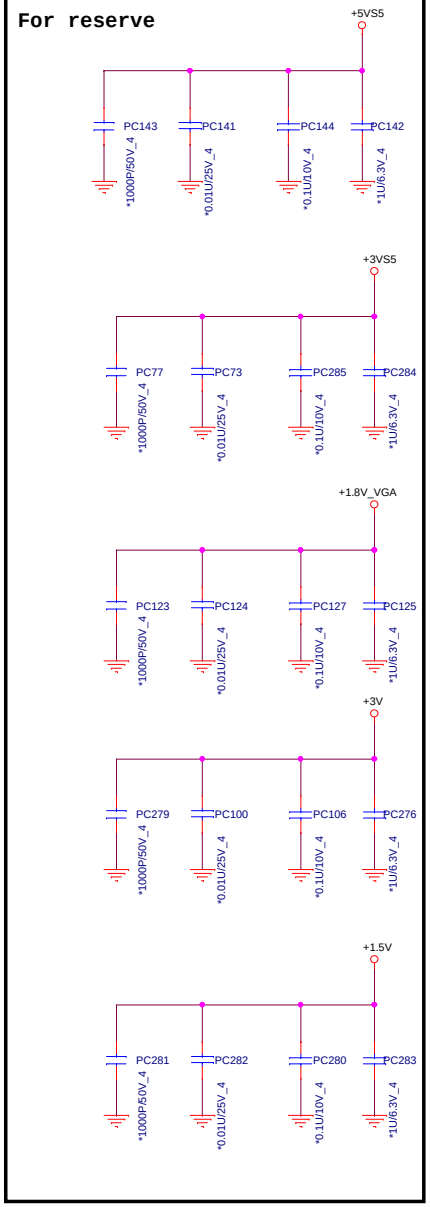


1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A





For reserve



+1.8V_VGA 11,15,16,18,19
+1.0V_VGA 14,16,18,19
+3V_VGA 14,18

NB5

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